

# Design Project 4

## MOSFET XOR Gate

ELECENG 2EI4

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# Circuit Schematic:

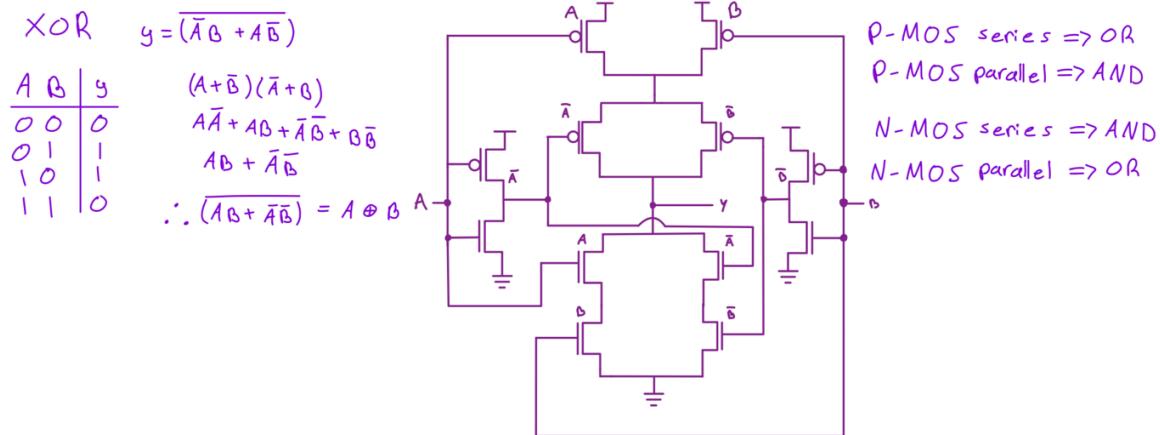


Figure 1: Circuit schematic

The XOR gate was built using two CD4007B IC chips. These chips provide a total of six NMOS and six PMOS transistors, allowing us to create a full XOR gate using CMOS logic.



Figure 2: Physical Circuit Implementation

## Ideal Sizing:

In CMOS logic design, proper transistor sizing is key to ensure balanced switching performance and signal integrity. Furthermore, NMOS transistors naturally conduct better than PMOS transistors as they are typically sized with a ratio of 2:1 instead of a 5:1, compensating for the lower conductivity of PMOS devices. This results in an ideal p-type to n-type sizing ratio of 5:2 for the XOR gate design. However, our course kits only came CD4007B IC chips which do not allow manual adjustment of transistor sizes. Nonetheless, we have access to six NMOS and six PMOS transistors. This makes it possible to implement the required number of devices for a standard XOR gate. While the sizes are not adjustable, the performance of the NMOS and PMOS transistors closely matches the ideal ratio, allowing our circuit to almost operate as a functional XOR gate and closely match its timing behavior.

## Functional Testing:

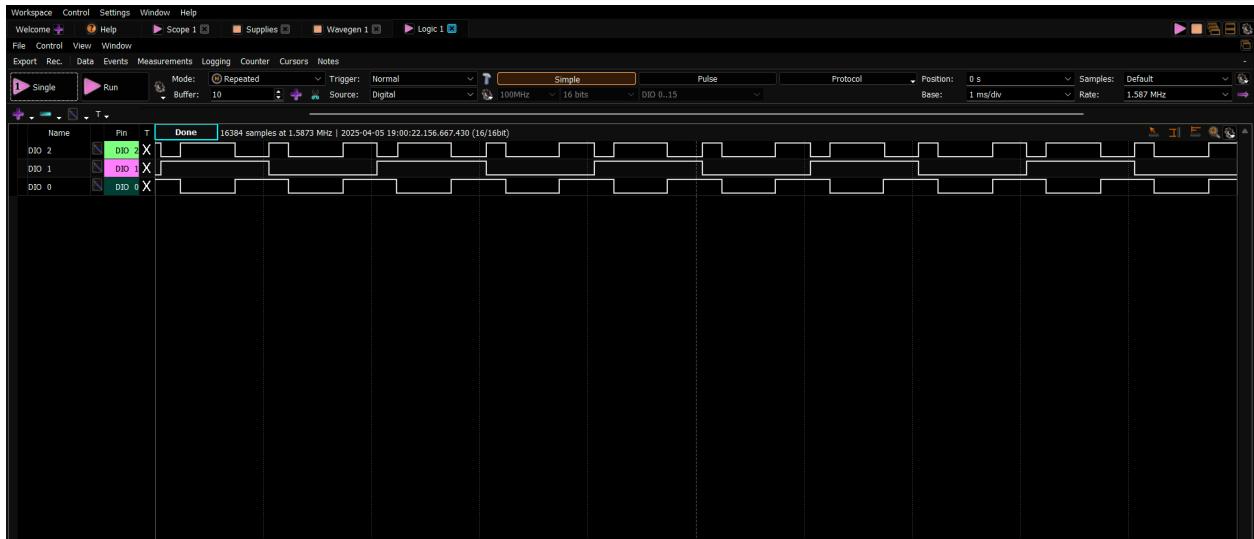


Figure 3: Logic Analyzer (DIO 2 = output, DIO 1 = A, DIO 0 = B)

To check if our XOR gate worked properly, we used the digital I/O pins on the AD3. DIO 0 and DIO 1 were set as inputs and DIO 2 was set as an output. Each was connected to the wave generator so we could cycle through all four possible input combinations: 00, 01, 10, and 11. By monitoring the output from the on DIO 2 using the AD3, it can be observed that, the output went HIGH when one input was HIGH and the other was LOW (01 or 10), and stayed LOW when both inputs were the same (00 or 11). This result matches the XOR truth table and confirmed that our circuit was wired correctly and functioning as intended.

# Static Level Testing:

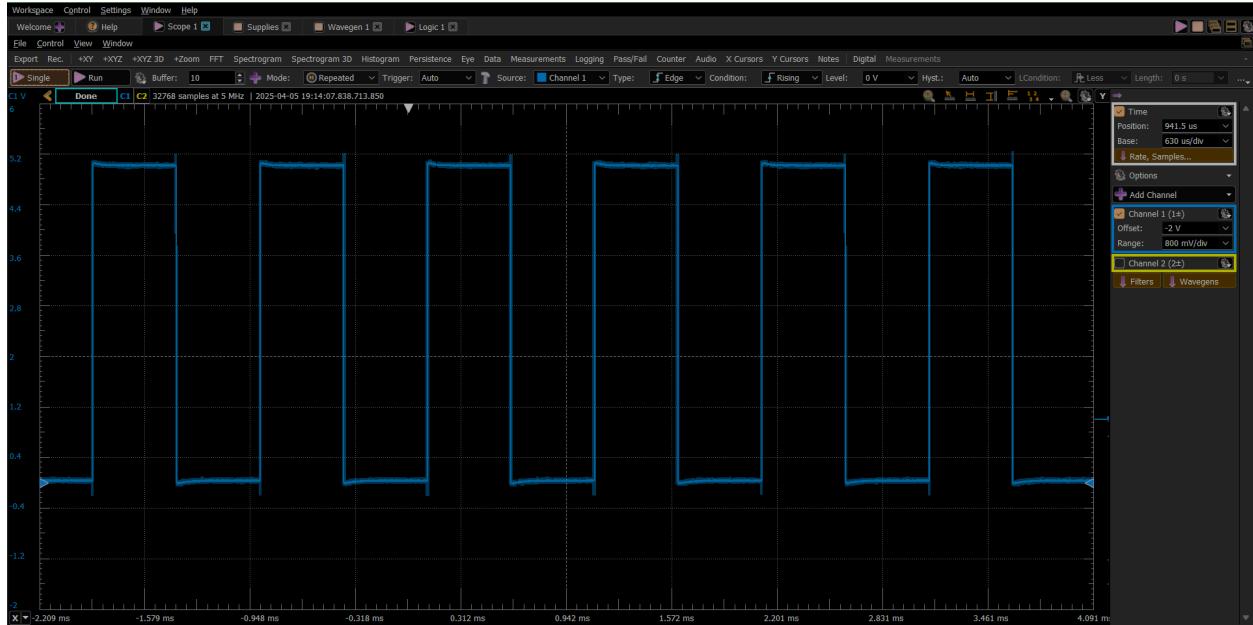


Figure 4: AD3 scope for static level testing, input A as HIGH and input B as a square waveform

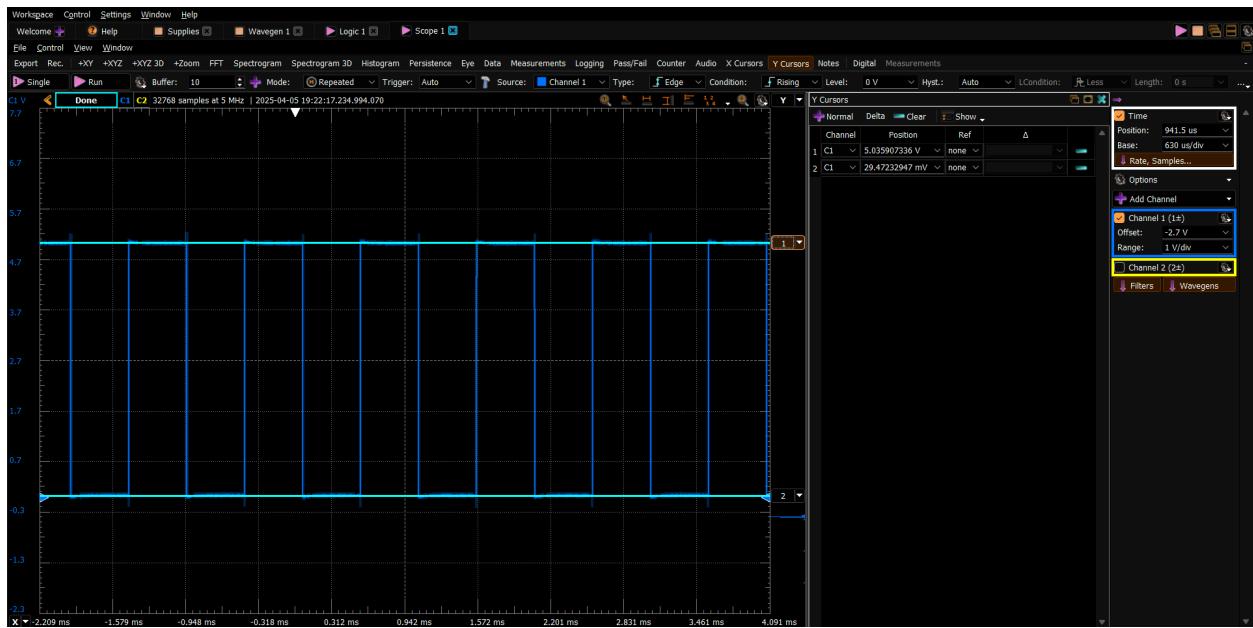


Figure 5: AD3 scope for static level testing



Figure 6: AD3 scope for static level testing with swapped inputs

To examine how the XOR gate handles logic levels, input A was fixed at a constant 5V (HIGH), and input B had a square wave applied, ranging from 0V to 5V. With this setup, the output voltage reached a high value of 5.0359 V, representing the peak voltage and a minimum value of 29.472 mV, representing the minimum voltage, As seen in figure 5.

We then swapped the two inputs and repeated the test. This time, the output measured a peak value of 5.0398V of and minimum value of 33.462 mV, as seen in Figure 6. Even though there was a small difference in the readings, especially in the low voltage value, the variation is so minor that it is almost negligible and did not impact the logic behavior of the XOR gate.

## Timing:

To measure how quickly the XOR gate responds to input changes, we monitored the rise and fall times for the output signal. This defines the time it takes for the output voltage to switch between 10% and 90% of its whole voltage range (HIGH & LOW). For rise time, we looked at how long it took for the output to go from 10% up to 90% of its peak value. For fall time, we measured the time it took to drop from 90% down to 10%. These thresholds were calculated based on the max & min values from the waveform.

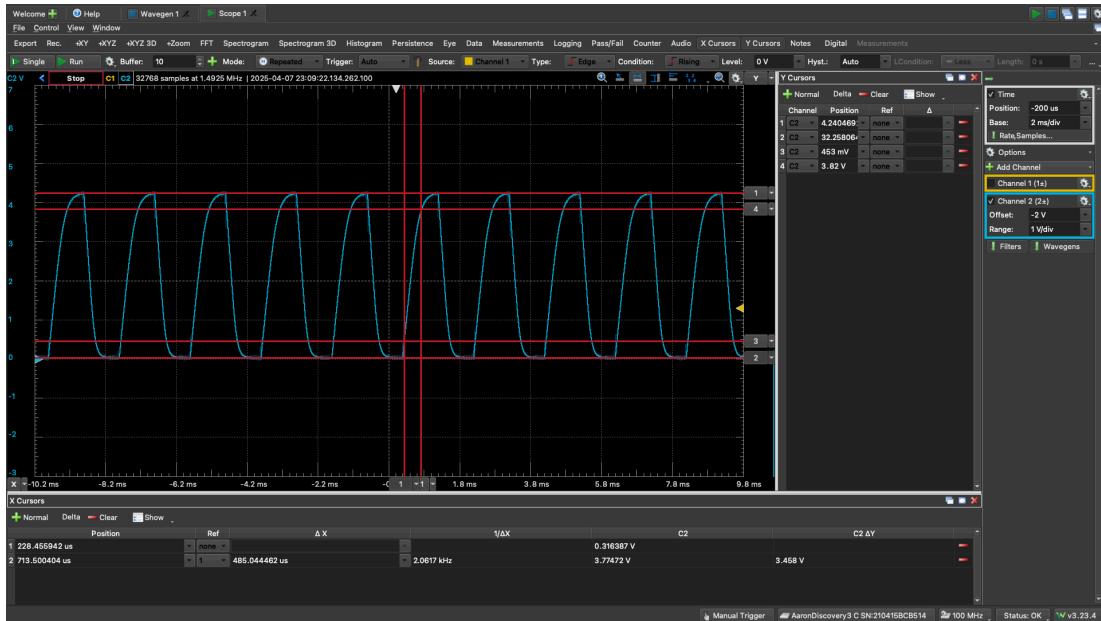


Figure 7: AD3 scope measuring the rise time with a capacitor

Figure 7 shows the output waveform used to measure the rise time. The minimum and maximum output voltages were recorded as 4.24 V and 32.25 mV, giving a total voltage swing of 4.207 V. Using these values, the 10% and 90% threshold voltages were calculated to be 453 mV and 3.82 V. With the oscilloscope cursors placed at these points on the rising edge, the time it took for the voltage to transition between them was measured to be 485  $\mu$ s. This rise time showcases the effects of the 100 nF capacitor, adding some delay.

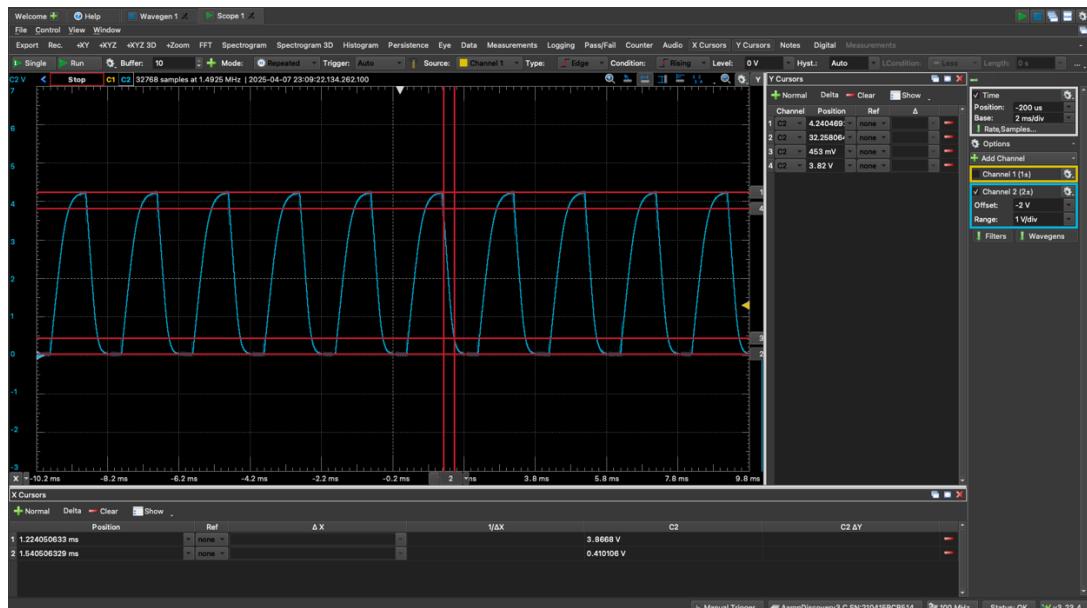


Figure 8: AD3 scope measuring the fall time with a capacitor

In Figure 8, the output voltage swing remained at 4.207 V, the 10% and 90% threshold levels also stayed the same as in the rise time calculation. During the falling edge, the time it took for the output voltage to drop between these two points was measured using oscilloscope cursors and found to be 316  $\mu$ s. This fall time showcases how the 100 nF capacitor discharges, affecting how fast the output voltage decreases.

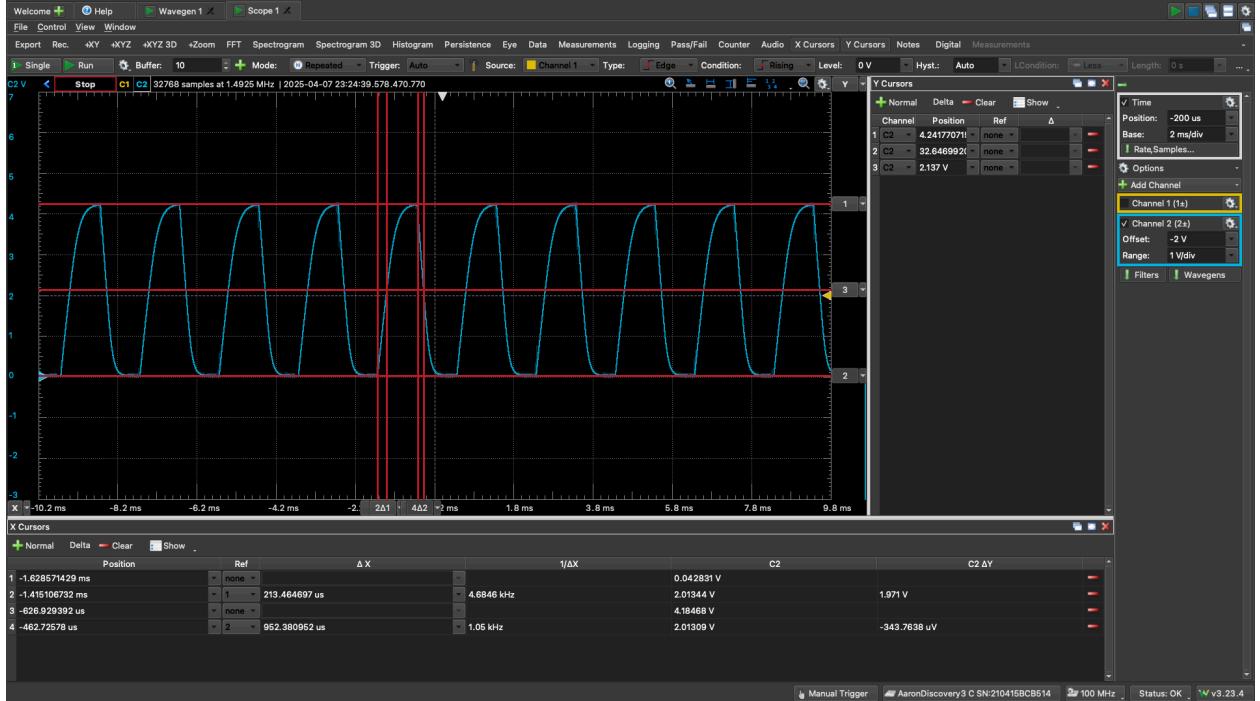


Figure 9: Measuring  $T_{PHL}$  with a capacitor as load

To measure propagation delay, we looked at when the input and output signals crossed the halfway point of the output voltage, which was around 2.137 V. For the rising edge, the delay between the input reaching that point and the output following was 213  $\mu$ s ( $\tau_{PLH}$ ). For the falling edge, the delay was 952  $\mu$ s ( $\tau_{PHL}$ ). Using these values, the average of can be used to calculate the total delay of the circuit, which was 582.5  $\mu$ s. This tells us how quickly the XOR gate reacts when the input changes.

$$(\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2} = \frac{213 \mu s + 952 \mu s}{2} = 582.5 \mu s)$$

## References:

- [1] A. S. Sedra, K. C. Smith, T. C. Carusone, and V. Gaudet, *Microelectronic Circuits*, 8th ed. New York, NY, USA: Oxford Univ. Press, 2019. [Accessed Mar. 26, 2025]
- [2] “Project 2”, Avenue to Learn, March 25, 2025 [Accessed Mar. 26, 2025]
- [3] National Semiconductor Corporation, “MOS Data Sheets - CD4007M/CD4007C Dual Complementary Pair Plus Inverter.” National Semiconductor, Feb. 1988. [Accessed Mar. 26, 2025]