Arunabha Ghosh

647-675-3762 | aaronghosh9@gmail.com | linkedin.com/in/aaron-ghosh | github.com/aaronghsh

Education:

McMaster University **Expected Graduation April 2027**
Bachelor of Engineering in Electrical Engineering (B.Eng.)(Co-op) *Hamilton, Ontario*

Relevant Coursework:

- Digital Logic Design
- Control Systems
- Data Structures and Algorithms
- Signals and Systems
- Microprocessor Systems
- Communication Systems

Skills:

Languages: Python, Perl, C, C++, Assembly, SystemVerilog, VHDL, MATLAB, Bash, R, TypeScript, JavaScript, Git
Development Tools: Cadence OrCAD PSpice, GitHub, Intel Quartus, ModelSim, Autodesk Suite, Altium Design
Design Concepts: RTL Design, UVM Verification, FPGA Programming, PCB Design, Static Timing Analysis

Experience:

Supply & Demand **May 2025 – August 2025**
Experience Technician *Mississauga, Ontario*

- Calibrated projection-mapping systems using OpenCV and LiDAR-based motion sensors to ensure precise spatial alignment and real-time collision detection within interactive exhibits
- Integrated AR subsystems with physical display modules, synchronizing virtual overlays to user motion data for a seamless mixed-reality experience
- Diagnosed and resolved performance issues across hardware and network systems, reducing latency while improving overall accuracy and reliability

City of Brampton **February 2023 – November 2023**
STEM Instructor *Brampton, Ontario*

- Mentored 25+ students weekly about engineering principles and values through interactive learning modules
- Facilitated critical thinking skills through hands-on activities such as robotics, coding, and circuit design
- Coordinated closely with 5 other instructors to ensure students with a welcoming environment that helps foster innovation, teamwork, and creativity

Projects:

Configurable Memory Controller: *Perl, SystemVerilog, Intel Quartus, ASIC/SoC Design, UVM* **November 2025**

- Implemented a **parameterized memory controller** in SystemVerilog following **ASIC and SoC design principles**, supporting configurable burst length, data width, and latency cycles
- Designed **synthesizable RTL** with distinct **read/write FSMs** and ready/valid handshake protocols
- Developed a **UVM-based testbench** for functional verification using randomized read/write transactions and scoreboard-driven validation
- Automated design verification with **Perl scripts** that generate concise CSV summaries of simulation results

3D LiDAR Scanner: *C, Python, Assembly, Open3D, Microcontroller, Embedded Systems* **April 2025**

- Engineered an embedded system capable of 3D spatial mapping using a **TI-MSP432E401Y microcontroller**, **VL53L1X Time-of-Flight sensor**, and **28BYJ-48 stepper motor**
- Programmed in **C** and **Assembly**, transmitted real-time data from the sensor to the MCU via **I2C**, then via **UART** to a Python-based visualization script
- Rendered **interactive 3D point clouds** using **Open3D** and visualized scanned environments with accurate spatial depth

CMOS XOR Gate: *MOSFETS, Digital Logic, AD3, Circuit Design, PSpice* **March 2025**

- Prototyped a **CMOS XOR logic gate** using discrete **NMOS** & **PMOS** transistors from CD4007B ICs
- Verified functionality using **logic analyzers** and static/dynamic waveform tests
- Measured rise/fall times and propagation delay to **validate signal integrity** and response time
- Validated gate logic through voltage-level and timing analysis, ensuring correct XOR behavior and level transition

AC–DC Power Supply: *Zener Diodes, RC Filter Circuit, AD3, Circuit Design, PSpice* **February 2025**

- Designed a DC power supply converting 120 V AC (1 kHz) to 3 V DC ± 0.1 V at 10 mA using a **full-wave center-tapped rectifier** and **RC filter network**
- Optimized **RC filter performance** in PSpice to minimize output ripple voltage and maximize rectifier efficiency and maintain voltage stability under variable load conditions
- Validated waveform integrity and output stability, achieving 97% correlation between simulated and measured waveforms