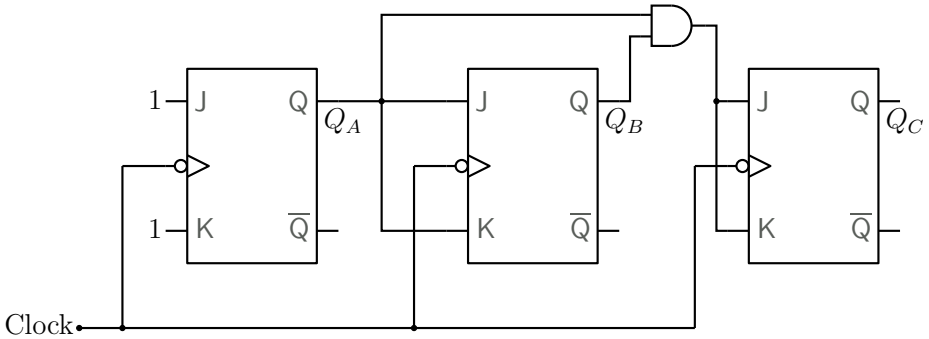
EE 112 (MBP): HW 2 (January 2017)

1. Sketch Q_A, Q_B, Q_C for 8 clock pulses, assuming $Q_A = Q_B = Q_C = 0$ in the beginning.



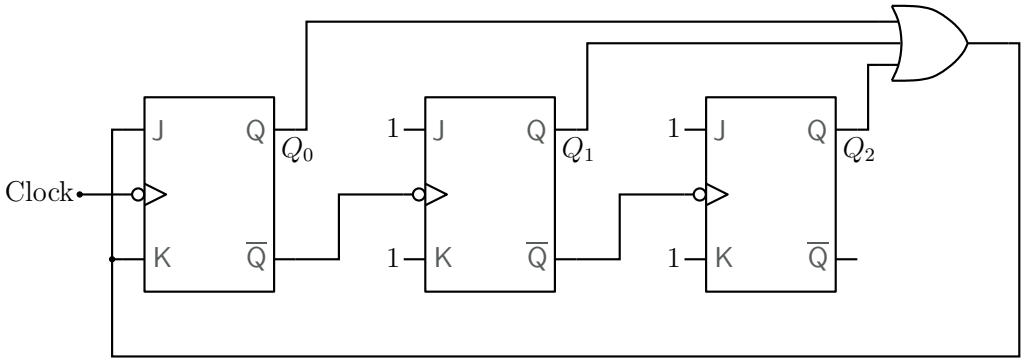
2. Simplify the Boolean expression, $Y = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,\overline{B}\;\overline{C} + A\,\overline{B}\,C$

3. Obtain a minimal sum-of-products form for

   (a) $Y = \overline{A}\,B\,\overline{C}\;\overline{D} + A\,B\,\overline{C}\;\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,\overline{B}\,C\,\overline{D}$

   (b) $Y = \overline{A}\;\overline{B}\;\overline{C}\;\overline{D} + \overline{A}\;\overline{B}\;\overline{C}\,D + \overline{A}\,B\,\overline{C}\;\overline{D} + \overline{A}\,B\,\overline{C}\,D + A\,B\,C\,D + A\,B\,C\,\overline{D}$

4. Sketch Q_2, Q_1, Q_0 for 10 clock pulses, assuming $Q_2 = Q_1 = Q_0 = 1$ in the beginning.



5. Design decoding logic in order to get a square wave output with frequency $f_c/8$ (where f_c is the clock frequency) and a duty cycle of $\dfrac{3}{8}$ (37.5 %) for the counter of Q 1.

6. Design decoding logic in order to get a square wave output with frequency $f_c/4$ (where f_c is the clock frequency) and a duty cycle of $\dfrac{1}{4}$ (25 %) for the counter of Q 1.