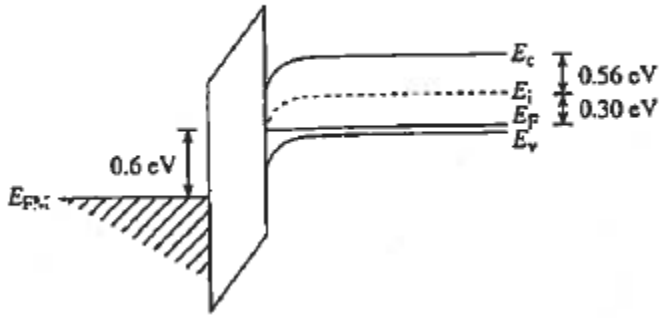
ASSIGNMENT 4

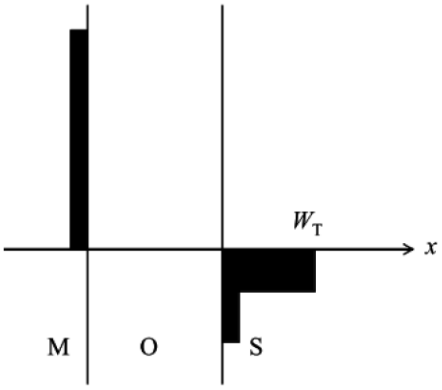
MOSCAP & BJT (Total Marks = 65)

Q1) The following figure is a dimensioned energy band diagram for an ideal MOSCAP at T=300K, $V_G \neq 0$, x_o=0.1μm. Note that $E_F = E_i$ at the Si—SiO_2 interface. **(1+2+2+2- 7Marks)**



a) Does equilibrium condition prevail inside the semiconductor?
b) Determine φ_F (fermi level), φ_S, V_G, x_o (depletion width).
c) Draw the block charge diagram.
d) Sketch the shape of low frequency C-V characteristics with proper marking.

Q2) The DC state of an ideal MOS-capacitor is characterized by the block charge diagram shown in the following figure. **(2 marks each - 10 marks)**



a) (i) Is the semiconductor n- or p-type? Explain.
(ii) Is the device accumulation, depletion or inversion biased? Explain.

b) Draw the energy band diagram corresponding to the charge state pictured in the block charge diagram.

c) By appropriately modifying the block charge diagram, characterize the charge state inside the MOS-C when a high-frequency ac signal is applied to the device.

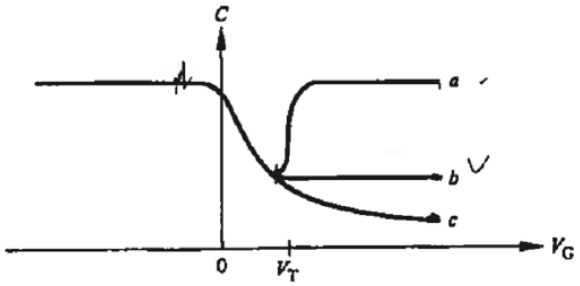
d) Sketch the general shape of the high-frequency C-V characteristic to be expected from the structure. Place a '×' on the C-V characteristic at a point that roughly correspond to the state pictured in the block charge diagram shown above.

e) While biased at the same gate voltage giving rise to the figure, the MOS-C is somehow totally deep depleted. Draw the block charge diagram describing the new state of the system.

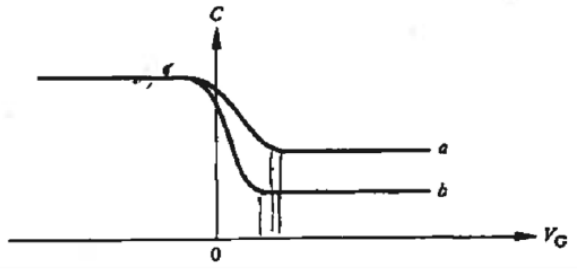
Q3) An ideal MOS is operated at T=300K, x_o=0.1 $\mu m(depletion\ width)$, N_D= $2X10^{15}cm^{-3}$ and area = 10^3cm^2. **(2+1+1+1= 5 Marks)**

a) Sketch the general shape of high frequency C-V characteristics.
b) Defining C_{max} to be the maximum high frequency capacitance, determine C_{max}.
c) Defining C_{min} to be the minimum high frequency capacitance, determine C_{min}.
d) If V_G=V_T, determine φ_S (surface potential).

Q4) i) Consider the C-V curves shown in figure (a). For which curve(s) is an equilibrium inversion layer present when $VG>VT$? Explain. **(1+1 marks)**
ii) C-V curves derived from two MOSCAPs with the same gate area are compared in figure (b). The MOSCAP exhibiting curve *b* has (choose one: a thinner, the same, a thicker) oxide and (choose one: a lower, the same, a higher) doping than the MOSCAP exhibiting curve *a*. Briefly explain how you arrived at your chosen answers. **(2+2 marks)**



(a)



(b)

Q5) An ideal MOS (φ_{MS} = 0) is operated at T=300K, x_o=0.1 μm, N_D= $2X10^{15}cm^{-3}$ and area = 10^3cm^2. **(2+2+1= 5Marks)**

a) Compute V_T.
b) Suppose the gate bias is such that $\phi_S = 3\phi_F/2$. Draw the MOS-C energy band diagram corresponding to the specified gate bias.
c) Suppose the gate bias is such that $\phi_S = 5\phi_F/2$ Draw the block charge diagram corresponding to the specified gate bias.

Q6) Consider a p-MOS capacitor with p+ poly-Si gate and n-Si substrate with no oxide and interface harges. HFCV measurements with slow ramp rate yields maximum and minimum capacitance values of C_{max}=$7\times10^{-7}F/cm^2$ and C_{min}=$3.25\times10^{-8}F/cm^2$, respectively. Assume gate Fermi level at suitable edge of the gate poly-Si band.

a) Draw the HFCV curve and mark accumulation, depletion and inversion regimes. **(1+1 marks)**
b) Find oxide thickness (t_{ox}), and substrate doping (N_D). **(1+2 marks)**
c) Find C_{FB},C_{MG} and mark them on HFCV in (a). **(1+1+1 marks)**
d) Calculate V_{FB} ,V_{MG} , V_T. **(1+1+1 marks)**
e) Plot band diagrams corresponding to flat band (FB), mid gap (MG) and threshold. **(3+3+3 marks)**

Hints:

- Use iterative method to find N_D.
- For calculating C_{FB}, assume d_{Si}=L_D. Here L_D is extrinsic Debye length.
- Flat band (FB), mid gap (MG) and threshold correspond to surface potential of ψ_{Si}=0, ϕ_F,$and\ 2\phi_F$, respectively.

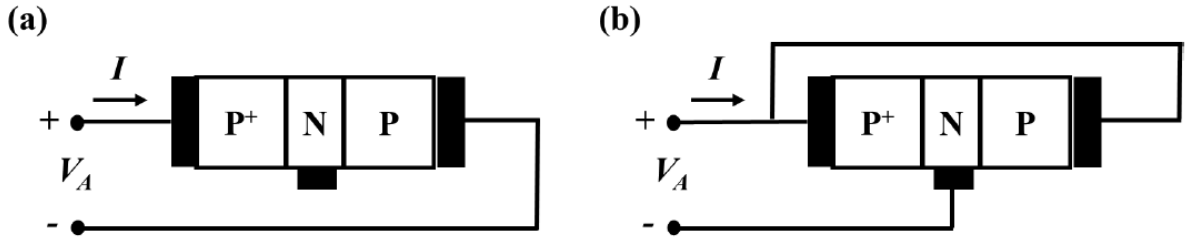
Use the following values for this particular problem.

ϵ_0=9×10$^{-14}F/cm$, ϵ_{Si}=12ϵ_0, ϵ_{ox}=4ϵ_0, kT=25 meV.

Q7) Consider an ideal MOSCAP (V_{FB}=0 V) with t_{ox}=100 $nm\ SiO_2$ (x=0 at the Si/SiO$_2$ interface and x=t_{ox} at the gate-metal/SiO$_2$ interface.). Assume E_i−E_F = 0.3 eV for silicon and ϵ_{SiO2} = 3.9ϵ_0 for SiO$_2$.

a) What is the threshold voltage (V_T) for given MOSCAP? **(2 Marks)**
b) If we introduce a sheet (two dimensional) charge with density Q_{ox} within the SiO$_2$ at x=x_{ox} (distance x_{ox} away from the Si/SiO$_2$ interface). What is the new V_{FB} and V_T? **(3 Marks)**

Q8) When one of the BJT terminals is left floating (unconnected) or two of the terminals are connected together, the BJT behaves like a diode. Consider a *pnp* BJT configured as shown:



Derive the $I\ vs.V_A$ relationship for this "diode" using the Ebers-Moll equations. (I should be expressed only in terms of VA and the Ebers-Moll parameters.) **(3+4 Marks)**