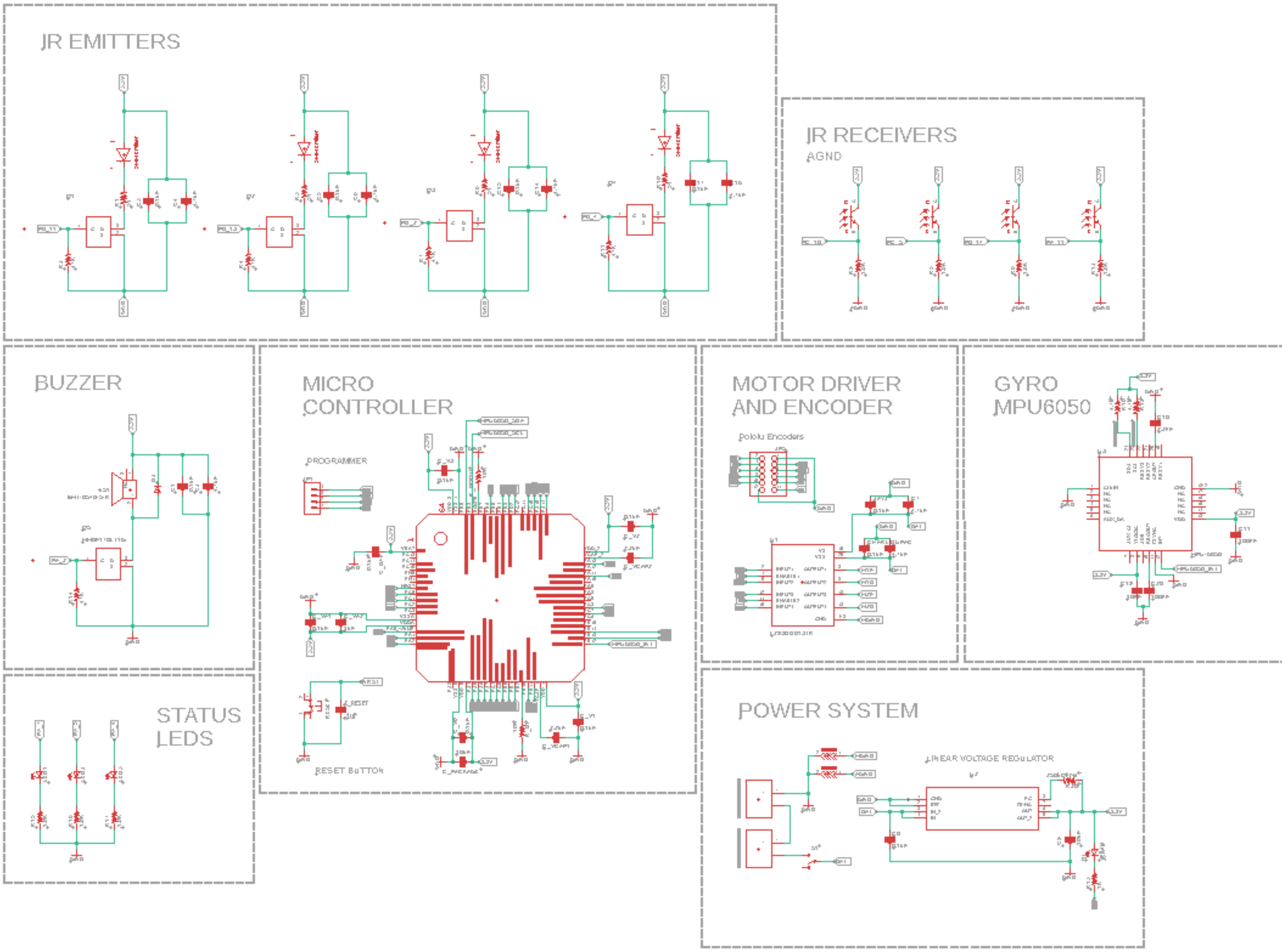
MICROMOUSE

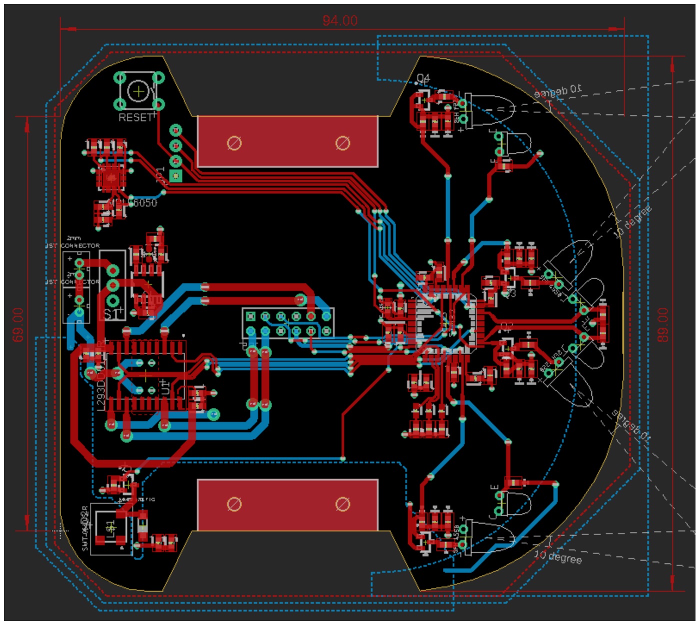
SCHEMATIC

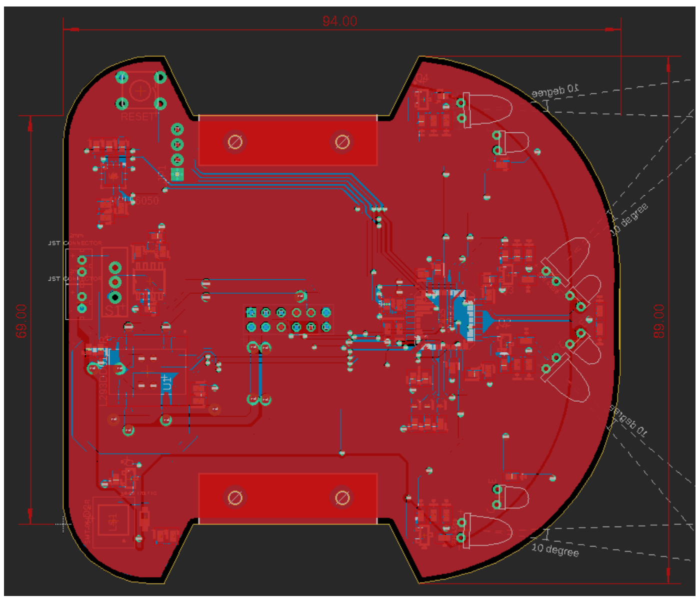


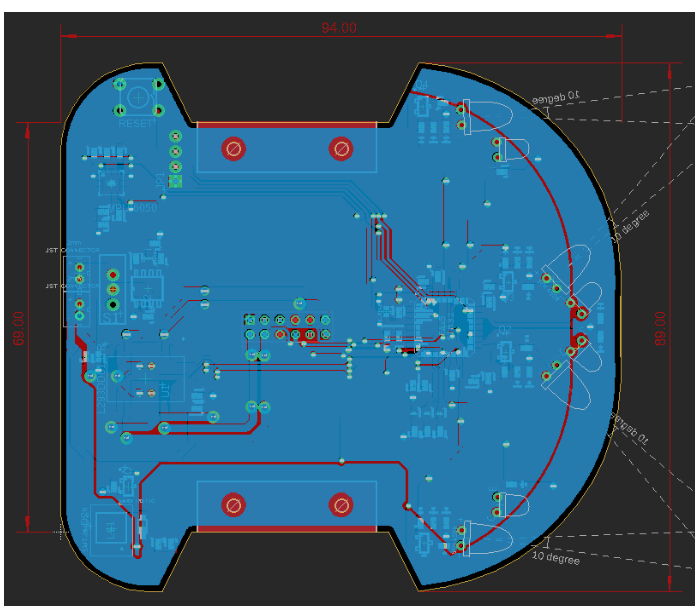
KEY SUMMARY

- 3-axis accelerometer and gyroscope (MPU6050) to measure speed and track the orientation of the mouse
- Status LEDs and a buzzer for easier debugging and interfacing with the microcontroller
- IR emitters and receivers to detect maze walls and corners
- Magnetic encoder to track the position of the mouse, and for precision turning and general maneuvering
- Dual H-bridge motor driver (L293DD) to change the direction of rotation of the brushed DC gearmotors
- Simple 3.3V LDO regulator (TPS76833Q) to power the microcontroller with minimal footprint
- On-board MCU (STM32F405RG) to run maze-solving algorithm and generic operations such as wall-detection and moving

BOARD (TOP & BOTTOM)

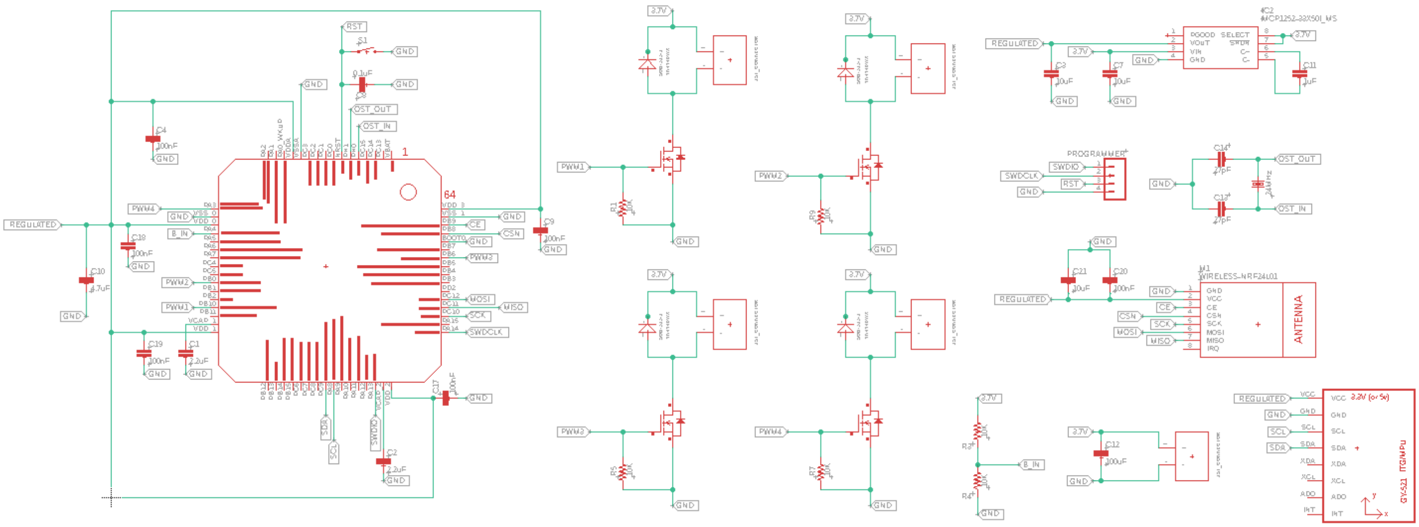




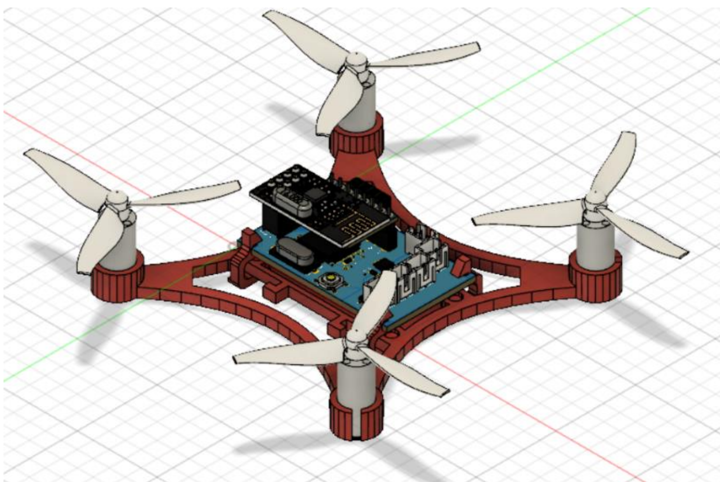


MINI QUADCOPTER

SCHEMATIC



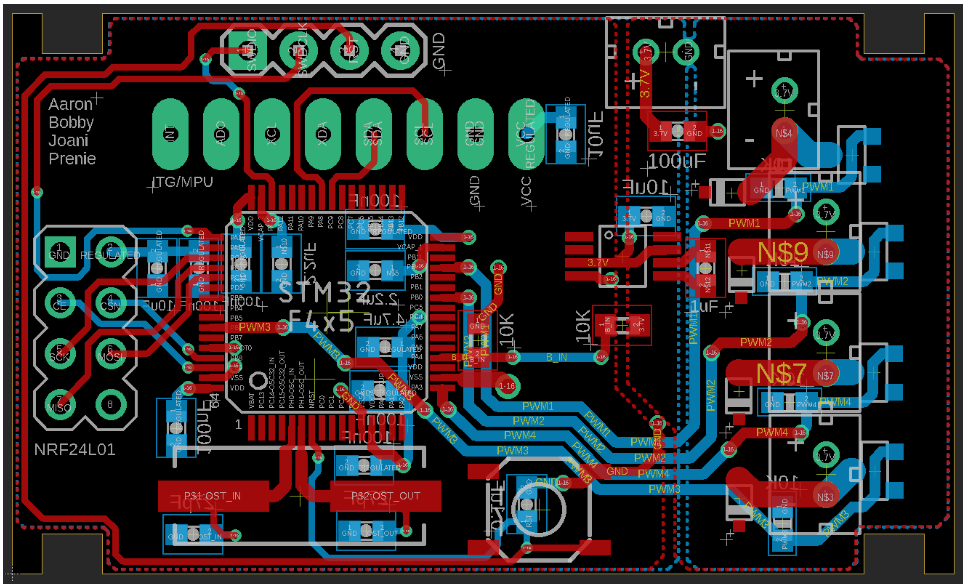
3D Model

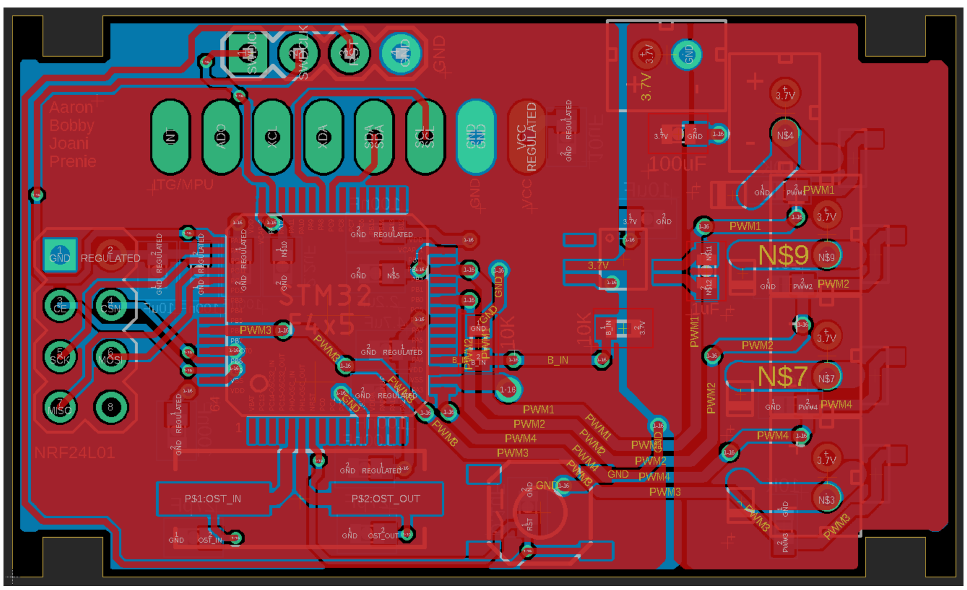


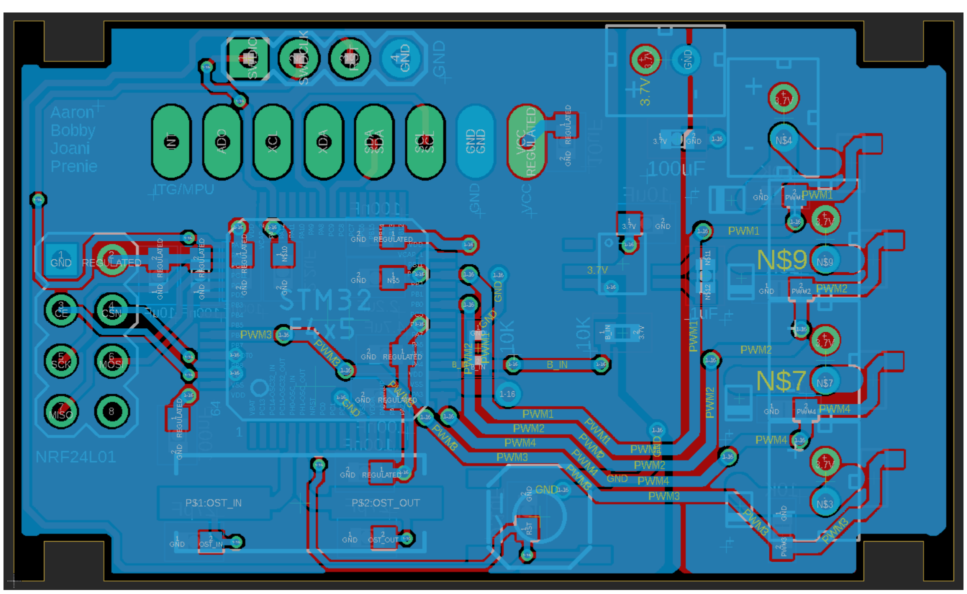
KEY SUMMARY

- 3-axis accelerometer and gyroscope (MPU6050) to track orientation of quadcopter for flight stability
- 2.4 GHz wireless transceiver (NRF24L01) to communicate with RC transmitter wirelessly
- Simple low-side drivers (BSS138) to drive 4 coreless DC motors
- External 24 MHz crystal oscillator (ABLS2) for accurate frequency and frequency stability
- 3.3V charge pump DC/DC converter (MCP1252) for low noise, higher efficiency, and a smaller footprint
- On-board MCU (STM32F405RG) to execute flight controller software code

BOARD (TOP & BOTTOM)

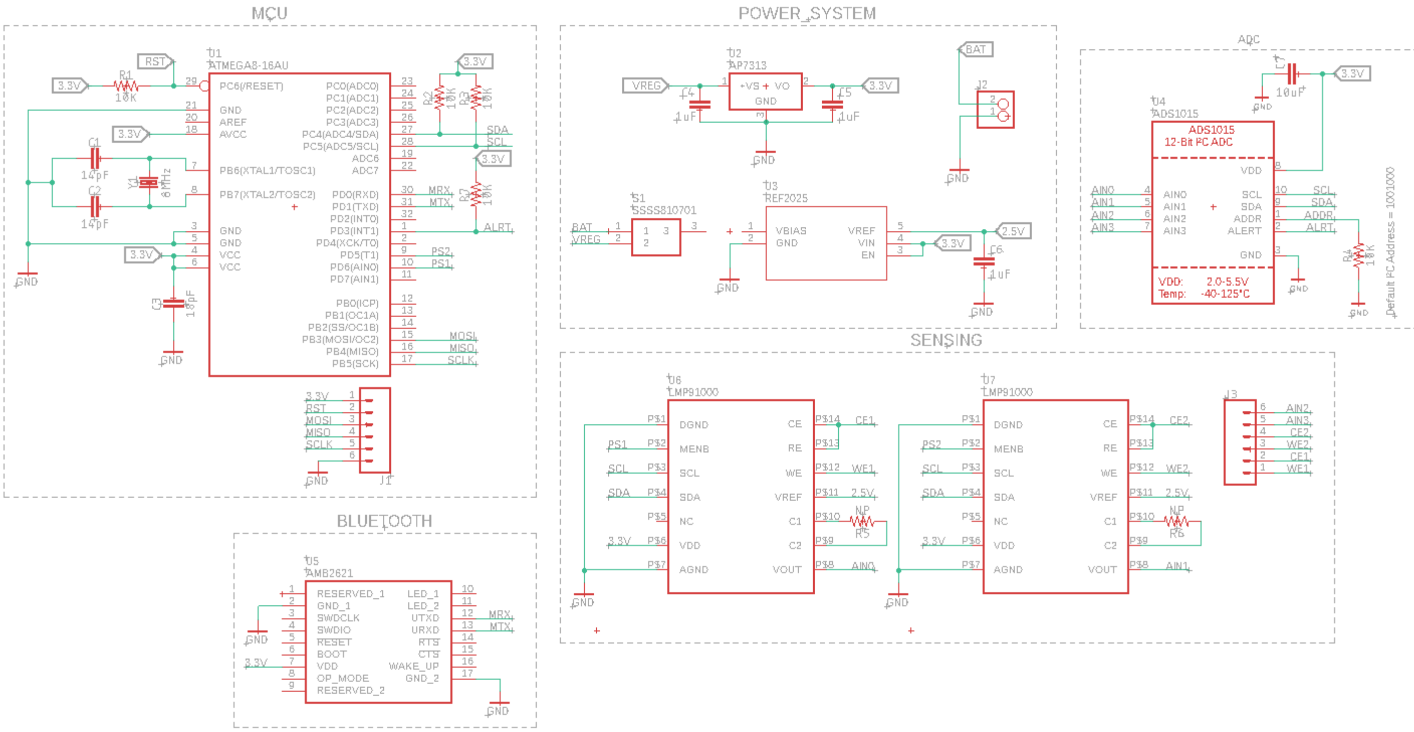






WEARABLE SWEAT SENSOR

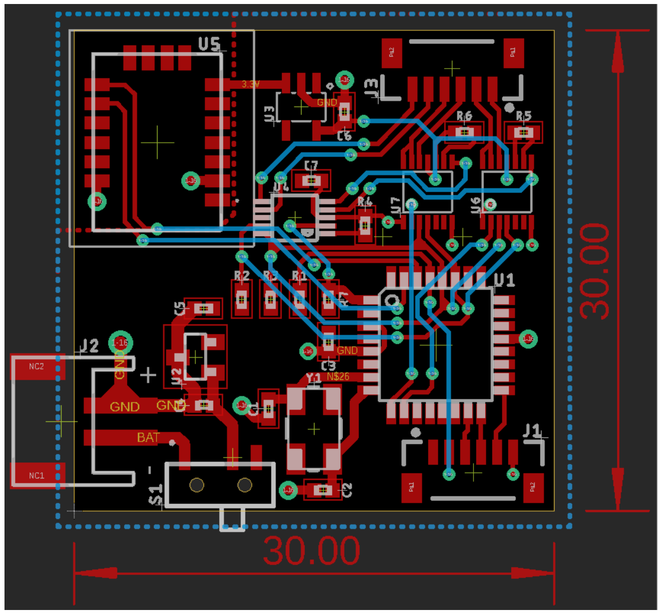
SCHEMATIC

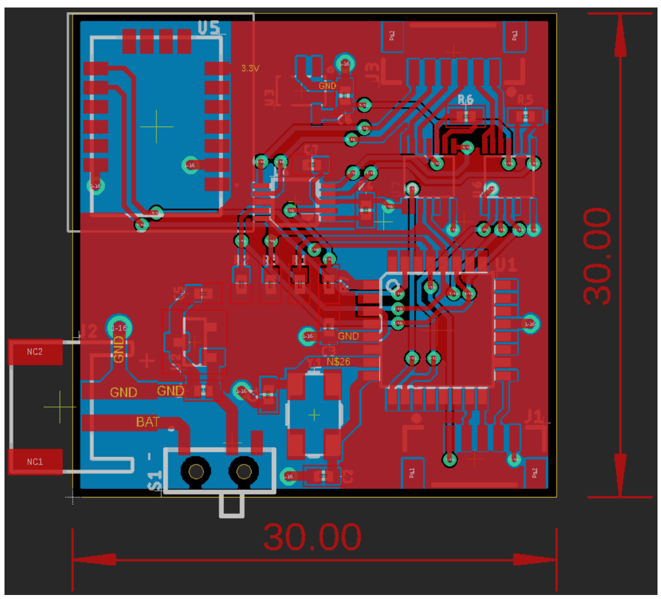


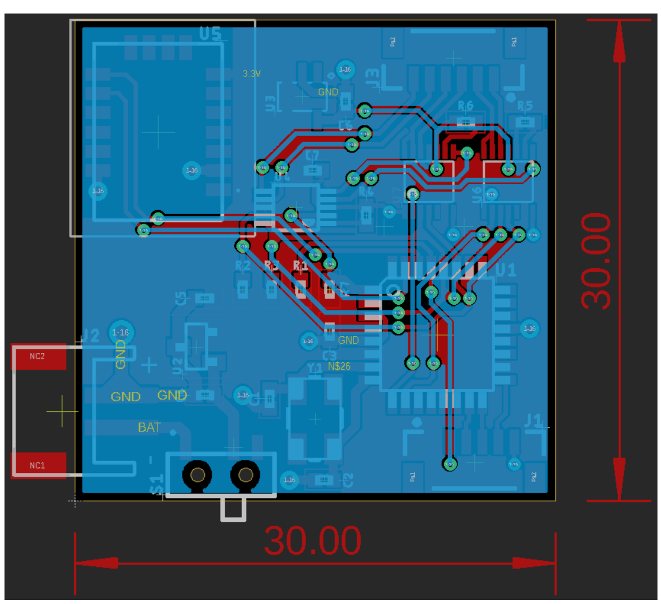
KEY SUMMARY

- Fully integrated wearable sensor arrays for multiplexed *in-situ* sweat analysis
- 12-bit ADC (ADS1015) for precise measurements of trace amounts of sweat metabolites and electrolytes
- AFE potentiostats (LMP91000) for low power electrochemical sensing
- BLE 4.2 module (AMB2621) to enable wireless functionality with a mobile application
- Simple 3.3V LDO regulator (AP7313) to power the ADC, potentiostats, and the ATmega8 chip

BOARD (TOP & BOTTOM)







A 1.25 GHz 0.23 pJ
4-bit Absolute-Value Detector
for use in Neural Spike Sorting

Aaron Lim
Prathyush Sivakumar

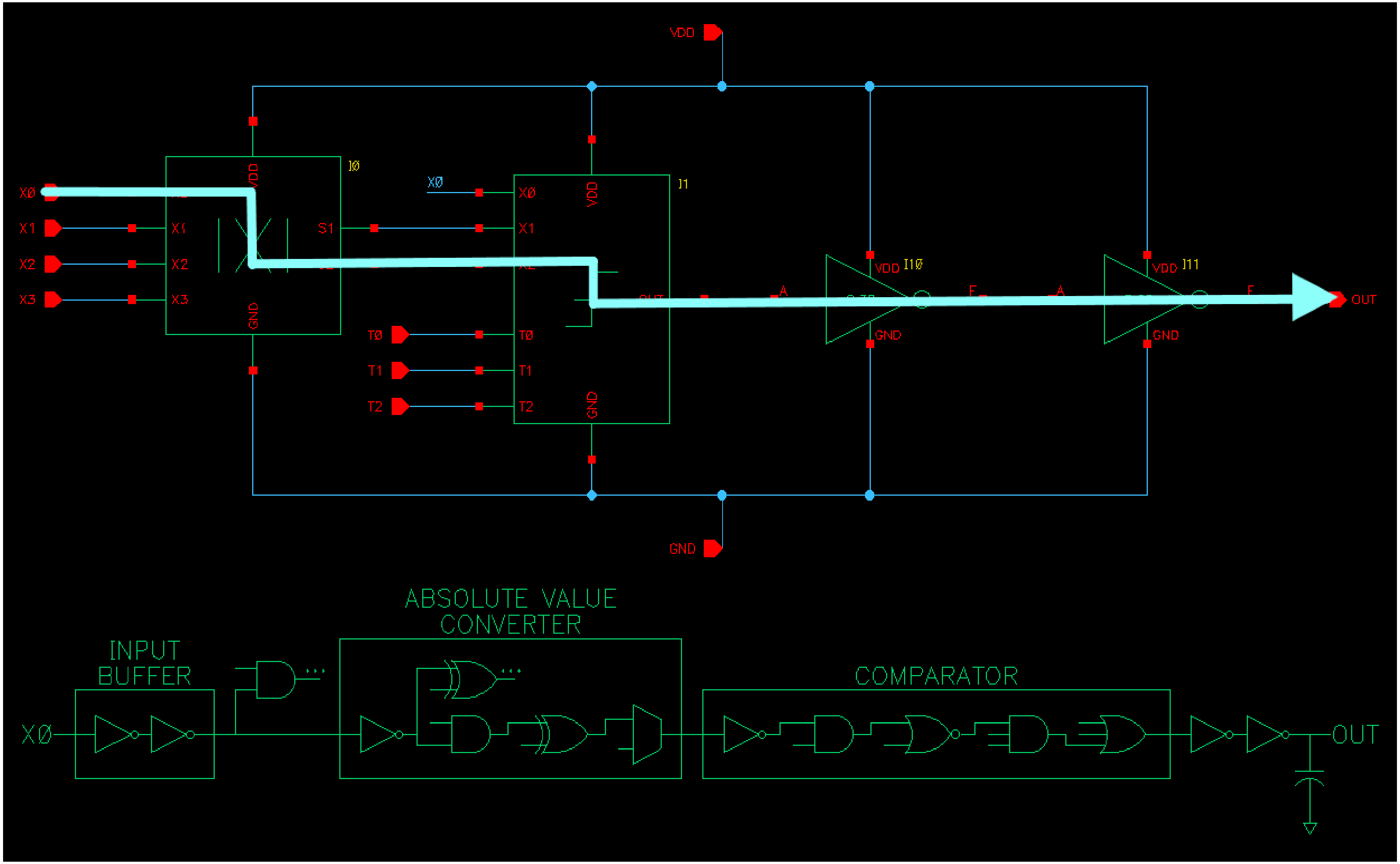
Design Summary

- Optimized 3-Bit Ripple-Carry Adder + Comparator, Static CMOS + Pass Transistor Logic (PTL)
- Moderate Area, Fast, Compact Design (Extra Room for Additional Logic)

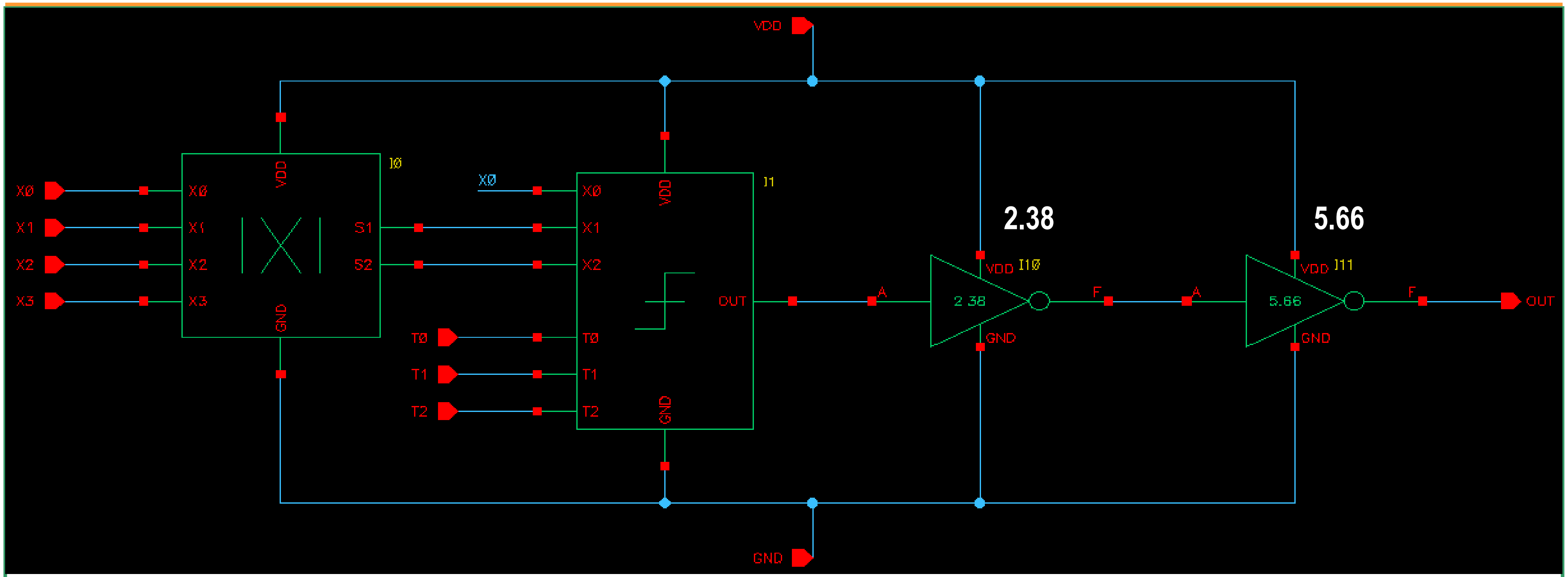
**VDD = 1V*

Schematic	Layout size	Energy	Verification
$t_{p\_X0\rightarrow OUT}$ = 778 ps	X= 21.6 µm	Sch E = 204 fJ	Func: Y / N
$t_{p\_X1\rightarrow OUT}$ = 620 ps	Y= 19.5 µm	Layout E = 226 fJ	DRC: Y / N
$t_{p\_X2\rightarrow OUT}$ = 524 ps	A = 421.2 µm^2		LVS: Y / N
$t_{p\_X3\rightarrow OUT}$ = 599 ps	AR = 1.11		
t_p = 778 ps			

Critical Path Analysis



Design Optimization



- Isolated high fan-out using sized output buffer (i.e. two sized inverters) to minimize delay
- Simplified adder design by realizing classes of inputs. Resulted in much fewer logic gates
- Used PTL for MUX and XOR to reduce no. of transistors to implement logic
- Used only 2 1-bit MUXs by realizing that MSB and LSB are always the same

Functionality Check (Schematic)

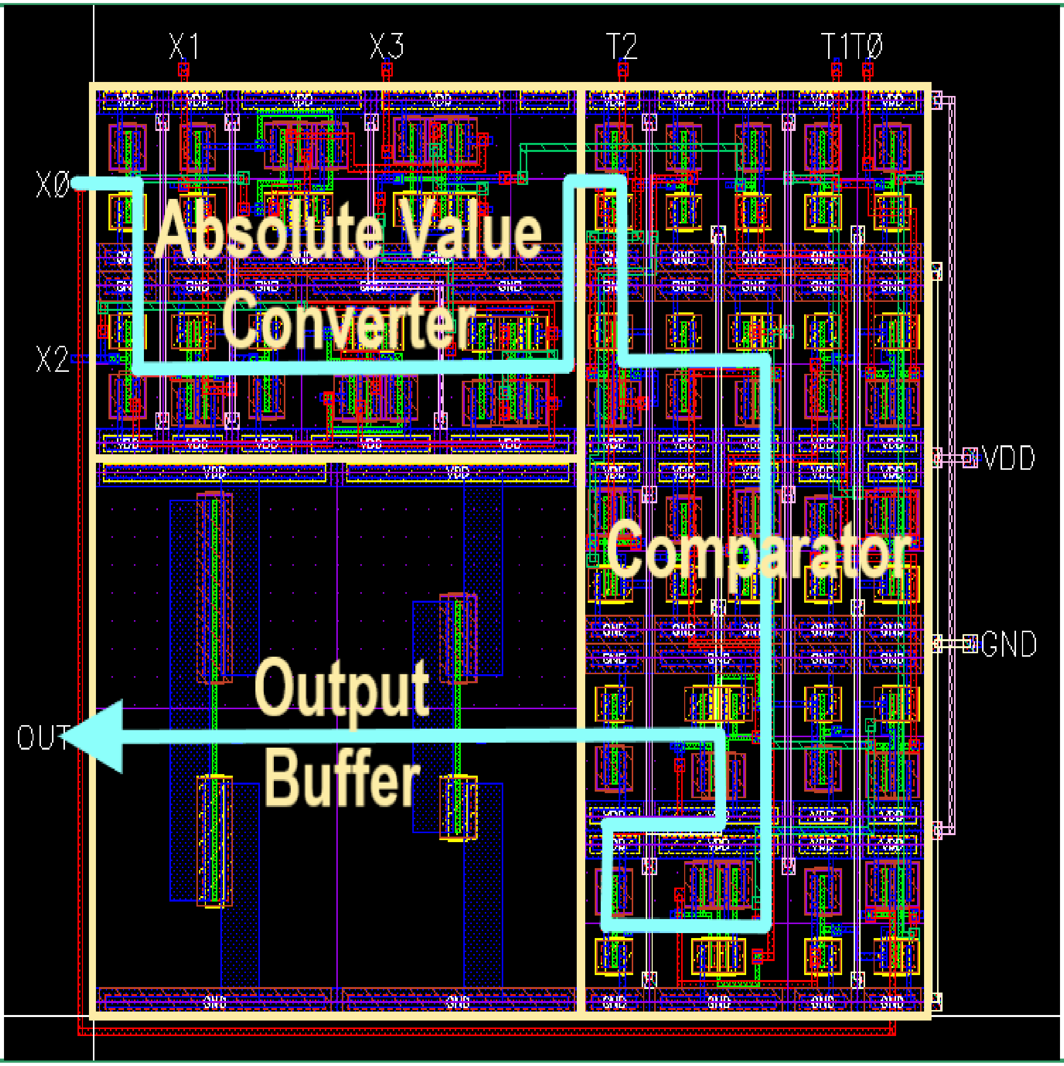
Absolute-Value Detector Layout

2 *Highlight critical path*

1 *Show layout*

6 *Anything else*

Density: 88.2%



3 *Indicate size*

Y = 19.5µm

X = 21.6µm

4 *AR, Area*

Aspect ratio: 1.11

Area: 421.2µm²

5

Discussion

- **Three most important features of your design**
  - Isolation of large load capacity / high fan-out using sized output buffer
  - PTL for MUX and XOR for reduced power consumption
  - Compact and systematic layout with room for extra logic
- **Given another chance, 3 things you would do different**
  - Perform further sizing analysis to achieve optimum propagation delay
  - Optimize critical path by reordering transistors