A 1.25 GHz 0.23 pJ 4-bit Absolute-Value Detector for use in Neural Spike Sorting

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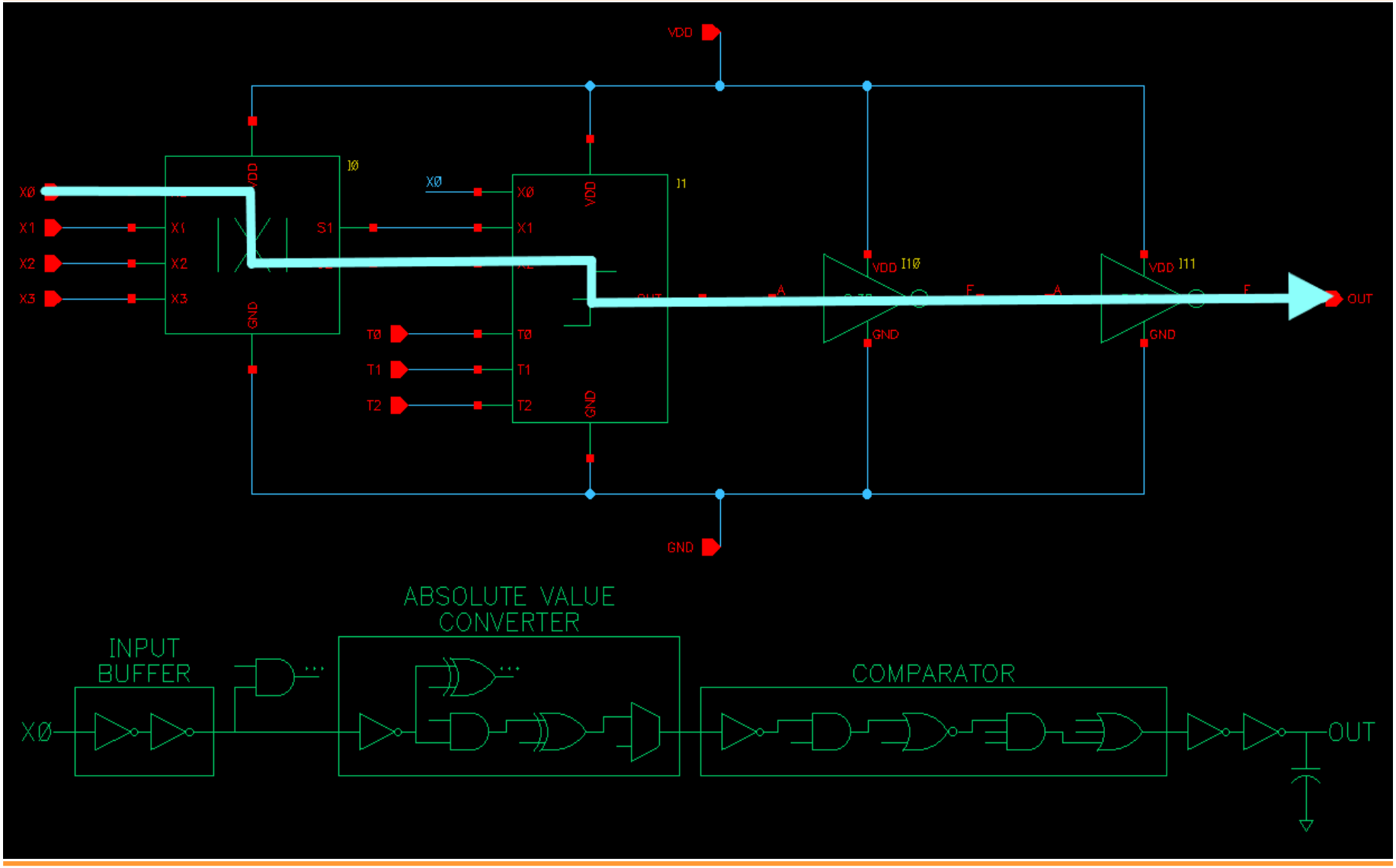
Design Summary

- Optimized 3-Bit Ripple-Carry Adder + Comparator, Static CMOS + Pass Transistor Logic (PTL)
- Moderate Area, Fast, Compact Design (Extra Room for Additional Logic)

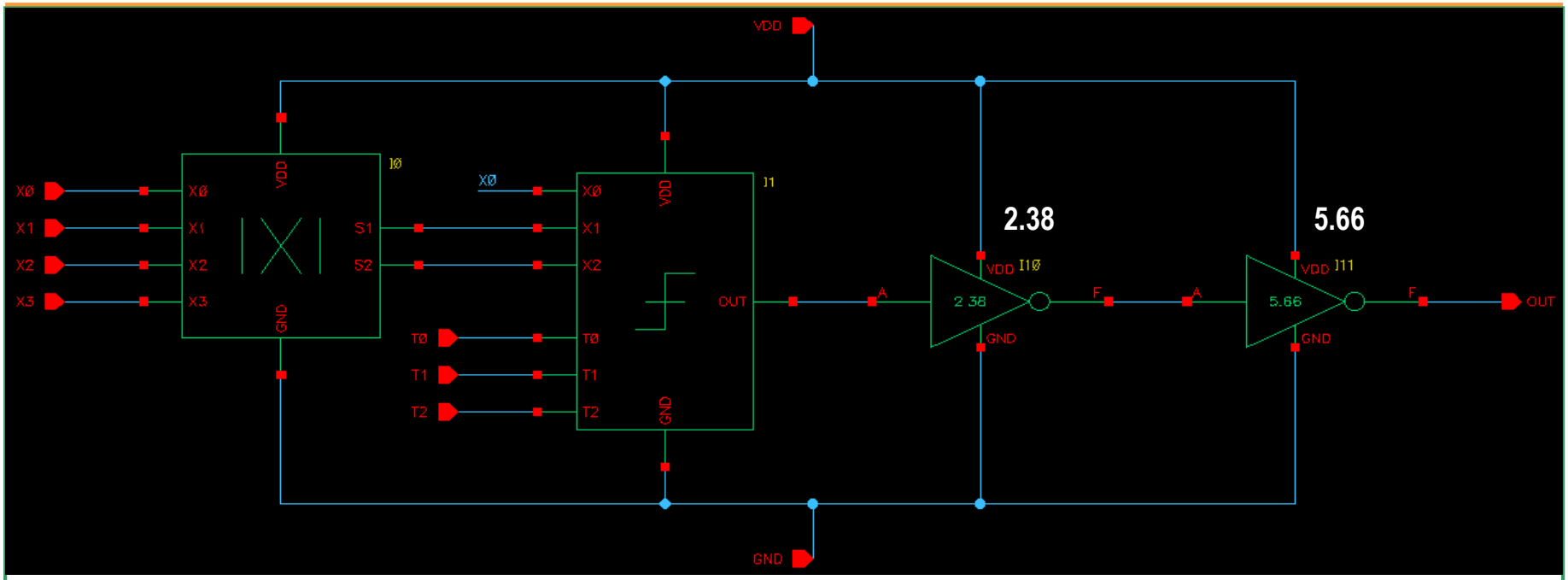
**VDD = 1V*

Schematic	Layout size	Energy	Verification
$t_{p\_X0\rightarrow OUT}$ = 778 ps	X= 21.6 µm	Sch E = 204 fJ	Func: Y / N
$t_{p\_X1\rightarrow OUT}$ = 620 ps	Y= 19.5 µm	Layout E = 226 fJ	DRC: Y / N
$t_{p\_X2\rightarrow OUT}$ = 524 ps	A = 421.2 μm^2		LVS: Y / N
$t_{p\_X3\rightarrow OUT}$ = 599 ps	AR = 1.11		
t_p = 778 ps			

Critical Path Analysis



Design Optimization



- Isolated high fan-out using sized output buffer (i.e. two sized inverters) to minimize delay
- Simplified adder design by realizing classes of inputs. Resulted in much fewer logic gates
- Used PTL for MUX and XOR to reduce no. of transistors to implement logic
- Used only 2 1-bit MUXs by realizing that MSB and LSB are always the same

Functionality Check (Schematic)

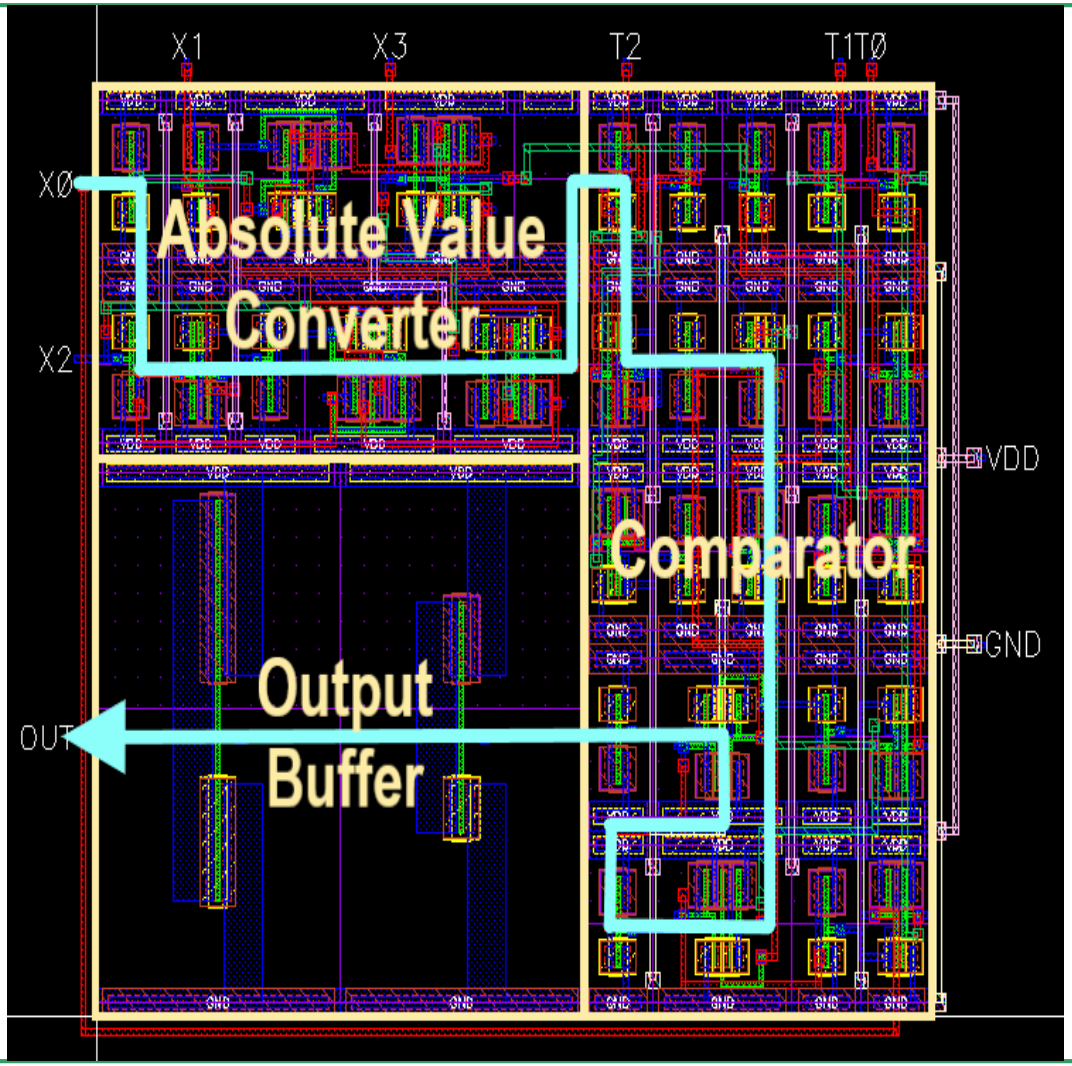
Absolute-Value Detector Layout

2 *Highlight critical path*

1 *Show layout*

6 *Anything else*

Density: 88.2%



3 *Indicate size*

Y = 19.5µm

X = 21.6µm

4 *AR, Area*

Aspect ratio: 1.11

Area: 421.2µm²

5

Discussion

- **Three most important features of your design**
  - Isolation of large load capacity / high fan-out using sized output buffer
  - PTL for MUX and XOR for reduced power consumption
  - Compact and systematic layout with room for extra logic
- **Given another chance, 3 things you would do different**
  - Perform further sizing analysis to achieve optimum propagation delay
  - Optimize critical path by reordering transistors