```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : EX_WB_tb
4   -- Design      : EX_WB
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : c:\my_designs\EX_WB\EX_WB\src\EX_WB_tb.vhd
11  -- Generated   : Fri May  1 14:34:57 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Testbench for the EX/WB register for storing the W_EN
    signal, ALU result, and the register to write back to.
18  --  Checks if the correct value is outputted from the register each clock
    cycle.
19  --
20  ------------------------------------------------------------------------
    ----
21  library work;
22  use work.all;
23  library IEEE;
24  use IEEE.std_logic_1164.all;
25  use IEEE.NUMERIC_STD.all;
26
27  entity EX_WB_tb is
28  end EX_WB_tb;
29
30  --}} End of automatically maintained section
31
32  architecture EX_WB_tb of EX_WB_tb is
33  signal CLK, I_W_EN, O_W_EN : std_logic;
34  signal I_Res, O_Res : std_logic_vector(127 downto 0);
35  signal I_regD, O_regD : std_logic_vector(4 downto 0);
36  constant period : time := 20ns;
37  begin
38
39      uut : entity EX_WB port map (CLK => CLK, I_W_EN => I_W_EN, O_W_EN =>
    O_W_EN, I_Res => I_Res, O_Res => O_Res,
40          I_regD => I_regD, O_regD => O_regD);
41
42      clk_process : process
43      begin
44          CLK <= '0';
45          wait for period/2;
46          CLK <= '1';
47          wait for period/2;
48      end process;
49
50      tb : process
```

```
51      begin
52          wait for period/2;
53
54          I_W_EN <= '1';
55          I_Res <= (others => '1');
56          I_regD <= (others => '1');
57          wait for period;
58
59          I_W_EN <= '0';
60          I_Res <= (127 downto 64 => '1', others => '0');
61          I_regD <= (4 downto 3 => '1', others => '0');
62          wait for period;
63
64          I_W_EN <= '1';
65          I_Res <= (63 downto 0 => '1', others => '0');
66          I_regD <= (2 downto 0 => '1', others => '0');
67          wait for period;
68
69          I_W_EN <= '0';
70          I_Res <= (others => '0');
71          I_regD <= (others => '0');
72          wait for period;
73
74          wait;
75
76      end process;
77
78  end EX_WB_tb;
79
```