File: C:/my_designs/Instruction_Fetch/Instruction_Fetch/src/IF_Stage_tb.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : IF_Stage_tb
4   -- Design      : Instruction_Fetch
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        :
    C:\my_designs\Instruction_Fetch\Instruction_Fetch\src\IF_Stage_tb.vhd
11  -- Generated   : Sat May  2 21:01:38 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description :  Testbench for the IF stage. After loading the Instruction
    Buffer with the instructions from the text file,
18  --  checks if the instructions from the buffer are being outputted at each
    clock cycle.
19  --
20  ------------------------------------------------------------------------
    ----
21  library work;
22  use work.all;
23  library IEEE;
24  use IEEE.std_logic_1164.all;
25  use IEEE.NUMERIC_STD.all;
26  use std.textio.all;
27  use ieee.std_logic_textio.all;
28
29  entity IF_Stage_tb is
30  end IF_Stage_tb;
31
32  --}} End of automatically maintained section
33
34  architecture IF_Stage_tb of IF_Stage_tb is
35  signal Instruction_Index : std_logic_vector(5 downto 0);
36  signal CLK : std_logic;
37  signal Instruction_Data, Instruction : std_logic_vector(24 downto 0);
38  constant period : time := 20ns;
39  begin
40
41      uut : entity IF_Stage port map (Instruction_Index => Instruction_Index,
    CLK => CLK, Instruction_Data => Instruction_Data, Instruction =>
    Instruction);
42
43      store : process
44      file F : TEXT open READ_MODE is "ESE345_Assembler.txt";
45      variable L : LINE;
46      variable temp : std_logic_vector(24 downto 0);
47      variable count : unsigned(5 downto 0) := "000000";
48      begin
```

```
49      if not ENDFILE(F) then
50              READLINE(F, L);
51              READ(L, temp);
52              Instruction_Data <= temp;
53              Instruction_Index <= std_logic_vector(count);
54              count := count + 1;
55          end if;
56          wait for period;
57      end process;
58
59      clk_process : process
60      begin
61          CLK <= '0';
62          wait for period/2;
63          CLK <= '1';
64          wait for period/2;
65      end process;
66
67  end IF_Stage_tb;
68
```