File: C:/my_designs/EX/EX/src/EX_tb.vhd (/EX_tb)

```
1   ----------------------------------------------------------------------------
    ----
2   --
3   -- Title       : EX_tb
4   -- Design      : EX
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
    ----
9   --
10  -- File        : C:\my_designs\EX\EX\src\EX_tb.vhd
11  -- Generated   : Tue Apr 28 13:21:20 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
    ----
16  --
17  -- Description : Testbench for the EX stage. Tests the some of the ALU's
    capability of 29 Instructions. Also tests if the correct input is passed
18  --  to the ALU inputs depending on the forwarding selector bits.
19  --
20  ----------------------------------------------------------------------------
    ----
21  library work;
22  use work.all;
23  library IEEE;
24  use IEEE.std_logic_1164.all;
25  use IEEE.NUMERIC_STD.all;
26
27  entity EX_tb is
28  end EX_tb;
29
30  --}} End of automatically maintained section
31
32  architecture EX_tb of EX_tb is
33  signal Mux1_Selector, Mux2_Selector, Mux3_Selector : std_logic;
34  signal I_regA, I_regB, I_regC, I_forward, Res : std_logic_vector(127 downto
    0);
35  signal ALUop : std_logic_vector(19 downto 0);
36  constant period : time := 20ns;
37  begin
38
39      uut : entity EX
40          port map (Mux1_Selector => Mux1_Selector, Mux2_Selector =>
    Mux2_Selector, Mux3_Selector => Mux3_Selector, ALUop => ALUop,
41          I_regA => I_regA, I_regB => I_regB, I_regC => I_regC, I_forward =>
    I_forward, Res => Res);
42
43      tb : process
44      begin
45          wait for period/2;
46
47          --R3 5 Instruction
48          ALUop <= "11XXX00101XXXXXXXXXX";
49          --All muxes send regular output
```

```
50          I_regA <= (31 downto 0 => '1', others => '0');
51          I_regB <= (1 downto 0 => '1', others => '0');
52          I_regC <= (0 => '1', others => '0');
53          Mux1_Selector <= '0';
54          Mux2_Selector <= '0';
55          Mux3_Selector <= '0';
56          I_forward <= std_logic_vector(to_unsigned(100, I_forward'length));

57          wait for period;
58
59          --R4 2 Instruction
60          ALUop <= "10010XXXXXXXXXXXXXX";
61          --Mux1 forwards output
62          I_forward <= std_logic_vector(to_unsigned(3, I_forward'length));
63          Mux1_Selector <= '1';
64          wait for period;
65
66          --R4 4 Instruction
67          ALUop <= "10100XXXXXXXXXXXXXX";
68          --Mux2 forwards output
69          I_regA <= (others => '0');
70          I_forward <= std_logic_vector(to_unsigned(4, I_forward'length));
71          Mux2_Selector <= '1';
72          wait for period;
73
74          --R3 3 Instruction
75          ALUop <= "11XXX00011XXXXXXXXXX";
76          --Mux3 forwards output
77          I_forward <= std_logic_vector(to_unsigned(5, I_forward'length));
78          Mux3_Selector <= '1';
79          wait for period;
80
81          wait;
82      end process;
83
84  end EX_tb;
85
```