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2  --
3  -- Title       : Forwarder
4  -- Design      : Forwarder
5  -- Author      : Aaron Lin and Hang Chen
6  -- Company     : Stony Brook University
7  --
8  -----
9  --
10 -- File        : c:\my_designs\Forwarder\Forwarder\src\Forwarder.vhd
11 -- Generated   : Thu Apr 30 22:29:54 2020
12 -- From       : interface description file
13 -- By        : Itf2Vhdl ver. 1.22
14 --
15 -----
16 --
17 -- Description : This is the forwarding unit that determines if data from
18 -- the WB stage needs to be forwarded to the ALU input for the
19 -- following instruction to use. It does this by checking the input
20 -- registers of the instruction in the ALU and comparing them to the
21 -- register to be written to in the WB stage.
22 --
23 -----
24 library IEEE;
25 use IEEE.std_logic_1164.all;
26
27 entity Forwarder is
28     port(
29         W_EN : in STD_LOGIC;
30         Mux1_Selector : out STD_LOGIC;
31         Mux2_Selector : out STD_LOGIC;
32         Mux3_Selector : out STD_LOGIC;
33         regA : in STD_LOGIC_VECTOR(4 downto 0);
34         regB : in STD_LOGIC_VECTOR(4 downto 0);
35         regC : in STD_LOGIC_VECTOR(4 downto 0);
36         regD : in STD_LOGIC_VECTOR(4 downto 0)
37     );
38 end Forwarder;
39
40 --}} End of automatically maintained section
41
42 architecture Forwarder of Forwarder is
43 begin
44     process(W_EN, regA, regB, regC, regD)
45     begin
46         if W_EN = '1' then
47             if regD = regC then
48                 Mux1_Selector <= '1';
49             else
50                 Mux1_Selector <= '0';
51             end if;
52         end if;
53     end process;
54 end Forwarder;

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52         if regD = regB then
53             Mux2_Selector <= '1';
54         else
55             Mux2_Selector <= '0';
56         end if;
57
58         if regD = regA then
59             Mux3_Selector <= '1';
60         else
61             Mux3_Selector <= '0';
62         end if;
63     else
64         Mux1_Selector <= '0';
65         Mux2_Selector <= '0';
66         Mux3_Selector <= '0';
67     end if;
68 end process;
69
70 end Forwarder;
71
```