File: C:/my_designs/ESE_345/EX_WB/EX_WB/src/EX_WB.vhd (/EX_WB_tb/uut)

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : EX_WB
4   -- Design      : EX_WB
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : c:\my_designs\EX_WB\EX_WB\src\EX_WB.vhd
11  -- Generated   : Fri May  1 14:30:19 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Register between EX and WB stage for storing the W_EN
    signal, result from ALU, and the register to write back to.
18  --
19  ------------------------------------------------------------------------
    ----
20  library IEEE;
21  use IEEE.std_logic_1164.all;
22
23  entity EX_WB is
24       port(
25           I_W_EN : in STD_LOGIC;
26           O_W_EN : out STD_LOGIC;
27           CLK : in STD_LOGIC;
28           I_Res : in STD_LOGIC_VECTOR(127 downto 0);
29           I_regD : in STD_LOGIC_VECTOR(4 downto 0);
30           O_Res : out STD_LOGIC_VECTOR(127 downto 0);
31           O_regD : out STD_LOGIC_VECTOR(4 downto 0)
32           );
33  end EX_WB;
34
35  --}} End of automatically maintained section
36
37  architecture EX_WB of EX_WB is
38  begin
39
40      process(CLK)
41      variable W_EN : std_logic := '0';
42      variable Res : std_logic_vector(127 downto 0) := (others => '0');
43      variable regD : std_logic_vector(4 downto 0) := (others => '0');
44      begin
45          if rising_edge(CLK) then
46              W_EN := I_W_EN;
47              Res := I_Res;
48              regD := I_regD;
49              O_W_EN <= W_EN;
50              O_Res <= Res;
51              O_regD <= regD;
52          end if;
```

```
53      end process;
54  end EX_WB;
55
```