```
1    ------------------------------------------------------------------------
     -----
2    --
3    -- Title       : ID_EX_tb
4    -- Design      : ID_EX
5    -- Author      : Aaron Lin and Hang Chen
6    -- Company     : Stony Brook University
7    --
8    ------------------------------------------------------------------------
     -----
9    --
10   -- File        : c:\my_designs\ID_EX\ID_EX\src\ID_EX_tb.vhd
11   -- Generated   : Fri May  1 13:48:43 2020
12   -- From        : interface description file
13   -- By          : Itf2Vhdl ver. 1.22
14   --
15   ------------------------------------------------------------------------
     -----
16   --
17   -- Description : Testbench for the ID/EX register for storing the W_EN
     signal, registers A, B, C, and D, the data of
18   --  registers A, B, and C, and ALUop. Checks if the correct value is
     outputted from the register each clock cycle.
19   --
20   ------------------------------------------------------------------------
     -----
21   library work;
22   use work.all;
23   library IEEE;
24   use IEEE.std_logic_1164.all;
25   use IEEE.NUMERIC_STD.all;
26
27   entity ID_EX_tb is
28   end ID_EX_tb;
29
30   --}} End of automatically maintained section
31
32   architecture ID_EX_tb of ID_EX_tb is
33   signal CLK, I_W_EN, O_W_EN : std_logic;
34   signal I_regA, I_regB, I_regC, I_regD, O_regA, O_regB, O_regC, O_regD :
     std_logic_vector(4 downto 0);
35   signal I_ALUop, O_ALUop : std_logic_vector(19 downto 0);
36   signal I_regA_Data, I_regB_Data, I_regC_Data, O_regA_Data, O_regB_Data,
     O_regC_Data : std_logic_vector(127 downto 0);
37   constant period : time := 20ns;
38   begin
39
40       uut : entity ID_EX port map (CLK => CLK, I_W_EN => I_W_EN, O_W_EN =>
     O_W_EN,
41           I_regA => I_regA, I_regB => I_regB, I_regC => I_regC, I_regD =>
     I_regD,
42           O_regA => O_regA, O_regB => O_regB, O_regC => O_regC, O_regD =>
     O_regD, I_ALUop => I_ALUop, O_ALUop => O_ALUop,
43           I_regA_Data => I_regA_Data, I_regB_Data => I_regB_Data,
     I_regC_Data => I_regC_Data,
44           O_regA_Data => O_regA_Data, O_regB_Data => O_regB_Data,
     O_regC_Data => O_regC_Data);
```

```
45
46      clk_process : process
47      begin
48          CLK <= '0';
49          wait for period/2;
50          CLK <= '1';
51          wait for period/2;
52      end process;
53
54      tb : process
55      begin
56          wait for period/2;
57
58          I_W_EN <= '1';
59          I_regA <= (others => '1');
60          I_regB <= (3 downto 0 => '1', others => '0');
61          I_regC <= (2 downto 0 => '1', others => '0');
62          I_regD <= (others => '0');
63          I_ALUop <= (0 => '1', others => '0');
64          I_regA_Data <= (1 => '1', others => '0');
65          I_regB_Data <= (2 => '1', others => '0');
66          I_regC_Data <= (3 => '1', others => '0');
67          wait for period;
68
69          I_W_EN <= '0';
70          I_regA <= (3 downto 0 => '1', others => '0');
71          I_regB <= (2 downto 0 => '1', others => '0');
72          I_regC <= (others => '0');
73          I_regD <= (others => '1');
74          I_ALUop <= (1 => '1', others => '0');
75          I_regA_Data <= (4 => '1', others => '0');
76          I_regB_Data <= (1 downto 0 => '1', others => '0');
77          I_regC_Data <= (2 downto 0 => '1', others => '0');
78          wait for period;
79
80          I_W_EN <= '1';
81          I_regA <= (2 downto 0 => '1', others => '0');
82          I_regB <= (others => '0');
83          I_regC <= (others => '1');
84          I_regD <= (3 downto 0 => '1', others => '0');
85          I_ALUop <= (2 => '1', others => '0');
86          I_regA_Data <= (3 downto 0 => '1', others => '0');
87          I_regB_Data <= (4 downto 0 => '1', others => '0');
88          I_regC_Data <= (2 downto 1 => '1', others => '0');
89          wait for period;
90
91          I_W_EN <= '0';
92          I_regA <= (others => '0');
93          I_regB <= (others => '1');
94          I_regC <= (3 downto 0 => '1', others => '0');
95          I_regD <= (2 downto 0 => '1', others => '0');
96          I_ALUop <= (3 => '1', others => '0');
97          I_regA_Data <= (3 downto 2 => '1', others => '0');
98          I_regB_Data <= (4 downto 3 => '1', others => '0');
99          I_regC_Data <= (others => '0');
100         wait for period;
101
```

```
102          wait;
103
104      end process;
105
106  end ID_EX_tb;
107
```