File: C:/my_designs/ALU/ALU/src/R3_16_tb.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : R3_16_tb
4   -- Design      : ALU
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : C:\my_designs\ALU\ALU\src\R3_16_tb.vhd
11  -- Generated   : Sat Apr 25 00:26:29 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Testbench for the R3 10000 Instruction. Checks if packed
    unsigned subtraction is carried out correctly without correction
18  --  for underflows. Each of the 8 16 bit fields are tested.
19  --
20  ------------------------------------------------------------------------
    ----
21  library work;
22  use work.all;
23  library IEEE;
24  use IEEE.std_logic_1164.all;
25  use IEEE.NUMERIC_STD.all;
26
27  entity R3_16_tb is
28  end R3_16_tb;
29
30  --}} End of automatically maintained section
31
32  architecture R3_16_tb of R3_16_tb is
33  signal ALUop : std_logic_vector(19 downto 0);
34  signal Res, regA_Data, regB_Data, regC_Data : std_logic_vector(127 downto 0
    );
35  constant period : time := 20ns;
36  begin
37
38      uut : entity ALU
39          port map (ALUop => ALUop, Res => Res, regA_Data => regA_Data,
    regB_Data => regB_Data, regC_Data => regC_Data);
40
41      tb : process
42      begin
43          wait for period/2;
44
45          ALUop <= "11XXX10000XXXXXXXXXX";
46
47          --31 downto 16 tests (3 - maximum); 15 downto 0 tests (maximum - 3)
48          regB_Data <= (17 downto 16 => '1', 15 downto 0 => '1', others =>
    '0');
49          regA_Data <= (31 downto 16 => '1', 1 downto 0 => '1', others => '0'
    );
```

```
50          wait for period;
51
52          --63 downto 48 tests (3 - maximum); 47 downto 32 tests (maximum -
    3)
53          regB_Data <= (49 downto 48 => '1',  47 downto 32 => '1', others =>
    '0');
54          regA_Data <= (63 downto 48 => '1', 33 downto 32 => '1', others =>
    '0');
55          wait for period;
56
57
58          --95 downto 80 tests (3 - maximum); 79 downto 64 tests (maximum -
    3)
59          regB_Data <= (81 downto 80 => '1', 79 downto 64 => '1', others =>
    '0');
60          regA_Data <= (95 downto 80 => '1', 65 downto 64 => '1', others =>
    '0');
61          wait for period;
62
63          --127 downto 112 tests (3 - maximum); 111 downto 96 tests (maximum
    - 3)
64          regB_Data <= (113 downto 112 => '1',  111 downto 96 => '1', others
    => '0');
65          regA_Data <= (127 downto 112 => '1', 97 downto 96 => '1', others =>
    '0');
66          wait for period;
67
68          wait;
69      end process;
70
71  end R3_16_tb;
72
```