File: C:/my_designs/ESE_345/IF_ID/IF_ID/src/IF_ID.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : IF_ID
4   -- Design      : IF_ID
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : c:\my_designs\IF_ID\IF_ID\src\IF_ID.vhd
11  -- Generated   : Fri May  1 11:45:22 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Single 25 bit register for storing Instruction between IF
    and ID stage.
18  --
19  ------------------------------------------------------------------------
    ----
20  library IEEE;
21  use IEEE.std_logic_1164.all;
22
23  entity IF_ID is
24       port(
25           CLK : in STD_LOGIC;
26           I_Instruction : in STD_LOGIC_VECTOR(24 downto 0);
27           O_Instruction : out STD_LOGIC_VECTOR(24 downto 0)
28           );
29  end IF_ID;
30
31  --}} End of automatically maintained section
32
33  architecture IF_ID of IF_ID is
34  begin
35      process(CLK)
36      variable reg : std_logic_vector(24 downto 0) := (others => '0');
37      begin
38          if rising_edge(CLK) then
39              reg := I_Instruction;
40              O_Instruction <= reg;
41          end if;
42      end process;
43  end IF_ID;
44
```