File: C:/my_designs/Instruction_Fetch/Instruction_Fetch/src/IF_Stage.vhd

```
1   ----------------------------------------------------------------------------
2   --
3   -- Title       : IF_Stage
4   -- Design      : Instruction_Fetch
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ----------------------------------------------------------------------------
9   --
10  -- File        : c:\my_designs\Instruction_Fetch\Instruction_Fetch\src\IF_Stage.vhd
11  -- Generated   : Sat May  2 14:07:32 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ----------------------------------------------------------------------------
16  --
17  -- Description : This is the top level design for the IF stage. It consists of the PC, PC Adder, and the Instruction Buffer.
18  --
19  ----------------------------------------------------------------------------
20  library work;
21  use work.all;
22  library IEEE;
23  use IEEE.std_logic_1164.all;
24
25  entity IF_Stage is
26       port(
27           CLK : in STD_LOGIC;
28           Instruction_Data : in std_logic_vector(24 downto 0);
29           Instruction_Index : in std_logic_vector(5 downto 0);
30           Instruction : out STD_LOGIC_VECTOR(24 downto 0)
31           );
32  end IF_Stage;
33
34  --}} End of automatically maintained section
35
36  architecture IF_Stage of IF_Stage is
37  signal I_PC, address : std_logic_vector(5 downto 0);
38  begin
39
40      u1 : entity PC port map (CLK => CLK, PC_Next => I_PC, PC => address);
41      u2 : entity PC_Incrementer port map (PC => address, PC_Next => I_PC);
42      u3 : entity Instruction_Buffer port map (Instruction_Index => Instruction_Index, CLK => CLK, PC => address, Instruction => Instruction, Instruction_Data => Instruction_Data);
43  end IF_Stage;
44
45
46
```