File: C:/my_designs/ESE_345/IF_ID/IF_ID/src/IF_ID_tb.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : IF_ID_tb
4   -- Design      : IF_ID
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : c:\my_designs\IF_ID\IF_ID\src\IF_ID_tb.vhd
11  -- Generated   : Fri May  1 11:58:58 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Testbench for the single 25 bit register for storing the
    Instruction from the IF stage. Checks if the correct value is
18  --  outputted from the register each clock cycle.
19  --
20  ------------------------------------------------------------------------
    ----
21  library work;
22  use work.all;
23  library IEEE;
24  use IEEE.std_logic_1164.all;
25  use IEEE.NUMERIC_STD.all;
26
27  entity IF_ID_tb is
28  end IF_ID_tb;
29
30  --}} End of automatically maintained section
31
32  architecture IF_ID_tb of IF_ID_tb is
33  signal I_Instruction, O_Instruction : std_logic_vector(24 downto 0);
34  signal CLK : std_logic;
35  constant period : time := 20ns;
36  begin
37
38      uut : entity IF_ID
39          port map (CLK => CLK, I_Instruction => I_Instruction, O_Instruction
    => O_Instruction);
40
41
42      clk_process : process
43      begin
44          CLK <= '0';
45          wait for period/2;
46          CLK <= '1';
47          wait for period/2;
48      end process;
49
50      tb : process
51      begin
```

```
52          wait for period/2;
53
54          I_Instruction <= (others => '1');
55          wait for period;
56
57          I_Instruction <= (24 downto 13 => '1', others => '0');
58          wait for period;
59
60          I_Instruction <= (12 downto 0 => '1', others => '0');
61          wait for period;
62
63          I_Instruction <= (others => '0');
64          wait for period;
65
66          wait;
67
68      end process;
69  end IF_ID_tb;
70
```