File: C:/my_designs/Forwarder/Forwarder/src/Forwarder_tb.vhd

```
1   ------------------------------------------------------------------------
    -----
2   --
3   -- Title       : Forwarder_tb
4   -- Design      : Forwarder
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    -----
9   --
10  -- File        : c:\my_designs\Forwarder\Forwarder\src\Forwarder_tb.vhd
11  -- Generated   : Thu Apr 30 22:43:54 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    -----
16  --
17  -- Description : This is the testbench for the Forwarding Unit. Checks if
    the correct Mux is triggered to select the forwarded output
18  --  from WB stage if the input registers to the ALU is the same as the
    register to be written in the WB stage.
19  --
20  ------------------------------------------------------------------------
    -----
21  library work;
22  use work.all;
23  library IEEE;
24  use IEEE.std_logic_1164.all;
25  use IEEE.NUMERIC_STD.all;
26
27  entity Forwarder_tb is
28  end Forwarder_tb;
29
30  --}} End of automatically maintained section
31
32  architecture Forwarder_tb of Forwarder_tb is
33  signal W_EN, Mux1_Selector, Mux2_Selector, Mux3_Selector : std_logic;
34  signal regA, regB, regC, regD : std_logic_vector(4 downto 0);
35  constant period : time := 20ns;
36  begin
37
38      uut : entity Forwarder port map (W_EN => W_EN, Mux1_Selector =>
    Mux1_Selector, Mux2_Selector => Mux2_Selector, Mux3_Selector =>
    Mux3_Selector,
39          regA => regA, regB => regB, regC => regC, regD => regD);
40
41      tb : process
42      begin
43          wait for period/2;
44
45          --No forwarding because prior instruction is not writing to
    register
46          regA <= (others => '1');
47          regB <= (3 downto 0 => '1', others => '0');
48          regC <= (others => '0');
```

```
49          regD <= (others => '1');
50          W_EN <= '0';
51          wait for period;
52
53          --No forwarding due to different registers being written back to
    and being used in ALU input
54          W_EN <= '1';
55          regD <= (1 => '1', others => '0');
56          wait for period;
57
58          --Forwarding to Mux1
59          regD <= (others => '0');
60          wait for period;
61
62          --Forwarding to Mux2
63          regD <= (3 downto 0 => '1', others => '0');
64          wait for period;
65
66          --Forwarding to Mux3
67          regD <= (others => '1');
68          wait for period;
69
70          --Forwarding to Mux1 and Mux2
71          regC <= (1 => '1', others => '0');
72          regB <= (1 => '1', others => '0');
73          regD <= (1 => '1', others => '0');
74          wait for period;
75
76          --Forwarding to Mux1 and Mux3
77          regC <= (2 => '1', others => '0');
78          regA <= (2 => '1', others => '0');
79          regD <= (2 => '1', others => '0');
80          wait for period;
81
82          --Forwarding to Mux2 and Mux3
83          regA <= (3 => '1', others => '0');
84          regB <= (3 => '1', others => '0');
85          regD <= (3 => '1', others => '0');
86          wait for period;
87
88          --Forwarding to all
89          regC <= (4 => '1', others => '0');
90          regB <= (4 => '1', others => '0');
91          regA <= (4 => '1', others => '0');
92          regD <= (4 => '1', others => '0');
93          wait for period;
94
95          wait;
96
97      end process;
98
99  end Forwarder_tb;
100
```