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c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.asdb c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.awc
```

Signal name	Value	16	24	32	40	48	56	64	72	80	ns	
CLK	0											
I_W_EN	1											
O_W_EN	0											
I_DataIn	000...											
O_regA_Data	000...											
O_regB_Data	000...											
O_regC_Data	000...											
O_regA	04											
O_regB	04											
O_regC	0B											
O_regD	14											
I_regD	04											
O_ALUop	??C...											
Instruction	1?5...											

Cursor 1

Signal name	Value	96	104	112	120	128	136	144	152	160	ns
CLK	0										
I_W_EN	1										
O_W_EN	0										
I_DataIn	000...										
O_regA_Data	000...										
O_regB_Data	000...										
O_regC_Data	000...										
O_regA	04										
O_regB	04										
O_regC	0B										
O_regD	14										
I_regD	04										
O_ALUop	??C...										
Instruction	1?5...										

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c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.asdb c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.awc
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[illegible]

Cursor 1

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c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.asdb c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.awc
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Signal name	Value	256	264	272	280	288	296	304	312	320	ns
CLK	0										
I_W_EN	1										
O_W_EN	0										
I_DataIn	000...										
O_regA_Data	000...										
O_regB_Data	000...										
O_regC_Data	000...										
O_regA	04										
O_regB	04										
O_regC	0B										
O_regD	14										
I_regD	04										
O_ALUOp	??C...										
Instruction	1?5...										

Cursor 1

```
c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.asdb c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.awc
```

Signal name	Value	
CLK	0	
I_W_EN	1	
O_W_EN	0	
+ I_DataIn	000...	00000000000000000000000000000010
+ O_regA_Data	000...	00000000000000000000000000000010
+ O_regB_Data	000...	00000000000000000000000000000010
+ O_regC_Data	000...	00000000000000000000000000000000
+ O_regA	04	04
+ O_regB	04	04
+ O_regC	0B	< 05 X 06 X 07 X 08
+ O_regD	14	14
+ I_regD	04	04
+ O_ALUOp	??C...	< ??484 X ??884 X ??C84 X ??084
+ Instruction	1?5...	< 1?29094 X 1?31094 X 1?39094 X 1?41094

Cursor 1

c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.asdb c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.awc

Signal name		Value	ns																
CLK	0																		
I_W_EN	1																		
O_W_EN	0																		
I_DataIn	000...																		
O_regA_Data	000...																		
O_regB_Data	000...																		
O_regC_Data	000...																		
O_regA	04																		
O_regB	04																		
O_regC	0B																		
O_regD	14																		
I_regD	04																		
O_ALUop	??C...																		
Instruction	1?5...																		
Cursor 1																			

```
c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.asdb c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.awc
```

Signal name	Value	496	504	512	520	528	536	544	552	560	ns
CLK	0										
I_W_EN	1										
O_W_EN	0										
I_DataIn	000...										
O_regA_Data	000...										
O_regB_Data	000...										
O_regC_Data	000...										
O_regA	04										
O_regB	04										
O_regC	0B										
O_regD	14										
I_regD	04										
O_ALUOp	??C...										
Instruction	1?5...										

Cursor 1

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c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.asdb c:/my_designs/ID_Stage/ID_Stage/src/ID_Stage.awc
```

Signal name	Value	ns															
CLK	0																
I_W_EN	1																
O_W_EN	0																
I_DataIn	000...	00000000000000000000000000000010															
O_regA_Data	000...	00000000000000000000000000000010															
O_regB_Data	000...	00000000000000000000000000000010															
O_regC_Data	000...	00000000000000000000000000000001				00000000000000000000000000000000				00000000000000000000000000000010				00000000000000000000000000000000			
O_regA	04	04															
O_regB	04	04															
O_regC	0B	02				03				04				0B			
O_regD	14	14															
I_regD	04	04															
O_ALUOp	??C...	??884				??C84				??084				??C84			
Instruction	1?5...	1?11094				1?19094				1?21094				1?59094			

Cursor 1