File: C:/my_designs/ALU/ALU/src/R3_19_tb.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : R3_19_tb
4   -- Design      : ALU
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : C:\my_designs\ALU\ALU\src\R3_19_tb.vhd
11  -- Generated   : Sat Apr 25 11:27:23 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Testbench for the R3 10011 Instruction. Checks if the
    bitwise logical NAND is carried out correctly.
18  --
19  ------------------------------------------------------------------------
    ----
20  library work;
21  use work.all;
22  library IEEE;
23  use IEEE.std_logic_1164.all;
24  use IEEE.NUMERIC_STD.all;
25
26  entity R3_19_tb is
27  end R3_19_tb;
28
29  --}} End of automatically maintained section
30
31  architecture R3_19_tb of R3_19_tb is
32  signal ALUop : std_logic_vector(19 downto 0);
33  signal Res, regA_Data, regB_Data, regC_Data : std_logic_vector(127 downto 0
    );
34  constant period : time := 20ns;
35  begin
36
37       uut : entity ALU
38          port map (ALUop => ALUop, Res => Res, regA_Data => regA_Data,
    regB_Data => regB_Data, regC_Data => regC_Data);
39
40      tb : process
41      begin
42          wait for period/2;
43
44          ALUop <= "11XXX10011XXXXXXXXXX";
45          regB_Data <= (127 downto 96 => '1', 95 downto 64 => '1', 63 downto
    32 => '0', 31 downto 0 => '0');
46          regA_Data <= (127 downto 96 => '0', 95 downto 64 => '1', 63 downto
    32 => '0', 31 downto 0 => '1');
47          wait for period;
48
```

```
49          wait;
50      end process;
51
52  end R3_19_tb;
53
```