File: C:/my_designs/ALU/ALU/src/R3_7_tb.vhd

```
1   ------------------------------------------------------------------------
    ----
2   --
3   -- Title       : R3_7_tb
4   -- Design      : ALU
5   -- Author      : Aaron Lin and Hang Chen
6   -- Company     : Stony Brook University
7   --
8   ------------------------------------------------------------------------
    ----
9   --
10  -- File        : C:\my_designs\ALU\ALU\src\R3_7_tb.vhd
11  -- Generated   : Fri Apr 24 22:02:07 2020
12  -- From        : interface description file
13  -- By          : Itf2Vhdl ver. 1.22
14  --
15  ------------------------------------------------------------------------
    ----
16  --
17  -- Description : Testbench for the R3 00111 Instruction. Checks if the
    absolute value of the difference of each of the 16 8 bits is calculated
18  --  correctly without correction for overflows and underflows. Cases in
    which the output is 128 are ignored.
19  --
20  ------------------------------------------------------------------------
    ----
21  library work;
22  use work.all;
23  library IEEE;
24  use IEEE.std_logic_1164.all;
25  use IEEE.NUMERIC_STD.all;
26
27  entity R3_7_tb is
28  end R3_7_tb;
29
30  --}} End of automatically maintained section
31
32  architecture R3_7_tb of R3_7_tb is
33  signal ALUop : std_logic_vector(19 downto 0);
34  signal Res, regA_Data, regB_Data, regC_Data : std_logic_vector(127 downto 0
    );
35  constant period : time := 20ns;
36  begin
37
38       uut : entity ALU
39          port map (ALUop => ALUop, Res => Res, regA_Data => regA_Data,
    regB_Data => regB_Data, regC_Data => regC_Data);
40
41      tb : process
42      begin
43          wait for period/2;
44
45          ALUop <= "11XXX00111XXXXXXXXXX";
46
47          regB_Data <= (127 => '1', 111 => '0', 110 downto 96 => '1', 95
    downto 80 => '0', 65 downto 64 => '1', others => '0');
48          regA_Data <= (127 downto 113 => '0', 112 => '1', 111 downto 97 =>
    '1', 96 => '0', 81 downto 80 => '1', 79 downto 64 => '0', others => '0');
```

```
49          wait for period;
50
51          regB_Data <= (63 => '1', 48 => '0', 47 downto 32 => '1', 31 downto
    16 => '0', 1 downto 0 => '1', others => '0');
52          regA_Data <= (63 downto 49 => '0', 48 => '1', 47 downto 33 => '1',
    32 => '0', 17 downto 16 => '1', 15 downto 0 => '0', others => '0');
53          wait for period;
54
55          wait;
56      end process;
57
58  end R3_7_tb;
59
```