

**TRADING UTILIZATION FOR CIRCUITRY:
HARDWARE-SOFTWARE CO-DESIGN FOR REAL-TIME
SOFTWARE-BASED SHORT-CIRCUIT PROTECTION**

by

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THESIS

Submitted to the Graduate School

of Wayne State University,

Detroit, Michigan

in partial fulfillment of the requirements

for the degree of

MASTER OF SCIENCE

2018

MAJOR: COMPUTER SCIENCE

Approved by:

Advisor

Date

DEDICATION

To Ellen, Kevin, Sue, Carina, and Connor.

ACKNOWLEDGEMENTS

This research has been supported in part by:

the US National Science Foundation (CNS Grant Nos. 0953585, 1205338, & 1618185)

and a Thomas C. Rumble Graduate Fellowship from Wayne State University.

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CHAPTER 1 Introduction

1.1 Motivation and Applications

From cell phones to solar panels, devices of all sizes require power semiconductors to control, direct, and manage the flow of electricity. Batteries, CPUs, and photovoltaic inverters all leverage this flow of electricity, known as current, to perform tasks from actuation to computation. In excess, however, current leads to thermal cycling and can be degrading or destructive to power circuitry. One cause of excessive current is short-circuiting. A short-circuit occurs when current travels through an alternate, unintended path in a circuit often with little or no resistance. This alternate path of travel with no resistance leads to high current, increased heat, and often circuit damage. This potential for damage creates a need for short-circuit protection.

The need for short protection can be seen in a variety of applications relying on power semiconductors including power converters and inverters [10]. In an industrial setting, this can include photovoltaic systems and hybrid fuel cells [21]. In a consumer setting, this can include cell phones and other portable electronics like the recent Samsung Galaxy Note 7 which was recalled due to fires caused by short-circuits in the device battery [8].

To mitigate the risk of short-circuits, devices using power-semiconductors can be constructed with short-circuit protection in the form of a fuse, thermal breaker, or other hardware designated to prevent the high current responsible for circuit damage. This short-circuit protection, however, is often fixed circuitry dedicated solely to short detection. In such systems, little flexibility is afforded to circuits which operate at varying voltages and currents over their lifetime as designers must protect against short-circuits at the highest currents and voltages, even if they are not the most frequently used. Moreover, the rise in semiconductor power density continues to reduce the required latency for detecting and halting shorts [9].

1.2 Problem Statement

In light of the motivation above, the problem of designing flexible short-circuit protection systems can be viewed through the lens of real-time software. Given the inherent possibility of catastrophic failure in short-circuit protection systems and the time-sensitive nature of current rise during short-circuits, we seek to frame the problem as one of hardware-software co-design via hard real-time systems. Specifically, we aim to address the problem of short-circuit protection in direct current (DC) resistor-inductor (RL) circuits - circuits containing resistors and inductors where current flows in only one direction.

To address the need for flexible, short-circuit protection, our problem statement is:

Given a Direct-Current Resistor-Inductor circuit, devise a hardware-software co-design approach which relates hard-real time requirements to hardware size. More specifically, our objective is to construct a hardware-software relationship which allows designers to:

1. minimize hardware size while meeting maximum real-time utilization requirements, and
2. minimize real-time utilization while meeting maximum hardware size requirements.

1.3 Proposed Solution

To address the need for flexible, real-time short-circuit protection, we propose a short-protection method via a real-time task as follows:

A DC RL circuit containing an air-core inductor placed in series between the system's resistive load and ground has is connected (and controlled) by a microcontroller. The microcontroller executes a real-time task responsible for sampling voltage across the inductor (or a small resistor) to measure current via an Analog-to-Digital Converter (ADC) pin. Short protection is accomplished by identifying the maximum expected current and the maximum rate of current change as limited

by the circuit's inductor. Using the inductor spatial parameters in conjunction with ADC sampling times, a minimum sampling period is derived for the real-time task. From this minimum period, a relationship between minimum real-time utilization under Earliest Deadline First (EDF) scheduling and inductor volume is provided. Real-time or physical system constraints may be applied to this relationship to facilitate the hardware-software co-design of a real-time short-circuit protection system.

This approach is intended to allow existing systems with microprocessors to migrate short-circuit protection from dedicated-circuitry-only to a software-based implementation and future systems to be designed with the proposed hardware-software tradeoff in mind.

1.4 Contributions

The software-based protection methods depicted herein provide an alternative short-circuit protection technique to circuit designers. By relating utilization to the volume of (and board space consumed by) an inductor, system designers may trade short-protection circuitry for real-time task utilization on the microcontroller, leveraging either end of the relationship to meet fault-tolerance and space requirements. For example, applications with little available board space may opt for smaller inductors (minimizing board space) and greater utilization. Example applications include smaller IGBT modules as found in electric vehicles or applications where minimizing weight is import[12]. In contrast, larger applications with more available board space or a greater real-time task set may opt for a larger inductor and thus a smaller utilization for the short-protection task. Example applications include high power IGBT modules in photovoltaic and wind turbine inverters [21][2]. Perhaps most importantly, the established relationship between board space and processor utilization acts as a conduit through which advancements in electrical engineering may improve

real-time system efficiency and vice versa. To summarize, our contributions include¹:

- 1.** a software-based short protection method for Direct Current Resistor-Inductor circuits,
- 2.** a relationship between air-core inductor spatial parameters and real-time processor utilization under preemptive uniprocessor EDF scheduling for short-circuit protection,
- 3.** a process for identifying optimal inductor orientation given a fixed volume, and
- 4.** a process for minimizing utilization given a fixed volume for an air-core inductor and vice versa.

1.5 Outline

Chapter 2 details the related work in both problem domains. Chapter 3 provides an electronics background and nomenclature overview. Chapter 4 provides the first paper contribution, a model for identifying circuit properties. Chapter 5 depicts short protection methods given the constraints provided in the circuit model. Chapter 6 formalizes the relation between real-time scheduling and short-circuit protection. Chapter 7 provides the model optimization for both fixed board constraints and fixed real-time utilization as contributions from this paper. Chapter 8 details experiments conducted to validate the proposed relationship and theoretical utilization. Chapter 9 discusses the results of experimentation. Chapter 10 identifies conclusions and future work.

¹This work was published in the 2017 IEEE 23rd International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA) under the same title [19] and is an extension upon the related senior thesis by Willcock [18].

CHAPTER 2 Related Work

To the best of our knowledge, current approaches to short-circuit protection are rooted in dedicated circuitry and do not use adaptive real-time processing. Modern methodologies include Zone Selective Interlocking on systems with alternating current (AC) which, while successful, cannot be directly applied to DC [4]. Other methods use the Rogowski coil in conjunction with differential and integral signals from the coil to detect a short [17]. While feasible, the Rogowski coil implementation is large and does not slow current rise in the system. Some methods only require sampling of gate emitter voltage and a reference voltage [9]. Krone et al. use the gate emitter voltage, but also reference the DC link capacitors to assist in protection [13]. Each method, while different, relies solely on dedicated circuitry for short protection. Although variations exist in the components used and the design of the circuits, we sought an alternative where required circuitry was minimized.

Furthermore, protection methods relying on the change in current, as in Hain and Bakran [6], require an inductor. This approach also includes auxiliary MOSFETs, latch circuits, and comparators. Additionally, some current protection methods relying on gate charge require differential amplifiers attached to auxiliary MOSFETs as found in Horiguchi et al. which also require an inductor in test circuits [10]. Both models have more components than the single inductor required for protection in this approach, providing more motivation for software-based protection.

In the area of cyber-physical and real-time systems, the senior thesis [18] upon which this work and its conference-published variant [19] are based focused primarily on establishing a relationship between the inductance of an inductor and the utilization required for the task. This work extends the results of Willcock [18] by incorporating board space consumed into the utilization calculation and providing experimental validation of the extended relationship with low-cost hardware. Excluding the preceding variant of this work, we are unaware of other cyber-physical or real-time works

specific to short protection. However, works identifying adaptive real-time tasks with multiple operating modes are present [11]. Examples include thermal-aware computing in Hettiarachchi et al [7] and rate-adaptive tasks as in Buttazzo et al. [3]. Biondi and Buttazzo furthered this model with thorough analysis of its implications on the executing processor [1]. These works address properties of environment and power-aware real-time tasks but are not specific to short-circuit protection.

CHAPTER 3 Electronics Background

The following chapter covers background required for constructing the proposed circuit model. It includes an overview of nomenclature, DC RL circuits, inductors, and short-circuits. These electronics fundamentals can be found in a typical collegiate physics textbook [20].

3.1 Nomenclature

For the purposes of describing our approach, we rely on the following nomenclature:

Term	Symbol	Unit	Description
Current	I	Ampere (A)	The rate of electric charge flow
Inductance	L	Henry (H)	The ability to induce electromotive force (voltage)
Voltage	V	Volt (V)	The difference in electric potential between two points

3.2 First-Order DC RL Circuits

Direct current (DC) circuits are circuits in which the direction of current flow does not change [20]. A DC circuit in which current passes through a resistor and an inductor is deemed a DC RL circuit where "R" represents the resistor and "L" the inductor. The model presented in Chapter 4 relies on a first-order DC RL circuit with the resistor and inductor in series. An example first-order DC RL circuit is provided in Figure 3.1 with two resistors and an inductor in series.

3.3 Inductors

An inductor is a passive electronic component typically illustrated as a coil or four- which resists change in current flow through itself. This property is useful as current through an inductor cannot change instantaneously. Equations describing these properties are provided in Chapter 5.

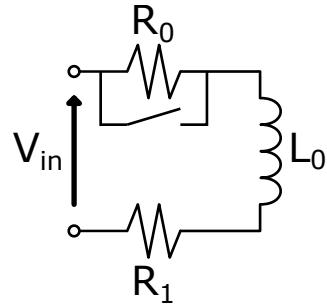


Figure 3.1: Model DC RL Circuit

A DC RL circuit with load R_0 , inductor L_0 , resistor R_1 , and switch for inducing shorts.

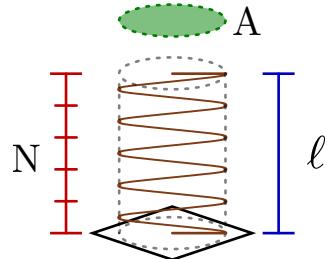


Figure 3.2: Spatial parameters of an air core inductor

3.3.1 Spatial Parameters

The model proposed in Chapter 4 will rely on a single, air-core inductor. The spatial properties of an inductor may be modeled as seen in Figure 3.2. The figure describes a solenoid-style inductor where N represents the number of complete turns, A is the area of a coil, ℓ represents the length of the inductor. The relationship between these parameters and inductance can be constructed from fundamental electricity and magnetism equations found in [20]. This relationship is modeled as:

$$L = \frac{\mu N^2 A}{\ell} \quad (3.1)$$

where μ is the permeability of free space. For our purposes, we assume the spatial parameters are fixed – i.e., ℓ , A , and N are static¹. Equation (3.1) will be referenced in Chapter 5 to relate current-flow to inductor size and in Chapter 7 to optimize hardware-software co-design solutions.

¹In Chapter 7, we consider variable sized inductors as part of our hardware-software co-design optimization.

3.3.2 Assumption of Constant Turn Density

Equation (3.1) contains the term $\frac{N}{\ell}$, referred to as *turn density*. *Turn density* must remain constant with an increase in length for inductance to increase. Thus if an inductor is to be extended from length ℓ to $2 \cdot \ell$, the number of turns N should be doubled accordingly (to $2 \cdot N$) to maintain constant *turn density*. Doubling both N and ℓ results in doubled inductance L . Whenever a change in inductor length ℓ is suggested, we assume the number of turns is doubled as well to maintain constant *turn density*. We rely on this assumption throughout Chapter 7.

3.3.3 Inductor Core Composition

The core of a solenoid-style inductor can be defined as the area within the coiled wire. In practice, many inductors are manufactured with ferromagnetic cores which increase the inductance for the same volume. In our model, we assume this core is empty and contains only air. Equation (3.1) reflects this assumption as it applies only to air-core inductors. We view this assumption as an upper bound on board space consumed since ferromagnetic core inductors provide a greater inductance by volume [5].

3.4 Definition of Short and Fault Types

For the purposes of this model, a short is defined as the flow of current through an alternate, unintended path in a circuit with little or no impedance. In the event of a short, this loss of impedance causes a large change in current which can be slowed and detected through careful reliance on an inductor's ability to resist instantaneous changes in current. However, short-circuits lead to joule heating, the process whereby current through a conductor releases heat modeled as:

$$\text{Heat} \propto RI^2t \quad (3.2)$$

Here, R is resistance, I is current, and t is time [20]. The thermal buildup from joule heating is responsible for the permanent damage that can result from a short and therefore serves as motivation for short-circuit protection. Protection from damage, however, requires catching two short-circuit fault types: the Fault under Load (FUL) and the Hard-Switching Fault (HSF).

3.4.1 Fault Under Load vs Hard-Switching Fault

In the context of short-circuit protection, a Fault Under Load is a short-circuit fault where a circuit has an active load at the time of the fault. In this type of fault, the current and impedance are both non-zero. Intuitively, this means the circuit is "on" at the instant the short-circuit occurs. The short forces current to rise, often above desired operating ranges. This fault type, commonly analyzed in IGBTs, has been studied in [16].

In contrast, a Hard-Switching Fault is a short-circuit fault where the circuit does not have an active load at the time of the fault [10]. In contrast to an FUL, an HSF does not have an initial operating current since there must be a short-circuit path before the circuit is "on".

3.5 Current as a Function of Time

In the proposed system, a real-time task must be related to the change in current through an inductor. The following equation will provide such a relationship used Chapter 5:

$$I(t) = \frac{V}{R}(1 - e^{-t\frac{R}{L}}) \quad (3.3)$$

where $I(t)$ is current at time t , V is a constant voltage to the circuit, R is resistance, and L is inductance.

CHAPTER 4 Electronic System Model

In the previous chapter, an electronics background was provided as context for our approach. In this chapter, we will define and describe the system model from an electronics perspective. Relying on the provided background, we propose an electronics model with four primary components:

1. a DC RL circuit to which software-based short-circuit protection is applicable and board space is consumed by air-core solenoid-style inductor,
2. an Operating Current Model (OCM) to characterize first-order DC RL circuits,
3. two short-circuit detection methods for first-order DC RL circuits, and
4. a real-time sporadic task for short protection.

The short-circuit detection methods will be discussed in Chapter 5 and the real-time model (and its utilization analysis under uniprocessor EDF scheduling) will be discussed in Chapter 6.

4.1 DC RL Short-Circuit Schematic

Figure 3.1 is a model DC RL circuit with a switch for simulating a short-circuit. This schematic provides the requirements for the monitored, short-protected circuit: a voltage supply V_{in} , circuit load R_0 , inductor L_0 , and the optional, low-value resistor R_1 used for sensing current. If R_1 is not used, the resistance through inductor L_0 may be used to calculate current. Note that the short occurs via the switch around R_0 .

As previously mentioned, in a manufactured circuit the spatial parameters and inductor value of L_0 in Figure 3.1 are expected to be fixed. During the design phase however, inductor parameters may be altered to increase space efficiency. These properties are afforded by Equation (3.1).

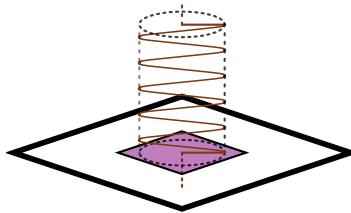


Figure 4.1: Board Space Consumed by an Inductor

The highlighted square circumscribing area A of the inductor represents the board space consumed by a solenoid-style air-core inductor.

4.2 Board Space Consumed

For ease of analysis, we assume the axis of the inductor is mounted perpendicular to the board as shown in Figure 4.1. Therefore, the board space consumed by the inductor is defined as the square that circumscribes area A of the inductor as seen in Figure 3.2:

$$A_{consumed} = \frac{4}{\pi}A \quad (4.1)$$

This definition of board space consumed will be referenced in Chapter 7 where the provided model is optimized for minimum board space consumption and volume.

4.3 Operating Current Model

To simplify the analysis of DC RL circuits, we propose an Operating Current Model (OCM) for characterizing the circuit's maximum current, maximum voltage, and critical current. Hereafter, we model DC RL circuits as:

$$C = (\Gamma_I, I_{crit}) \quad (4.2)$$

where C is the circuit described using parameters Γ_I and I_{crit} . Γ_I is defined such that:

$$\Gamma_I = (\gamma_1, \gamma_2, \dots, \gamma_n) \quad (4.3)$$

$$\gamma_i = (I_i, V_i) \quad \text{for all } i = 1, \dots, n \quad (4.4)$$

Here Γ_I is composed of n operating current sets γ_i where i is the index of an operating current set.

Each operating current set is a 2-tuple of an operating current, I_i , and operating voltage, V_i . The resistance, R , of each operating current set can be solved using Ohm's Law and is not included.

I_{crit} is defined as the critical current of the system as determined by the user. The critical current represents the current value at which the system physically degrades or, in practice, the current value the user wishes to avoid reaching.

Two final derivable parameters I_{max} and V_{max} , are extracted from the OCM as follows:

$$I_{max} = \max_{i \in \Gamma_I} \{\gamma_i\} \quad \text{and} \quad V_{max} = \max_{i \in \Gamma_I} \{\gamma_i\} \quad (4.5)$$

Note that if $I_{crit} = I_{max}$, any current flow over I_{max} is assumed to be damaging and may not be prevented through this short protection model. Thus, we assume $I_{max} < I_{crit}$.

CHAPTER 5 Methods of Protection

The intersection of electronics modeling and real-time systems begins with strategies for detecting and halting short-circuits. To detect a short in the generalized first-order DC RL circuit, as seen in Figure 3.1, we present two methods for detection:

1. a simple comparison of current, I , against maximum current, I_{max} and
2. a comparison of change in current, ΔI , against the maximum change in current, ΔI_{max} , allowed.

Both methods are applicable to any system which samples current of a monitored circuit. To prevent damage from shorts and fully utilize the following protection methods, power to the monitored circuit(s) must be removed immediately upon detection of a short. Without removal of power, these methods merely support detection and not protection.

5.1 Method 1: Maximum Operating Current

The first method for detecting short circuits in a DC RL circuit is to identify when current rises above I_{max} . A current value above I_{max} indicates some malfunction caused current to rise above the maximum current in the OCM. When $I > I_{max}$, power to the monitored circuit should be disabled to protect the hardware.

5.2 Method 2: Maximum Change in Current

The second method of detection requires observing the rate of change of current. From Equation (3.3) it is known that, given a constant voltage and resistance, the current will converge to $\frac{V}{R}$. During convergence, the slope of ΔI approaches zero. The derivative of Equation (3.3) provides

the value of $\Delta_{\max}I$:

$$\Delta I = \frac{\partial}{\partial t} I(t) = \frac{\partial}{\partial t} \left(\frac{V}{R} (1 - e^{-t \frac{R}{L}}) \right) = \frac{V}{L} e^{-t \frac{R}{L}} \quad (5.1)$$

Assuming constant inductance, resistance, and voltage, the largest values of ΔI occur at $t = 0$ and $R = 0$ while excluding infinite inductance ($L \neq +\infty$). This leads to the following conclusions:

1. If $R \neq 0$, $\frac{dI(t)}{dt} = \frac{V}{L}$ instantaneously at time $t = 0$ only. Assuming no short has occurred, the change in current between any two consecutive current samples should be less than $\frac{V}{L}$.

Formally, $\forall \delta > 0, t \geq 0, \frac{|I(t+\delta) - I(t)|}{\delta} < \frac{V}{L}$

2. If the change in current between two consecutive current samples is equivalent to $\frac{V}{L}$, then $R = 0$ and a short is occurring.

We can safely state the maximum ΔI through an inductor at any time t , including $t = 0$, is:

$$\Delta_{\max}I = \frac{V}{L}$$

Since all non-superconducting materials will provide some impedance, the $\Delta_{\max}I$ should have a threshold, ϵ , which serves as an implementation-specific offset. When consecutive current samples are compared, $\Delta_{\max}I = \frac{V}{L} - \epsilon$ should be used as the point of comparison. If a $\Delta I \approx \Delta_{\max}I$, it is likely that $R \approx 0$ and a short is occurring. A benefit of using $\Delta_{\max}I$ is the potential for short detection before I_{\max} has been reached. In HSFs, there is no initial current ($I(0) = 0$) which could allow ΔI to approach $\Delta_{\max}I$ before I exceeds I_{\max} .

5.3 Time-to-Detection

The previous section discussed methods of detecting short-circuits which cover the logical requirements of the real-time short-protection task but did not provide any explicit temporal con-

straints. As previously mentioned, short-protection systems are time-sensitive and a valuable short-circuit detection occurs before critical current levels are reached. To do so requires determining the time taken for current to rise from its present value, I , to the critical current, I_{crit} . For the remainder of this paper, we deem this the *time-to-detection*.

5.3.1 Arbitrary Operating Voltage

If the OCM for the circuit in question contains a single operating voltage, it must hold that:

$$\forall V \in \Gamma_I, V = V_{max} \quad (5.2)$$

If Equation (5.2) holds, the *time-to-detection* is:

$$\delta(I, V) = \frac{I_{crit} - I}{V} \cdot L \quad (5.3)$$

where $\delta(I, V)$ is *time-to-detection*, I is current, I_{crit} is the critical current, V is voltage, and L is inductance. The function provides the time required for current to rise from I , to the critical current, I_{crit} , in a DC RL circuit with voltage V and inductance L . This function demonstrates that lower currents and voltages provide a lower *time-to-detection*.

However, to use this function for identifying the smallest time-to-detection in an OCM with multiple voltages would be optimistic. Suppose, for example, a DC RL circuit allows for two operating voltages, V_ℓ and V_h such that $V_\ell < V_h$. Suppose now that at the instant a short-circuit occurs the operating voltage increases from V_ℓ to V_h . The value of $\delta(I, V_\ell)$, calculated before the short-circuit occurred, will be an overestimate of the time required for I to exceed I_{crit} . To address this, we define the

5.3.2 Maximum Operating Voltage

Since using Equation (5.3) becomes optimistic when multiple operating voltages are involved, we can remove optimism by replacing V from Equation (5.3) with V_{max} :

$$\delta(I, V_{max}) = \frac{I_{crit} - I}{V_{max}} \cdot L \quad (5.4)$$

Equation (5.4) ensures a short combined with an instantaneous voltage change to V_{max} is still detected before reaching I_{crit} .

5.3.3 Minimum Time-to-Detection

To provide the worst-case time-to-detection, we use the maximum current, I_{max} and voltage, V_{max} , from the OCM. This *minimum time-to-detection* is defined as:

$$\delta_{min} = \delta(I_{max}, V_{max}) = \frac{I_{crit} - I_{max}}{V_{max}} \cdot L \quad (5.5)$$

This time frame represents time taken for current to rise from the maximum operating current, I_{max} , to the critical current, I_{crit} , with the highest voltage, V_{max} . This *minimum time-to-detection* will be used as a temporal constraint for the proposed real-time task.

CHAPTER 6 Real-time System Model

Thus far, the spatial properties of an inductor have been related to its inductance. Thereafter, inductance is found to determine the maximum possible current rise at any given time, $\frac{V}{L}$ Amperes per second. This leads to the shortest time span over which a short would need to be detected, the *minimum time-to-detection* δ_{min} . Using δ_{min} , we provide a real-time system short-circuit protection task and its timing requirements. Before doing so, we present a real-time background on the sporadic task model and uniprocessor EDF scheduling.

6.1 Sporadic Task Model

In real-time systems, *sporadic tasks* are defined by a *worst-case execution time* (WCET) e_i , relative deadline d_i , and minimum period p_i . The relative deadline is the time between each job arrival and its deadline. The minimum period is the smallest time between successive job arrivals. We use a sporadic task to model the short-circuit protection task [15]. The proposed sporadic task will have an *implicit deadline* where a new job of the short-circuit task T_{scd} may arrive at the absolute deadline of the previous job.

For our short-circuit task T_{scd} , the execution time depends on the short-circuit protection algorithm used, processor speed, and ADC conversion time. Thus, the execution time is not assessed here but modeled as e_{scd} .

The minimum period, however, is derived from Equation (5.4) which provides a scaling *time-to-detection*. The minimum period of the sporadic task must be half the value of the *minimum time-to-detection*. This is required to ensure one full job of T_{scd} is completed strictly after the short-circuit begins. This requirement is demonstrated in Figures 6.1 and 6.2 where T_{scd} executes with a period equal to δ_{min} and $\frac{\delta_{min}}{2}$. Recall that δ_{min} time units after a short, the current level

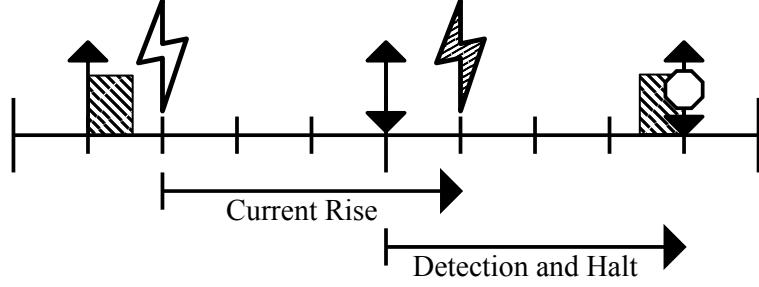


Figure 6.1: Failed Short Protection Schedule
 T_{scd} executing with $p_{scd} = \delta(I_{max}, V_{max}) = 4$.

The short begins at $t = 2$ and I_{crit} is reached at $t = 6$ before T_{scd} can halt the short.

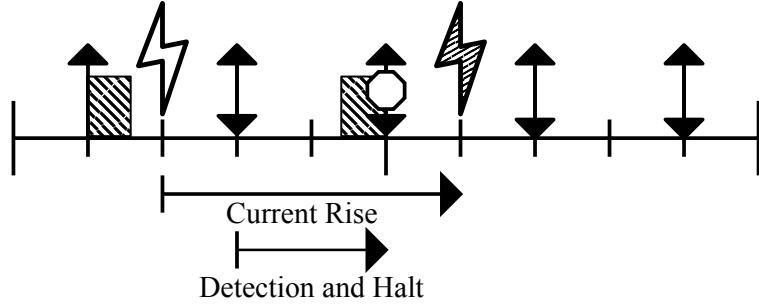


Figure 6.2: Successful Short Protection Schedule
 T_{scd} executing with $p_{scd} = \frac{\delta(I_{max}, V_{max})}{2} = 2$.
The short begins at $t = 2$ and is halted by T_{scd} at $t = 5$ before I_{crit} is reached.

has reached a I_{crit} . Each sporadic job is triggered $\delta(I, V_{max})/2$ seconds after the release of the preceding job, allowing release times to scale with current. The temporal requirements may be converted into a real-time sporadic task $T_{scd} = (e_{scd}, p_{scd})$ with the following parameters:

$$e_{scd} = \text{worst case execution time of short-circuit algorithm} \quad (6.1)$$

$$p_{scd} = \frac{\delta(I_{max}, V_{max})}{2} \quad (6.2)$$

6.2 Preemptive Uniprocessor EDF Scheduling

With T_{scd} defined, we derive its utilization under preemptive uniprocessor EDF scheduling.

According to [14], a set of implicit-deadline sporadic tasks is schedulable with EDF if and only if:

$$\sum_{i=1}^n \frac{e_i}{p_i} \leq 1 \quad (6.3)$$

where i is the index of a task in the set, e_i is the execution time, and p_i is the period. Since we use a single, sporadic task with implicit deadlines, the utilization for T_{scd} is:

$$U(T_{scd}) = \frac{2 \cdot e_{scd}}{\delta(I, V_{max})} \quad (6.4)$$

Using the *minimum time-to-detection*, Equation (6.4) becomes:

$$U(T_{scd}) = \frac{2 \cdot e_{scd}}{\delta(I_{max}, V_{max})} \quad (6.5)$$

Substituting in Equations (5.3) and (3.1) gives:

$$U(T_{scd}) = \left(\frac{2 \cdot e_{scd}}{(I_{crit} - I_{max})} \cdot V_{max} \cdot \frac{\ell}{\mu N^2 A} \right) \quad (6.6)$$

Equation 6.6 relates the inductor spatial parameters to T_{scd} utilization.

CHAPTER 7 Model Optimization

Having related the board space consumed by an inductor and the real-time utilization under EDF schedulability, we propose an optimal solution for fixed values on either end of the relationship. Given a fixed utilization we propose a minimized board space consumption. Given a fixed allowable board space, we propose a minimized real-time utilization. Before optimization analysis of the model, we clarify the optimal inductor orientation for a given prism.

7.1 Optimal Inductor Orientation

In practice, hardware-software co-design is constrained by real-world factors such as size, weight, power, and cost. In this paper, we focus on space as a constraint on our proposed model. Given a fixed volume of space to implement the proposed short-protection system, we must consider the optimal orientation of our solenoid-style air-core inductor inside the fixed volume which maximizes inductance. To find the inductor orientation providing the highest inductance for a given space, we consider two constraints:

1. The area A from Equation (3.1) requires a square area with regard to board space.
2. The board space must be defined in three dimensions: a length ℓ , width w , and height h .

Allowable board space is therefore defined as a set:

$$P = \{\ell, w, h\} \quad (7.1)$$

This set provides the prism dimensions in which the inductor resides. Independent of the prism's orientation, $A_{consumed}$ must be the smallest square to circumscribe the area A of the inductor. The largest square face on which the inductor's area, A , can be placed is limited by the median

dimension in P . Thus, the square of the median is used to fit the largest possible square area:

$$A_{consumed} = \text{median}(P)^2 \quad (7.2)$$

The only remaining dimension is deemed the length of the inductor:

$$\ell = \min(P) \quad (7.3)$$

A visualization of possible orientations can be found in Appendix B along with an explicit example. As previously mentioned and validated in Section 3.3.2, the *Assumption of Constant Turn Density* applies to ℓ and is required for the remaining model optimization.

7.2 Fixed Board Constraints

Having defined equations for consumed area in terms of the volume allotted for the inductor, we address the first optimization problem where the board space is constrained. This approach is useful in situations where the embedded application, or the region of space allotted for short-circuit protection hardware, is restricted in size. Suppose allotted board space is restricted to the prism:

$$P = \{\ell, w, h\}$$

where each element of the set is defined in meters. Combining Equations (4.1) and (7.2) for the area of the inductor A gives:

$$A = \frac{\pi}{4} A_{consumed} = \frac{\pi}{4} \cdot \text{median}(P)^2$$

By substitution of Equation 7.4 into Equation (6.6), the utilization requirement becomes:

$$U(T_{scd}) = \frac{2 \cdot e_{scd} \cdot V_{max} \cdot \min(P)}{(I_{crit} - I_{max}) \cdot \mu \cdot N^2 \cdot \frac{\pi}{4} \cdot \text{median}(P)^2} \quad (7.4)$$

The equation above gives us a minimum utilization requirement for meeting short-circuit protection requirements given the constrained board space and OCM - which provides I_{crit} and I_{max} .

7.3 Fixed Utilization

Having addressed the fixed-volume constraint, we now address the second approach by fixing the maximum utilization allowed short-circuit protection process. This approach is useful in situations where the microprocessor executing T_{scd} is responsible for other tasks which inherently limit $U(T_{scd})$. Suppose the allotted utilization is u . Relying on Equation (6.5) we find the minimum time-to-detection $\delta(I_{max}, V_{max})$ is solved as:

$$\delta_{min} = \delta(I_{max}, V_{max}) = \frac{2 \cdot e_{scd}}{u}$$

Applying Equation (5.5) and isolating L we find:

$$L = \frac{2 \cdot e_{scd} \cdot V_{max}}{u \cdot (I_{crit} - I_{max})}$$

Substituting Equation (3.1) in for L and isolating inductor spatial parameters results in:

$$\frac{A}{\ell} = \frac{2 \cdot e_{scd} \cdot V_{max}}{u \cdot (I_{crit} - I_{max}) \cdot \mu \cdot N^2}$$

Finally, substituting the prism area consumed (Equation 7.2) and prism length (Equation 7.3) into Equation 7.5 above gives:

$$\frac{\text{median}(P)^2}{\text{min}(P)} = \frac{4}{\pi} \cdot \frac{2 \cdot e_{scd} \cdot V_{max}}{u \cdot (I_{crit} - I_{max}) \cdot \mu \cdot N^2} \quad (7.5)$$

This result indicates the air core inductor used in the DC RL circuit must have a minimum allotted board space defined by P which satisfies the above equation.

The model optimizations above highlight how fixed board space can be used to prescribe a minimum utilization and vice versa. We now seek to validate our short-circuit protection model the next chapter where we discuss our experiments and subsequently our results.

CHAPTER 8 Experiments

To implement and validate the application of the software-based approach, we conducted four separate experiments. The following section presents the experiment setup and outlines the conducted experiments. Additionally, the projected utilization for the experiments is presented.

8.1 Experiment Outline

The experiments conducted measured both FUL and HSF short-circuits focusing primarily on FUL short-circuits as they have a smaller time-to-detection. Table 8.1 highlights the variations between experiments which can be summarized as follows: Experiment 1 examines the performance of our approach under FUL short-circuits in terms of detection latency and maximum current reached at the time of detection. Experiment 2 examines the performance under HSF short-circuits also in terms of latency and maximum current reached at the time of detection. Experiment 3 demonstrates how fixing utilization and varying inductance under FUL short-circuits relates to current at the time of detection. Experiment 4 demonstrates the same relationship but with varying utilization and fixed inductance.

Experiment	Fault Type	Demonstrates
1	FUL	Baseline
2	HSF	Lower initial I
3	FUL	Scaling L
4	FUL	Scaling U

Table 8.1: Experiment Descriptions

8.2 Setup

Aside from the variations described above, all experiments were conducted as described here. Short-circuit protection for each experiment was performed on Microchip's DM164103-4 demo board

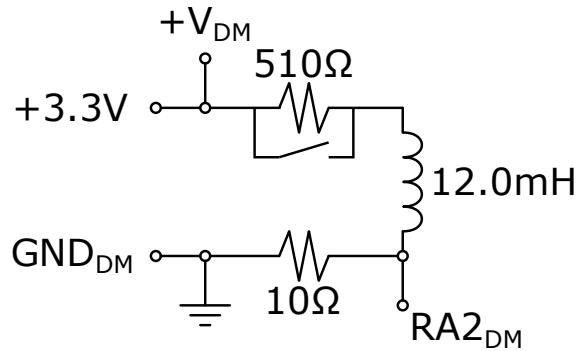


Figure 8.1: Experiment Setup Schematic
Experiment Setup Schematic

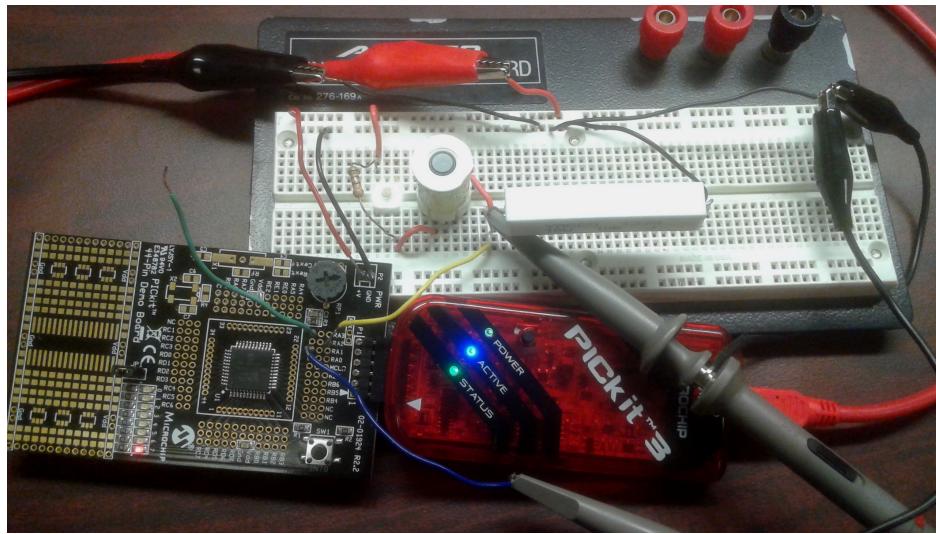


Figure 8.2: Experiment Setup Image

with a PIC18F45K20 CPU. The demo board and programmer were selected for their relatively low cost to encourage reproducibility. Figure 8.1 depicts the experimental circuit schematic. In the schematic, subscripts *DM* refer to connections made to the Microchip demo board. The setup also requires attaching oscilloscope probes to ports RA2 in Figure 8.1 and RA1 on the demo board. Figure 8.2 depicts the proper connection of all materials in Experiment 1. All probe connections route off-camera to the oscilloscope. An extended list of non-trivial materials used in the experiments can be found in Appendix A.

The circuit was run in advance of experiments to identify experimental operating currents and

voltages and their respective maximums. This process could be avoided by analyzing the tolerance values for all components used but was explicitly measured here to provide exact values. The OCM for the setup using solid, 22 American Wire Gauge (AWG) copper wire was:

$$C = (\Gamma_I, 150mA) \quad \Gamma_I = (\gamma_0) \quad \gamma_0 = (7.74mA, 3.3V)$$

Although the resistor R_1 pictured in 8.2 is a 10W power resistor capable of handling higher current, we defer to the power rating of a conventional though-hole power resistor which we assume to be 0.5 Watts. Since 150 mA through a 0.5 Watt resistor exceeds the power rating at an operating voltage of 3.3 V, 150 mA is considered the critical current I_{crit} for the circuit.

After deriving the OCM from the circuit, Equation (4.5) provides the maximum operating current and voltage:

$$I_{max} = 7.74mA \quad V_{max} = 3.3V$$

Note that the critical current is 150mA meaning current above 7.74mA is considered unexpected behavior while current at or above 150mA is damaging. Having constructed the mathematical model of our system, we may now project the utilization requirement in the following section.

8.3 Projected Utilization

Using the OCM derived from the experiment setup, we apply Equations 6.4 and 6.5 as the scaling utilization and minimum utilization. For this projected utilization, our protection method required an execution time of 25 microseconds. Figure 8.3 depicts the projection of fixed minimum utilization and the scaling utilization. The minimum utilization indicates the expected minimum utilization required to detect a short-circuit in the experiment. The scaling utilization represents the minimum utilization required at *any* given value of I as derived from Equation (6.4). These

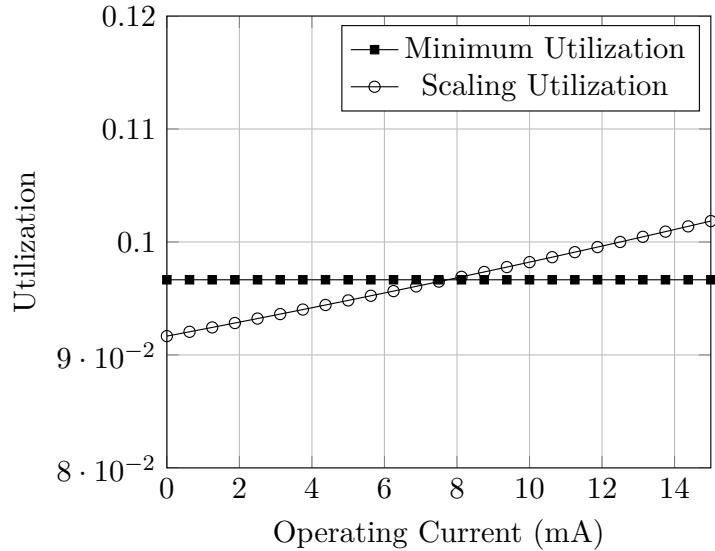


Figure 8.3: Simulated Utilization vs. Operating Current

projected utilizations indicate the provided short-protection approach could safely detect and halt a short-circuit before critical current levels are reached at a uniprocessor utilization of under 0.1. The scaling utilization curve indicates the lower minimum utilization requirement for systems with lower operating currents.

CHAPTER 9 Results

9.1 Experiments 1 and 2: FUL and HSF Detection

To validate the hardware-software co-design approach, two short-circuit fault types were induced in separate experiments. As shown in Table 8.1, Experiment 1 induced an FUL short while Experiment 2 induced an HSF short. Each experiment was run three times with all data provided in Table 9.1. In the table, I_c is the current at the time of detection and Δt is the latency between short-circuit and detection. Three runs per fault type was selected due to time required to manually induce the short and reset each experiment.

Both experiments demonstrate successful detection of FUL and HSF short-circuits before current rises above I_{crit} . Both experiments also demonstrate latency one-tenth of the minimum time to detection. For experiment 1, using the FUL, the short-circuit was manually induced while the circuit was powered. In contrast, experiment 2 required removal of load resistor R_0 from Figure 8.1. This ensures the short-circuit begins immediately upon powering the circuit. As a result of this change, there is no initial current in the HSF as there is with the FUL short.

In addition to the comparison table, an example FUL waveform is shown in Figure 9.1 as it was the most used short-circuit fault test. The plot shows the circuit current, sampled on port RA2,

Fault	R (Ohm)	I_c (mA)	Δt (us)	U(T _{scd})
FUL	510	42.400	159.79	0.1316
FUL	510	38.800	142.59	0.1316
FUL	510	20.000	50.39	0.1316
HSF	0	35.200	149.60	0.1316
HSF	0	35.200	72.01	0.1316
HSF	0	35.200	175.20	0.1316

Table 9.1: FUL and HSF Comparison

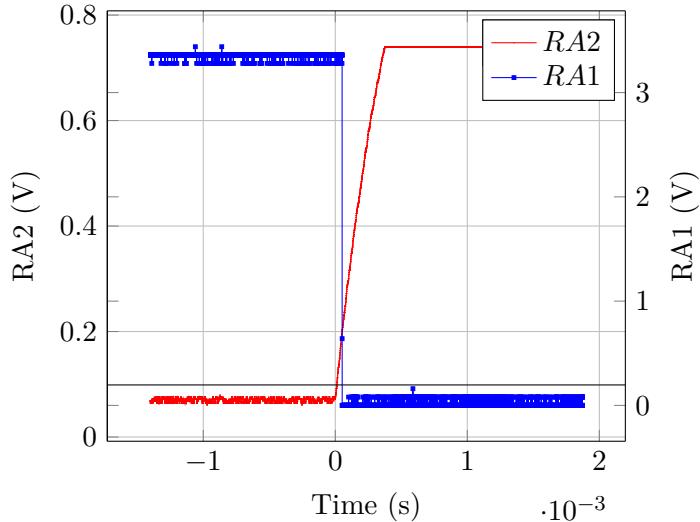


Figure 9.1: FUL Short Waveform

rise immediately after the short-circuit. The short-circuit detection signal, output on port RA1, shows the output signal voltage drop to zero indicating the detection of a fault and the cutting of power by the microprocessor. Due to its similar nature, the waveform for the HSF experiment is excluded. The current at the time of detection for both fault types in all runs did not exceed I_{crit} , 150mA; thus, the proposed short-circuit protection succeeded in safely mitigating damage from both FUL and HSF short-circuits.

9.2 Experiments 3 and 4: Inductance and Utilization Scaling

Experiments 3 and 4 focused on demonstrating the potential for scaling inductance and utilization as co-design parameters are changed. In Experiment 3, the schematic depicted in Figure 8.1 was used with varying sized inductors as opposed to experiment 1 and 2 which used fixed values. For each inductance value, L , a FUL short was induced. Real-time utilization was maximized at 100%, $U = 1.0$, to demonstrate the broadest range of inductors. As seen in Figure 9.2, a decrease in inductance given a constant utilization results in a higher current at the time of detection. This trend validates the relationship presented in Equation 6.6. In conjunction with the optimal inductor

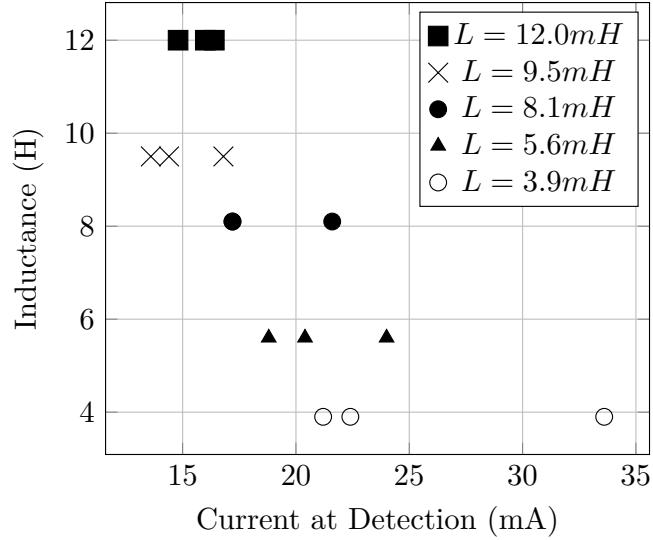


Figure 9.2: Experiment 3 Results: Scaling Inductance
Experiment 3 Results: Inductance vs Current at Detection

orientation analysis, the results show short-circuit detection at lower current levels can be traded for a smaller inductor consuming less board space.

A similar procedure was used in Experiment 4 but with fixed inductor sizes and varying real-time utilizations. In Experiment 4, the schematic in Figure 8.1 is used but with an inductance of $L = 12\text{mh}$. This large value of inductance was selected to demonstrate the broadest range of real-time utilizations. The results, presented in Figure 9.3, show a decrease in utilization given a constant inductance leads to a higher current at the time of detection. This again validates the relationship provided in Equation (6.6).

The results of Experiment 3 and Experiment 4 indicate that $U(T_{scd})$ can be traded with inductance L in our model to maintain a stable current at the time of detection. It follows that inductor size and board space consumed by the proposed short-circuit protection model may be traded with the utilization of the provided software-based protection approach.

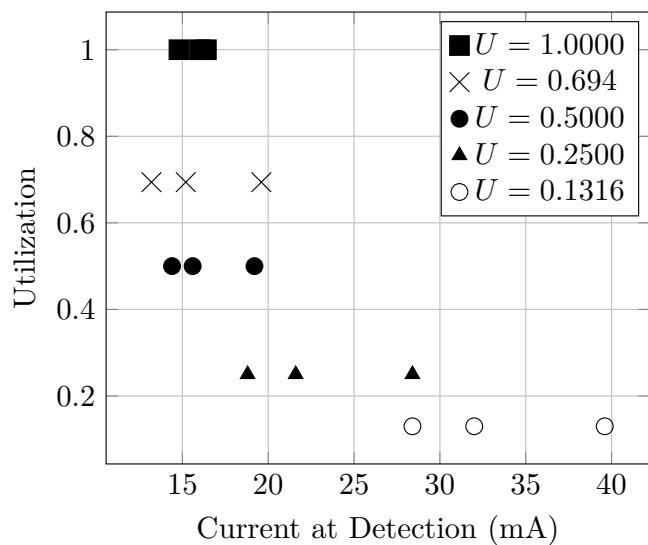


Figure 9.3: Experiment 4 Results: Scaling Utilization
Experiment 4 Results: Utilization vs Current at Detection

CHAPTER 10 Conclusion

This work provides a novel solution for hardware-software co-design of real-time software-based short-circuit protection systems – cyber-physical systems in which the inductive properties of a DC RL circuit are leveraged to construct a sporadic, real-time short-circuit protection task. We established a relationship between utilization and board space consumed by the air-core, solenoid-style inductor placed in-circuit which can be optimized for both fixed inductor volume and fixed uniprocessor utilization.

Like preceding works on engine control [1] and thermal-aware systems [7], this work demands further investigation into the real-time control of physical systems demonstrating dynamic behavior. Further study on the energy and performance trade-off between hardware, software, and physical system dynamics is reserved for future work.

APPENDICES

APPENDIX A Materials

Non-trivial materials used in the experiments can be found in Figure A.1. Excluded from the materials list are elements including cooper wire, breadboards, and a power supply. To minimize cost of replication, through-hole parts are used in place of smaller, surface-mount components.

Item	Manufacturer	Part Number(s)
Debugger	Microchip	PG164130
Inductor	Triad Magnetics	RC-1; RC-2; RC-3
Microprocessor	Microchip	DM164130-4
Oscilloscope	RIGOL	DS1102E
Oscilloscope Probe	HANTEK	PP-150
Power Resistor	YAGEO	1334 10W 10R J
Resistor	N/A	510Ω 5% resistor

Figure A.1: Materials List
Materials list for Experiments 1-4

APPENDIX B Inductor Orientation Visualization

Given an allowable board space defined as a prism, $P = \{\ell, w, h\}$, there are only three unique orientations for an air-core, solenoid-style inductor in the space. The inductor may be oriented with A located on:

1. the plane formed by l and w extending along h .
2. the plane formed by l and h extending along w .
3. the plane formed by w and h extending along l .

Figure B.1 depicts each of these orientations inside a prism with dimensions:

$$P = \{3, 2, 1\}$$

Notice the inductor consuming the most volume has its area A on the plane formed by the two largest dimensions.

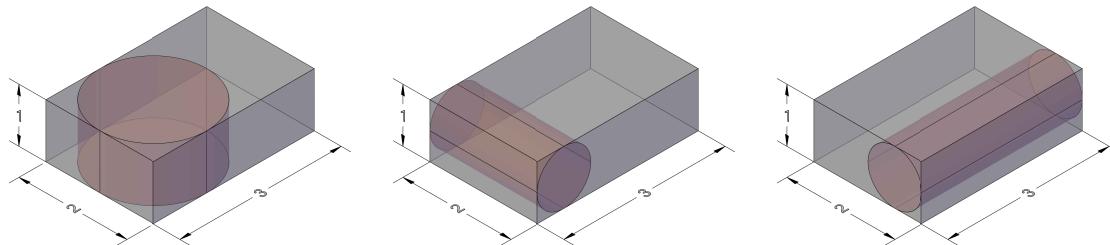


Figure B.1: Inductor Orientation Visualization
Possible orientations of air-core, solenoid-style inductors in a constrained space

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ABSTRACT

TRADING UTILIZATION FOR CIRCUITRY: HARDWARE-SOFTWARE CO-DESIGN FOR REAL-TIME SOFTWARE-BASED SHORT-CIRCUIT PROTECTION

by

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October 2018

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Short-circuit faults are a potential source of damage to circuitry in DC-powered systems. Industrial applications including power converters, inverters, and insulated-gate bipolar transistors (IGBTs) often rely on fault protection systems in the form of dedicated circuitry to prevent damage. To increase flexibility in short-circuit protection and decrease dedicated circuitry, a software-based approach is presented. This implementation requires minimal circuitry and allows for trade-off between board space and processor utilization. The design relies on a single inductor and microprocessor running a real-time task for identifying current and monitoring circuitry for faults. Experiments demonstrate detection of both hard-switching faults (HSF) and fault under load (FUL) shorts. The depicted relationship between processor utilization and board space consumed by the circuitry is confirmed through experimentation and allows optimization of board space with respect to utilization and vice versa. As a result, the proposed software-based protection is implementable with the addition of a single component and protects against damage from both HSF and FUL shorts.