# Aarush Goradia

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## EDUCATION

**Princeton University** May 2027
B.S.E. in Electrical and Computer Engineering, Minor in Computer Science & English
Cumulative GPA: 3.69
Relevant Coursework: Contemporary Logic Design, Programming Systems, Data Structures and Algorithms, Advanced Circuit Design, Computer Architecture, Machine Learning, Probability and Stochastic Systems

## HARDWARE EXPERIENCE

*Technology Development Intern*, **Advanced Micro Foundry**, Singapore June 2025 - Present
- Developed a Python & C++ based program to automate preliminary checks on GDS files for fabrication requirements, transforming a previously manual process and reducing review time from hours to minutes.
- Rewrote core GDS analysis routines in C++ to reduce execution time by 15–20× over prior Python implementations.
- Built interactive wafer optimization scripts in Python using Jupyter to maximize die count based on configurable parameters.
- Integrated automated DRC and validation routines into tape-out workflows, collaborating closely with engineers.

*Head of Embedded Systems,* **Princeton Rover Team**, Princeton, NJ September 2024 – Present
- Design, prototype, and build a Mars rover to compete in the University Rover Challenge 2025.
- Programmed the 915 MHz and 2.4 GHz communications systems between the base station and the rover.
- Designed power delivery and peripheral electronics PCB for Rover functioning using KiCAD.

*Independent Researcher*, **Sengupta Lab,** Princeton, NJ August 2024 – May 2025
- Scripted (Python) & simulated transformer layouts in Cadence Virtuoso to create a synthetic geometry-performance dataset.
- Trained a 3-layer 32-neuron multi-layer perceptron neural network using Python to predict transformer geometry from lumped parameters with 90% accuracy.
- Wrote a Python algorithm to automate cascaded transformer-based low-noise amplifiers using the model's predictions.
- Authored two research papers detailing transformer layout simulation, model training pipeline, and LNA synthesis automation; each received an A from faculty reviewers.

*PUnC (Princeton University Computer)* November 2024 – December 2024
- Designed a custom 16-instruction processor using FSM-based control and datapath logic.
- Wrote and simulated Verilog modules using AMD Vivado and deployed to an FPGA board for functional testing.

## SOFTWARE EXPERIENCE

*FixedPointDSP* July 2025
- Built a header-only fixed-point C++ library with customizable overflow policies using modern type-safe design.
- Implemented FIR filters, dynamic coefficient generation, DFT, FFT, and convolution support.
- Achieved 100% test coverage with GoogleTest; benchmarked FFT with GoogleBenchmark to confirm O(*n log n*) complexity.

*AI Engineering Intern,* **AI Seer**, Singapore May 2024 - July 2024
- Built a LangChain Agent process (Python) with custom tools to fact check which increased accuracy from 85% to 92%.
- Built a live-stream transcription system with real-time speaker diarization and punctuation, using whisper in Python.
- Presented the web app to Singapore's Senior Minister of State for Communications and Information.
- Filed patent for the fact checking process: U.S. Patent Application No.: 19/011,265.

## SKILLS

**Programming Languages:** Advanced in Python, Java; Intermediate in C, C++, Verilog, Linux CLI; Basic in HTML, CSS, ARM Assembly; Currently Learning: SystemVerilog
**Design Software:** KiCAD, AMD Vivado, NX Siemens, Cadence Virtuoso, Cadence EMX, KLayout
**Hardware Skills:** PC Building, Embedded Systems Prototyping (Arduino, Microcontrollers)
**Languages:** English (Native), Chinese (Fluent), Hindi (Intermediate), Gujarati (Speaking Fluency)