Version 1 Student ID: ________________________

Department of Electrical and Software Engineering

Schulich School of Engineering

ENCM 511: Embedded Systems Interfacing

MID TERM TEST I: SAMPLER SET

NOTE: This document provides an example of the "style" of questions, but does not reflect the number of questions to be asked in the mid-term test.

Notes:

- Answer ALL questions
- Show ALL working
- This is a closed-book test
- You are allowed to use an approved calculator
- Write your ID number on every page
- Poorly presented answers, while otherwise correct, may not score full marks
- State any assumptions that you make, especially as needed to clarify your answers

EXAMPLES FOR QUESTION ONE

(a) What is an **embedded system**?

(b) Embedded Systems are often characterized as **reactive**. What does it mean for a system to be "reactive"?

(c) Give an example of, and explain, the concept of a **functional requirement** for an embedded system.

EXAMPLES FOR QUESTION TWO

(a) The pins on the PIC24F16KA101 microcontroller that we use in this class are multiplexed. Explain what is meant by pin multiplexing. Why is pin multiplexing useful?

(b) What are the different uses of the following special function registers: TRISA, PORTA, LATA, and CNPU1?

(c) Explain the concept of polling.

(d) Write C code to demonstrate the use of polling (of RA4):

```
int main(void) {

    /* assume correct SFR bits are set */

    while(1) {







    }
    return 0;
}
```

EXAMPLES FOR QUESTION THREE (10 marks)

(a) Assume we want to are want to use TIMER2 (16-bit timer), with TCKPCS<1:0> = 0b00 and the system oscillator set to 8 MHz. What is the minimum time interval that this timer can produce?

(b) What is the maximum time interval that this timer can produce?

(c) Assume that we want to keep using the 8 MHz FOSC. Explain what we can do with the timer configuration to increase the TIMER2 range.

(d) Write a simple interrupt service routine (ISR) to set a global variable `uint8_t t2FLAG`, every time the timer interval elapses, ensuring that the rest of the C program can operate normally while the timer is operating.

```
// assume there is a global variable called t2FLAG that is available

void __attribute__((interrupt, no_auto_psv)) _T2Interrupt(void)  {




}
```

Selected Excerpts from the PIC24F16KA102 Family Datasheet

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R-0, HSC	R-0, HSC	R-0, HSC	U-0	R/W-x[1]	R/W-x[1]	R/W-x[1]
—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0
bit 15							bit 8

R/SO-0, HSC	U-0	R-0, HSC[2]	U-0	R/CO-0, HS	U-0	R/W-0	R/W-0
CLKLOCK	—	LOCK	—	CF	—	SOSCEN	OSWEN
bit 7							bit 0

Legend:	CO = Clearable Only bit		
SO = Settable Only bit	HS = Hardware Settable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC<2:0>:** Current Oscillator Selection bits

- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC<2:0>:** New Oscillator Selection bits[1]

- 111 = 8 MHz Fast RC Oscillator with Postscaler (FRCDIV)
- 110 = 500 kHz Low-Power Fast RC Oscillator (FRC) with Postscaler (LPFRCDIV)
- 101 = Low-Power RC Oscillator (LPRC)
- 100 = Secondary Oscillator (SOSC)
- 011 = Primary Oscillator with PLL module (XTPLL, HSPLL, ECPLL)
- 010 = Primary Oscillator (XT, HS, EC)
- 001 = 8 MHz FRC Oscillator with Postscaler and PLL module (FRCPLL)
- 000 = 8 MHz FRC Oscillator (FRC)

Note 1: Reset values for these bits are determined by the FNOSC Configuration bits.

2: Also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 7 **CLKLOCK:** Clock Selection Lock Enabled bit

If FSCM is enabled (FCKSM1 = 1):
1 = Clock and PLL selections are locked
0 = Clock and PLL selections are not locked and may be modified by setting the OSWEN bit

If FSCM is disabled (FCKSM1 = 0):
Clock and PLL selections are never locked and may be modified by setting the OSWEN bit.

bit 6 **Unimplemented:** Read as '0'

bit 5 **LOCK:** PLL Lock Status bit(2)
1 = PLL module is in lock or PLL module start-up timer is satisfied
0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit
1 = FSCM has detected a clock failure
0 = No clock failure has been detected

bit 2 **Unimplemented:** Read as '0'

bit 1 **SOSCEN:** 32 kHz Secondary Oscillator (SOSC) Enable bit
1 = Enable secondary oscillator
0 = Disable secondary oscillator

bit 0 **OSWEN:** Oscillator Switch Enable bit
1 = Initiate an oscillator switch to clock source specified by NOSC<2:0> bits
0 = Oscillator switch is complete

Note 1: Reset values for these bits are determined by the FNOSC Configuration bits.
2: Also resets to '0' during any valid clock switch or whenever a non-PLL Clock mode is selected.

11.0 I/O PORTS

Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the I/O ports, refer to the *"PIC24F Family Reference Manual"*, **Section 12. "I/O Ports with Peripheral Pin Select (PPS)"** (DS39711). Note that the PIC24F16KA102 family devices do not support Peripheral Pin Select features.

All of the device pins (except VDD and VSS) are shared between the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

11.1 Parallel I/O (PIO) Ports

A parallel I/O port that shares a pin with a peripheral is, in general, subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 displays how ports are shared with other peripherals and the associated I/O pin to which they are connected.

When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin may be read, but the output driver for the parallel port bit will be disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin may be driven by a port.

All port pins have three registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Data Latch register (LATx), read the latch. Writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device will be disabled. That means the corresponding LATx and TRISx registers, and the port pin will read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

Note:	The I/O pins retain their state during Deep Sleep. They will retain this state at wake-up until the software restore bit (RELEASE) is cleared.

11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORT, LAT and TRIS registers for data control, each port pin can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The maximum open-drain voltage allowed is the same as the maximum V_{IH} specification.

11.2 Configuring Analog Port Pins

The use of the AD1PCFG and TRIS register controls the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP.

11.3 Input Change Notification

The input change notification function of the I/O ports allows the PIC24F16KA102 family of devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature is capable of detecting input Change-of-States even in Sleep mode, when the clocks are disabled. Depending on the device pin count, there are up to 23 external signals (CN0 through CN22) that may be selected (enabled) for generating an interrupt request on a Change-of-State.

There are six control registers associated with the CN module. The CNEN1 and CNEN2 registers contain the interrupt enable control bits for each of the CN input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each CN pin also has a weak pull-up/pull-down connected to it. The pull-ups act as a current source that is connected to the pin and the pull-downs act as a current sink to eliminate the need for external resistors when push button or keypad devices are connected.

On any pin, only the pull-up resistor or the pull-down resistor should be enabled, but not both of them. If the push button or the keypad is connected to V_{DD}, enable the pull-down, or if they are connected to V_{SS}, enable the pull-up resistors. The pull-ups are enabled separately using the CNPU1 and CNPU2 registers, which contain the control bits for each of the CN pins.

Setting any of the control bits enables the weak pull-ups for the corresponding pins. The pull-downs are enabled separately using the CNPD1 and CNPD2 registers, which contain the control bits for each of the CN pins. Setting any of the control bits enables the weak pull-downs for the corresponding pins.

When the internal pull-up is selected, the pin uses V_{DD} as the pull-up source voltage. When the internal pull-down is selected, the pins are pulled down to V_{SS} by an internal resistor. Make sure that there is no external pull-up source/pull-down sink when the internal pull-ups/pull-downs are enabled.

Note:	Pull-ups and pull-downs on change notification pins should always be disabled whenever the port pin is configured as a digital output.

REGISTER 22-5: AD1PCFG: A/D PORT CONFIGURATION REGISTER

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PCFG15	PCFG14	—	PCFG12	PCFG11	PCFG10	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PCFG15:** Analog Input Pin Configuration Control bit
1 = Analog channel is disabled from input scan
0 = Internal band gap (VBG) channel is enabled for input scan

bit 14 **PCFG14:** Analog Input Pin Configuration Control bit
1 = Analog channel is disabled from input scan
0 = Internal VBG/2 channel is enabled for input scan

bit 13 **Unimplemented:** Read as '0'

bit 12-10 **PCFG<12:10>:** Analog Input Pin Configuration Control bits
1 = Pin for corresponding analog channel is configured in Digital mode; I/O port read is enabled
0 = Pin is configured in Analog mode; I/O port read is disabled; A/D samples pin voltage

bit 9-6 **Unimplemented:** Read as '0'

bit 5-0 **PCFG<5:0>:** Analog Input Pin Configuration Control bits
1 = Pin for corresponding analog channel is configured in Digital mode; I/O port read is enabled
0 = Pin configured in Analog mode; I/O port read is disabled; A/D samples pin voltage

REGISTER 13-1: T2CON: TIMER2 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32[1]	—	TCS	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer2 On bit
When T2CON<3> = 1:
1 = Starts 32-bit Timer2/3
0 = Stops 32-bit Timer2/3
When T2CON<3> = 0:
1 = Starts 16-bit Timer2
0 = Stops 16-bit Timer2

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer2 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer2 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit[1]
1 = Timer2 and Timer3 form a single 32-bit timer
0 = Timer2 and Timer3 act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timer2 Clock Source Select bit
1 = External clock from pin, T2CK (on the rising edge)
0 = Internal clock (Fosc/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: In 32-bit mode, the T3CON control bits do not affect 32-bit timer operation.

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit in T2CON<3>.
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the interrupt enable bit, TxIE; use the priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON bit (TxCON<15> = 1).

REGISTER 8-1: SR: ALU STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC
—	—	—	—	—	—	—	DC[(1)]
bit 15							bit 8

R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC	R/W-0, HSC
IPL2[(2,3)]	IPL1[(2,3)]	IPL0[(2,3)]	RA[(1)]	N[(1)]	OV[(1)]	Z[(1)]	C[(1)]
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as ‘0’

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits[(2,3)]

111 = CPU interrupt priority level is 7 (15); user interrupts disabled
110 = CPU interrupt priority level is 6 (14)
101 = CPU interrupt priority level is 5 (13)
100 = CPU interrupt priority level is 4 (12)
011 = CPU interrupt priority level is 3 (11)
010 = CPU interrupt priority level is 2 (10)
001 = CPU interrupt priority level is 1 (9)
000 = CPU interrupt priority level is 0 (8)

Note 1: See Register 3-1 for the description of these bits, which are not dedicated to interrupt control functions.

2: The IPL bits are concatenated with the IPL3 bit (CORCON<3>) to form the CPU interrupt priority level. The value in parentheses indicates the interrupt priority level if IPL3 = 1.

3: The IPL Status bits are read-only when NSTDIS (INTCON1<15>) = 1.

REGISTER 8-5: IFS0: INTERRUPT FLAG STATUS REGISTER 0

R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
NVMIF	—	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPF1IF	T3IF
bit 15							bit 8

R/W-0, HS	U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0, HS
T2IF	—	—	—	T1IF	OC1IF	IC1IF	INT0IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 8 **T3IF:** Timer3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **T2IF:** Timer2 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3 **T1IF:** Timer1 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1

R/W-0, HS	R/W-0, HS	R/W-0, HS	U-0	U-0	U-0	U-0	U-0
U2TXIF	U2RXIF	INT2IF	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-0	R/W-0
—	—	—	INT1IF	CNIF	CMIF	MI2C1IF	SI2C1IF
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 4 **INT1IF:** External Interrupt 1 Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CNIF:** Input Change Notification Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **CMIF:** Comparator Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-9: IEC0: INTERRUPT ENABLE CONTROL REGISTER 0

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NVMIE	—	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPF1IE	T3IE
bit 15							bit 8

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
T2IE	—	—	—	T1IE	OC1IE	IC1IE	INT0IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 9 **SPF1IE:** SPI1 Fault Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 8 **T3IE:** Timer3 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **T2IE:** Timer2 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request not is enabled

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **T1IE:** Timer1 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-10: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
U2TXIE	U2RXIE	INT2IE	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	INT1IE	CNIE	CMIE	MI2C1IE	SI2C1IE
bit 7							bit 0

bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 3 **CNIE:** Input Change Notification Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **CMIE:** Comparator Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 8-14: IPC1: INTERRUPT PRIORITY CONTROL REGISTER 1

U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	T2IP2	T2IP1	T2IP0	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **T2IP<2:0>:** Timer2 Interrupt Priority bits
111 = Interrupt is Priority 7 (highest priority interrupt)
•
•
•
001 = Interrupt is Priority 1
000 = Interrupt source is disabled

bit 11-0 **Unimplemented:** Read as ‘0’

8.4 Interrupt Setup Procedures

8.4.1 INITIALIZATION

To configure an interrupt source:

1. Set the NSTDIS Control bit (INTCON1<15>) if nested interrupts are not desired.
2. Select the user-assigned priority level for the interrupt source by writing the control bits in the appropriate IPCx register. The priority level will depend on the specific application and type of interrupt source. If multiple priority levels are not desired, the IPCx register control bits, for all enabled interrupt sources, may be programmed to the same non-zero value.

> **Note:** At a device Reset, the IPCx registers are initialized, such that all user interrupt sources are assigned to Priority Level 4.

3. Clear the interrupt flag status bit associated with the peripheral in the associated IFSx register.
4. Enable the interrupt source by setting the interrupt enable control bit associated with the source in the appropriate IECx register.

8.4.2 INTERRUPT SERVICE ROUTINE

The method that is used to declare an ISR and initialize the IVT with the correct vector address depends on the programming language (i.e., C or assembler) and the language development toolsuite that is used to develop the application. In general, the user must clear the interrupt flag in the appropriate IFSx register for the source of the interrupt that the ISR handles. Otherwise, the ISR will be re-entered immediately after exiting the routine. If the ISR is coded in assembly language, it must be terminated using a RETFIE instruction to unstack the saved PC value, SRL value and old CPU priority level.

TABLE 4-4: ICN REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CNEN1	0060	CN15IE[1]	CN14IE	CN13IE	CN12IE	CN11IE[1]	—	CN9IE	CN8IE	CN7IE[1]	CN6IE	CN5IE	CN4IE	CN3IE	CN2IE	CN1IE	CN0IE	0000
CNEN2	0062	—	CN30IE	CN29IE	—	CN27IE[1]	—	—	CN24IE[1]	CN23IE	CN22IE	CN21IE	—	—	—	—	CN16IE[1]	0000
CNPU1	0068	CN15PUE[1]	CN14PUE	CN13PUE	CN12PUE	CN11PUE[1]	—	CN9PUE	CN8PUE	CN7PUE[1]	CN6PUE	CN5PUE	CN4PUE	CN3PUE	CN2PUE	CN1PUE	CN0PUE	0000
CNPU2	006A	—	CN30PUE	CN29PUE	—	CN27PUE[1]	—	—	CN24PUE[1]	CN23PUE	CN22PUE	CN21PUE	—	—	—	—	CN16PUE[1]	0000
CNPD1	0070	CN15PDE[1]	CN14PDE	CN13PDE	CN12PDE	CN11PDE[1]	—	CN9PDE	CN8PDE	CN7PDE[1]	CN6PDE	CN5PDE	CN4PDE	CN3PDE	CN2PDE	CN1PDE	CN0PDE	0000
CNPD2	0072	—	CN30PDE	CN29PDE	—	CN27PDE[1]	—	—	CN24PDE[1]	CN23PDE	CN22PDE	CN21PDE	—	—	—	—	CN16PDE[1]	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: These bits are not implemented in 20-pin devices.

TABLE 4-12: PORTA REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5[1]	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	—	—	—	—	—	—	—	—	TRISA7[4]	TRISA6	—	TRISA4	TRISA3[5,6]	TRISA2[5]	TRISA1	TRISA0	00DF
PORTA	02C2	—	—	—	—	—	—	—	—	RA7[4]	RA6	RA5	RA4[3]	RA3[5,6]	RA2[5]	RA1[2]	RA0[2]	xxxx
LATA	02C4	—	—	—	—	—	—	—	—	LATA7[4]	LATA6	—	LATA4	LATA3[5,6]	LATA2[5]	LATA1	LATA0	xxxx
ODCA	02C6	—	—	—	—	—	—	—	—	ODA7[4]	ODA6	—	ODA4	ODA3[5,6]	ODA2[5]	ODA1	ODA0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: This bit is available only when MCLRE = 0.
2: A read of RA1 and RA0 results in '0' when debug is active on the PGC2/PGD2 pin.
3: A read of RA4 results in '0' when debug is active on the PGC3/PGD3 pin.
4: These bits are not implemented in 20-pin devices.
5: These bits are available only when the primary oscillator is disabled (POSCMD<1:0> = 00); otherwise read as '0'.
6: These bits are available only when the primary oscillator is disabled or EC mode is selected (POSCMD<1:0> = 00 or 11) and CLKO is disabled (OSCIOFNC = 0); otherwise read as '0'.

TABLE 4-13: PORTB REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C8	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11[3]	TRISB10[3]	TRISB9	TRISB8	TRISB7	TRISB6[3]	TRISB5[3]	TRISB4	TRISB3[3]	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02CA	RB15	RB14	RB13	RB12	RB11[3]	RB10[3]	RB9	RB8	RB7	RB6[3]	RB5[3]	RB4[2]	RB3[3]	RB2	RB1[1]	RB0[1]	xxxx
LATB	02CC	LATB15	LATB14	LATB13	LATB12	LATB11[3]	LATB10[3]	LATB9	LATB8	LATB7	LATB6[3]	LATB5[3]	LATB4	LATB3[3]	LATB2	LATB1	LATB0	xxxx
ODCB	02CE	ODB15	ODB14	ODB13	ODB12	ODB11	ODB10	ODB9	ODB8	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: A read of RB1 and RB0 results in '0' when debug is active on the PGEC1/PGED1 pins.
2: A read of RB4 results in '0' when debug is active on the PGEC3/PGED3 pins.
3: PORTB bits, 11, 10, 6, 5 and 3, are not implemented in 20-pin devices.