Lab 2

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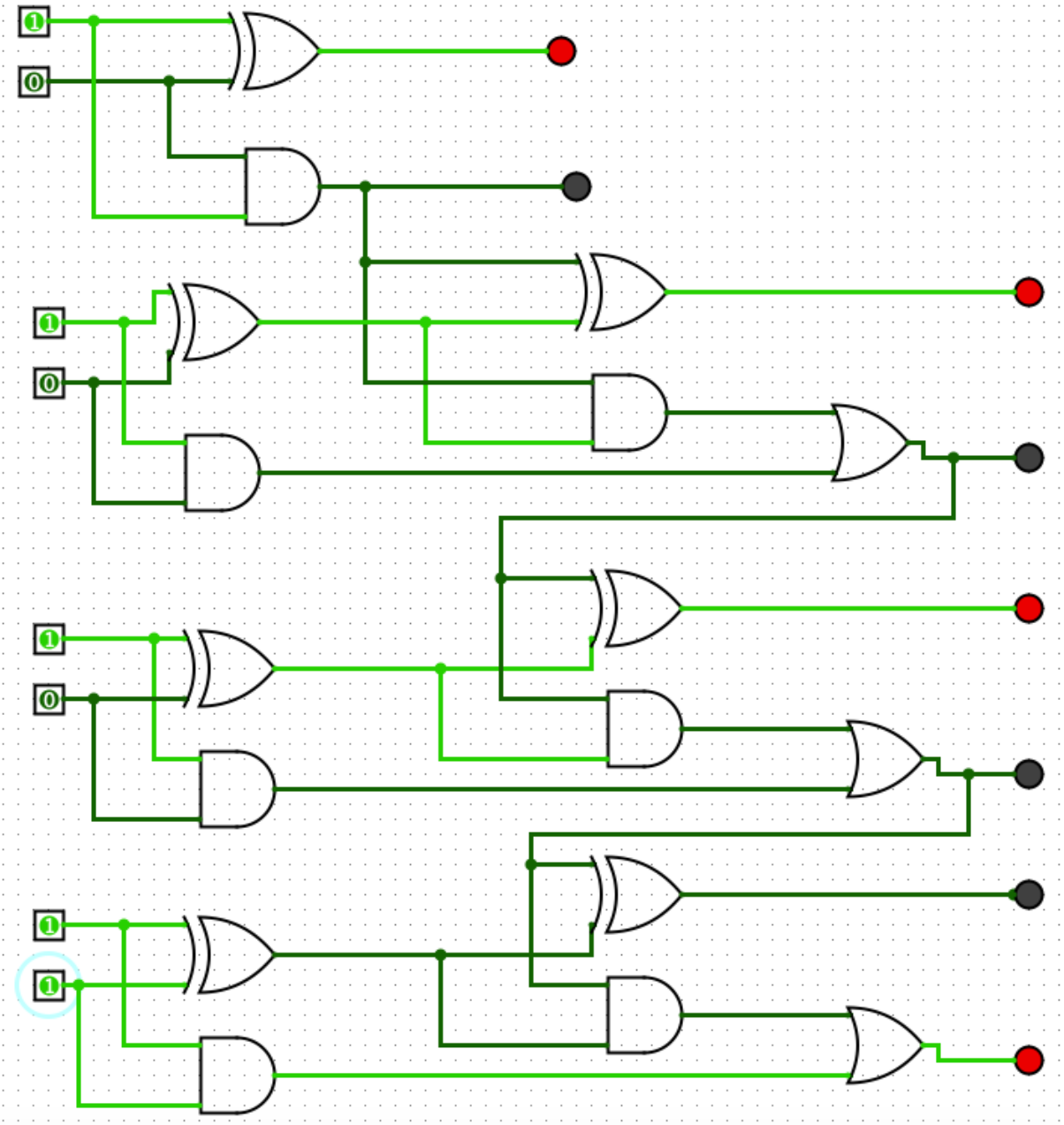
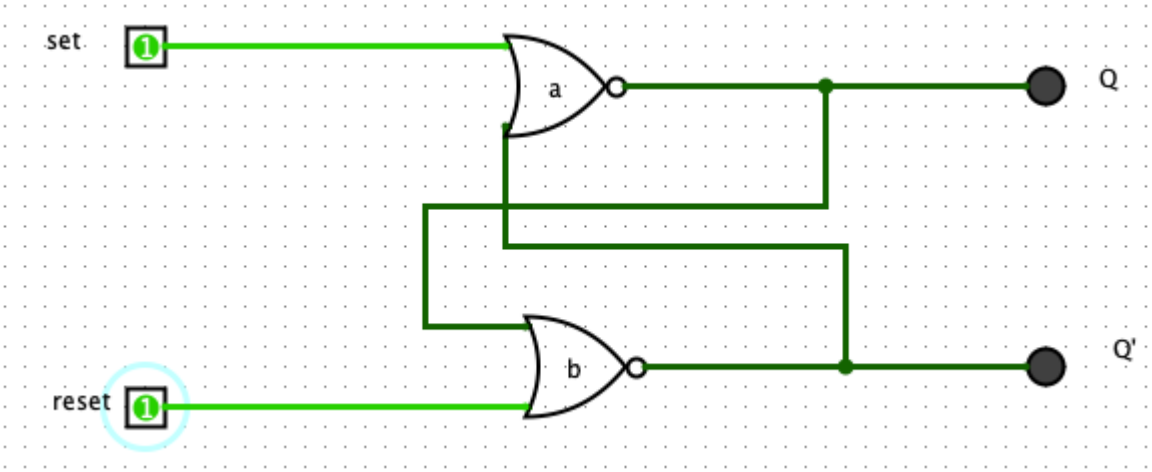
4-Bit adder



Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

R-S Flip Flop

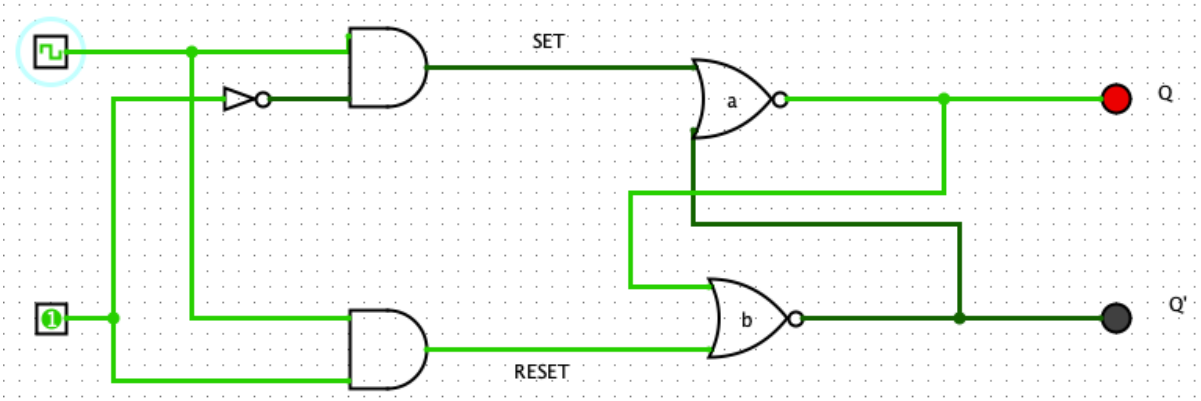


Set	Reset	Q	Q’
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0

1) In an R-S flip flop, if the reset is set to be 0 and set is 1, the set will make the output Q 0 making the input of B (0,0) which will make output Q’ to be 1 and vice versa.
2) As the name suggests, in normal conditions the flip flop circuit should have opposite outputs. When the circuit is set to be (0,0) and set to (1,1) after that

we can see that either of the outputs will get 1 or 0 and it's indeterminate. This is the problem that it causes in digital circuit design.

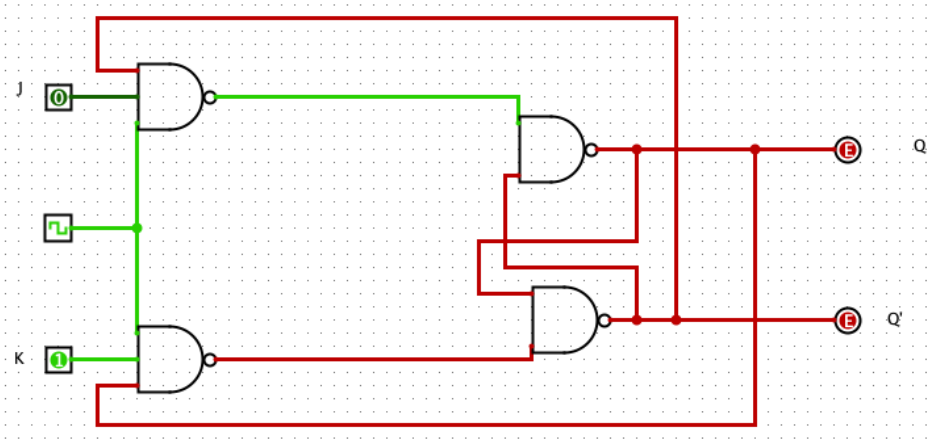
D FLIP FLOP



Clock	Input	Q	Q'
0	0	0	1
0	1	0	1
1	1	1	0
1	0	0	1

1) In a D Flip Flop, the results cant be observed until the clock is ticked. In a D flip flop, the value of the input is the same as the value of output Q, this can't be observed until the clock is ticked. Which just makes it an RS flip flop which is controlled using a clock.
2) The role of the clock is to make sure that the input that the flip flop gets from the input one is directly opposite.
3) A limitation of RS Flip Flop is that it cant work if both the inputs are set to be the same, in a D Flip Flop this is resolved by using a clock that gives opposite inputs making it overcome the limitations of RS Flip Flop.

JK FLIP FLOP



J	K	Q (when clocked)	Q’ (when clocked)
0	0	No change	
1	0	1	0
0	1	0	1
1	0	Toggle	

1) To convert a JK flip flop to a D Flip Flop we need to drive its J and K inputs with a D Input using a NOT gate.

D INPUT	OUTPUT
0	0
0	1
1	0
1	1

2) By turning J and K inputs to 1.