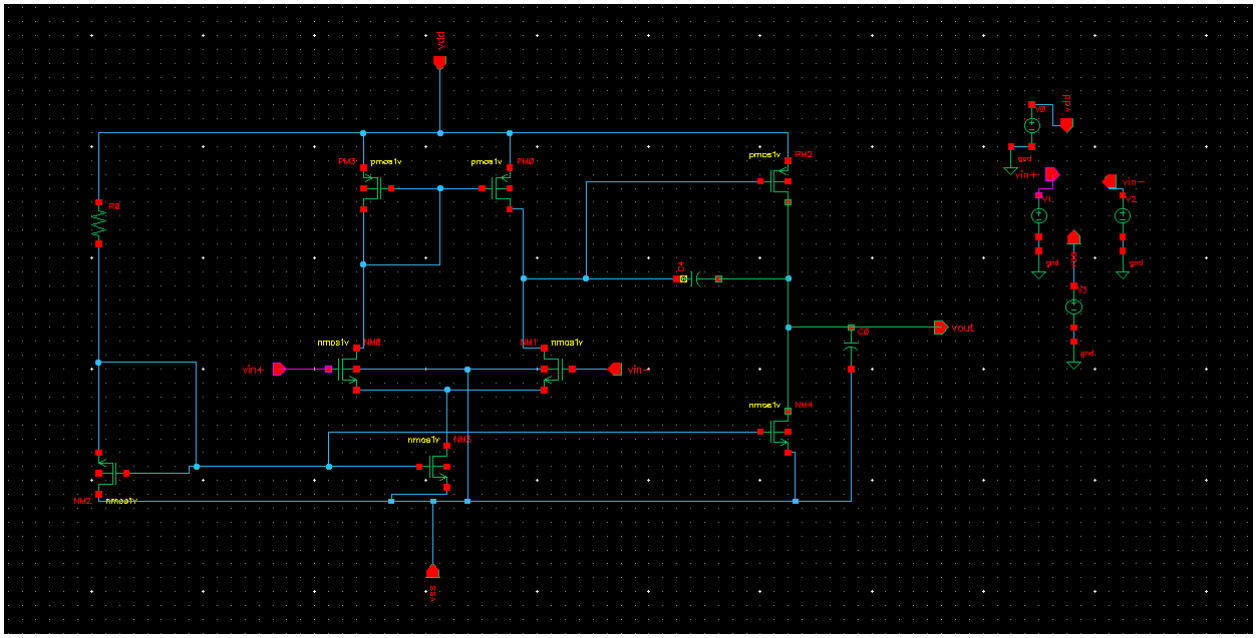


PMOS specifications:

Active Load Pair (PM3, PM0):

- **Width (W):** 6 µm
- **Length (L):** 500 nm

Second Stage Driver / Common Source (PM2):

- **Width (W):** 80 µm
- **Length (L):** 500 nm
- *Configuration: Implemented using 2 fingers of 40 µm each to bypass the 50 µm width limit*

NMOS Transistors (Qty: 5)

- **Differential Input Pair (NM0, NM1):**
  - **Width (W):** 3 µm
  - **Length (L):** 500 nm

Current Mirror & Biasing Network (NM2, NM3, NM4):

- Includes the Tail Current Source, Second Stage Load, and Diode-connected Bias transistor.
- **Width (W):** 20 µm
- **Length (L):** 500 nm

2. Passive Components

These are used for the compensation network (Miller Compensation).

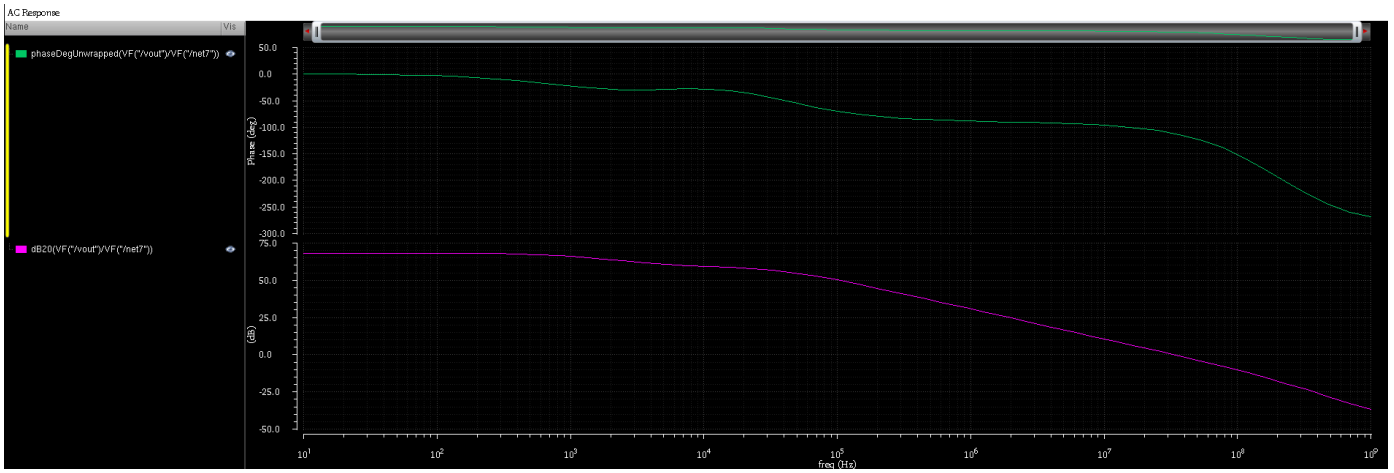
- **Resistor (Rz):** 40 kΩ (40 kilo-ohms)
- **Capacitor (Cc):** 2 pF (2 pico-farads)

3. Power Supply & Input Biasing

- **Supply Voltages:**
  - **VDD (Positive Supply):** 1.8 V DC
  - **VSS (Ground):** 0 V DC

Input Signals (Vin+ and Vin-):

- **AC Magnitude:** 1 V
- **AC Phase:** 0° for one input and 180° for the other to create a differential signal
- **DC Bias Voltage (Common Mode):**
  - *Initial:* 1.8 V (Resulted in poor gain).
  - *Optimized:* **800 mV (0.8 V)**.
  - Changing the DC input bias to 800 mV significantly improved the performance



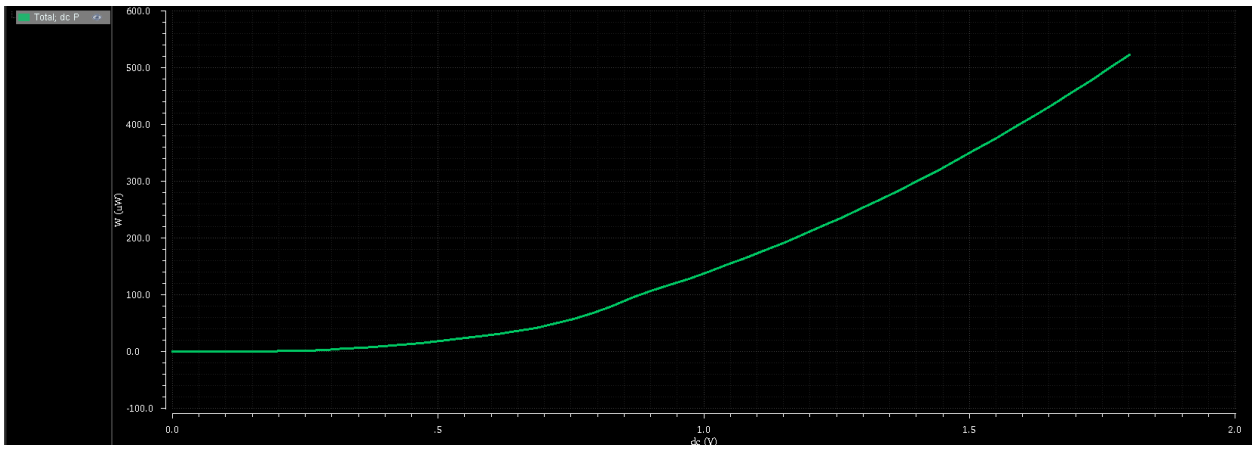
Calculated open loop AC gain and phase Margin using **AC ANALYSIS**

Gain - 67.9591 dB

Phase Margin - 68.2108 dB

Unity Gain Bandwidth - 34.1096 MHz

Bandwidth - 1.38528 KHz

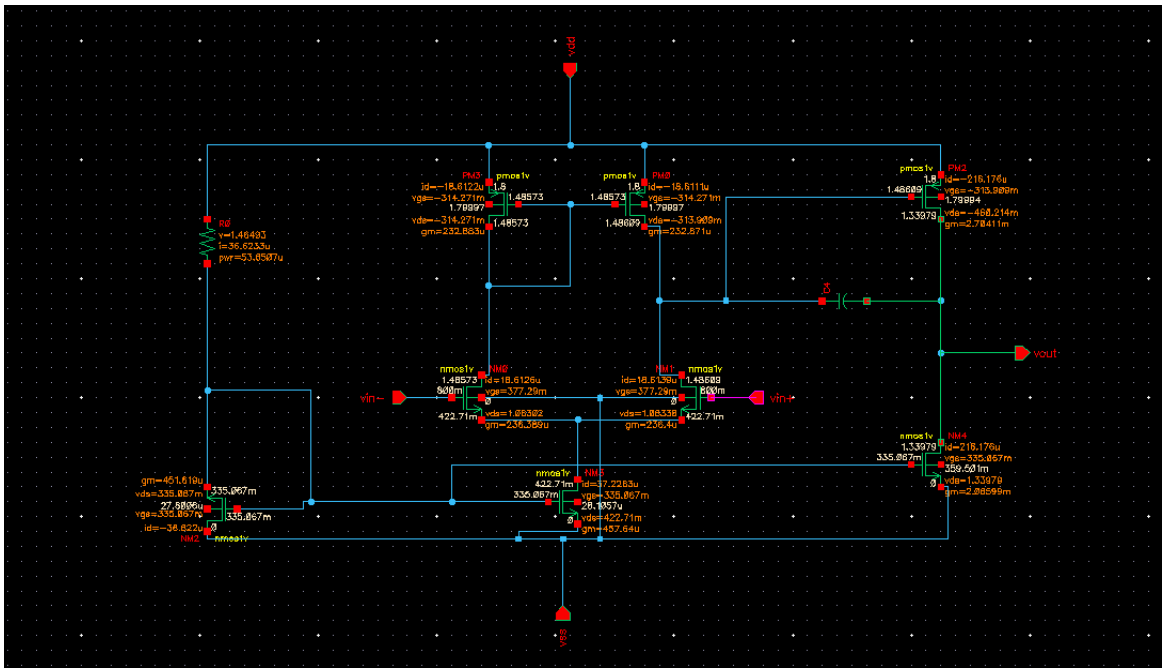


Total DC power v/s power supply variation

STATIC POWER - 522.045 uW (DC Power)

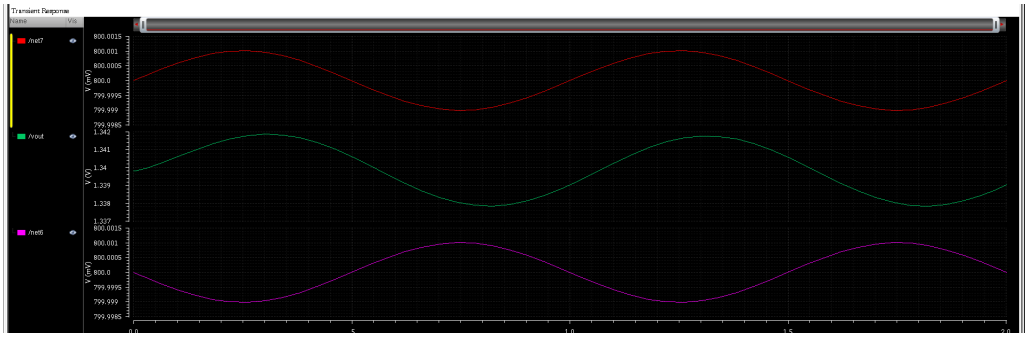
Avg POWER - 522.045 uW (from transient analysis)

DC OPERATING POINTS

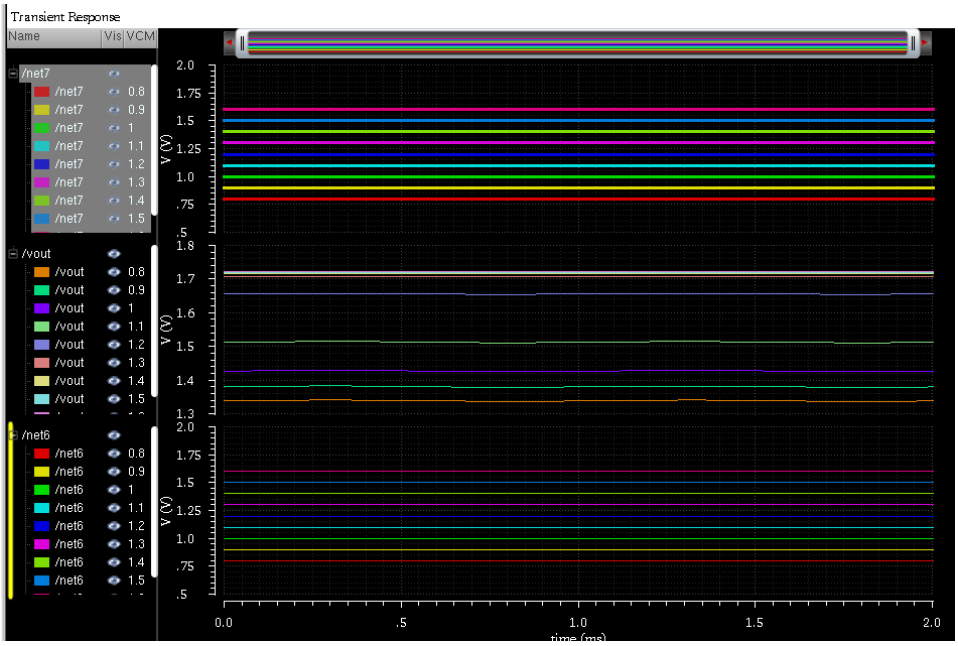


Verified that all transistors are in saturation region

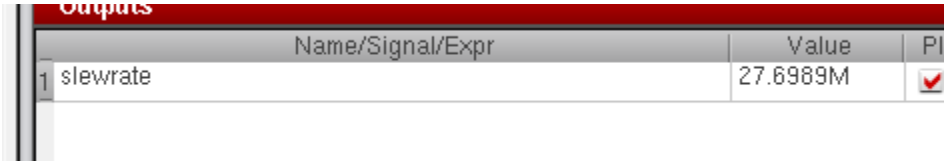
TRANSIENT RESPONSE



PARAMETRIC ANALYSIS (varying the VCM)

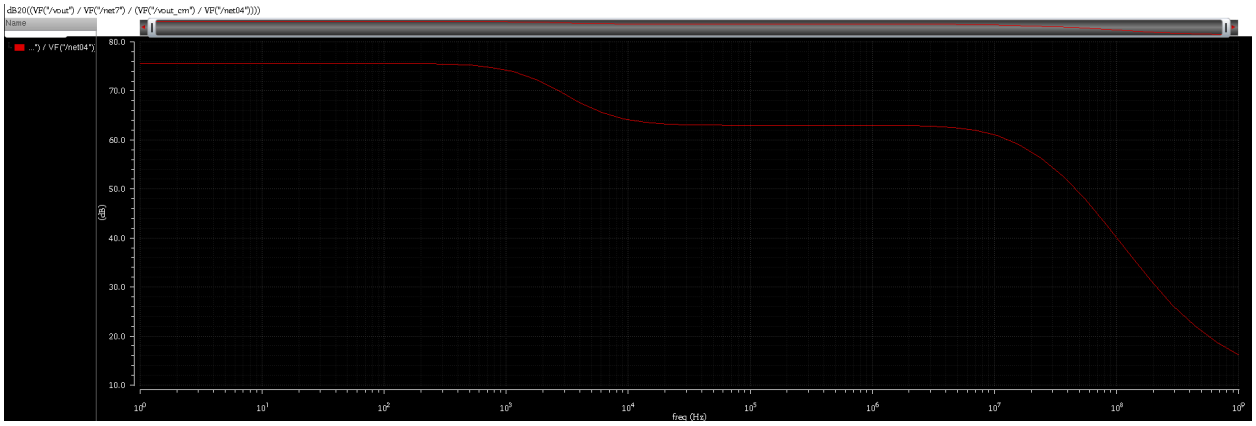


SLEW RATE CALCULATION :



Using vpulse instead of vsin

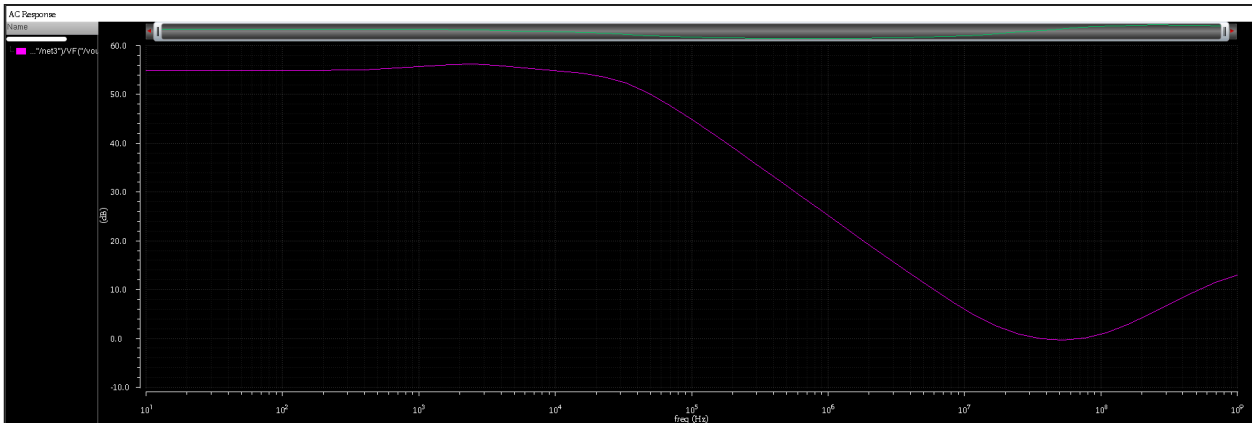
CMRR CALCUATION :



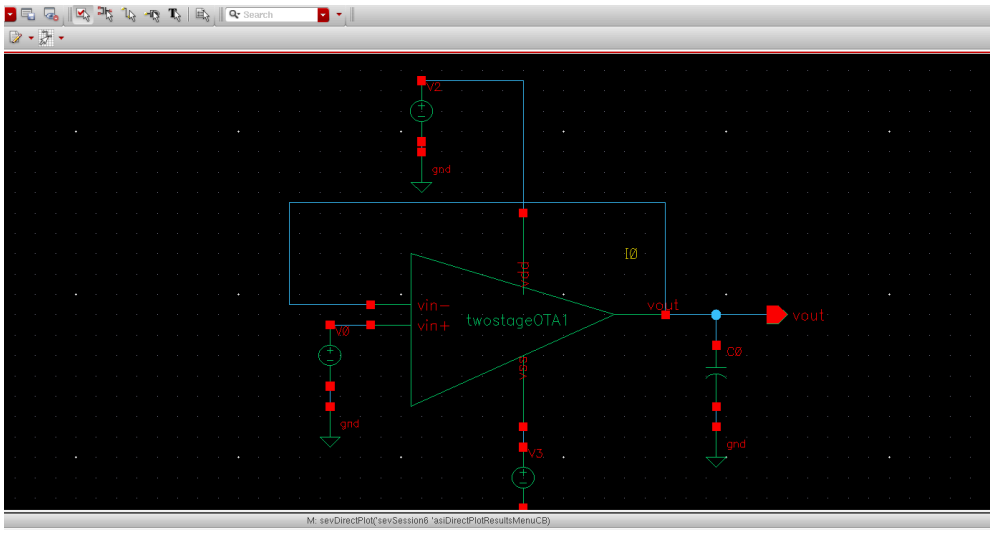
CMRR - 75.5611 dB

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	CMRR	75.5611	☑	☐	
2	dB20((VF("/vout") / VF("/net7") / (VF("/vout_...	wave	☑	☐	

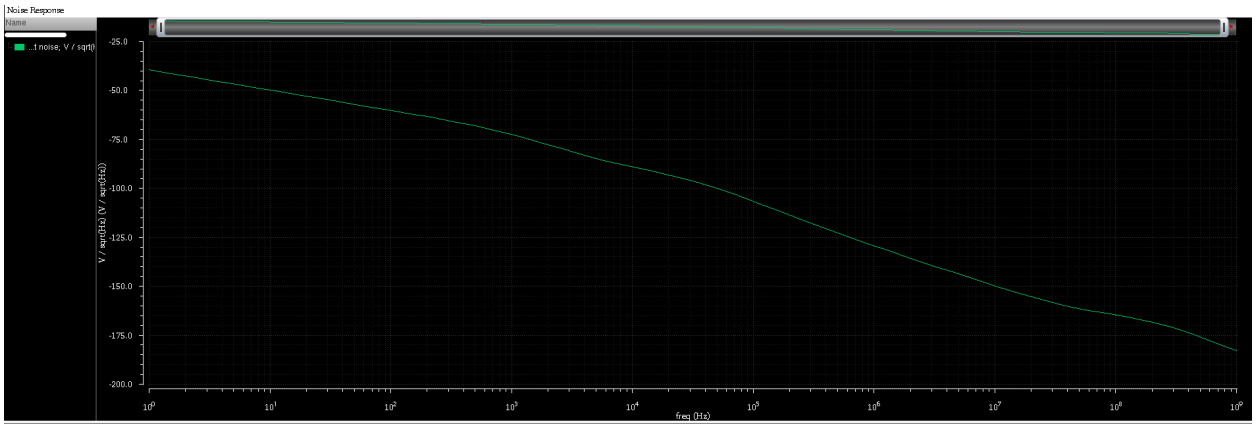
PSSR CALCULATION *(done using XF analysis)*



This is closed loop PSSR plotted using this circuit →



NOISE RESPONSE *(done using noise analysis)*



**********FIN**********