UART+GPIO FPGA Project

Revision: *1.0*

Date: *15 Oct 2020*

QuickLogic Corporation

1   Requirement:

2   Pinout:

Sl. No.	Signal Name	PAD Number	Direction	Description
UART				
1	UART_TX		Output	
2	UART_RX		Input	
GPIO				
1	GPIO_io[0]		I/O	
2	GPIO_io[0]		I/O	
3	GPIO_io[0]		I/O	
4	GPIO_io[0]		I/O	

3   FPGA Interrupts:

Sl. No.	FPGA Interrupts to M4	Interrupt Description
1	FB_INTERRUPT_0	Reserved
2	FB_INTERRUPT_1	Reserved
3	FB_INTERRUPT_2	UART 0 INTR
4	FB_INTERRUPT_3	Reserved

4 Address Map Specification

4.1 Memory Map

The EOS 3B system maps the FPGA IP into the address range of 0x40020000 to 0x4003FFFF. This address range provides 128K bytes of address range for FPGA based IP. The following tables further define the registers within this range.

Table 1-1: FPGA IP Register Space

Register	Block	Space Allocated	Remarks
0x40020000 – 0x400200FF	FPGA IP Registers	256 bytes	
0x40020100 – 0x40020FFF	Reserved		
0x40021000 – 0x400217FF	UART 0	512 Words	
0x400218FF – 0x40023FFF	Reserved		
0x40024000 – 0x400240FF	GPIO controller	64 Words	
0x40024100 – 0x4003FFFF	Reserved		

4.2 Register Address Table

The following sections will outline the expected allocation of registers and describe their operations.

4.2.1 FPGA Registers Address Table

Table 1-2 shows the expected allocation of FPGA Registers address space.

Table 1-2: FPGA IP Register Table

Register	Block	Reset Value	Remarks
0x40020000	IP Device ID	0xABCD0011	Read only
0x40020004	IP Revision number	0x0100	Read only Version
0x40020008 – 0x400200FF	Not Used	0x0	

4.2.2   UART 0 Register Map

UART 0 has a base address that starts at offset 0x1000 from the FPGA's base address (0x40020000 + 0x1000). The register map for the UART is described in a separate document, and can be found along with the RTL source code for the UART (currently in QuickLogic's s3-gateway repository on github, under ip_modules).

4.2.1   GPIO controller Register Map

The GPIO Controller has a base address that starts at offset 0x4000 from the FPGA's base address (0x40020000 + 0x4000). The register map for the GPIO Controller is described in a separate document, and can be found along with the RTL source code for the GPIO (currently in QuickLogic's s3-gateway repository on github, under ip_modules).

5 Revision History

Date	Revision	Author	Description
17 Sep 2020	1.00	Randy O	Initial Release
21 Sep 2020	1.01	Randy O	Removed the UART register map, since it's now described in a separate document. Updated QuickLogic's address.

6   Copyright and Trademark Information

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