Aaryan Dhawan

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Education/Affiliation

Virginia Tech, BS in Computer Engineering, Chip-Scale Integration — August 2020 - May 2024
Virginia Tech, M.Eng in Computer Engineering, VLSI and Design Automation — August 2024 - May 2026
Virginia Tech, Member of the BRICCS Research Group — Joined March 2025

- GPA: 3.7
- **Coursework:** Computer Architecture, VLSI circuit design, Digital/RTL design, Semiconductor manufacturing

Skills

C/C++ , Verilog/SystemVerilog, Python, MIPS/RISC-V Assembly, Xilinx Vivado ML, Intel Quartus Prime, Cadence Virtuoso

Projects

RISC-V Pipeline RTL Design and Verification — Fall 2025

- Designing a 5-stage pipeline for the RISC-V ISA, supporting most RV32I Base Integer Instructions using SystemVerilog
- Planning to use Cadence Genus and Innovus to generate Digital IC layout for Performance, Power, Area optimization, JasperGold suite for verification

Spiking Neural Network, Reservoir Computing Learning Engine RTL Design — June 2025 - Present

- Identified areas for optimization in State-of-the-Art RTL design for hardware learning engines
- Implemented resources reduction techniques to improve overall power consumption and increased system throughput
- Researching further extensions and applications of the learning engine design

Hardware Friendly Learning Rule for Spiking Neural Network — April 2025 - Present

- Researching highly performative neural network learning rules, optimized for binary classification
- Applying learning rules in a hardware efficient manner for local learning in a novel design for a Spiking neural network dealing with uni-variate data sets

Izhikevich Spiking Neural Network for FPGAs, — Spring 2025

- Used a hardware-efficient Izhikevich neuron model to create two Spiking Neural Networks for Character Recognition; Targeted fast inference performance and low resource utilization.

Improving Graph Algorithm Performance through CPU Design — Fall 2024

- Led a group in researching how to improve performance of graph algorithm based applications through changes in processor architecture through the UC-Berkeley Chipyard framework
- Targeted low-power, mobile based CPUs and SoC architectures; Achieved 2/3x Speed Up over industry-standard designs

VLSI Circuit Design Projects — Fall 2023

- Series of VLSI circuit design project using Cadence Virtuoso, revolving designing and testing integrated circuit schematics and layouts
- Ranging from basic logic gates to 16-bit Fast Adders and 12-bit Braun Multiplier layouts.

ReRAM Research Capstone Project — Fall 2023 - Spring 2024

- Led a senior level research group in understanding the thermodynamics and design of an experimental Resistive RAM chip. Assisted in model design in Ansys Workbench
- Develop Python based GUI to perform thermal analysis to validate experiments and visualize data