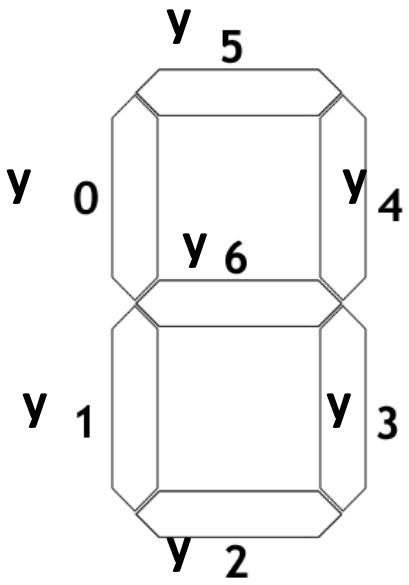
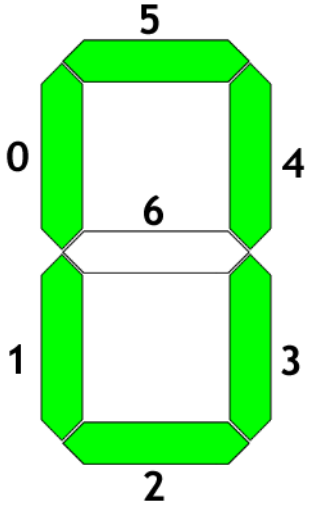
7-segment display logic synthesis

Codifica BCD dell'ingresso

	$x_3x_2x_1x_0$
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001



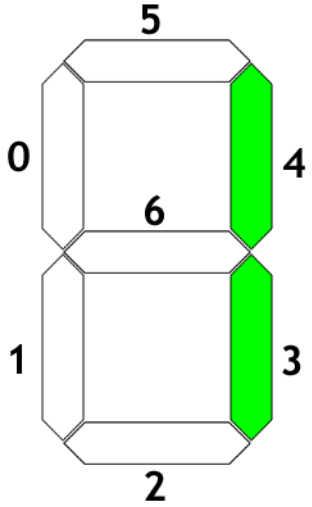
7-segment display logic synthesis



n=0

x=0000

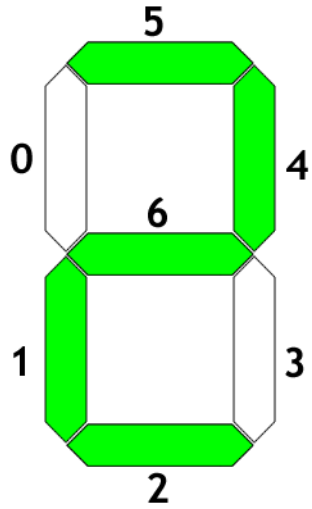
y=1111110



n=1

x=0001

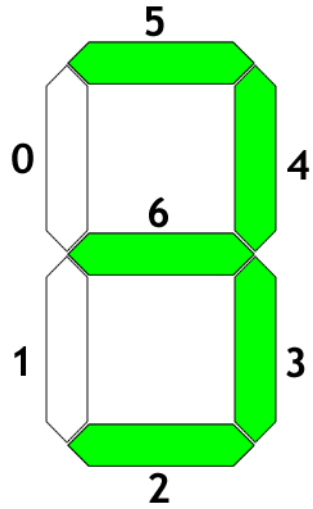
y=0001100



n=2

x=0010

y=0110111

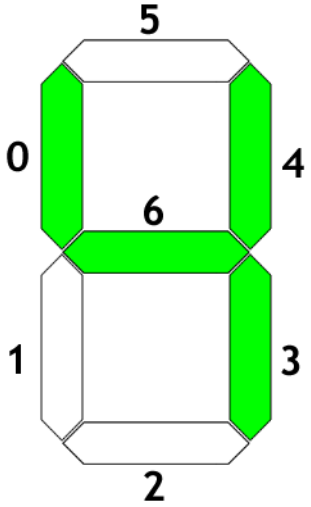


n=3

x=0011

y=0011111

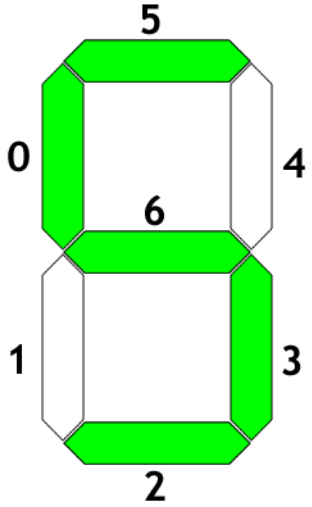
7-segment display logic synthesis



n=4

x=0100

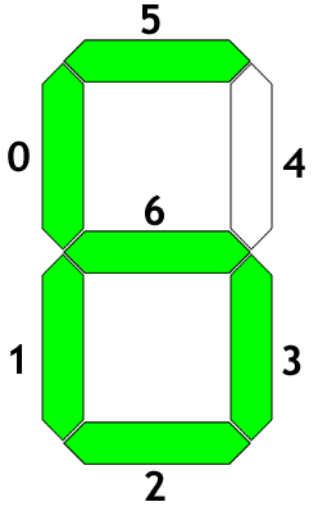
y=1001101



n=5

x=0101

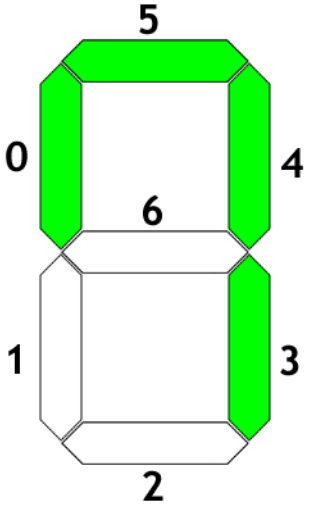
y=1011011



n=6

x=0110

y=1111011

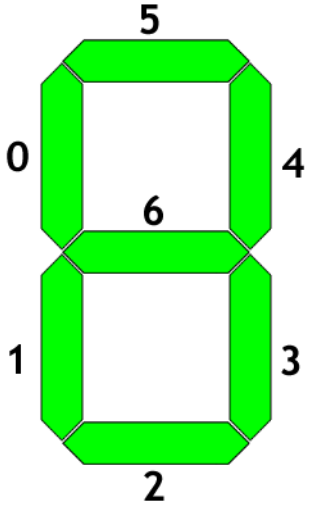


n=7

x=0111

y=1001110

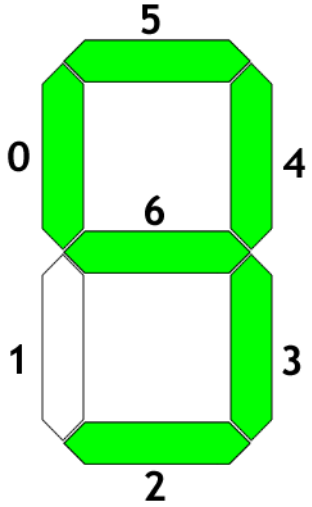
7-segment display logic synthesis



n=8

x=1000

y=1111111



n=9

x=1001

y=1011111

7-segment display logic synthesis

n	x_3	x_2	x_1	x_0	y_0	y_1	y_2	y_3	y_4	y_5	y_6
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	0	0	1	1	0	0
2	0	0	1	0	0	1	1	0	1	1	1
3	0	0	1	1	0	0	1	1	1	1	1
4	0	1	0	0	1	0	0	1	1	0	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	1	1	1	0	1	1
7	0	1	1	1	1	0	0	1	1	1	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	0	1	1	1	1	1

7-segment display logic synthesis

y_0

x_4x_3 \ x_2x_1	00	01	11	10
00	1			
01	1	1	1	1
11	-	-	-	-
10	1	1	-	-

$$y_0 = \overline{x_2}\,\overline{x_1} + x_3 + x_4$$