B.Sc. Engg. CSE 2nd Semester **10 February2022 (Morning)**

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION **SUMMER SEMESTER, 2020-2021**

DURATION: 1 Hour 30 Minutes **FULL MARKS: 75**

CSE 4205: Digital Logic Design

Answer **all 3 (three)** questions. Marks of each question and corresponding CO and PO are written in the right margin with brackets.

Write examination information on the **top page** and write **studentID** and **page number** in every page of the answer script. Submission pdf should be renamed as **studentID_CourseCode_MID.pdf**

The use of pencil is recommended to discourage any writing from being crossed

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1. a) According to the design procedure of combinational circuit, implement a circuit that will take a 4-bit binary number as input and its output will be the 2's complement of the input number. Design the circuit with **minimum number** of basic logic gates. 10 (CO5) (PO3)

   b) Implement the following Boolean function, ***F*** with the different **2-level forms** listed below: 10 (CO1) (PO1)

   $$F(x, y, z) = ((x \oplus y) + z)$$

   i. AND – NOR
   ii. OR – NAND
   iii. NAND – AND
   iv. NOR – OR

   Note: Assume that both the normal and complement inputs are available.

   c) Implement the Boolean function $\boldsymbol{F = abcd}$ using only two-input NAND gates. 5 (CO1) (PO1)

2. a) Simplify the following Boolean function, ***F*** into product of sums form by means of tabulation method stating the lists of all prime implicants and essential prime implicants: 10 (CO4) (PO2)

   $$F(a, b, c, d) = b'd + a'b + b'c' + a'c'd'$$

   b) Assume that we consider two decimal digits in BCD for arithmetic addition and subtraction, together with any carry from a previous stage. The decimal digits in the output must be expressed in BCD. Now design a block diagram that addresses the aforementioned scenario by incorporating the relevant function tables and simplification processes. 10 (CO5) (PO3)

   c) The adder-subtractor circuit designed in question 2(c) has a mode input ***M*** to control their operations and data inputs ***A*** and ***B.*** If ***M***, ***A*** and ***B*** have the following values, determine the values of the ***sum*** outputs and the ***carry***: 5 (CO1) (PO1)

	M	***A***	***B***
i.	0	0111	0110
ii.	0	1000	1001
iii.	1	0111	1000
iv.	1	0101	0111
v.	1	0000	0001

3. a) Consider the following Boolean function ***F***, together with the don't-care conditions ***d***. Implement the simplified function using: 10 (CO4) (PO3)
   i. 2 level NAND gates
   ii. 2 level NOR gates

$$F\ (A, B, C, D) = ABC + A'B'CD' + A'BC'D$$
$$d = B'D + A'BD' + AB'D'$$

Note: Assume that both the normal and complement inputs are available.

b) A limited number system of base 12 is adopted at Central Departmental Shop (CDS) in IUT to count beverage cans. They will allow at most four integer digits in their numbers. The weights of the digits in their significant positions are 12^3, 12^2, 12, and 1. Special names are given to the weights as follows: 12 =1 dozen, 12^2=1 gross, and 12^3=1 great gross. Answer the followings: 6 (CO1) (PO1)
   i. $(6\ great\ gross + 8\ gross + 7\ dozen + 4)\ +\ (1\ gross\ + 7\ dozen\ + 9)\ = ?$
   ii. Find the representation in base 12 (adopted by CDS, IUT) for 7569_{10} beverage cans.

c) What is self-complementary code? What are the advantages of these codes over Binary Coded Decimals? Justify your answer with proper examples. 4 (CO3) (PO2)

d) Design a combinational circuit of a four-bit Gray code to binary number converter with exclusive-OR gates 5 (CO1) (PO1)