B. Engg. / HD CSE 2nd Semester

31 October 2017

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION — SUMMER SEMESTER, 2016-2017

DURATION: 3 Hours — FULL MARKS: 150

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **8 (eight)** questions. Answer any **6 (six)** of them.

Figures in the right margin indicate marks.

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1. Sensors are used to monitor the pressure and the temperature of a chemical solution stored in a vat. The circuitry for each sensor produces a HIGH voltage when a specified maximum value is exceeded. An alarm requiring a LOW voltage input must be activated when either the pressure or the temperature is excessive. Design a circuit for this application. 5

   i. Find the complement of $F = x + yz$; then show that $F.F' = 0$ and $F + F' = 1$. 10

   ii. Show that the dual of the exclusive-OR is equal to its complement.

2. Design a combinational circuit that converts a decimal digit from 2,4,2,1 code to 8,4,-2,-1 code. 10

3. Use a Karnaugh map to simplify the following expression to minimum form as directed: 12

   i. $F(W,X,Y,Z) = (X+Y')(W+Z')(X'+Y'+Z')(W+X+Y+Z)$ *(To minimum SOP form)*

   ii. $F(A,B,C,D) = A'B' + AB'+C'D'+CD'$ *(To minimum POS form)*

4. A majority function is a combinational circuit which generates output 1 when the input variables have more 1s than 0s and 0 otherwise. Based on this argument design a 3-input majority function. 8

5. Show that $A \odot B \odot C \odot D = \sum (0, 3, 5, 6, 9, 10, 12, 15)$. 5

6. In number system, complements play a vital role in subtraction. There are two different methods of complement - r's and (r-1)'s complements. What are the basic reasons behind using two different types of complements in number system? 5

7. An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, and g) select the corresponding segments in the display, as shown in Fig. 1(a). The numeric display chosen to represent the decimal digit is shown in Fig. 1(b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display. 20

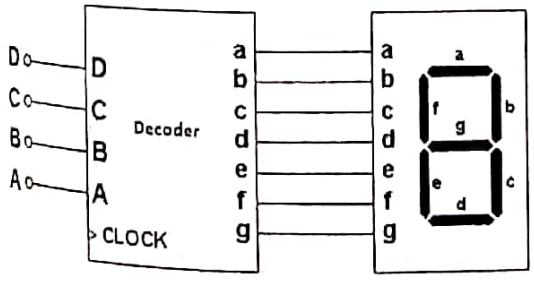

Figure 1(a): Segment Designation.

Figure 1(b): Numerical designation for display.

8. a) What are the differences between a synchronous counter and an asynchronous counter? 7

   b) In sequential circuit, "Race around condition" creates a problem generating unstable output. Explain how it is generated in sequential circuit but not in combinational circuit with appropriate timing diagram. Describe possible remedies to fix this problem with appropriate examples and figures. 8

c) How can a universal shift register can be developed from a bidirectional shift register? Draw a figure of a 4 bits universal shift register where register operation will be selected according to the following table (Table 1).

Table 1: Register option table for question 4(c)

Mode Variables		Register Operation
S_1	S_0	
0	0	Parallel Loading
0	1	Shift Left
1	0	Shift Right
1	1	No Change

5. a) Write down the truth table of a D flip-flop. From the table prove that $Q_{(t+1)} = D$. Where D is the present input and $Q_{(t+1)}$ is the next state of the output.

b) Consider an analog clock as Fig. 2(a) and corresponding binary analog clock which is also presented in Fig. 2(b). In this binary analog clock, you can count from 0001(Binary of 1_{10}) to 1100(Binary of 12_{10}). Now you have to draw an asynchronous counter circuitry considering this binary analog clock.

*[**Hints:** An asynchronous counter starts counting from its highest or lowest possible state. For 4 bits asynchronous counter, lowest and highest states are 0000 and 1111 respectively. But both of these states are absent for this scenario. So initially you can start your count from 0000 state but it won't be repeated anymore.]*

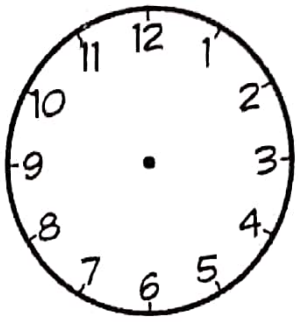

Figure 2(a): Analog Clock.

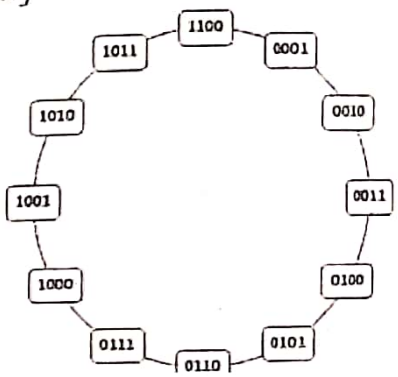

Figure 2(b): Binary Analog Clock.

c) Discuss relative comparison among R-S flip flop, J-K flip flop and Master-Slave flip flop with the help of appropriate diagrams and truth tables.

6. a) "The ROM is used to implement a complex combinational circuit in one IC package."- based on this statement discuss its internal configuration and how it is used as memory device.

b) How is the 4-to-2 encoder different from a 4-to-1 multiplexer? Draw the truth tables for following combinational circuits:

i. 16-to-4 priority encoder.
ii. 16-to-1 multiplexer.

c) Derive the state diagram from the following state table (Table 2).

Table 2: State table for question 6(c)

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

Reduce the number of the states in the state table and tabulate the reduced state table. Also show the reduced state diagram.

starting from state 'd' of the given state table, find the output sequence (different states) generated with an input sequence 0 1 1 1 0 0 1 0 0 1 1. Do the same for the reduced state table state diagram and show that the output sequence is the same for the both cases for a same input sequence.

To build a ripple counter toggle (T) flip flop is normally used. In a Digital Logic Design experimental experiment you are asked to implement a 4 bit ripple up-down counter but there is a scarcity of T flip flop in laboratory. Only you can use D flip flop as they are available at that moment. You know the conversion between different flip flops. Now how can you implement T flip flop using only D flip flop? 8

For an output cycle of 10 clock pulses, draw the 3 outputs Q_0, Q_1 and Q_2 of the ripple counter on the grid in Fig. 3. State which output is the MSB and which is the LSB. Assume that you start in the all-zeros state (000) as shown below. Assume the J-K flip-flops are rising-edge-triggered. 7

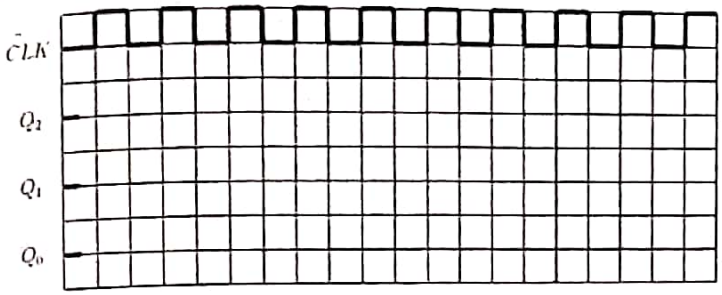

Figure 3: Timing Diagram.

A full subtractor is a combinational circuit that can take three bits as input and produce two bits as output. Now implement a full subtractor circuitry using convenient multiplexer. 10

In Fig. 4 a Pattern Detection Machine is demonstrated which recognizes the sequence "0110". This pattern detection machine is nothing but a finite state machine that represents a sequential circuit. It produces output *found = 1* when the sequence is occurred otherwise *found = 0*. Based on this scenario answer the following questions: 20

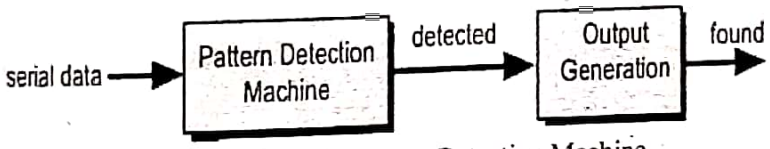

Figure 4: Pattern Detection Machine.

i. Draw and label the transitions in the state diagram where states are **START**, **GOT0**, **GOT01**, **GOT011**, and **GOT0110**.
ii. Write the state table from the state diagram.
iii. Using J-K flip flop build a pattern detector circuit which can detect the sequence "0110" following *Design procedure*.
iv. For the following input bit stream, generate the output bit stream considering '*overlapping*' condition:
Input bit stream = 00111001101101010 5

What is the purpose of power-on **LOAD** input in register?

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B.Sc. Engg. / HD CSE 2nd Semester 27 October 2018

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION **SUMMER SEMESTER, 2017-2018**

DURATION: 3 Hours **FULL MARKS: 150**

CSE 4205: Digital Logic Design

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1. a) Show that the dual of the exclusive-OR is equal to its complement. 5

   b) Find the value of x for the following equations: 10

   i. x = 9's complement of $(453)_{10}$

   ii. $(110101.101)_2 = (x)_4$

   iii. x = BCD of 8620

   iv. x = Excess-3 code of 37

   c) Define following terms (Draw diagram if necessary): 10

   i. Demultiplexer

   ii. Encoder

   iii. Pulse and Edge Trigger

   iv. Race Condition

2. a) Suppose, input to a combinational circuit is a 4 bit binary number. Design a circuit with minimum gates for the following: 15

   i. Output, P = 1, if the number is prime

   ii. Output, Q = 1, if the number is divisible by 3

   b) Obtain the simplified Boolean expressions for output *F* and *G* in terms of the input variables in the circuit of Figure below and construct their truth table. 10

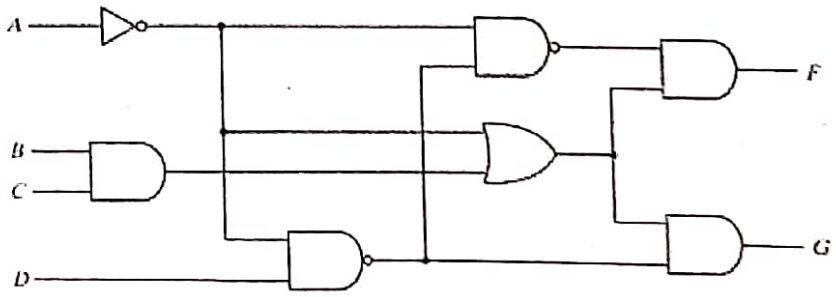

Figure 1: A combinational Circuit.

3. a) Design a combinational circuit that generates the 9's complement of a BCD digit. 10

   b) Show that the characteristic equation for the complement output of a *JK* flip-flop is $Q(t+1) = J'Q' + KQ$. 8

   c) Explain the differences among a truth table, a state table, a characteristic table, and an excitation table. Also, write the differences among a Boolean equation, a state equation, a characteristic equation, and a flip-flop input equation. 7

4. a) What is Master-Slave flip-flop? Explain with block diagram and logic diagram. 5
   b) Design the conversion of JK flip flop into D flip flop and T flip flop. 10
   c) Design a 5 bit parity generator and parity checker with their corresponding equations. 10

5. a) Design a BCD to Seven segment display circuit using decoder. 10
   b) A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations. 15

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

   i. Draw the logic diagram of the circuit.
   ii. List the state table for the sequential circuit.
   iii. Draw the corresponding state diagram.

6. a) Design a modulo-16 counter, using JK flip flop with the following sequence:
   7,6,5,4,3,2,1,0,8,9,10,11,12,13,14,15,7,6,5,... 20
   b) What is the maximum propagation delay from clock to output for the counter of the Question 6.(a)? Explain your answer assuming necessary variables. 5

7. a) What is the difference between serial and parallel transfer? What type of register is used in each case? 5
   b) Draw the logic diagram of a four-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs S_1 and S_0. The register operates according to the following function table (Table 1). 10

Table 1: Selection modes

S_1	S_0	Register Operation
0	0	No change
1	0	Complement the four outputs
0	1	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

   c) Write down the necessary equation accomplished by a 4 bit binary adder. Design that 4 bit magnitude comparator following those equations. 10

8. a) The content of a 4 bit shift register is initially 1101. The register is shifted six times to the right, with the serial input being 101101. What is the content of the register after each shift? 5
   b) Construct a binary counter that counts from 0 through binary 127. 10
   c) What is carry propagation delay of Binary Parallel Adder? How it can be reduced? Explain with necessary equation and figure. 10

. Engg. / HD CSE 2nd Semester (64)

25 October 2016

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MESTER FINAL EXAMINATION — SUMMER SEMESTER, 2015-2016

RATION: 3 Hours — FULL MARKS: 150

CSE 4205: Digital Logic Design

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) Describe the operation of a 3-bit up-down ripple counter using J-K flip-flop with relevant diagram. 7

) Explain the operation of a 4 bit bidirectional shift register using D flip-flop and provide necessary figure. 10

) Distinguish between PLA and PAL. Design disjoined PLA and PAL for the Boolean functions given below: 8

$X(a,b,c) = \sum (2,3,5,7)$

$Y(a,b,c) = \sum (0,1,5)$

$Z(a,b,c) = \sum (0,2,3,5)$

a) Find the value of **x** for the following equations: 5

i. $(13442)_7 = (321020)\mathbf{x}$

ii. $(110101)_2 = (\mathbf{x})_{\text{Gary code}}$

b) Describe the operation of a clocked S-R flip-flop with appropriate truth table, characteristic table, excitation table, characteristic equation and graphic symbol. How can a clocked S-R flip-flop can be converted into a clocked D flip-flop? 10

c) Design an asynchronous BCD counter and explain its operation. Mention a different type of name for this counter. 10

a) Draw the following combinational logic circuit with appropriate truth table: 10

i. Octal-to-binary encoder

ii. Binary-to-octal decoder

b) Derive the state diagram from the following state table given in Table 1. Reduce the number of the states in the state table and tabulate the reduced state table. Also show the reduced state diagram. 10

Table 1: State table for Question 3(b)

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

Starting from state '*d*' of the given state table, find the output sequence generated with an input sequence 0 1 1 1 0 0 1 0 0 1 1. Do the same for the reduced state table/state diagram and show that the output sequence is the same for the both cases for a same input sequence.

c) Write down the truth table of a T flip-flop. From the table prove that $Q_{(t+1)} = \overline{Q_{(t)}}$. Where $Q_{(t)}$ is the present state and $Q_{(t+1)}$ is the next state of the output.

4. a) How can a full adder be implemented with the help of half adder? Draw necessary diagram.
   b) Explain 'Race around' condition with appropriate timing diagram. Describe possible remedies with appropriate examples.
   c) Explain how a 2-bit gray code counter can be developed with J-K flip-flop with necessary diagram.

5. a) Design a 16:1 multiplexer with the help of 4:1 multiplexer.
   b) What are the differences between a synchronous and an asynchronous counter?
   c) How can register store data with the help of flip-flop which store only a single bit? Explain with necessary diagram.

6. a) "NAND and NOR gates can be defined as universal gate"- Explain. Design all basic logic gates using NAND and NOR gates.
   b) How can a universal shift register can be developed from a bidirectional shift register? Draw a figure of a universal shift register.
   c) What do you mean by preset and clear input in the flip-flop? Use J-K flip-flop to describe their operations with necessary diagram and truth table.

7. a) Obtain the simplified expressions in i. POS and ii. SOP form for the Boolean function: $F(w,x,y,z) = \prod(0,1,2,4,5,7,11,15)$
   b) Develop the state table containing the present state, next state, input and output for the state diagram given below. Also find out the state equations for this state diagram.

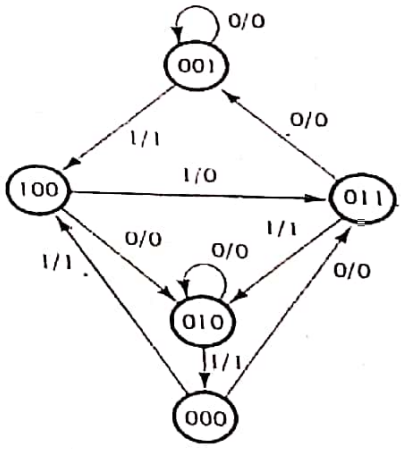

Figure 1: State diagram for Question 7(b)

   c) "Flip-flop can be used to develop a counter"- Explain with necessary timing diagram.

8. a) Distinguish between edge triggering and pulse duration/level triggering. Explain how a step signal can be converted to an impulse signal using necessary circuit diagram.
   b) Convert the D flip-flop to the T flip-flop following necessary steps.
   c) Compare among R-S, J-K and master-slave J-K flip-flops with necessary diagram.