B.Sc. Engg.(EE)/ BDEE, 3rd Sem. 74 Date: March 14, 2017 (Tue)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination
Course No.: Math 4301
Course Title: Mathematics III

Winter Semester, A.Y. 2015-2016
Time: 90 Minutes
Full Marks: 75

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper.

1. a) Examine the validity of $\underline{a}\times(\underline{b}\times\underline{c})=(\underline{a}.\underline{c})\underline{b}-(\underline{a}.\underline{b})\underline{c}$ when $\underline{a}=(1,1,1)$, $\underline{b}=(2,-1,3)$, $\underline{c}=(1,-1,0)$. 10

   b) Examine whether $\underline{F}=e^x\sin(yz)\underline{i}+ze^x\cos(yz)\underline{j}+ye^x\cos(yz)\underline{k}$ is irrotational. If so find a scalar function $\phi(x, y, z)$ at $\left(0, 2, \frac{\pi}{6}\right)$ such that $\underline{F}=\nabla\phi$. 10

   c) Show that $\underline{a}.\left(\nabla\frac{1}{r}\right)=-\frac{\underline{a}.\underline{r}}{r^3}$. 5

2. a) Establish the formula for $L\{e^{kt}\sinh\mu t\}$, $L\{t^n e^{at}\}$ and also find $L^{-1}\left\{\frac{s+4}{s^2+6s+25}\right\}$. 3×5=15

   b) Solve for $Y(t)$ given that $Y''(t)-Y'(t)=F(t)$. 10

3. a) Use convolution theorem to find the solution of the integro-differential equation $Y(t)=i+\frac{1}{2}\int_0^t(t-u)^2Y(u)du$. 15

   b) Define the following: Error function, sine and cosine integral functions. Find $L^{-1}\left\{\frac{1}{s}\frac{1}{\sqrt{s+1}}\right\}$. 10

4. a) Use Laplace transform to evaluate (i) $\int_{-\infty}^{\infty}\frac{x\sin tx}{(x^2+a^2)}dx$ (ii) $\int_0^{\infty}\cos x^2dx$. 10+5=15

   b) An inductor of 2 henrys, a resistor of 16 ohms and a capacitor of 0.02 farads are connected in series with an e.m.f. of E volts. At $t=0$, the charge on the capacitor and current in the circuit are zero. Find the charge and current at any time $t>0$ if $E=100\sin 3t$. 10

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B.Sc. Engg. (EE/BDcE, 3rd Sem.) Date: March 10, 2016 (AN)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination
Course No.: EEE 4303
Course Title: Electronics II

Winter Semester, A.Y. 2015-2016
Time: 90 Minutes
Full Marks: 75

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Programmable calculators are not allowed. Do not write on this question paper.

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1. a) Draw an op amp circuit that will take three inputs and will give as output the average of the three inputs. Deduce the output expression.

   b) Draw an op amp integrator circuit and explain how it works.

2. a) What is common mode rejection in op amp? What is common mode rejection ratio (CMRR)? What value of CMRR is preferable, higher or lower value?

   b) Draw the circuit diagram of a unity-gain op amp amplifier. Why should we need such an amplifier?

3. a) List three advantages of FET over BJT. What are the different types of JFET available? With the sketch of construction of any one type, explain how JFET works.

   b) What is pinch-off voltage of FET? What is g_m of FET? How are they related to each other?

4. a) What are the significant differences between the construction of an enhancement type MOSFET and depletion type MOSFET? Discuss the operation of an enhancement type MOSFET.

   b) Design a self-bias FET amplifier to have a gain of 10. Use the following data to design: $V_{DD} = 20$ V, $V_{GSQ} = V_P/3$, $I_{DSS} = 12$ mA, $V_P = -3$ V, $y_{fs} = 25$ mS.

B.Sc. Engg. (EE)/ HDEE, 3rd Sem. Date: March 08, 2016 (Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination
Course No.: EEE 4305
Course Title: Electrical Machines I

Winter Semester, A. Y. 2015-2016
Time: 90 Minutes
Full Marks: 75

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper. Symbols carry their usual meanings.

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1. a) With neat diagram, explain in detail the principle of E.M.F. induction in a single loop generator. [15]

   b) Derive the equation of generated E.M.F. of DC generator. [05]

   c) Show that, the DC generator exhibits maximum efficiency when constant losses are equal to variable loss. [05]

2. a) Explain with neat diagram, the principle of current reversal in every armature conductor along the magnetic neutral axis. [14]

   b) Derive the formula for cross-magnetizing and demagnetizing AT/pole. [3+3]

   c) How to achieve the internal characteristics of a DC shunt generator? Use diagram to illustrate your answer. [05]

3. a) Explain in brief the motor principle with suitable diagram. Define back E.M.F. and mention its importance in motor operation. [5+3]

   b) Derive the terminal characteristics of DC shunt motor. Explain the flux control method of the DC shunt motor. [3+9]

   c) Derive the equation of the induced emf of the DC motor. [05]

4. a) A 22.38 kW, 440 V, 4-pole wave-wound DC shunt motor has 840 armature conductors and 140 commutator segments. Its full-load efficiency is 88% and the shunt field current is 1.8 A. If the brushes are shifted backward through 1.5 segments from the geometrical neutral axis, then find the demagnetizing and distorting AT/pole? [9]

   b) Graphically show the procedure to calculate the critical resistance and critical speed of a DC shunt generator. [3+3]

   c) A 4-pole, 240 V wave connected shunt motor gives 11.19 kW when running at 1000 rpm and drawing armature and field currents of 50 A and 1 A respectively. It has 540 conductors. Armature resistance is 0.1 Ω. Assuming a drop of 1 V per brush, find: [10]

      i. Total torque,
      ii. Useful torque,
      iii. Useful flux/pole,
      iv. Rotational losses and
      v. Efficiency.

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B.Sc. Engg. (EE)/HDEE, 3rd Sem. Date: March 11, 2016 (Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination | Winter Semester, A. Y. 2015-2016
Course No.: EEE 4307 | Time: 90 Minutes
Course Title: Digital Electronics | Full Marks: 100

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper.

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1. a) The Maya number system is a vigesimal (base-twenty) positional numeral system used by the pre-Columbian Maya civilization. The numerals of Maya number system is shown in Figure 1. 14

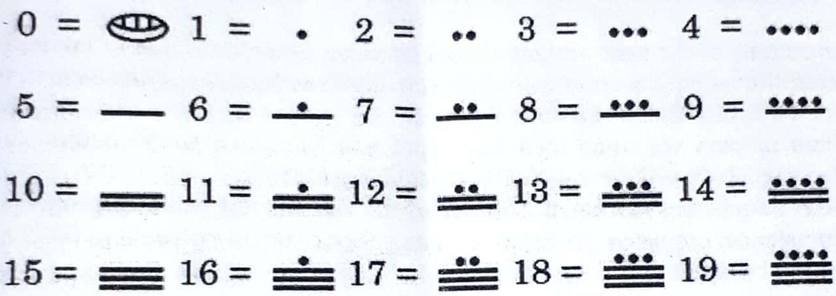

Figure 1.

Find the value of X.

(i)  $)_{Maya\ 20\ base} = (X)_8$

(ii) $(2C6B.F2)_{16} = (X)_{Maya\ 20\ base}$

b) The (r-1)'s complement of base-6 numbers is called the 5's complement.

(i) Obtain 5's complement of $(543210)_6$ 4

(ii) Perform subtraction operation $(543210)_6 - (553210)_6$ by taking (r-1)'s complement of the subtrahend. $6\frac{1}{3}$

c) Reduce the following Boolean expressions to the indicated number of literals: 9

(i) $\bar{A}\bar{C}+ABC+A\bar{C}$, to three literals

(ii) $\bar{A}B(\bar{D}+\bar{C}D)+B(A+\bar{A}CD)$, to one literal

(iii) $(\bar{A}+C)(\bar{A}+\bar{C})(A+B+\bar{C}D)$, to four literals

2. a) Design a two digit Octal adder. The adder will take two Binary Codded Octal (BCO) numbers, $A = A_2A_1A_0$ and $B = B_2B_1B_0$, and the reults are to be shown in BCO form. 20
(Hint: The BCO form of Octal number 14 is 001 100)

b) Simplify the following Boolean functions using Karnaugh-Map in (i) POS and (ii) SOP form. $13\frac{1}{3}$

(i) $F(A, B, C, D, E) = \sum(0, 1, 4, 5, 16, 17, 21, 25, 29)$

(ii) $F(w, x, y, z) = \Pi(1, 3, 5, 7, 13, 15)$

3. a) Construct the truth table for a 4 to 2 input priority encoder with input priorities D_1, D_2, D_0, and D_3 where, D_1 has the highest priority and D_3 has the lowest. The output binaries are denoted as y_0 and y_1. 10

b) Construct a 4 × 16 decoder with two 3 × 8 decoders with enable. 8 1/3

c) Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers. Implement a full adder with two 4 × 1 multiplexers. Show the internal diagram of 8 × 1 multiplexer only. Use block diagrams for the other multiplexers. 15

4. A combinational circuit with four input bits that represent a decimal digit in BCD gives four output bits that produce the 9's complement (in BCD) of the input digit. 33 1/3

(i) Design the combinational circuit with the most simplified Boolean functions.
(ii) Design the combinational circuit with 4× 16 Decoder.

The outputs of the both designs should be same. Sometimes due to internal damage of the circuit, the output becomes incorrect. The ouputs of (i) and (ii) can be sent through another Error Detecting Block shown in Figure 2.
If both outputs are equal then the output will be shown at the output side of the Error Detecting Block and the value of E should be equal to 0.
If both outputs are not equal then one of the ciruit is not working properly. So under this circumstance, output of the Error Detecting Block should be equal to 0000 and the value of E should be equal to 1.

(iii) Design the combinational logic of Error Detecting Block.

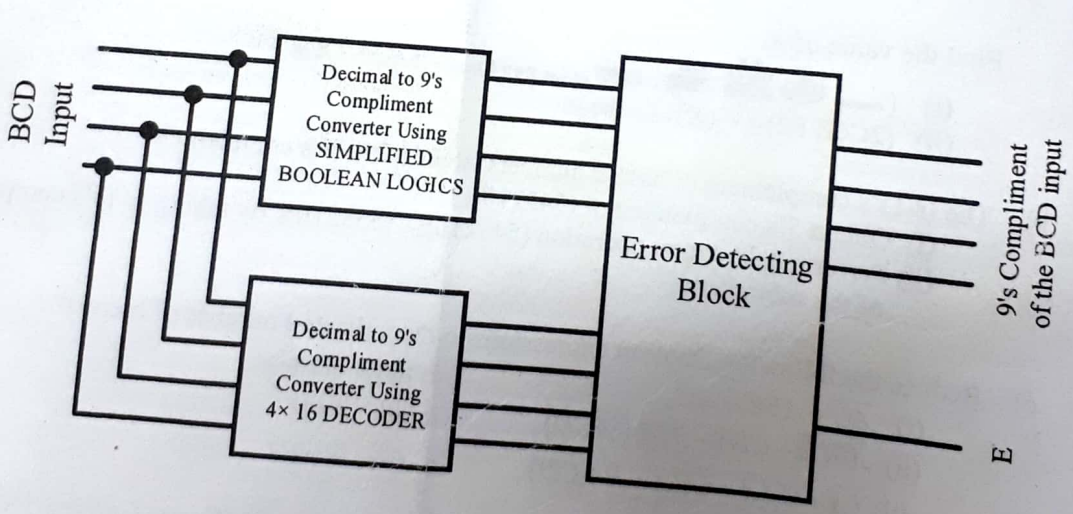

Figure 2.