B.Sc. Engg. (EE) 2nd Semester 73 Date: October 30, 2018 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

**DEPARTMENT OF ELECTRICAL & ELECTRONIC ENGINEERING**

Semester Final Examination
Course No.: EEE 4203
Course Title: Electronics I

Summer Semester, A.Y. 2017-2018
Time: 3 Hours
Full Marks: 150

There are 8(Eight) questions. Answer **any 6 (Six)** questions. Programmable calculators are not allowed. Figures in the margin indicate marks of the part questions. Do not write on this question paper. Assume reasonable value for any missing data.

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1(a) Find $V_o$ and I for the circuit shown in the Fig. 1(a). $v_I$ is a 1 kHz, 10 V peak sine wave, sketch the wave form resulting at $v_o$. What are its positive and negative peak values? Diodes are ideal. [09]

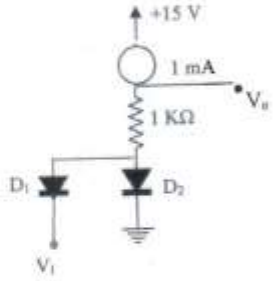


Fig. 1(a)

(b) For the circuit of Fig. 1(b), a string of three diodes are used to provide a constant voltage of about 2.1 V. Calculate percentage of change in this regulated voltage caused by [10]

(i) ±10% change in power-supply
(ii) connection of $R_L = 500\ \Omega$ load resistance. Assume n = 2.

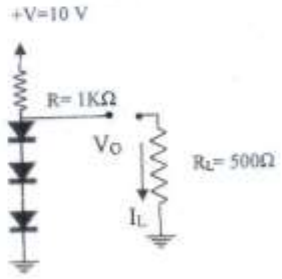


Fig. 1(b)

(c) Draw the circuit diagram of an AND gate using ideal diodes and describe how AND logic operation is performed in the circuit. 06

2.(a) Find the output wave-shapes for the following (Fig. 2(a)) clippers (diodes are ideal): [12]

(i) (ii)

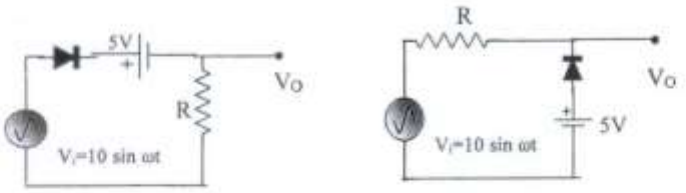


Fig. 2(a)

(b) Find the output wave-shapes for the following clampers (diodes are ideal) in Fig. 2(b): [13]

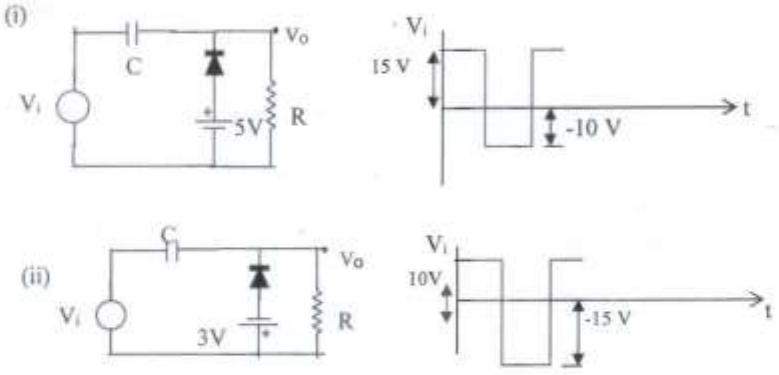


Fig. 2(b)

3.(a) Using the fact that a silicon diode has $I_S = 10^{-14}$ A at 25 °C and $I_S$ increases by 15% per °C rise in temperature, find the value of $I_S$ at 125 °C. [5]

(b) Using the diode equation in forward biasing region, find the expression of small signal resistance of a diode. What is the significance of this reisitance if the diode is used as a voltage regulator? [10]

(c) Determine the range of $R_L$ and $I_L$ that will result in load voltage being maintained at 10 V (assume $r_Z = 0$) for the following circuit shown the Fig. 3 (c) [10]

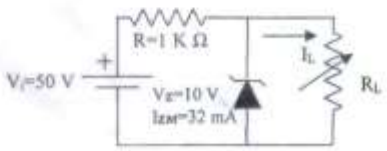


Fig. 3(c)

4.(a) Explain why a BJT is known as bipolar device. Define β and α of a BJT and establish the relation between them. If the value of α in a BJT is close to unity, what should be the value of the base current? [8]

(b) Calculate the value of $R_1$ and $R_C$ for the circuit in Fig. 4(b). The collector current $I_C = 1$ mA and the collector to emitter voltage $V_{CE} = 6$ V. Neglect the base current. [8]

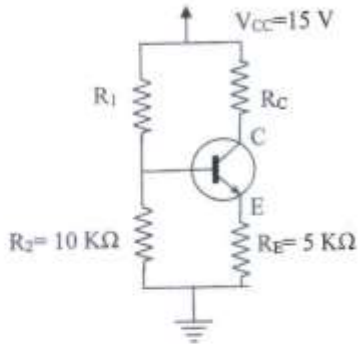


Fig. 4(b)

(c) For the circuit in the Fig. 4(c), it is required to determine the value of the voltage $V_{BB}$ that results in the transistor operating [9]
(i) in the active mode with $V_{CE} = 5$ V,
(ii) at the edge of saturation,
(iii) deep in saturation with $\beta_{forced} = 10$.
For simplicity, assume that $V_{BE}$ remains constant at 0.7 V. The transistor $\beta$ is specified to be 50.

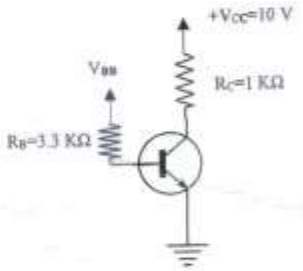


Fig. 4(c)

5.(a) The transistor in the circuit in Fig. 5(a) is specified to have β in the range of 50 to 150. Find the value of $R_B$ that results in saturation with an ODF at least 10. [08]

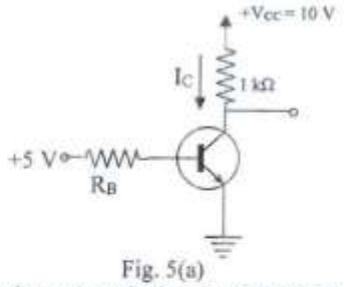


Fig. 5(a)

b) For the circuit in Fig. 5(b) determine whether the BJT is in active or saturation mode. Then determine $V_E$, $V_C$, $V_B$, $I_E$, $I_C$ and $I_B$. [12]

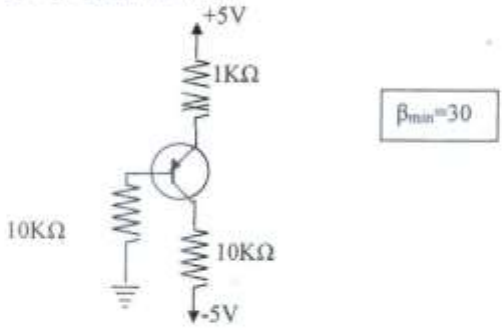


Fig. 5(b)

c) What is the sigficance of Q point in a BJT amplifier? Does its location affect the performance of the amplifier? [05]

6.(a) Draw a common emitter amplifier circuit. Draw its small signal equivalent circuit and find the expressions of (i) $R_{in}$ (ii) $A_v$ (iii) $G_v$ (iv) $A_{is}$ and (v) $R_O$. [15]

(b) For the above amplifier of Q. 6(a), $R_B$ =100 kΩ, $R_C$ = 8 kΩ, $R_L$ = 5 kΩ, $g_m$ = 40 mA/v, $r_\pi$ = 2.5 kΩ, $r_o$ = 100 kΩ, $r_e$ = 25 Ω. if $R_{sig}$= 5 k Ω and the sine-wave $v_\pi$ is limited to 5 mV peak, what is the maximum allowed peak of $v_{sig}$ and the corresponding peak amplitude of $v_o$. [10]

7.(a) Describe the differences between BJTs and FETs. Why JFETs are widely used in digital ICs? [05]

(b) Describe the operation principle of a depletion type n-channel JFETs with proper diagrams including semiconductor structure and output characteristics. How can a JFET be used as a variable resistor? [10]

(c) Given $I_{DSS}$ = 6 mA and $V_P$ = - 4.5 V; Using Shockley's equation draw the transfer characteristics of a deletion type n-channel MOSFET. If $V_{GS}$ is positive which region it will operate? What precaution has to be taken to have a positive gate to source voltage? [10]

8.(a) A depletion n-channel MOSFET amplifier has been biased with a configuration of a voltage divider configuration. Draw the circuit diagram for this arrangement. In the voltage divider branch set $R_1$= 110 MΩ, $R_2$=10 MΩ. The drain resistance, $R_D$ =1.8 kΩ and source resistance $R_S$ = 750 Ω. If $I_{DSS}$ = 6 mA and $V_P$= -3 V, determine $I_{DQ}$, $V_{GSQ}$ and $V_{DS}$. [12]

(b) The fixed bias configuration of a JFET has an operating point defined by $V_{GSQ}$ = - 2 V and $I_{DQ}$ = 5.625 mA, with $I_{DSS}$ = 10 mA and $V_P$ = - 8 V. The network is shown in Fig. 8(b) with an applied signal $V_i$. The value of $y_{os}$ is provided as 40 μS. [13]

(i) Determine $g_m$.
(ii) Find $r_d$.
(iii)Determine $Z_i$.
(iv)Calculate $Z_o$.
(v) Determine the voltage gain $A_v$.
(vi)Determine Av ignoring the effects of $r_d$.

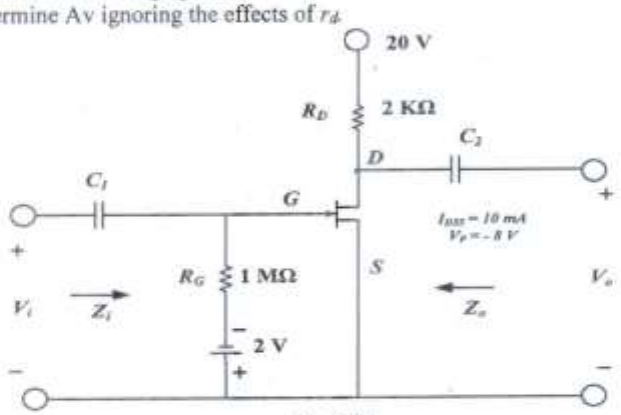


Fig. 8(b)

B.Sc. Engg. (EE), 2nd Sem. Date: October 28, 2019 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
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**DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING**

Semester Final Examination — Summer Semester, A.Y. 2018-2019
Course No.: EEE 4203 — Time: 3 hours
Course Title: Electronics I — Full Marks: 150

There are **8 (eight)** questions. Answer **any 6 (six)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper. Symbols preserve their usual meaning.

1. a) The input voltage Vi in Fig. 1(a) is a 1 kHz, 20 V peak to peak sine wave. Sketch the resulting output waveform at $V_0$ as indicated. 7

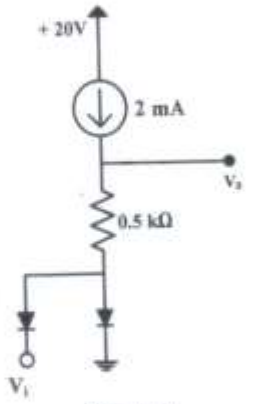


Fig. 1(a)

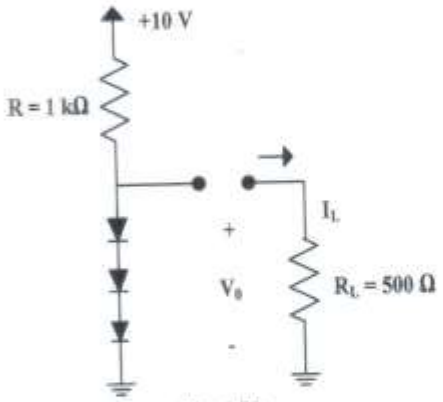


Fig. 1(b)

b) For the above circuit in Fig. 1(b), a string of three diodes are used to provide a constant voltage of about 2.1 volt. Calculate percentage of change in this regulated voltage caused by 8
(i) ±10% change in power supply.
(ii) Connection of load resistance, $R_L$. Assume, n = 2.

c) Determine the range of values of $R_L$ and $I_L$ for the figure shown in Fig. 1(c). 10

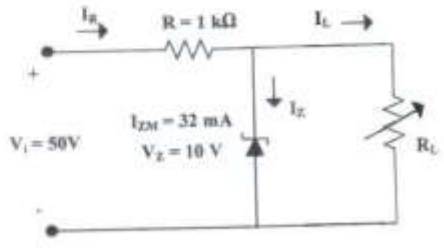


Fig. 1(c)

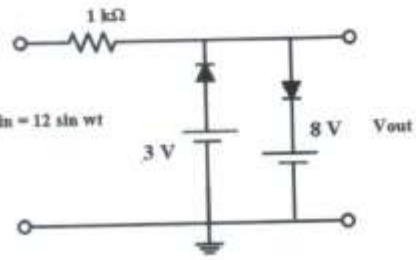
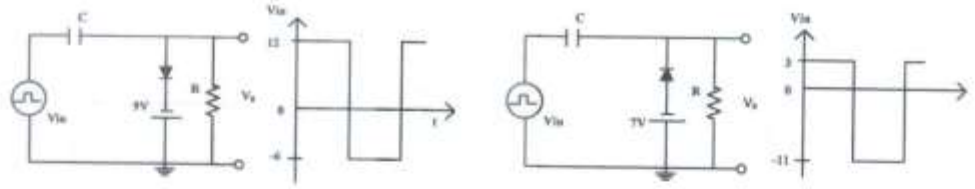


Fig. 2(a)

2. a) Find the output waveshape for the clipper shown in Fig. 2(a). Assume, all diodes are ideal 10

b) Find the output voltage waveshapes for the following clampers (with Si diodes) shown in Fig. 2(b). 15



(i) (ii)

Fig. 2(b)

3. a) What is an Early effect of a BJT? Derive the expression of output resistance considering the Early effect. 8

b) For the circuit in Fig. 3(b), determine the value of the voltage $V_{BB}$ that results in the transistor operating (i) in the active mode with $V_{CE} = 5$ V, (ii) at the edge of saturation and (iii) deep in saturation with $\beta_{forced} = 10$. Assume, $V_{BE} = 0.7$ V and $\beta = 50$. 10

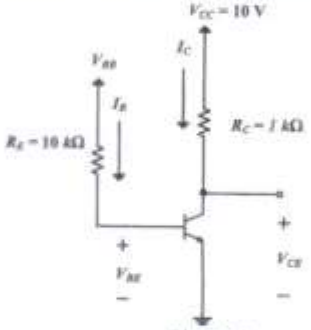



Fig. 3(b)

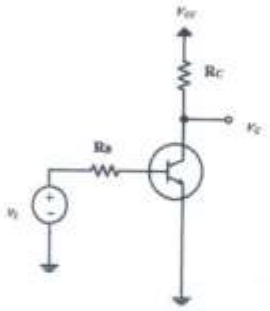



Fig. 3(c)

c) For the circuit shown in Fig. 3(c), calculate the base current, collector current and the collector voltage where $V_{CC} = +5$ V, $V_i = +5$ V, $R_B = R_C = 1$ kΩ and $\beta = 100$. If he transistor is saturated, find $\beta_{forced}$. What value should $R_B$ be raised to bring the transistor to the edge of saturation? 7

4. a) For the network of Fig. 4(a), Find $I_C$, $I_B$, $I_E$, $V_C$ and $V_E$ 10

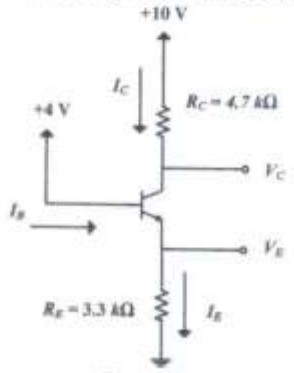



Fig. 4(a)

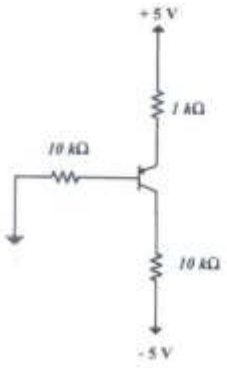



Fig. 4(b)

b) Analyze the circuit of Fig. 4(b) and find all the node voltages and branch currents. The minimum value of β is specified to be 30. 15

5. a) For the circuit of Fig. 5(a), determine the voltages at all nodes and currents through all branches. Assume, $\beta = 100$. 12

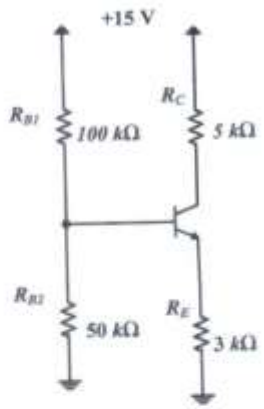


Fig. 5(a)

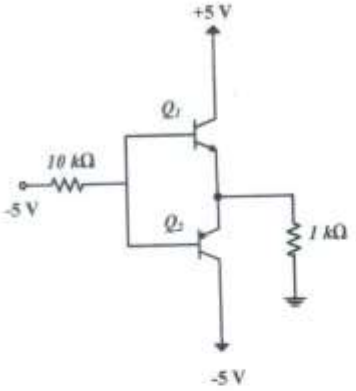


Fig. 5(b)

b) Evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 5(b). Assume, β = 100. 13

6. a) Derive the expression of $g_m$ , $r_\pi$ and $r_e$ for the small signal model of a BJT. 7

b) Analyze the transistor amplifier shown in Fig. 6(b) to determine its voltage gain $v_0/v_i$ Assume, $\beta = 100$ and neglect the early effect. 8

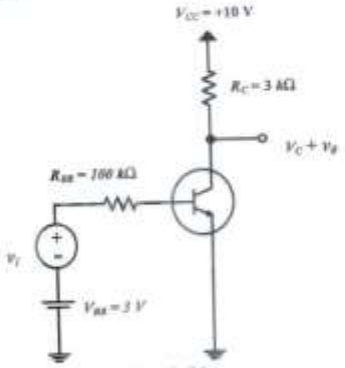


Fig. 6 (b)

c) A CE amplifier utilizes a BJT with β = 100 is biased at $I_C$ = 1 mA and has a collector resistance $R_C$ = 5 kΩ. Find $R_{in}$, $R_0$ and $A_{v0}$. If amplifier is fed with a signal source having a resistance of 5 kΩ and load resistance $R_L$ = 5 kΩ is connected to the output terminal, find the resulting $A_v$ and $G_v$. 10

7. a) What is the basic difference between JFET and BJT? Write down the advantages and disadvantages of JFET. 5

b) Determine (i) $V_{GS_Q}$ (ii) $I_{D_Q}$ (iii) $V_{DS}$ (iv) $V_S$ (iv) $V_G$ (v) $V_D$ for the circuit shown in Fig. 7(b). 10

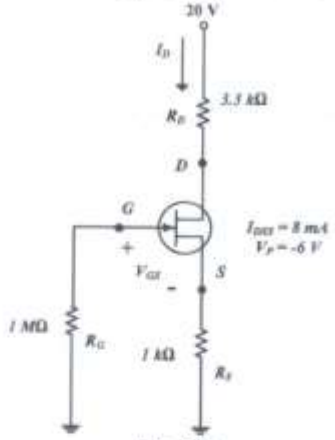



Fig. 7(b)

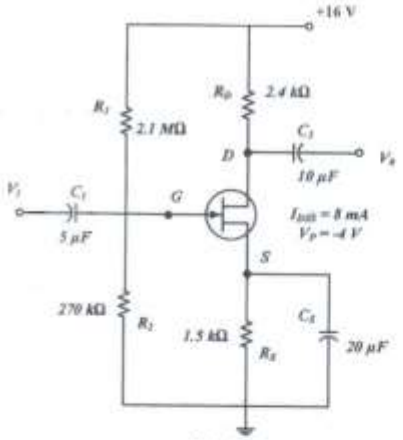



Fig. 7(c)

c) Determine (i) $I_{D_Q}$ and $V_{DS_Q}$ (ii) $V_D$ (iii) $V_S$ (iv) $V_{DS}$ (v) $V_{DG}$ for the network of Fig. 7(c). 10

8. a) What is the difference between depletion type MOSFET and enhancement type MOSFET with respect to transfer characteristics? 7

b) Determine $I_{D_Q}$ and $V_{DS_Q}$ for the enhancement type MOSFET shown in Fig. 8(b). 8

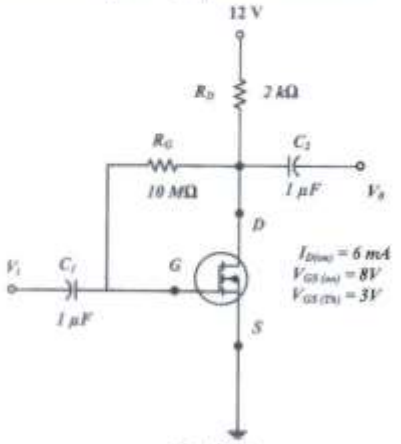



Fig. 8(b)

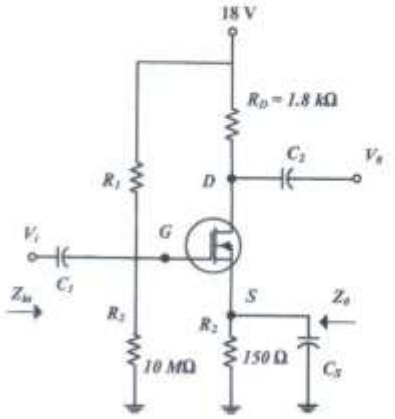



Fig. 8(c)

c) For the network of Fig. 8(c) $V_{GS_Q}$ = 0.35 V, $I_{D_Q}$ = 7.6 mA, $I_{DSS}$ = 6 mA, $V_P$ = -3V and $g_{OS}$ = 10 μS. 10

i. Determine $g_m$ and compare to $g_{m0}$
ii. Find $r_d$
iii. Sketch the ac equivalent network
iv. Find $Z_i$
v. Calculate $Z_o$
vi. Find $A_v$

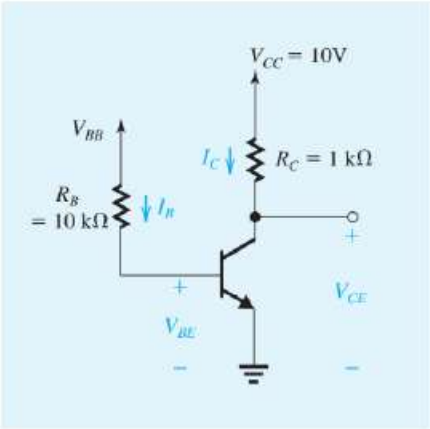
Q.1. (a) (i) The model of npn BJT in saturation mode reveals the following equation: 12.5

$$i_C = I_S e^{v_{BE}/V_T} - I_{SC} e^{v_{BC}/V_T}$$

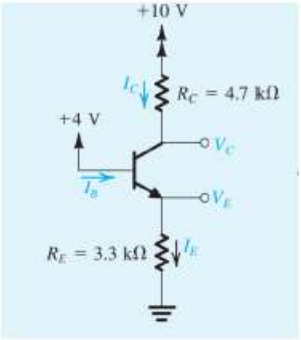
Draw the the $i_C$ vs $v_{CB}$ characteristic of the npn transistor fed with constant emitter current $I_E$ following the above equation. Clearly define different region of operations.

(ii) Find the value of Collector to Emitter voltage at the edge of saturation.

(iii) For the following figure, find the value of the voltage $V_{BB}$ in the transistor operating in deep saturation with $\beta_{forced}=8$

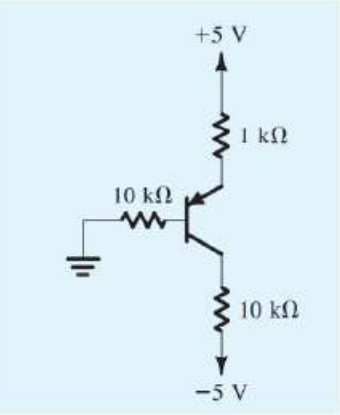



1.(b) For the circuit in the following Figure, find the highest voltage to which the base can be raised while the transistor remains in the active mode. Assume α =1. 12.5

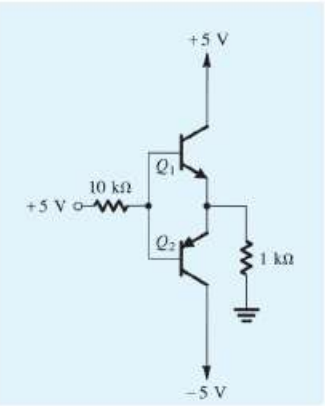


# Question Number 2

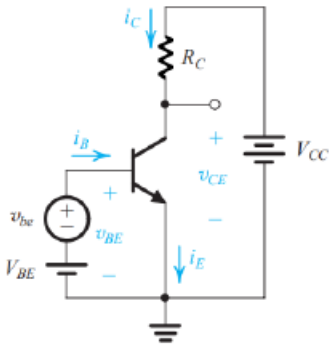
Q.2 (a) Determine the voltages at all nodes and the currents through all branches. 12.5
The minimum value of β is specified to be 20.




2.(b) Evaluate the voltages at all nodes and the currents through all branches in the circuit of the following circuit by replacing the feeding voltage to the bases +5 V by -5 V. Assume β = 100 if transistor operates in active region. 12.5



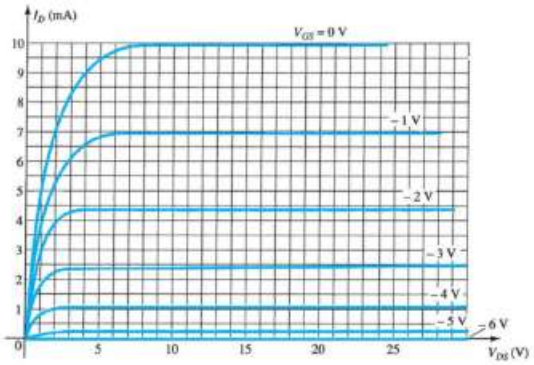
3. (a) In the circuit of the following figure, $V_{BE}$ is adjusted to yield a dc collector current of 1 mA. Let $V_{CC}$ = 15 V, $R_C$ = 10 kΩ, and β = 100. Find the voltage gain If $v_{be}$ = 0.005 sinωt volt, find $v_{C}(t)$ and $i_B(t)$. 12.5



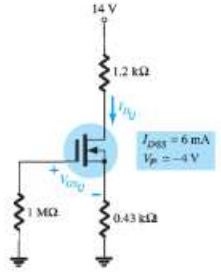

(b) Consider a CB amplifier utilizing a BJT biased at $I_C$=1 mA and with $R_C$=5 kΩ. Determine $R_{in}$, $A_{vo}$, $R_o$, if the amplifier is loaded in $R_L$= 5kΩ , what value of $A_v$ results? What $G_v$ is obtained if $R_{sig}$ = 5 KΩ? 12.5

Q.4. (a) (i) What are the main advantages of FETs over BJTs? 04

(ii) Using the following figure, sketch the transfer characteristics directly from the drain characteristics. Using the following figure to establish the values of $I_{DSS}$ and $V_P$, sketch the transfer characteristics using Shockley's equation 8.5




4. (b) For the self-bias configuration of the following figure, determine: (i) $I_{DQ}$ and $V_{GSQ}$. (ii) $V_{DS}$ and $V_D$. 12.5




**OR**

(b) Determine $Z_i$, $Z_o$, and Av for the following network.