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B.Sc. Engg. (EE)/HDEE, 3rd Sem, B.Sc.TE (2-Yr), 1st Sem. Date: March 02, 2015(Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination
Course No.: Math 4301
Course Title: Mathematics III

Winter Semester, A. Y. 2014-2015
Time: 90 Minutes
Full Marks: 75

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper.

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1. a) Define Laplace Transform and write down its important uses. 15

Derive the formula for $L\{e^{-kt}\sinh \mu t\}$; $L\{t^n e^{\lambda t}\}$ and find $L^{-1}\left\{\frac{s+4}{s^2+9s+2}\right\}$.

b) By Laplace Transform find the solution of $Y''(t)+k^2Y(t)=a$ with $Y(0)=1, Y'(0)=0$. 10

2. a) Establish that: $L\{t^n F(t)\}=(-1)^n\frac{d^n}{ds^n}\{f(s)\}$ and hence find the solution of 15

$Y''(t)+atY'(t)-2aY(t)=1$ with $Y(0)=Y'(0)=0, a>0$.

b) Evaluate the integral: $\int_0^\infty \frac{x\sin tx}{x^2+a^2}dx$ using Laplace Transform. 10

3. a) By Laplace Transform solve the boundary value problem: $\frac{\partial U}{\partial t}=2\frac{\partial^2 U}{\partial x^2}$ with 15

$$U(0,t)=0, U(5,t)=0, U(x,o)=10\sin 4\pi x-6\sin 6\pi x.$$

b) Show that the solution of Abel's integral equation: $F(t)=\int_0^t (t-u)^{-h}Y'(u)du$ can be written 10

in the form, $Y(t)=\frac{\sin b\pi}{\pi}\int_0^t F(u)(t-u)^{h-1}du$.

4. a) Show that the vectors $\underline{a}\times(\underline{b}\times\underline{c})$, $\underline{b}\times(\underline{c}\times\underline{a})$, $\underline{c}\times(\underline{a}\times\underline{b})$ are coplanar. 8

b) Examine whether $(\underline{a}\times\underline{b})\times(\underline{c}\times\underline{d})+(\underline{a}\times\underline{c})\times(\underline{d}\times\underline{b})+(\underline{a}\times\underline{d})\times(\underline{b}\times\underline{c})=-2[\underline{b}\underline{c}\underline{d}]\underline{a}$. 8

c) A particle moves along the curve $x=e^{-t}$, $y=2\cos 3t$, $z=2\sin 3t$. Determine the components of its velocity and acceleration at time $t=0$ in the direction of $2i-3j+k$. 9

B.Sc. Engg. (EE)/ HDEE, 3rd Sem. Date: March 09, 2015(Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination
Course No.: EEE 4303
Course Title: Electronics II

Winter Semester, A. Y. 2014-2015
Time: 90 Minutes
Full Marks: 75

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper. All symbols resemble their usual meaning.

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1. a) Draw the construction of a p-channel MOSFET that has a reduced effective length compared to that of a p-channel enhancement-type MOSFET, showing clearly the channel formed during pinch-off. State other advantages of this type of MOSFET apart from the channel length. Derive the equation of I_{DS} as a function of V_{GS} and V_{DS}. If the substrate is more positive than the source, how will the equation of I_{DS} get modified? Sketch the transfer curve representing the characteristics of this type of MOSFET. 15

b) Plot the voltage transfer characteristics of the n-channel enhancement type MOSFET illustrated in Fig. 1, clearly defining every region of operation and shade the region where the MOSFET operates in the triode region. 6

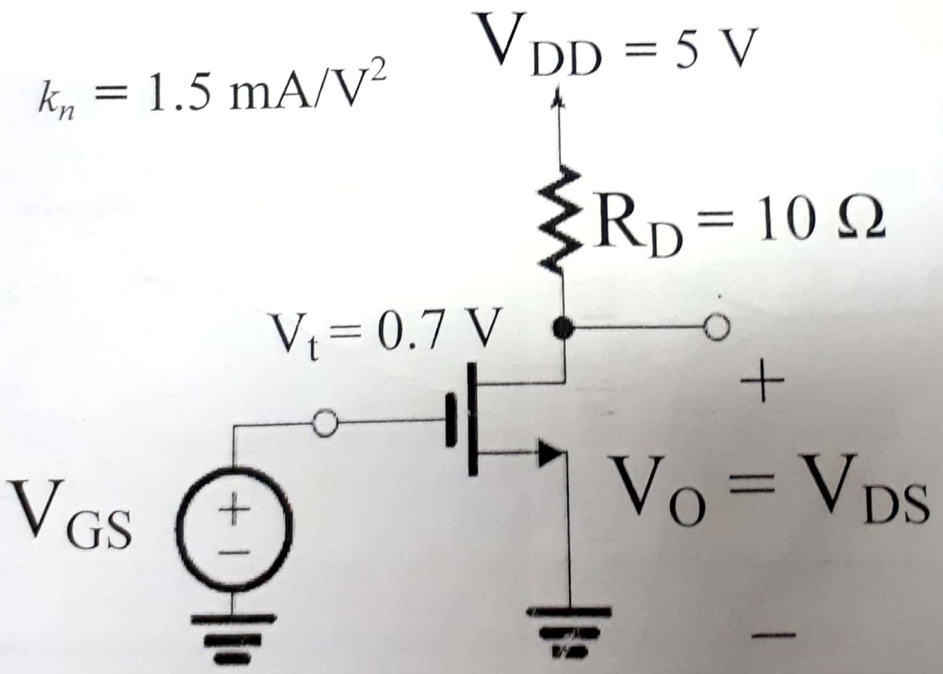

Fig. 1

c) Name a type of FET that is used in RF applications and state with reasons why it can be used in such applications. How the operation of it is different from MOSFET's and state which type of channel is inevitably used for this type of FET? 4

2. a) The NMOS (Q_n) and PMOS (Q_p) transistors in the circuit of Fig. 2 below are matched with $k_n'\left(\frac{W_n}{L_n}\right)=k_p'\left(\frac{W_p}{L_p}\right)=1.25\ \text{mA/V}^2$ and $V_{tn}=-V_{tp}=0.8\ \text{V}$. Assuming $\lambda=0$, for both devices, find the drain current i_{DN} and i_{DP} and the voltage V_o for $V_I=0$ V, 2.5 V, and -2.5 V.

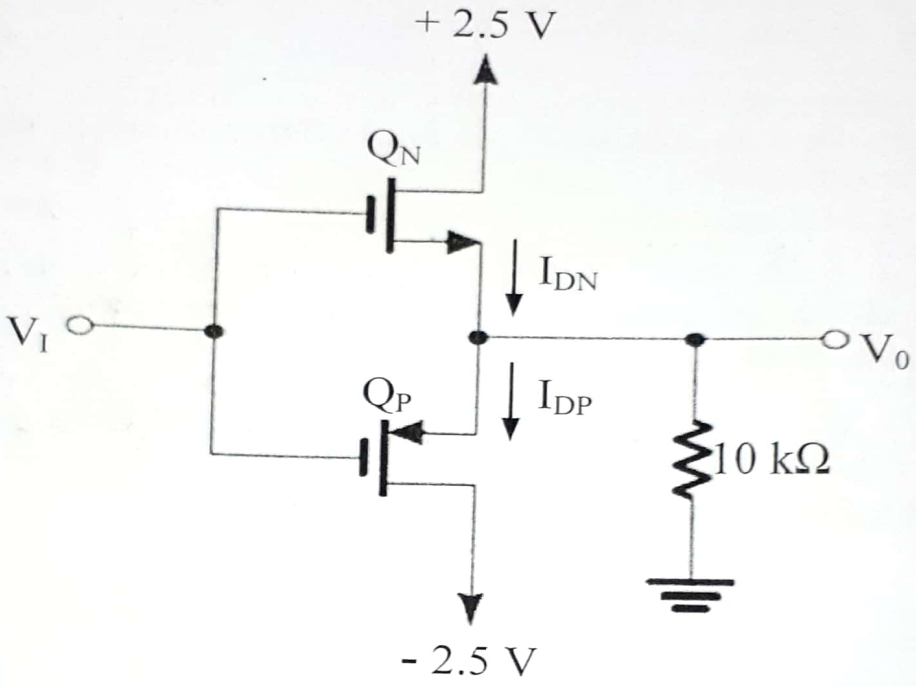

Fig. 2

b) Draw the CMOS logic circuit for the following boolean expressions

i. $Y=\overline{(A+B+C).D+(E.F)}$

ii. $Y=\overline{(A.B.C)+(E.F.G)}$

iii. $Y=\overline{\overline{(A+B).C}+\overline{(D+C)}}$

c) Draw the area of the operating region of a depletion type MOSFET if $I_{DS_{max}}=100$ mA, $V_{DS_{max}}=30$ V, $I_{DSS}=30$ mA, $V_p=-4$V and $P_{max}=900$ mW.

d) State the advantages of using OP-AMP for filter design instead of simple RLC circuits.

3. A student wants to use a triangular wave as an input to a 3rd order system with a differential equation: $\frac{d^3y(t)}{dt^3}+6\frac{d^2y(t)}{dt^2}+3\frac{dy(t)}{dt}+0.4y(t)=x(t)$, where $x(t)$ is the input and $y(t)$ is the output respectively. However, the student is provided with only 0.01 μF capacitors, 10 kΩ resistors, 20 kΩ resistors, supply voltage of +15 V and -15 V and OP-AMP 741 IC's.

i. Describe how the student would generate a bipolar triangular wave of 15 kHz showing the circuit with neat diagram.

ii. Unfortunately, the generated triangular wave was distorted due to the addition of high frequency noise of 40 kHz with amplitude of 0.5 V. He decides to remove the unwanted noise with the help of a filter. Describe how the student would design a specific 5^{th} order filter, to remove the unwanted noise and would also amplify the signal by a factor of 1.5. Illustrate the circuit with neat diagram.

iii. The triangular wave that he gets as an output from the filter is phase shifted by an angle of $\angle\theta$. He decides to shift the phase of the output from the filter further by $+90^0$ such that the phase angle of the triangular wave would be $\angle\theta + 90^0$. Describe how the student would use OP-AMP circuit to undergo this phase-shift operation. Illustrate the circuit with neat diagram.

iv. Finally he feeds this wave as an input to the aforementioned 3^{rd} order system. Describe how he would design the third-order system using only simple-integrator, inverting and non-inverting OP-AMP circuits.

4. a) Find the relationship between V_0 and V_I in the circuit of Fig. 3. What kind of operation does this circuit perform? Draw the bode-plot of the transfer function $\left(\frac{V_0}{V_I}\right)$ of this circuit, if R = 100 kΩ and C = 0.1 μF. 15

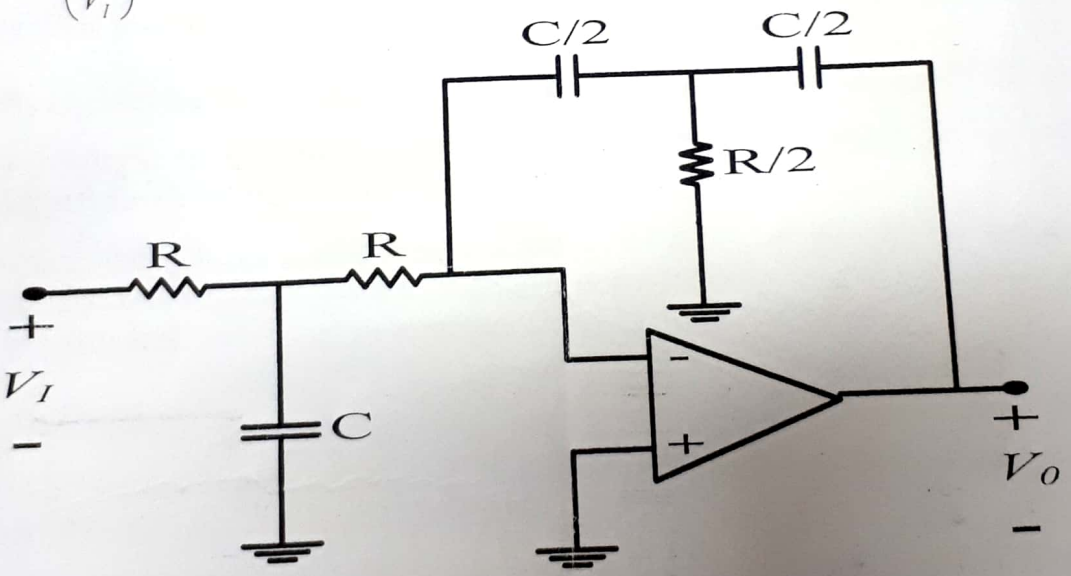

Fig. 3

b) You are provided with only two ideal OP-AMPs and plenty of resistors but all having a resistance value of 40 kΩ, along with a supply voltage of +15 V and 15 V. Use the available circuit components to implement the summing function 10

$$v_0 = v_1 + 2v_2 - 3v_3 - 4v_4.$$

where v_0 is the output and v_1, v_2, v_3 and v_4 are the inputs respectively.

B.Sc. Engg. (EE)/ HDEE, 3rd Sem. 14 Date: March 05, 2015 (Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination
Course No.: EEE 4305
Course Title: Electrical Machines I

Winter Semester, A. Y. 2014-2015
Time: 90 Minutes
Full Marks: 75

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper. Symbols carry their usual meanings.

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1. a) With neat diagram, explain in detail the principle of E.M.F. induction in a single loop generator. [15]

   b) The following information is given for a 4 pole, lap wound short shunt generator: $E_g = 230$ V, $I_a = 50$ A, $I_{sh} = 5$ A, $V = 200$ V, $R_a = 0.3\ \Omega$. Find R_{sh}, R_{se} and R_L. [05]

   c) A long-shunt generator delivers 50 A at 500 V and the resistances of the series field, shunt field and the armature are 0.03 Ω, 250 Ω and 0.05 Ω respectively. Calculate the generated E.M.F. [05]

2. a) What are the magnetic losses of DC machine? Is it possible to eliminate them completely? Explain. [2+5]

   b) What are dummy coil and equalizer ring? [2+2]

   c) Draw the power flow diagram of the DC machine. [03]

   d) Explain the process of commutation with neat diagram. [11]

3. a) Briefly explain the motor principle. Write down the significance of back E.M.F. [5+3]

   b) Draw a simple time controlled starter circuit of DC motor. What are the protections available from the starter circuit? [6+4]

   c) Determine the induced torque and shaft torque of 220 V, 4 pole series motor with 800 conductors' wave connected supplying a load of 8.2 kW by taking 45A from the mains. The flux per pole is 25 mWb and its armature circuit resistance is 0.6 Ω. [07]

4. a) What is lost torque? [02]

   b) Derive the terminal characteristics of DC series motor and hence explain why a series motor cannot be started under unloaded condition. [5+2]

   c) A 100 hp, 250 V, 350 A D.C. shunt motor has an armature resistance of 0.05 Ω. It is desired to design a starter circuit for this motor which will limit the maximum starting current to twice its rated value and which will switch out sections of resistance as the armature current falls to its rated value. [7+2+7]

   (i) Derive the formula for calculating the number of stages.

   (ii) How many stages of resistance will be required to limit the current to the range specified?

   (iii) What should be the value of each segment resistor? At what voltage each segment of resistance be cut out?

B.Sc. Engg. (EE)/HDEE, 3rd Sem. 15 Date: March 03, 2015 (Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination
Course No.: EEE 4307
Course Title: Digital Electronics

Winter Semester, A. Y. 2014-2015
Time: 90 Minutes
Full Marks: 100

There are **4 (four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper.

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1. a) Find the value of X. 10

(i) $(2134)_5 = (X)_{10}$
(ii) $(2134)_{10} = (X)_5$
(iii) $(1001.0101)_8 = (X)_{10}$
(iv) $(32514.2532)_8 = (X)_{16}$.

b) The (r-1)'s complement of base-6 numbers is called the 5's complement. 9
(i) Determine a procedure for obtaining 5's complement of base-6 numbers.
(ii) Obtain 5's complement of $(543210)_6$
(iii) Perform subtraction operation $(553210)_6 - (543210)_6$ by taking (r-1)'s complement of the subtrahend.

c) Reduce the following Boolean expressions to the indicated number of literals: 9

(i) $\bar{A}\bar{C} + ABC + A\bar{C}$ to three literals
(ii) $\bar{A}B(\bar{D} + \bar{C}D) + B(A + \bar{A}CD)$ to one literal
(iii) $(\bar{A} + C)(\bar{A} + \bar{C})(A + B + \bar{C}D)$ to four literals

d) Prove that $5\frac{1}{3}$

$$\bar{x} \oplus y = x \oplus \bar{y} = \overline{(x \oplus y)} = xy + \bar{x}\bar{y}$$

2. a) Design an adder which is capable to add three 4-bit binary numbers A, B and C. $13\frac{1}{3}$

b) Simplify the following Boolean functions using Karnaugh-Map in (i) POS and (ii) SOP form. 12

(i) $F(w, x, y, z) = \sum(0,2, 5,6, 7, 8, 10)$,
(ii) $F(w, x, y, z) = \Pi(0,1, 2, 4, 5, 7, 11, 15)$

c) Design a combinational circuit with four inputs and four outputs. The output generates the 2's complement of the input binary number. 8

3. a) Draw the logic diagram of an 8 × 1 multiplexer 10

b) Construct a 16 × 1 multiplexer with two 8 × 1 and one 2 × 1 multiplexers. Use block diagrams for the three multiplexers. $8\frac{1}{3}$

c) Tabulate the PLA programming table for the permanent storage shown below with total eight words and four bits per word. Minimize the number of product terms.

	F1	*F2*	*F3*	*F4*
Word 1	0	1	0	0
Word 2	1	1	0	1
Word 3	1	0	1	1
Word 4	0	0	0	1
Word 5	1	0	0	0
Word 6	0	0	0	1
Word 7	1	1	1	0
Word 8	0	1	0	1

4. Design a combinational circuit that compares three 2-bit binary numbers A, B and C. The circuit has four outputs x_1, x_2, x_3 and x_4 so that

$x_1 = 1$, $x_2 = 0$, $x_3 = 0$ and $x_4 = 0$ if A = B = C,
$x_1 = 0$, $x_2 = 1$, $x_3 = 0$ and $x_4 = 0$ if A is the highest valued number,
$x_1 = 0$, $x_2 = 0$, $x_3 = 1$ and $x_4 = 0$ if B is the highest valued number,
$x_1 = 0$, $x_2 = 0$, $x_3 = 0$ and $x_4 = 1$ if C is the highest valued number,
$x_1 = 0$, $x_2 = 1$, $x_3 = 1$ and $x_4 = 0$ if A = B > C,
$x_1 = 0$, $x_2 = 0$, $x_3 = 1$ and $x_4 = 1$ if B = C > A,
$x_1 = 0$, $x_2 = 1$, $x_3 = 0$ and $x_4 = 1$ if C = A > B.