B.Sc. Engg. SWE 2nd Semester 143

10 August 2018 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION **SUMMER SEMESTER, 2017-2018**

DURATION: 1 Hour 30 Minutes **FULL MARKS: 75**

CSE 4205: Digital Logic Design

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **4 (four)** questions. Question No.4 is **mandatory**. Answer any **2 (two)** from the remaining questions.

Figures in the right margin indicate marks.

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1. a) Design the proper switching circuit for the given Boolean expression: 6

$$F(A,B,C,D)=ABD'+ACD'+ABCD'$$

b) Assign a binary code in some orderly manner to the 52 playing cards. Use the minimum number of bits. (The four suits of cards are Clubs, Diamonds, Hearts, and Spades.) 7

c) Find the complement of F = x + yz; then show that F.F' = 0 and F + F' = 1. 12

2 a) Why is Gray Code known as 'Cyclic Code'? Is Gray code weighted or non-weighted code? Explain your answer for 3-bit Gray code. 7

b) Determine the base of the numbers in each case for the following operations to be correct: 6

i. $(34\times2)\times13=5$

ii. $353-16=33A$

c) Reduce the following Boolean Expressions to a minimum number of literals using the postulates and theorems of Boolean Algebra. Then draw the logic diagrams of the circuit that implement the original and simplified expressions: 6×2

i. $A'B(D'+C'D)+B(A+A'CD)$

ii. $X'+Y'+XYZ'$

3 a) Why does replacing 0's with 1's and 1's with 0's give us the 1's complement of a binary number? 5

b) Consider X,Y,Z as Input signals of logic gates. Draw the output signal of the following logic gates: 1.5×4

i. OR gate

ii. NAND gate

iii. NOR gate

iv. XOR gate

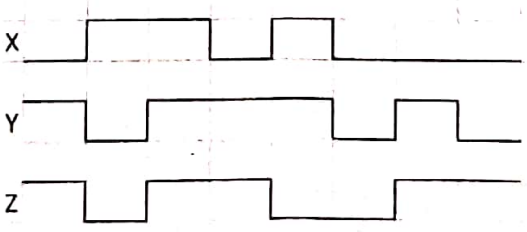

Figure 1: Figure for Question 3.(b)

c) Obtain the truth table of the following function and express the function in canonical SOP and POS form: 4+5+5

$$F(A,B,C,D)=AD+C'$$

[Mandatory]

4 a) Use the Quine-McCluskey tabular minimization method to minimize the function 15

$$F(A, B, C, D) = \sum m(0,3,5,6,7,10,12,13) + \sum d(2,9,15)$$

b) Use a Karnaugh map to simplify the following Boolean function: 10

$$F(A,B,C,D)=\sum m(0,1,2,3,8,10,11,12,14)$$

B.Sc. Engg. / HD CSE 2nd Semester (110)

21 August 2017 (Morning)

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MID SEMESTER EXAMINATION

SUMMER SEMESTER, 2016-2017

DURATION: 1 Hour 30 Minutes

FULL MARKS: 75

CSE 4205: Digital Logic Design

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There are **4 (Four)** questions. Answer any **3 (Three)** of them.

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a) What are the benefits of universal gates? Implement the functionalities of NAND gates using NOR gates and the functionalities of NOR gates using NAND gates. 7

b) Analyze the two output combinational circuit shown in Figure 1. Obtain the Boolean Functions for the two outputs and explain the circuit operations. 10

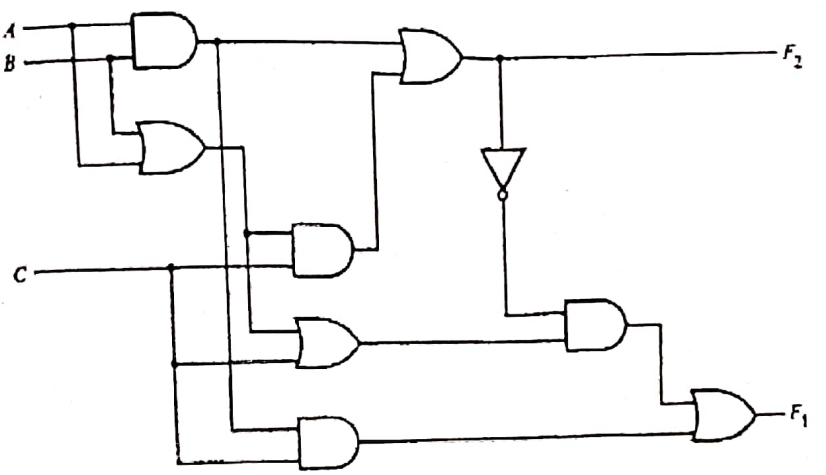

Figure 1: Combinational circuit.

c) Simplify the following Boolean expressions to a minimum number of literals. 8

i. $(A + B)'(A' + B')$

ii. $(x'y' + z)' + z + xy + wz$

2. a) Generally NAND and NOR gates are implemented and verified using 2 inputs. Can you extend the number of inputs of them (more than two) as we do for AND or OR gates. Justify your answer with proper explanation and circuit diagram. 5

b) *Parity generator* is a circuit that generates parity bit in the transmitter and *parity checker* is one that checks the parity in receiver. Now draw two circuit diagrams of parity generator and parity checker using exclusive-or and equivalence gates only for *4-bit message*. Consider **even parity** for parity generation and checking. 8

c) Following *Design Procedure*, design a 4-bit binary-to-gray code converter including function table and logic diagram. 12

3. a) Simplify the following Boolean functions using Karnaugh-Map in (i) POS and (ii) SOP form. 12

i. $F = ABC + A'B'CD' + A'BC'D$

a. $d = B'D + A'BD' + AB'D'$

ii. $F(w,x,y,z) = \prod(1, 3, 5, 7, 13, 15)$

b) Simplify the following Boolean function by means of *Quine-McCluskey* method and also implement the simplified expression using NOR gates only.

$$F(w,x,y,z) = \sum(0,1,5,7,8,10,14,15).$$

4. a) Suppose for arithmetic addition of two decimal digits, augend and addend are taken in BCD together with a possible carry from a previous stage. The output sum of the decimal digits must be represented in BCD. Now construct a block diagram that can solve the abovementioned problem with necessary function table and simplification steps.

b) It is necessary to multiply two binary numbers, each two bits long, in order to form their product in binary. Let the two numbers be represented by $a_1\ a_0$ and $b_1\ b_0$ where subscript 0 denotes the least significant bit.

i. Determine the number of output lines required.
ii. Find the simplified Boolean expressions for each output following necessary procedures.
iii. Draw the circuit diagram.

c) What is a self-complementary code? What are the advantages of these codes over BCD? Give corresponding examples that verify your answer.

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12 August 2016 (Afternoon)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
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Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION
DURATION: 1 Hour 30 Minutes

SUMMER SEMESTER, 2015-2016
FULL MARKS:75

CSE 4205: Digital Logic Design

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1. a) Convert the decimal number 165.125 into hexadecimal and binary. 6
   b) Perform the arithmetic operation (+36) + (-12) in binary using the signed-2's-complement representation for negative number. 7
   c) Explain the process of *transfer of information with registers.* 12

2. a) State and explain the De Morgan's theorem. 6
   b) Prove the distributive law using truth table. 7
   c) For the Boolean function $f(x,y,z) = \sum (m1, m4, m5, m6, m7)$ where m's are minterms 3×4
      i. Write the minimized form using Boolean Algebra.
      ii. Draw the truth table of the function.
      iii. Write function in the form of product ($\prod$) of maxterms.
      iv. Draw the digital logic circuit of the minimized function and mention the number of logic gates.

3. a) What do you understand by prime implicants and essential prime implicants? 4
   b) State different symbols for NAND, NOR and NOT gates along with their inputs and output functions. 6
   c) For the following Boolean function $f(a,b,c,d) = \sum (0,2,4,5,6,7,8,10,13,15)$, 3×5
      i. Draw its Karnaugh map.
      ii. Write its minimized function.
      iii. Draw the logic circuit by using only NAND gates.

4. a) What do you understand by universal gates? 2
   b) For the following functions $f(w,x,y,z) = \sum (0, 1,2,3,4,8,9,12)$,
      i. Write its minimized product of maxterms by using Karnaugh's map. 5
      ii. Draw its AND-OR-NOT logic diagram. 5
      iii. Implement the minimized function with the following two-level forms: 10
      NAND-AND and NOR-OR.
   c) Write short notes on VHDL. 3