

Memory Organization

LEC :7

TYPES OF MEMORY

8.1. TYPES OF MEMORY

Memory is an essential element of a computer. Without its memory, a computer is of hardly any use. Memory plays an important role in saving and retrieving data. The performance of the computer system depends upon the size of the memory. Memory is of following types:

1. Primary Memory (Internal)
2. Secondary Memory (External)

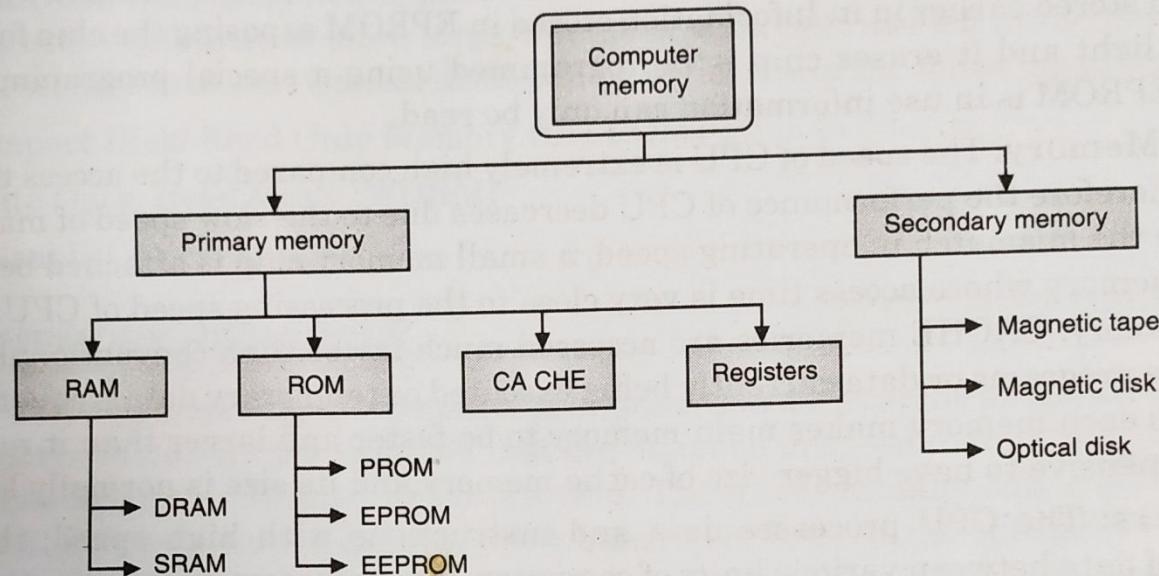
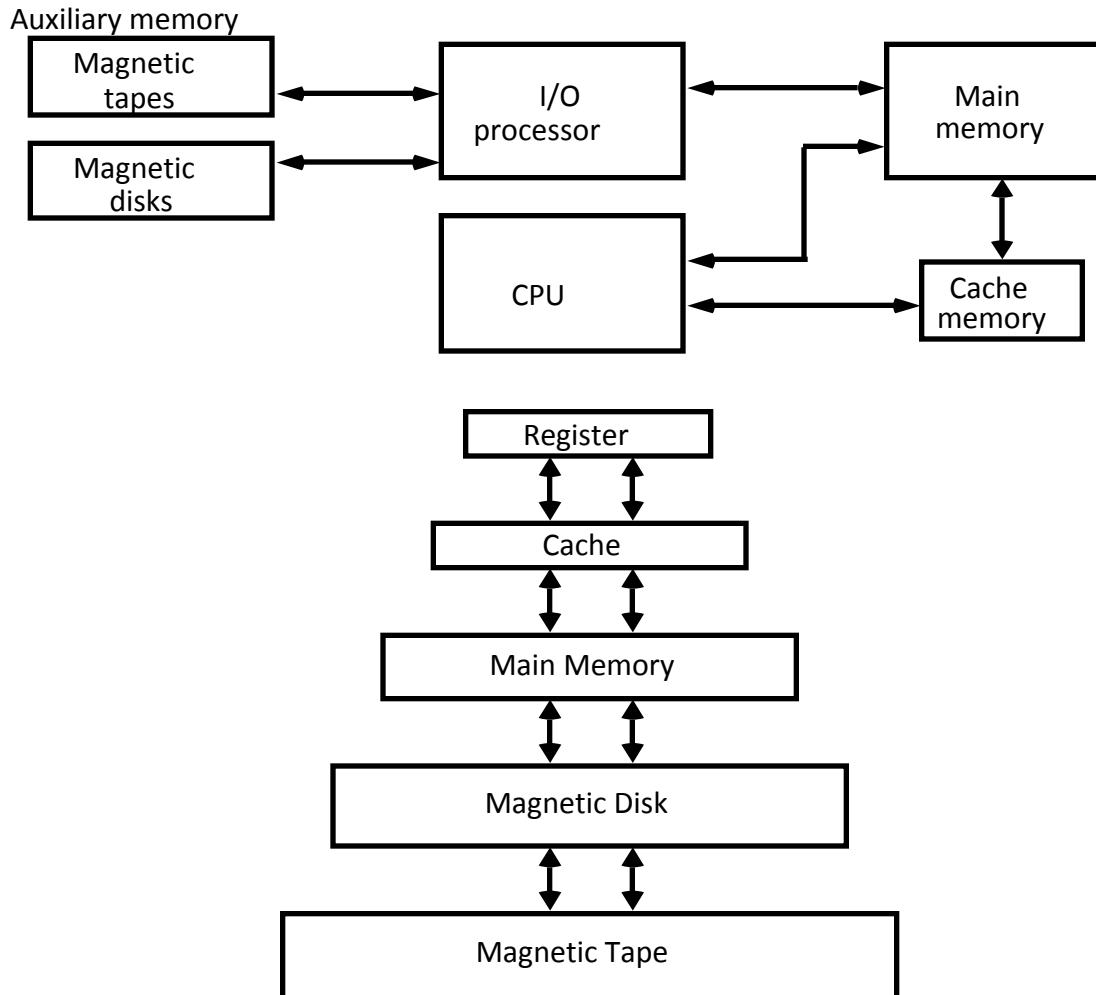


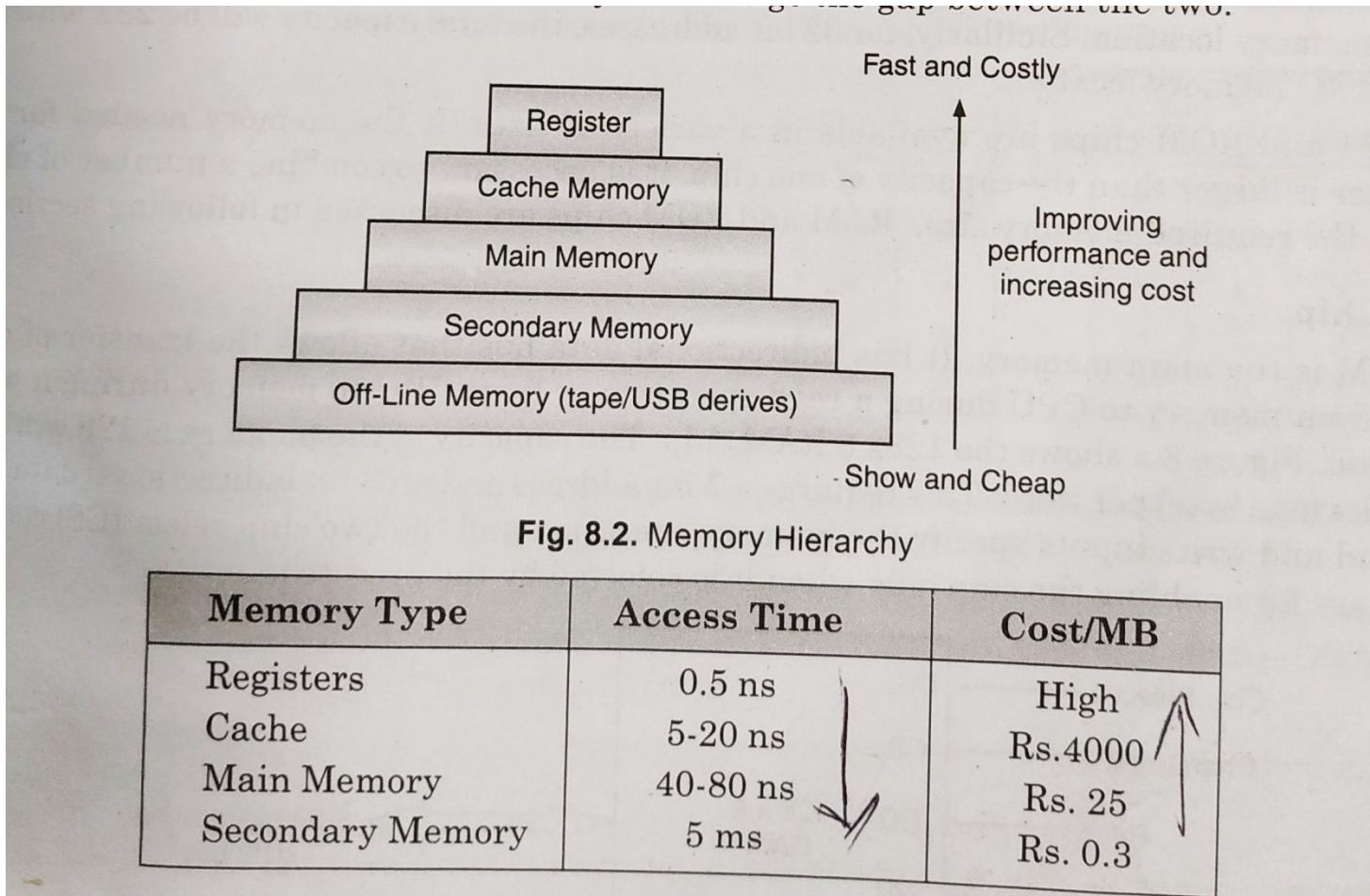
Fig. 8.1. Types of Memory

MEMORY HIERARCHY

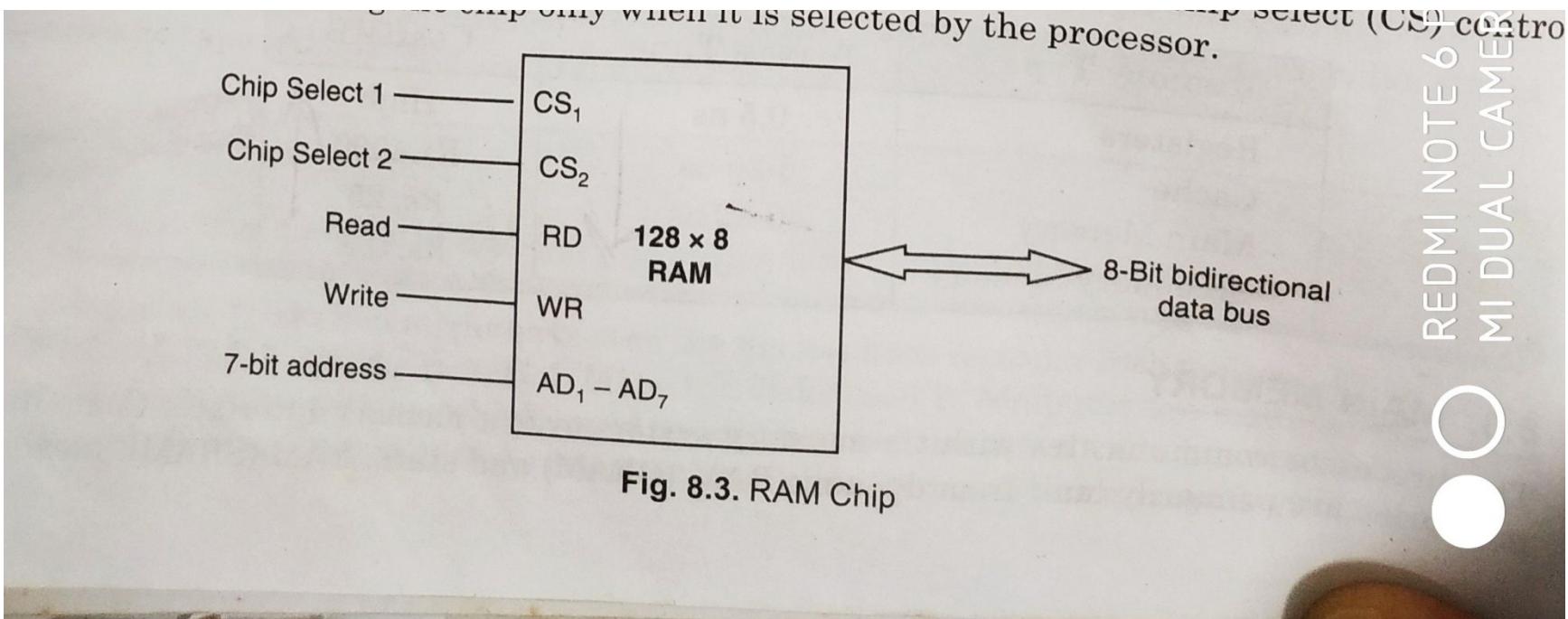
Memory Hierarchy is to obtain the highest possible access speed while minimizing the total cost of the memory system



THE MEMORY HIERARCHY



RAM CHIPS



FUNCTIONAL TABLE OF RAM

Table 8.1. Functional Table

CS₁	CS₂	RD	WR	Memory Operation	State of Data Bus
0	0	×	×	No Operation	High Impedance
0	1	×	×	No Operation	High Impedance
1	0	0	0	No Operation	High Impedance
1	0	0	1	Write Operation	Input Data to RAM
1	0	1	×	Read Operation	Output Data from RAM
1	1	×	×	No Operation	High Impedance

ROM CHIPS

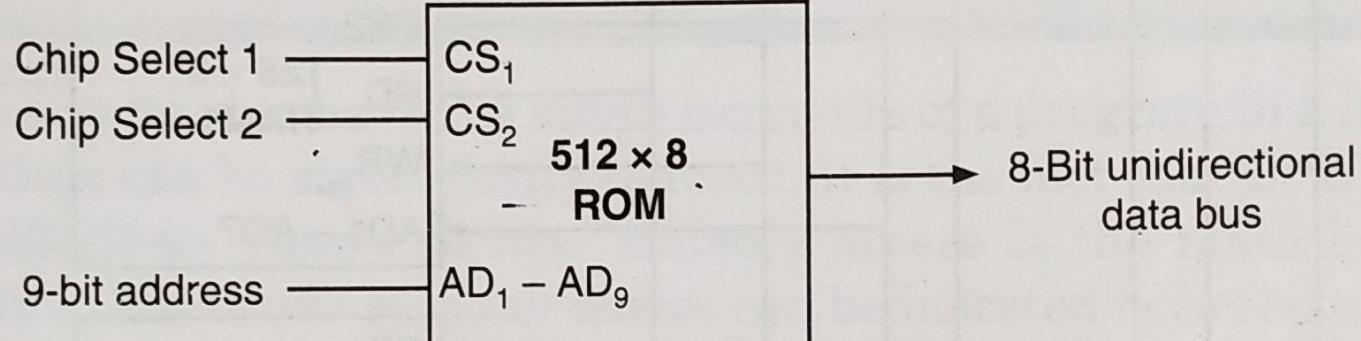


Fig. 8.4. ROM Chip

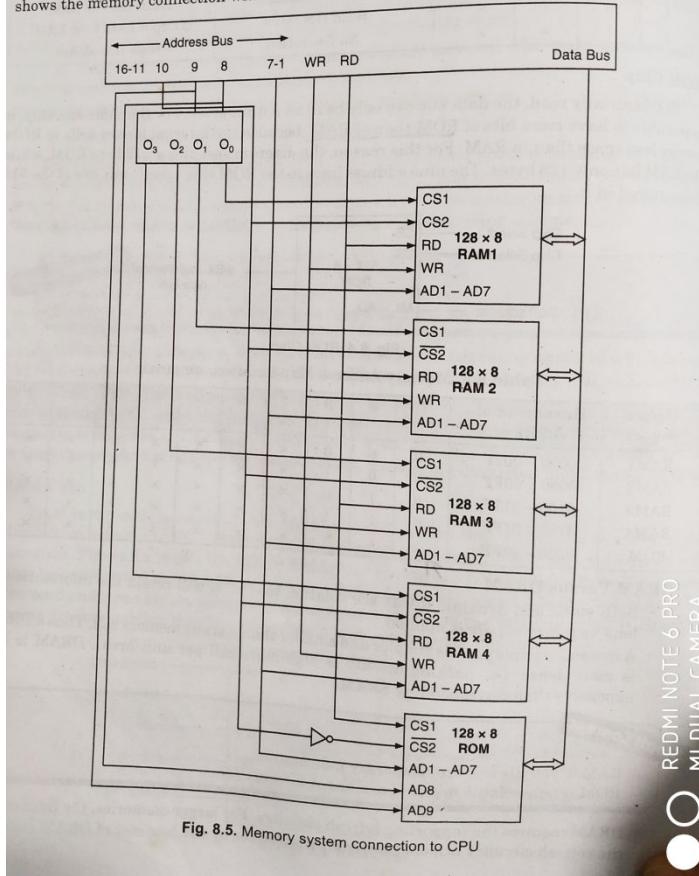
Memory address map of RAM

Table 8.2. Memory Address Map for Microcomputer

Memory connection to CPU

Memory Connection to CPU

The Memory system consists of all storage devices employed in a computer system from the slow but high-capacity secondary memory to a relatively faster main memory. Fig. 8.5 shows the memory connection with CPU.



SRAM VS DRAM

SRAM Versus DRAM :

- Both static and dynamic RAMs are volatile, that is, it will retain the information as long as power supply is applied.
- A dynamic memory cell is simpler and smaller than a static memory cell. Thus a DRAM is more dense, *i.e.*, packing density is high(more cell per unit area). DRAM is less expensive than corresponding SRAM.

Small Concept

- RAM is volatile to store temporary information.
- ROM is non-volatile to store permanent information.

- DRAM requires the supporting refresh circuitry. For larger memories, the fixed cost of the refresh circuitry is more than compensated for by the less cost of DRAM cells

CACHE MEMORY

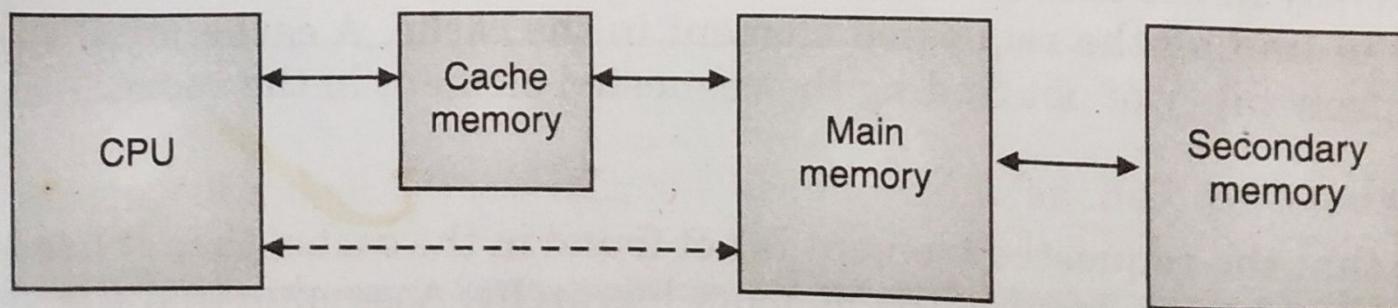


Fig. 8.6. Cache memory between CPU and the main memory

MEMORY INTERLEAVING

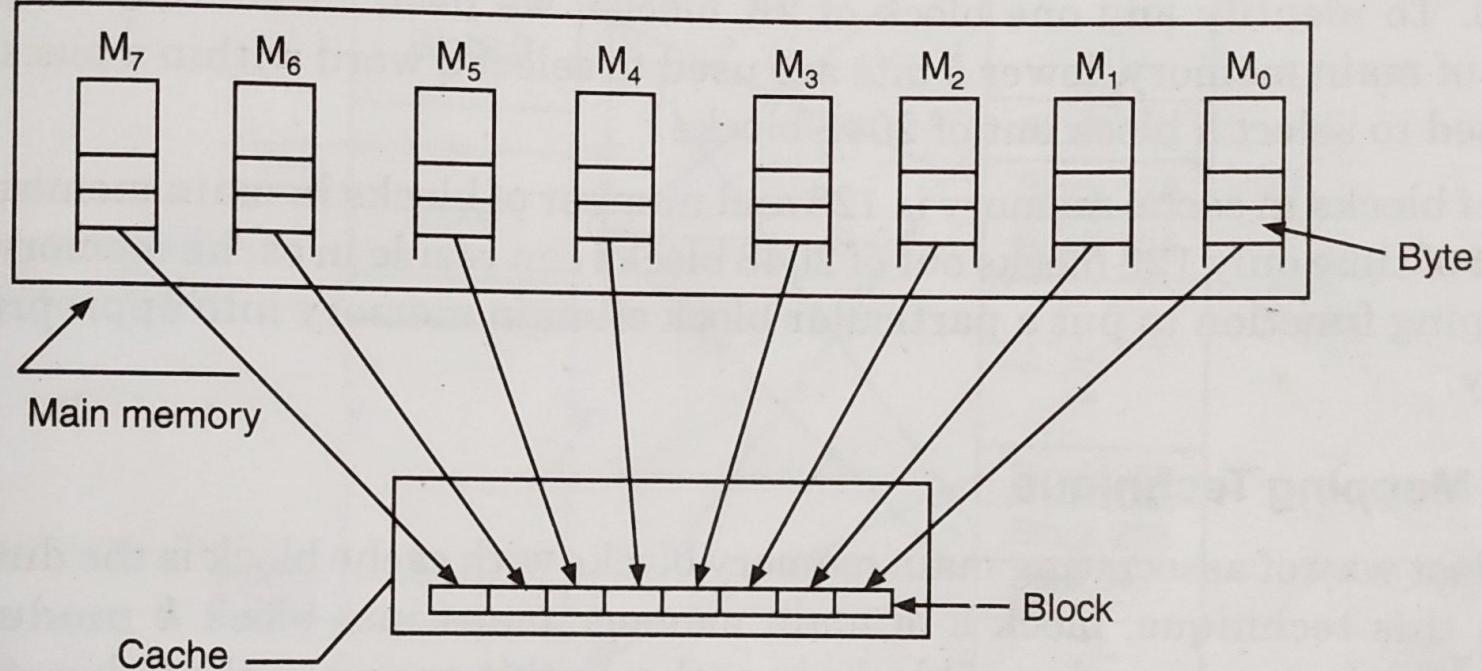


Fig. 8.7. Memory interleaving using eight modules

CACHE MAPPING FUNCTION

8.5. CACHE-MAPPING FUNCTIONS

The mapping functions are used to map a particular block of main memory to a particular block of cache. This mapping function is used to transfer the block from main memory to cache memory. Three different mapping functions are available:

- **Direct mapping:** A particular block of main memory can be brought to a particular block of cache memory. So, it is not flexible.
- **Associative mapping:** In this mapping function, any block of Main memory can potentially reside in any cache block position. This is much more flexible mapping method.
- **Block-set-associative mapping:** In this method, blocks of cache are grouped into sets, and the mapping allows a block of main memory to reside in any block of a specific set. From the flexibility point of view, it is in between to the other two methods.

DIRECT MAPPING

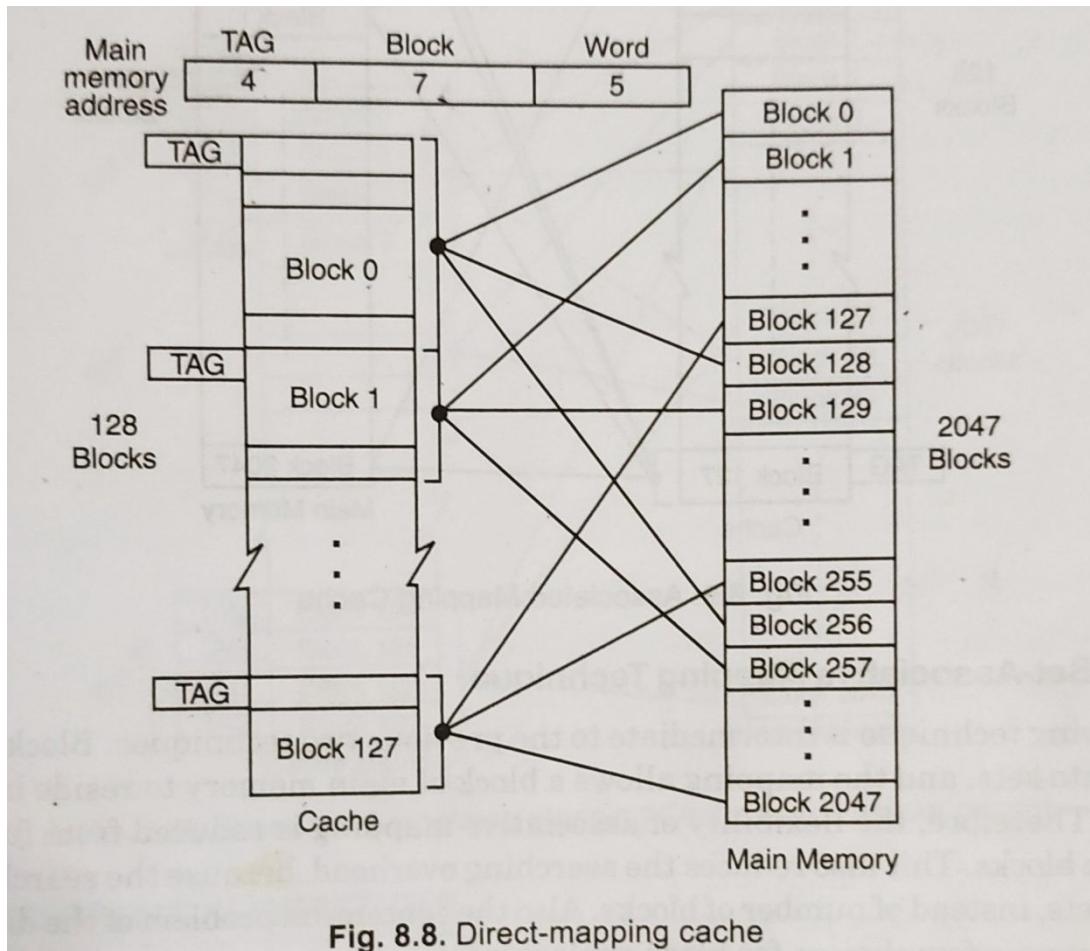
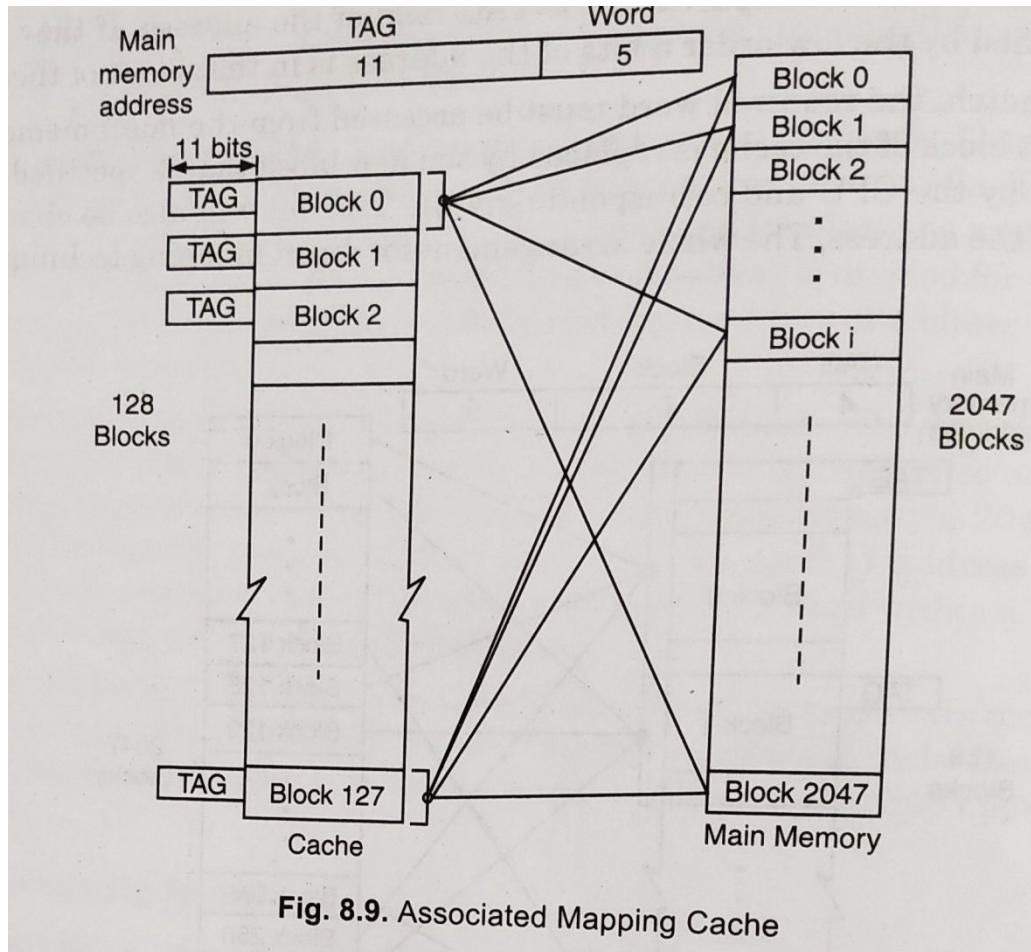


Fig. 8.8. Direct-mapping cache

ASSOSIATIVE MAPPING



BLOCK SET ASSOCIATIVE MAPPING

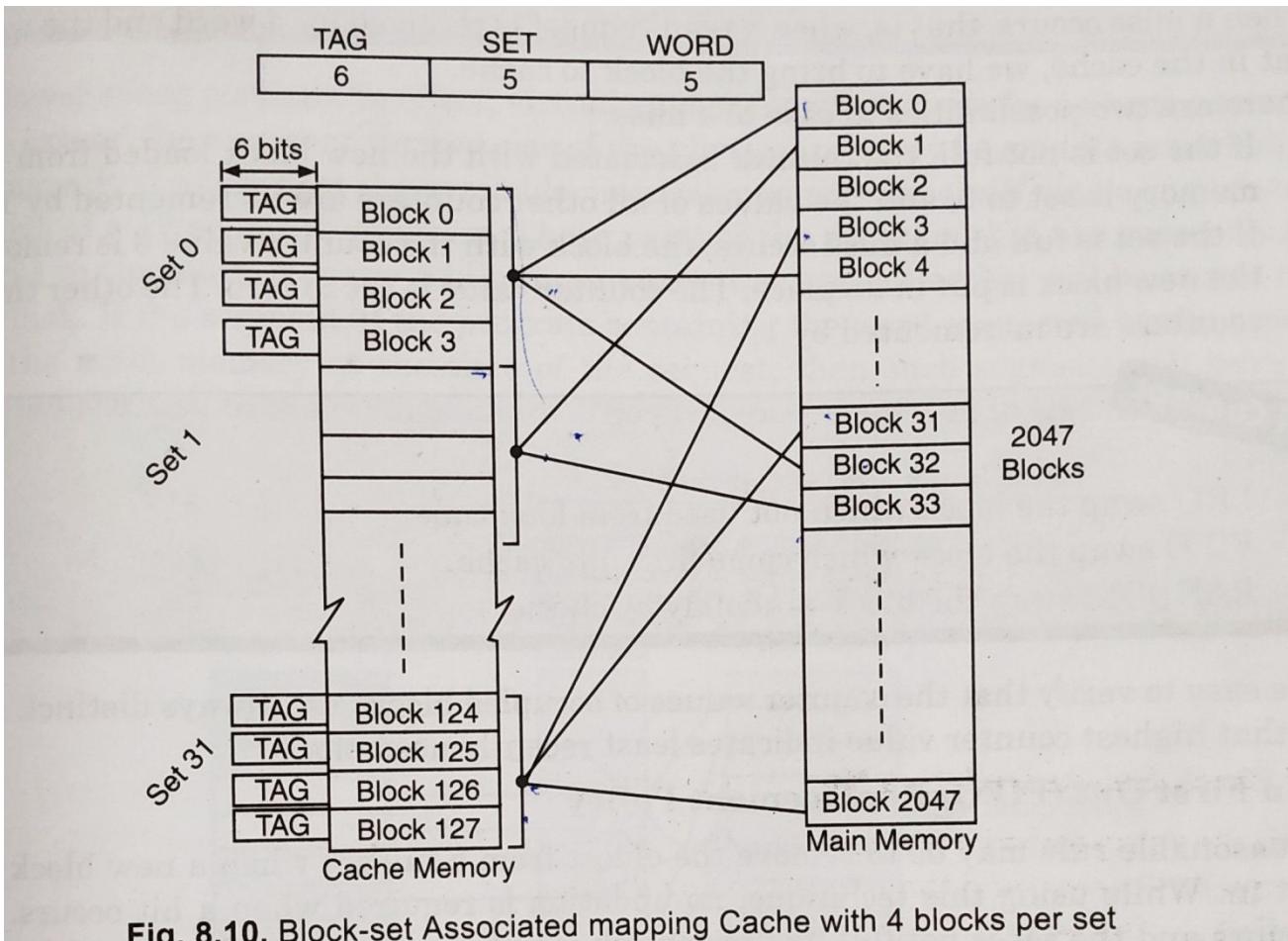
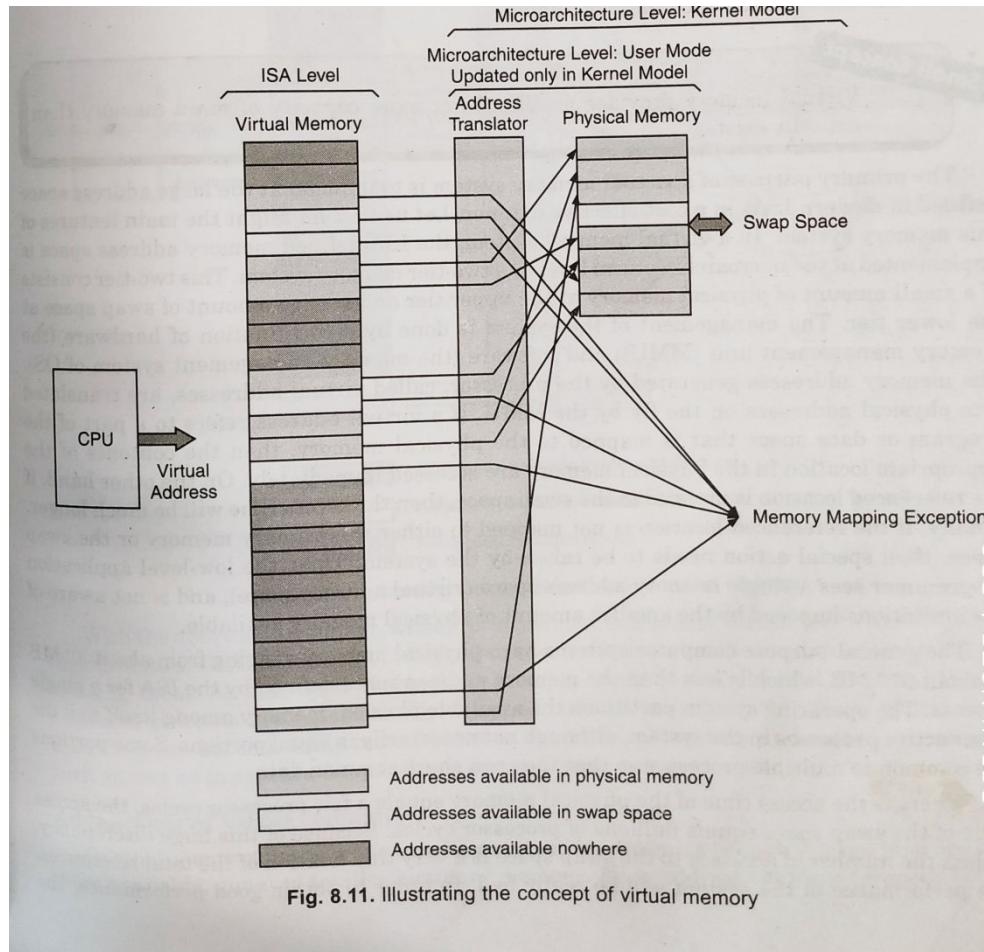


Fig. 8.10. Block-set Associated mapping Cache with 4 blocks per set

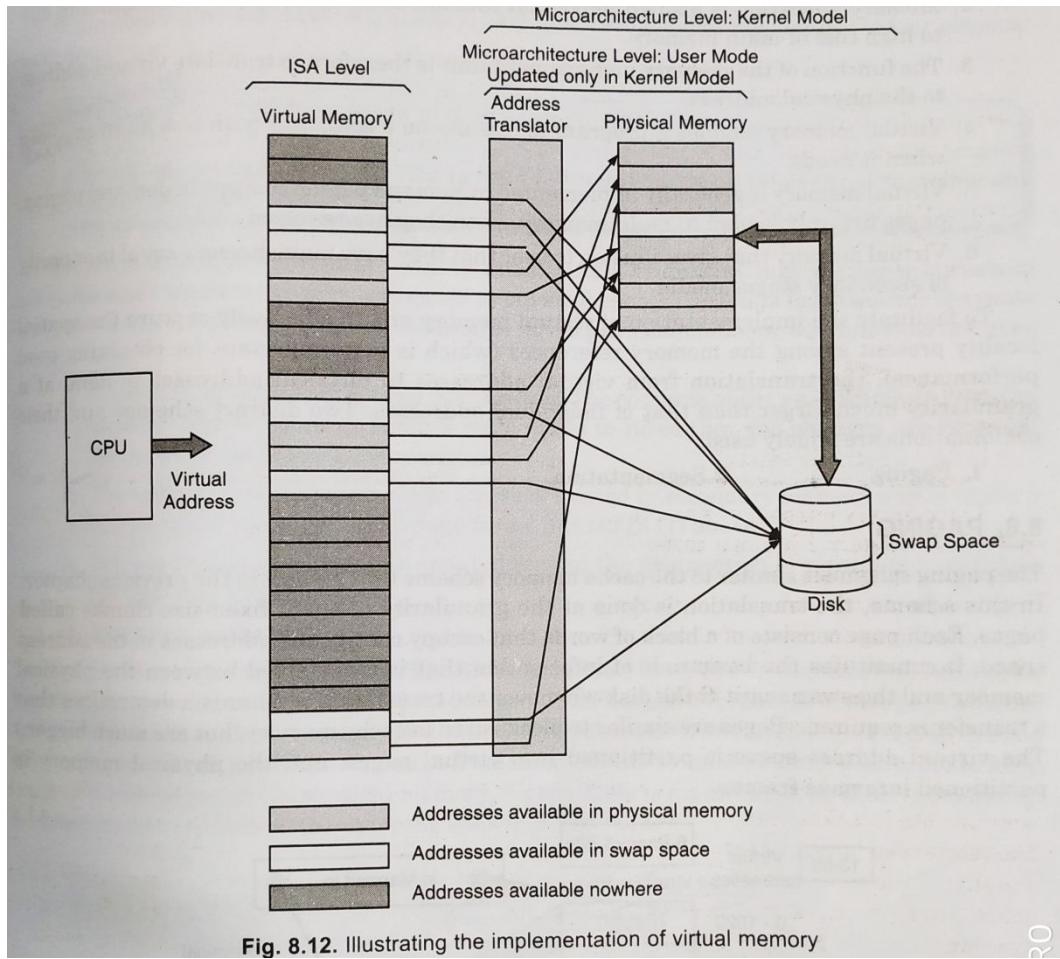
REPLACEMENT ALGORITHM

- LRU replacement policy
- FIFO replacement policy
- Random replacement policy

VIRTUAL MEMORY



VIRTUAL MEMORY



PAGEING

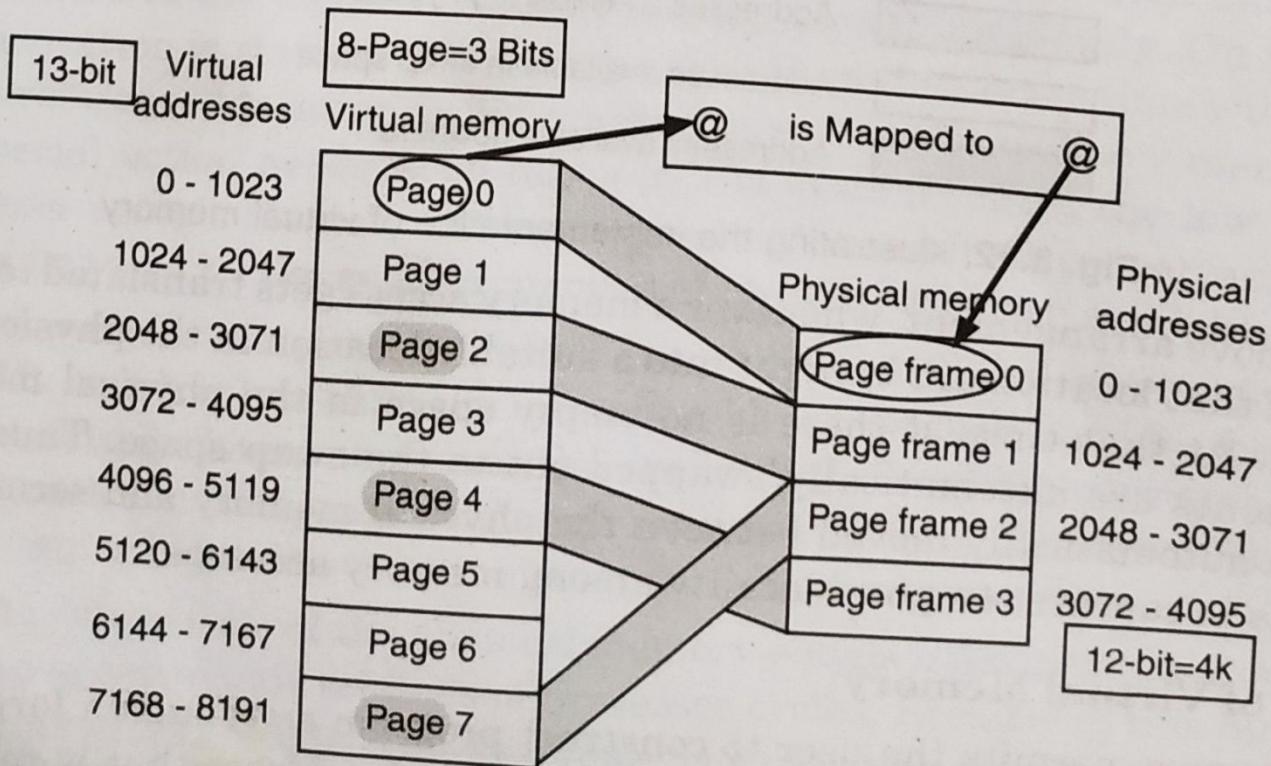
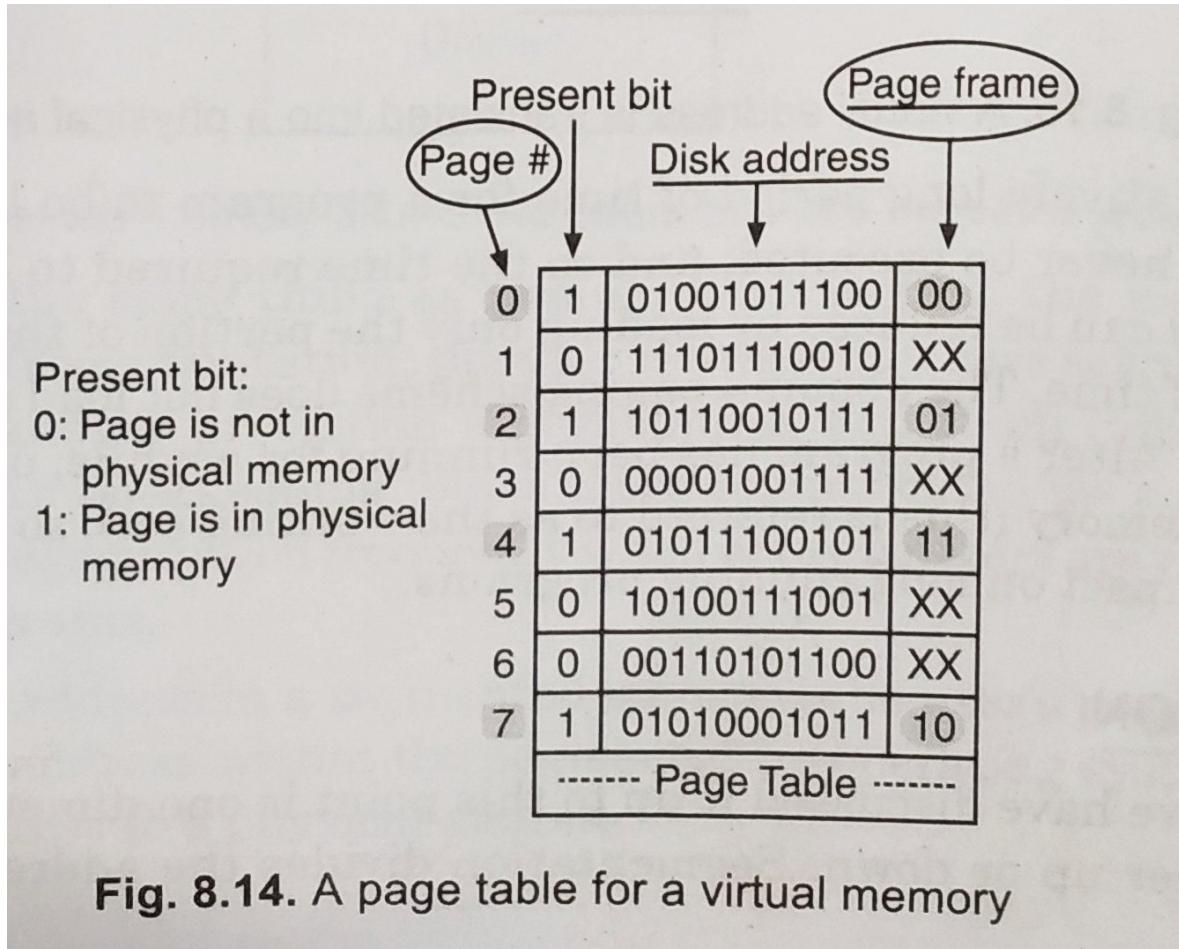
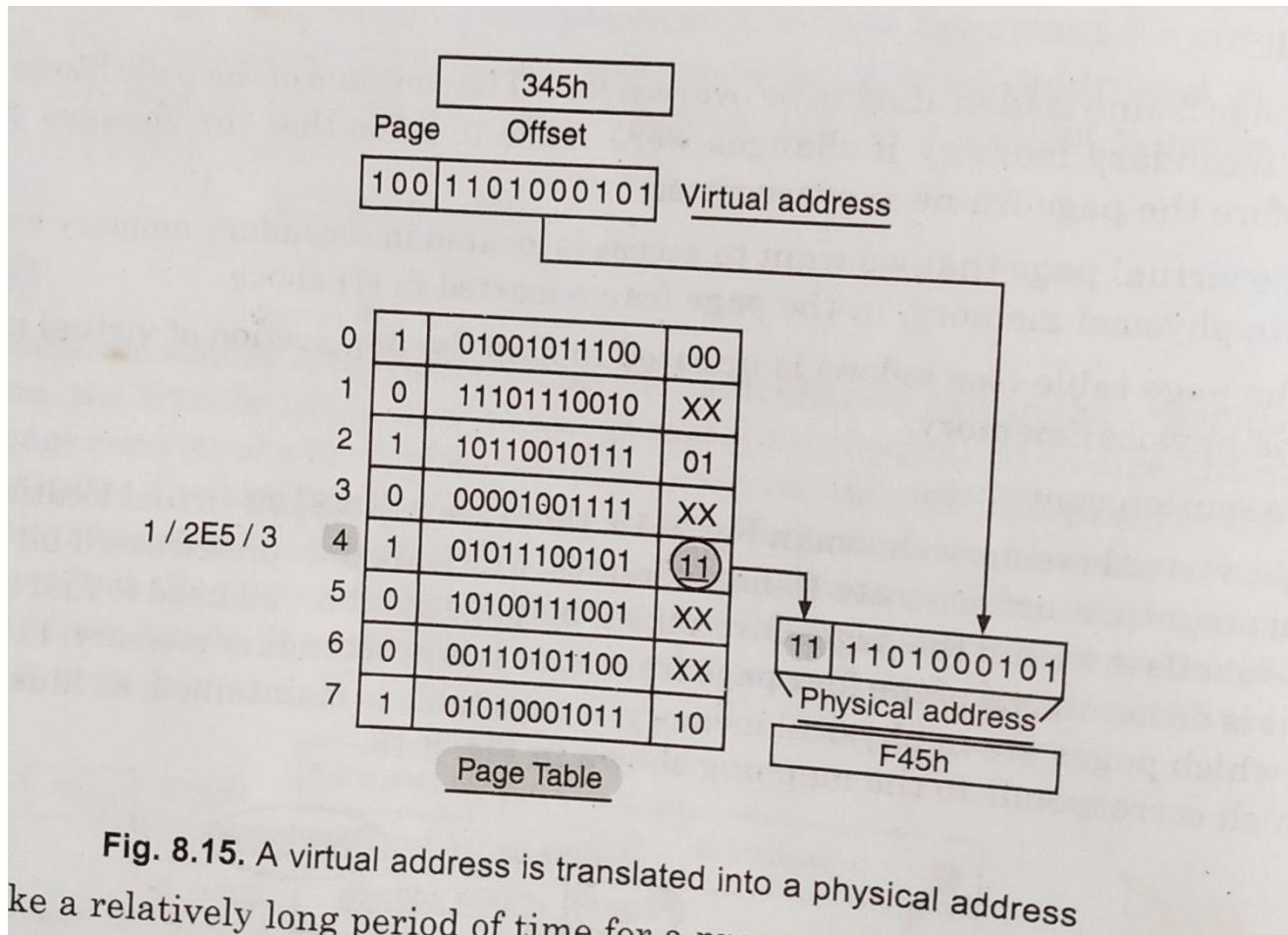


Fig. 8.13. A mapping between a virtual and a physical memory.

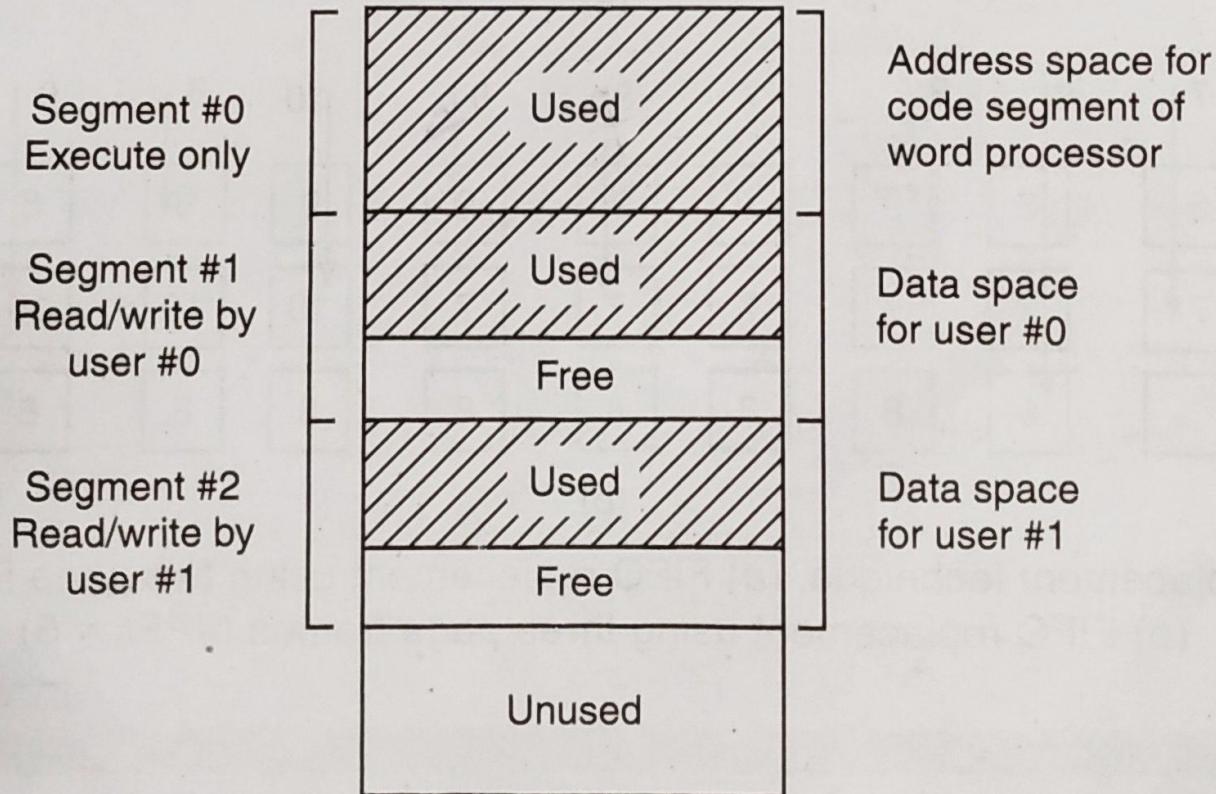
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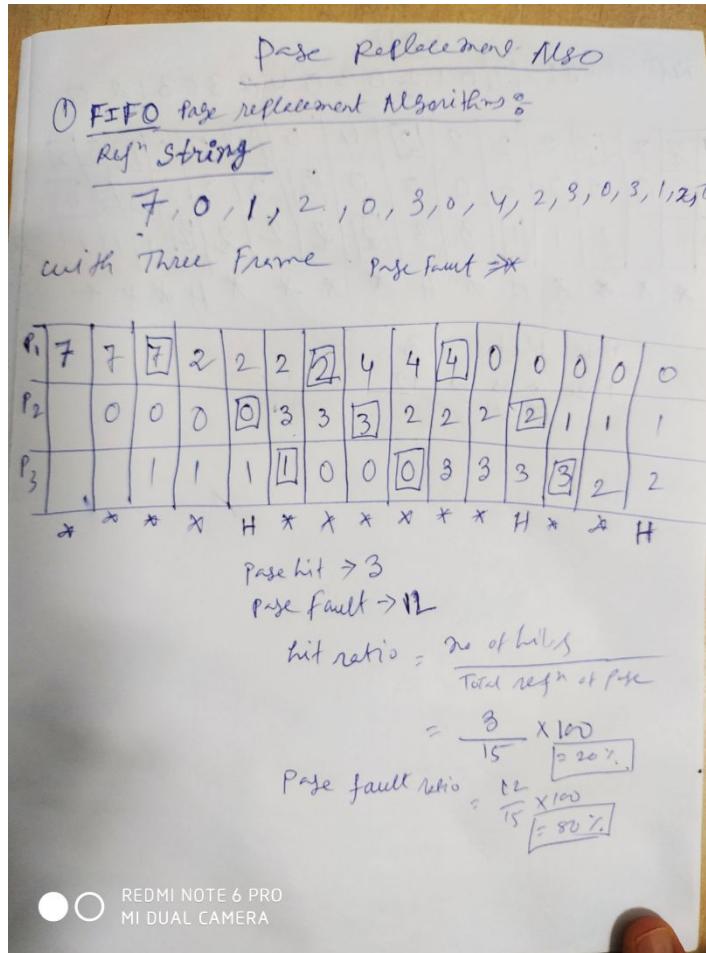
SEGMENTATION



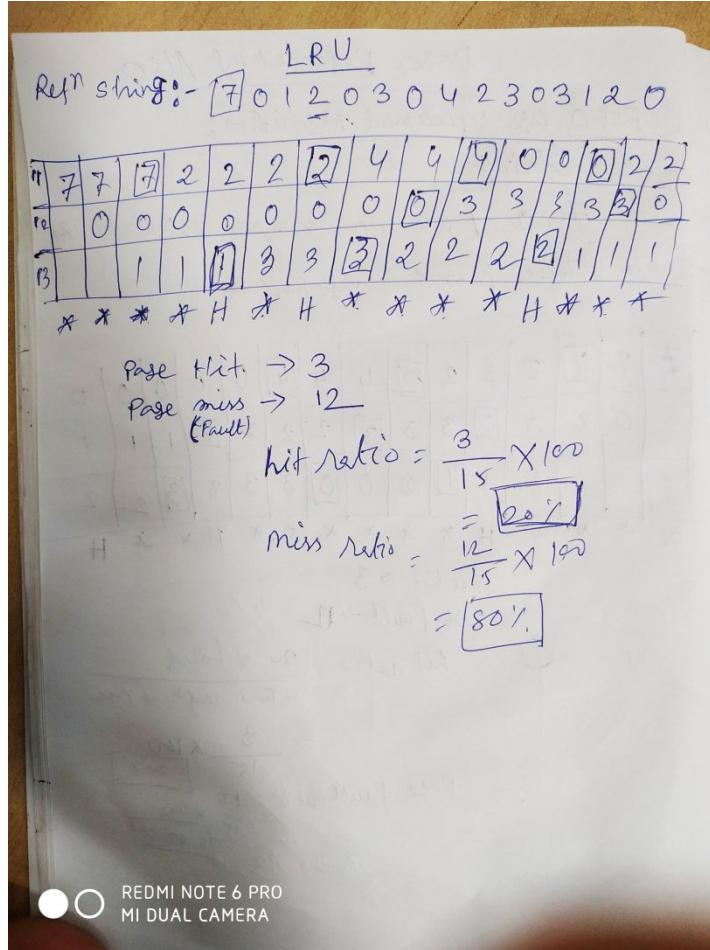
g. 8.16. A segmented memory allows two users to share the same word processor

PAGE REPLACEMENT ALGORITHMS

FIFO



LEAST RECENT USED ALGORITHMS



PROBLEMS

SOLVED PROBLEMS

- 8.1 ✓ (i) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?
- (ii) How many lines of the address bus must be used to access 2048 bytes of memory?
How many of these lines will be common to all chips?
- (iii) How many lines must be decoded for chip select? Specify the size of the decoders.

Ans. (i) Memory capacity = 2048 bytes

$$2^{11} = 2048 \text{ bytes}$$

$$2^7 = 128$$

$$2^4 = \underline{16 \text{ chips RAM}}$$

(ii) Memory capacity = 2048 bytes

$$\text{address bus} = 11(2^{11} = 2048)$$

$$128 = 2^7$$

= 7 lines to address each chip and 4 lines to decoder for selecting 16 chips. Thus, 7 lines out of 11 will be common to all chips.

(iii) Remaining 4 lines must be decoded for chip select the size of decoder is 4×16 .

PROBLEMS

8.2. How many ROM chips are required to produce a memory capacity of 4000 bytes? How many address lines are required to access the 4000 bytes? How many of these addresses will be common to all these chips?

Ans. $4000 \text{ bytes} = 4K \text{ bytes} = 2^2 \times 2^{10} \text{ bytes} = 2^{12} \text{ bytes}$.

ROM size = 256 byte = 2^8 byte

$$\text{No. of ROM chip req.} = \frac{2^{12}}{2^8} = 2^4 = 16$$

No. of add. Lines required to access 4 K bytes = 12.

256 No. of addresses will be common to all these chips.

8.3. For the following memory units (specified by the number of words the number of bits per word), determine the number of address lines, input/output lines and the number of bytes that can be stored in the specified memory

(i) $64K \times 8$

(ii) $16M \times 32$

(iii) $4G \times 64$

(iv) $2K \times 16$

Ans. (i) $64K \times 8$

i/p, o/p lines = 8

Address lines = 16

Mem = 64K

PROBLEMS

(ii) $16M \times 32$

i/p, o/p lines = 32

Add = 24

Mem = $64M (16M \times 4)$

(iii) $4G \times 64$

i/p, o/p lines = 64

Add = 32

Mem = $32GB (4G \times 8)$

(iv) $2K \times 16$

i/p, o/p = 16

Add = 11

Mem = 4K