AASHREY PATEL
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Education

Degree	Institution	CPI/%	Year
MTech	IIT Gandhinagar	8.46	2023-Present
BE	Vishwakarma Government Engineering College	8.62	2019 - 2023
Class XII	Shree Swaminarayan Public School, Gandhinagar	87.2	2018 - 2019
Class X	Shree Swaminarayan Public School, Gandhinagar	91.2	2016 - 2017

Internships

- **Postgraduate Researcher, NanoDC Lab IITGN** **[Dec'2024-Present]**
  - Designed RRAM Based Compressors and Multiplier for Approximate Computing for CNN workloads.
  - Chip Tapeout in 65nm UMC CMOS Technology – Role - Chip testing, Removing DRCs, RTL2GDSII flow. Functional testing of five stage RISC V Processor. Made it Radiation Hardened using TMR logic. Custom Layout for memory controller and its post layout simulations and PVT variations for final implementation on chip.

- **Research Intern, Radar Controller Application using RISC V Shakti Processor, Space Application Centre ISRO [Jan-May 2023]**
  - Role is to understand on RISC V architecture, Shakti Processor and add radar controller module to the SoC using AXI Interface and Interconnect.
  - Part of the team under the division, Microelectronics and Sensors Development.
    Learnings - Bluespec compiler, SoC Design, AXI Interconnect
    This project of RISC V processor will be used in ongoing and further ASIC chip development by ISRO. In this project I am able to do FPGA prototyping, write C applications to test various functionality like GPIO, UART, SPI etc.

Projects

- **Image Processing in Hardware**
  - Done Image Smoothing, Sharpening, Blending and Normalization in FPGA.
  - Developed 3 stage pipelined methodology for processing the image.
- **Approximate Computing using CMOS and RRAM Devices**
  - Hybrid Multiplier design using Exact and Approximate compressors for CNN applications
  - Memristor Ratioed Logic (MRL) design of Approximate compressors for power efficient applications
- **DLX processor design**
  - 3-stage pipelined processor design in Verilog
  - Fully synthesizable and implemented on FPGA.
- **In-Memory Computing using 6T and 8T SRAM**
  - Layout of 128x128 6T SRAM array with compute cells
  - Logic operations and muti-bit multiplication in SRAM array and its Monte Carlo Simulations.
- **Analog Differential Amplifier and OTA Design**
  - Specifications – Gain, output swing, ICMR, power budget and CMRR
- **Decoder design for Memory Access**
  - Calculated Logical Effort, Path Effort and Stage Effort of 4x16 Decoder for 128x128 array.
  - Best number of stages required to minimize total delay.
- **Indoor Navigation with shortest path algorithm**
  - **Utility of Project :-** Useful to our college students to find fastest and shortest path in the campus.
    - Contains website that navigate us to desired location.
    - Gives location with accuracy.
    - User Interactive.

Positions of Responsibility

- **Teaching Assistant, Indian Institute of Technology Gandhinagar** **[July'2023-Present]**
  - **Courses**: Digital Systems, Analog Circuits, Academic duty
  - **Instructors:** Dr. Joycee Mekie, Dr. Tarun Agrawal
- **Member of Odyssey Astronomy Club, IIT Gandhinagar** **[July'2023-Present]**
  - Active team participation and helping organizing team for the events.
- **Member of (National service scheme) NSS team** **[June'2019-July'2020]**
  - Part of the several social awareness events like ocean cleaning, paper bag distribution, helping needy people.
  - Treasurer in the college for NSS events.

Achievements

- Two times GATE Qualified with best **AIR 603**. MTech offers from IIT Kharagpur, IIT Hyderabad, IIT Bhubaneswar.
- Got college level recognition for our Indoor Navigation Project.

Skill Summary

- **Languages:** Verilog, C, C++, Python
- **Tools:** Cadence Virtuoso, Calibre, Genus, Innovus, Xilinx Vivado, Vitis, MIT Timeloop, Docker
- **Soft Skills:** Team work and Team management, learning by observing the Nature