Map Report

Sun Dec 11 14:40:32 2016

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Release 14.2 Map P.28xd (nt64)
Xilinx Mapping Report File for Design 'SW_top'
Design Information
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Command Line   : map -intstyle ise -p xc7z020-clg484-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -mt off -ir off -pr off -lc off
-power off -o SW_top_map.ncd SW_top.ngd SW_top.pcf
Target Device  : xc7z020
Target Package : clg484
Target Speed   : -3
Mapper Version : zynq -- $Revision: 1.55 $
Mapped Date    : Sun Dec 11 14:30:59 2016
Design Summary
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Number of errors:      0
Number of warnings:   90
Slice Logic Utilization:
  Number of Slice Registers:                   855 out of 106,400    1%
    Number used as Flip Flops:                 855
    Number used as Latches:                      0
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                0
  Number of Slice LUTs:                     21,367 out of  53,200   40%
    Number used as logic:                   20,848 out of  53,200   39%
      Number using O6 output only:          10,936
      Number using O5 output only:             220
      Number using O5 and O6:                9,692
      Number used as ROM:                        0
    Number used as Memory:                       0 out of  17,400    0%
    Number used exclusively as route-thrus:    519
      Number with same-slice register load:      0
      Number with same-slice carry load:       519
      Number with other load:                    0
Slice Logic Distribution:
  Number of occupied Slices:                 8,293 out of  13,300   62%
  Number of LUT Flip Flop pairs used:       21,517
    Number with an unused Flip Flop:        20,719 out of  21,517   96%
    Number with an unused LUT:                 150 out of  21,517    1%
    Number of fully used LUT-FF pairs:         648 out of  21,517    3%
    Number of unique control sets:              19
    Number of slice register sites lost
      to control set restrictions:              97 out of 106,400    1%
  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.
  OVERMAPPING of BRAM resources should be ignored if the design is
  over-mapped for a non-BRAM resource or if placement fails.
IO Utilization:
  Number of bonded IOBs:                        88 out of     200   44%
Specific Feature Utilization:
  Number of RAMB36E1/FIFO36E1s:                  0 out of     140    0%
  Number of RAMB18E1/FIFO18E1s:                  0 out of     280    0%
  Number of BUFG/BUFGCTRLs:                      2 out of      32    6%
    Number used as BUFGs:                        2
    Number used as BUFGCTRLs:                    0
  Number of IDELAYE2/IDELAYE2_FINEDELAYs:        0 out of     200    0%
  Number of ILOGICE2/ILOGICE3/ISERDESE2s:        0 out of     200    0%
  Number of ODELAYE2/ODELAYE2_FINEDELAYs:        0
  Number of OLOGICE2/OLOGICE3/OSERDESE2s:        0 out of     200    0%
  Number of PHASER_IN/PHASER_IN_PHYs:            0 out of      16    0%
  Number of PHASER_OUT/PHASER_OUT_PHYs:          0 out of      16    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHCEs:                             0 out of      72    0%
  Number of BUFRs:                               0 out of      16    0%
  Number of CAPTUREs:                            0 out of       1    0%
  Number of DNA_PORTs:                           0 out of       1    0%
  Number of DSP48E1s:                            0 out of     220    0%
  Number of EFUSE_USRs:                          0 out of       1    0%
  Number of FRAME_ECCs:                          0 out of       1    0%
  Number of ICAPs:                               0 out of       2    0%
  Number of IDELAYCTRLs:                         0 out of       4    0%
  Number of IN_FIFOs:                            0 out of      16    0%
  Number of MMCME2_ADVs:                         0 out of       4    0%
  Number of OUT_FIFOs:                           0 out of      16    0%
  Number of PHASER_REFs:                         0 out of       4    0%
  Number of PHY_CONTROLs:                        0 out of       4    0%
  Number of PLLE2_ADVs:                          0 out of       4    0%
  Number of PS7s:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of XADCs:                               0 out of       1    0%
Average Fanout of Non-Clock Nets:                2.88
Peak Memory Usage:  1070 MB
Total REAL time to MAP completion:  2 mins 36 secs
Total CPU time to MAP completion:   2 mins 6 secs
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Section 1 - Errors
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Section 2 - Warnings
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WARNING:LIT:701 - PAD symbol "clk" has an undefined IOSTANDARD.
WARNING:LIT:702 - PAD symbol "clk" is not constrained (LOC) to a specific
   location.
WARNING:PhysDesignRules:2452 - The IOB VGA_R<0> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_R<3> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_R<1> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_R<2> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB reset is either not constrained (LOC) to
   a specific location and/or has an undefined I/O Standard (IOSTANDARD). This
   condition may seriously affect the device and will be an error in bitstream
   creation. It should be corrected by properly specifying the pin location and
   I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<26> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<25> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<28> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<27> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<29> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<20> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<22> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<21> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<24> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<23> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<16> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<15> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<18> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
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   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<17> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<19> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<10> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<12> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<11> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<14> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<13> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<0> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<1> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<2> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<3> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<4> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<5> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<6> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB index<7> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_B<0> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_B<3> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_B<1> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_B<2> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_G<0> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
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   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_G<3> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_G<1> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_G<2> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<4> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<3> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<2> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<1> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<0> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<9> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<8> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<7> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<6> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_HS is either not constrained (LOC) to
   a specific location and/or has an undefined I/O Standard (IOSTANDARD). This
   condition may seriously affect the device and will be an error in bitstream
   creation. It should be corrected by properly specifying the pin location and
   I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq1<5> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB start_scoreboard is either not
   constrained (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB VGA_VS is either not constrained (LOC) to
   a specific location and/or has an undefined I/O Standard (IOSTANDARD). This
   condition may seriously affect the device and will be an error in bitstream
   creation. It should be corrected by properly specifying the pin location and
   I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<26> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<25> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<28> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<27> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
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   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<29> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<20> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<22> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<21> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<24> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<23> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<16> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<15> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB indexing_done is either not constrained
   (LOC) to a specific location and/or has an undefined I/O Standard
   (IOSTANDARD). This condition may seriously affect the device and will be an
   error in bitstream creation. It should be corrected by properly specifying
   the pin location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<18> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<17> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<19> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<10> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<12> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<11> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<14> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<13> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB clk is either not constrained (LOC) to a
   specific location and/or has an undefined I/O Standard (IOSTANDARD). This
   condition may seriously affect the device and will be an error in bitstream
   creation. It should be corrected by properly specifying the pin location and
   I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB button is either not constrained (LOC) to
   a specific location and/or has an undefined I/O Standard (IOSTANDARD). This
   condition may seriously affect the device and will be an error in bitstream
   creation. It should be corrected by properly specifying the pin location and
   I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<4> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
```

```
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<3> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<2> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<1> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<0> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB SW_done is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<9> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<8> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<7> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<6> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
WARNING:PhysDesignRules:2452 - The IOB seq2<5> is either not constrained (LOC)
   to a specific location and/or has an undefined I/O Standard (IOSTANDARD).
   This condition may seriously affect the device and will be an error in
   bitstream creation. It should be corrected by properly specifying the pin
   location and I/O Standard.
Section 3 - Informational
-------------------------
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to
   1.050 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.
Section 4 - Removed Logic Summary
---------------------------------
   4 block(s) optimized away
Section 5 - Removed Logic
-------------------------
Optimized Block(s):
TYPE            BLOCK
GND             M1/XST_GND
VCC             M1/XST_VCC
GND             XST_GND
VCC             XST_VCC
To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.
Section 6 - IOB Properties
--------------------------
```

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Slew Rate	Reg (s)	Resist
SW_done	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_B<0>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_B<1>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_B<2>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_B<3>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_G<0>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_G<1>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_G<2>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_G<3>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_HS	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_R<0>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_R<1>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_R<2>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_R<3>	IOB	OUTPUT	LVCMOS18		12	SLOW		
VGA_VS	IOB	OUTPUT	LVCMOS18		12	SLOW		
button	IOB	INPUT	LVCMOS18					
clk	IOB	INPUT	LVCMOS18					

index<0>	IOB	INPUT	LVCMOS18					
index<1>	IOB	INPUT	LVCMOS18					
index<2>	IOB	INPUT	LVCMOS18					
index<3>	IOB	INPUT	LVCMOS18					
index<4>	IOB	INPUT	LVCMOS18					
index<5>	IOB	INPUT	LVCMOS18					
index<6>	IOB	INPUT	LVCMOS18					
index<7>	IOB	INPUT	LVCMOS18					
indexing_done	IOB	INPUT	LVCMOS18					
reset	IOB	INPUT	LVCMOS18					
seq1<0>	IOB	INPUT	LVCMOS18					
seq1<1>	IOB	INPUT	LVCMOS18					
seq1<2>	IOB	INPUT	LVCMOS18					
seq1<3>	IOB	INPUT	LVCMOS18					
seq1<4>	IOB	INPUT	LVCMOS18					
seq1<5>	IOB	INPUT	LVCMOS18					
seq1<6>	IOB	INPUT	LVCMOS18					
seq1<7>	IOB	INPUT	LVCMOS18					
seq1<8>	IOB	INPUT	LVCMOS18					
seq1<9>	IOB	INPUT	LVCMOS18					
seq1<10>	IOB	INPUT	LVCMOS18					
seq1<11>	IOB	INPUT	LVCMOS18					
seq1<12>	IOB	INPUT	LVCMOS18					
seq1<13>	IOB	INPUT	LVCMOS18					
seq1<14>	IOB	INPUT	LVCMOS18					
seq1<15>	IOB	INPUT	LVCMOS18					
seq1<16>	IOB	INPUT	LVCMOS18					
seq1<17>	IOB	INPUT	LVCMOS18					
seq1<18>	IOB	INPUT	LVCMOS18					
seq1<19>	IOB	INPUT	LVCMOS18					
seq1<20>	IOB	INPUT	LVCMOS18					
seq1<21>	IOB	INPUT	LVCMOS18					
seq1<22>	IOB	INPUT	LVCMOS18					
seq1<23>	IOB	INPUT	LVCMOS18					
seq1<24>	IOB	INPUT	LVCMOS18					
seq1<25>	IOB	INPUT	LVCMOS18					
seq1<26>	IOB	INPUT	LVCMOS18					
seq1<27>	IOB	INPUT	LVCMOS18					
seq1<28>	IOB	INPUT	LVCMOS18					
seq1<29>	IOB	INPUT	LVCMOS18					
seq2<0>	IOB	INPUT	LVCMOS18					
seq2<1>	IOB	INPUT	LVCMOS18					
seq2<2>	IOB	INPUT	LVCMOS18					
seq2<3>	IOB	INPUT	LVCMOS18					
seq2<4>	IOB	INPUT	LVCMOS18					
seq2<5>	IOB	INPUT	LVCMOS18					
seq2<6>	IOB	INPUT	LVCMOS18					
seq2<7>	IOB	INPUT	LVCMOS18					
seq2<8>	IOB	INPUT	LVCMOS18					
seq2<9>	IOB	INPUT	LVCMOS18					
seq2<10>	IOB	INPUT	LVCMOS18					
seq2<11>	IOB	INPUT	LVCMOS18					
seq2<12>	IOB	INPUT	LVCMOS18					
seq2<13>	IOB	INPUT	LVCMOS18					
seq2<14>	IOB	INPUT	LVCMOS18					
seq2<15>	IOB	INPUT	LVCMOS18					
seq2<16>	IOB	INPUT	LVCMOS18					
seq2<17>	IOB	INPUT	LVCMOS18					
seq2<18>	IOB	INPUT	LVCMOS18					
seq2<19>	IOB	INPUT	LVCMOS18					
seq2<20>	IOB	INPUT	LVCMOS18					
seq2<21>	IOB	INPUT	LVCMOS18					
seq2<22>	IOB	INPUT	LVCMOS18					
seq2<23>	IOB	INPUT	LVCMOS18					
seq2<24>	IOB	INPUT	LVCMOS18					
seq2<25>	IOB	INPUT	LVCMOS18					
seq2<26>	IOB	INPUT	LVCMOS18					
seq2<27>	IOB	INPUT	LVCMOS18					
seq2<28>	IOB	INPUT	LVCMOS18					
seq2<29>	IOB	INPUT	LVCMOS18					
start_scoreboard	IOB	INPUT	LVCMOS18					

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

No Partitions were found in this design.

Area Group Information

No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

```
Section 12 - Control Set Information
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Use the "-detail" map option to print out Control Set Information.
Section 13 - Utilization by Hierarchy
------------------------------------
Use the "-detail" map option to print out the Utilization by Hierarchy section.
```