Map Report

Sun Dec 11 15:10:13 2016

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Release 14.2 Map P.28xd (nt64)
Xilinx Mapping Report File for Design 'memory_basepair'
Design Information
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Command Line   : map -intstyle ise -p xc7z020-clg484-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -mt off -ir off -pr off -lc off
-power off -o memory_basepair_map.ncd memory_basepair.ngd memory_basepair.pcf
Target Device  : xc7z020
Target Package : clg484
Target Speed   : -3
Mapper Version : zynq -- $Revision: 1.55 $
Mapped Date    : Sun Dec 11 15:07:42 2016
Interim Summary
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Slice Logic Utilization:
  Number of Slice Registers:                 3,290 out of 106,400    3%
    Number used as Flip Flops:               3,290
    Number used as Latches:                      0
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                0
  Number of Slice LUTs:                     70,995 out of  53,200  133% (OVERMAPPED)
    Number used as logic:                   70,991 out of  53,200  133% (OVERMAPPED)
      Number using O6 output only:          65,564
      Number using O5 output only:             120
      Number using O5 and O6:                5,307
      Number used as ROM:                          0
    Number used as Memory:                       0 out of  17,400    0%
    Number used exclusively as route-thrus:      4
      Number with same-slice register load:      0
      Number with same-slice carry load:         4
      Number with other load:                    0
Slice Logic Distribution:
  Number of LUT Flip Flop pairs used:       71,017
    Number with an unused Flip Flop:        69,281 out of  71,017   97%
    Number with an unused LUT:                  22 out of  71,017    1%
    Number of fully used LUT-FF pairs:       1,714 out of  71,017    2%
    Number of unique control sets:              13
    Number of slice register sites lost
      to control set restrictions:              46 out of 106,400    1%
  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.
  OVERMAPPING of BRAM resources should be ignored if the design is
  over-mapped for a non-BRAM resource or if placement fails.
IO Utilization:
  Number of bonded IOBs:                      144 out of     200   72%
    IOB Latches:                              116
Specific Feature Utilization:
  Number of RAMB36E1/FIFO36E1s:                 0 out of     140    0%
  Number of RAMB18E1/FIFO18E1s:                 0 out of     280    0%
  Number of BUFG/BUFGCTRLs:                     2 out of      32    6%
    Number used as BUFGs:                       2
    Number used as BUFGCTRLs:                   0
  Number of IDELAYE2/IDELAYE2_FINEDELAYs:       0 out of     200    0%
  Number of ILOGICE2/ILOGICE3/ISERDESE2s:     116 out of     200   58%
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    Number used as ILOGICE2s:                   116
  Number used as  ILOGICE3s:                     0
    Number used as ISERDESE2s:                   0
  Number of ODELAYE2/ODELAYE2_FINEDELAYs:        0
  Number of OLOGICE2/OLOGICE3/OSERDESE2s:        0 out of     200    0%
  Number of PHASER_IN/PHASER_IN_PHYs:            0 out of      16    0%
  Number of PHASER_OUT/PHASER_OUT_PHYs:          0 out of      16    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHCEs:                             0 out of      72    0%
  Number of BUFRs:                               0 out of      16    0%
  Number of CAPTUREs:                            0 out of       1    0%
  Number of DNA_PORTs:                           0 out of       1    0%
  Number of DSP48E1s:                            0 out of     220    0%
  Number of EFUSE_USRs:                          0 out of       1    0%
  Number of FRAME_ECCs:                          0 out of       1    0%
  Number of ICAPs:                               0 out of       2    0%
  Number of IDELAYCTRLs:                         0 out of       4    0%
  Number of IN_FIFOs:                            0 out of      16    0%
  Number of MMCME2_ADVs:                         0 out of       4    0%
  Number of OUT_FIFOs:                           0 out of      16    0%
  Number of PHASER_REFs:                         0 out of       4    0%
  Number of PHY_CONTROLs:                        0 out of       4    0%
  Number of PLLE2_ADVs:                          0 out of       4    0%
  Number of PS7s:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of XADCs:                               0 out of       1    0%
Design Summary
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Number of errors   :   3
Number of warnings :   2
Section 1 - Errors
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ERROR:Place:836 - Not enough free sites available for the components of the
   following type(s).
      LUT       Number of Components 141990     Number of Sites 106400
ERROR:Place:375 - The design does not fit in device.
    Total LUT Utilization      : 141990 out of 106400
    LUTs used as Logic         : 141990
    LUTs used as Memory        : 0
    FF Utilization             : 3290 out of 106400
ERROR:Pack:1654 - The timing-driven placement phase encountered an error.
Section 2 - Warnings
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WARNING:LIT:701 - PAD symbol "clk" has an undefined IOSTANDARD.
WARNING:LIT:702 - PAD symbol "clk" is not constrained (LOC) to a specific
   location.
Section 3 - Informational
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INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to
   1.050 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
Section 4 - Removed Logic Summary
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   2 block(s) optimized away
Section 5 - Removed Logic
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Optimized Block(s):
TYPE            BLOCK
GND             XST_GND
VCC             XST_VCC
To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.
Section 12 - Configuration String Details
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Use the "-detail" map option to print out Configuration Strings
Section 13 - Control Set Information
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Use the "-detail" map option to print out Control Set Information.
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