**Map Report**

**Sun Dec 11 14:11:22 2016**

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Release 14.2 Map P.28xd (nt64)
Xilinx Mapping Report File for Design 'DNA_Sequence_Mapping_top'
Design Information
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Command Line   : map -intstyle ise -p xc7z020-clg484-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -mt off -ir off -pr off -lc off
-power off -o DNA_Sequence_Mapping_top_map.ncd DNA_Sequence_Mapping_top.ngd
DNA_Sequence_Mapping_top.pcf
Target Device  : xc7z020
Target Package : clg484
Target Speed   : -3
Mapper Version : zynq -- $Revision: 1.55 $
Mapped Date    : Wed Dec 07 20:04:11 2016
Design Summary
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Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                   700 out of 106,400    1%
    Number used as Flip Flops:                 700
    Number used as Latches:                      0
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                0
  Number of Slice LUTs:                     14,244 out of  53,200   26%
    Number used as logic:                   13,838 out of  53,200   26%
      Number using O6 output only:           6,234
      Number using O5 output only:             148
      Number using O5 and O6:                7,456
      Number used as ROM:                        0
    Number used as Memory:                      16 out of  17,400    1%
      Number used as Dual Port RAM:             16
        Number using O6 output only:             0
        Number using O5 output only:             0
        Number using O5 and O6:                 16
      Number used as Single Port RAM:            0
      Number used as Shift Register:             0
    Number used exclusively as route-thrus:    390
      Number with same-slice register load:      4
      Number with same-slice carry load:       386
      Number with other load:                    0
Slice Logic Distribution:
  Number of occupied Slices:                 3,868 out of  13,300   29%
  Number of LUT Flip Flop pairs used:       14,281
    Number with an unused Flip Flop:        13,653 out of  14,281   95%
    Number with an unused LUT:                 37 out of  14,281    1%
    Number of fully used LUT-FF pairs:        591 out of  14,281    4%
    Number of unique control sets:             29
    Number of slice register sites lost
      to control set restrictions:            132 out of 106,400    1%
  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.
  OVERMAPPING of BRAM resources should be ignored if the design is
  over-mapped for a non-BRAM resource or if placement fails.
IO Utilization:
  Number of bonded IOBs:                      17 out of     200    8%
    Number of LOCed IOBs:                     17 out of      17  100%
Specific Feature Utilization:
  Number of RAMB36E1/FIFO36E1s:                0 out of     140    0%
  Number of RAMB18E1/FIFO18E1s:                0 out of     280    0%
  Number of BUFG/BUFGCTRLs:                    2 out of      32    6%
    Number used as BUFGs:                      2
    Number used as BUFGCTRLs:                  0
  Number of IDELAYE2/IDELAYE2_FINEDELAYs:      0 out of     200    0%
  Number of ILOGICE2/ILOGICE3/ISERDESE2s:      0 out of     200    0%
  Number of ODELAYE2/ODELAYE2_FINEDELAYs:      0
  Number of OLOGICE2/OLOGICE3/OSERDESE2s:      0 out of     200    0%
  Number of PHASER_IN/PHASER_IN_PHYs:          0 out of      16    0%
  Number of PHASER_OUT/PHASER_OUT_PHYs:        0 out of      16    0%
  Number of BSCANs:                            0 out of       4    0%
  Number of BUFHCEs:                           0 out of      72    0%
  Number of BUFRs:                             0 out of      16    0%
  Number of CAPTUREs:                          0 out of       1    0%
  Number of DNA_PORTs:                         0 out of       1    0%
  Number of DSP48E1s:                          0 out of     220    0%
  Number of EFUSE_USRs:                        0 out of       1    0%
  Number of FRAME_ECCs:                        0 out of       1    0%
  Number of ICAPs:                             0 out of       2    0%
  Number of IDELAYCTRLs:                       0 out of       4    0%
  Number of IN_FIFOs:                          0 out of      16    0%
  Number of MMCME2_ADVs:                       0 out of       4    0%
  Number of OUT_FIFOs:                         0 out of      16    0%
  Number of PHASER_REFs:                       0 out of       4    0%
  Number of PHY_CONTROLs:                      0 out of       4    0%
  Number of PLLE2_ADVs:                        0 out of       4    0%
  Number of PS7s:                              0 out of       1    0%
  Number of STARTUPs:                          0 out of       1    0%
  Number of XADCs:                             0 out of       1    0%
Average Fanout of Non-Clock Nets:              2.74
Peak Memory Usage:  1002 MB
Total REAL time to MAP completion:  2 mins 8 secs
Total CPU time to MAP completion:   1 mins 49 secs
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Section 1 - Errors
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Section 2 - Warnings
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Section 3 - Informational
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INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to
   1.050 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
INFO:Pack:1650 - Map created a placed design.
Section 4 - Removed Logic Summary
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   3 block(s) optimized away
Section 5 - Removed Logic
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Optimized Block(s):
TYPE            BLOCK
GND             SW/XST_GND
VCC             SW/XST_VCC
GND             XST_GND
To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.
Section 6 - IOB Properties
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| IOB Name | Type | Direction | IO Standard | Diff Term | Drive Strength | Slew Rate | Reg (s) | Resist |
|---|---|---|---|---|---|---|---|---|
| VGA_B<0> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_B<1> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_B<2> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_B<3> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_G<0> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_G<1> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_G<2> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_G<3> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_HS | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_R<0> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_R<1> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_R<2> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_R<3> | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| VGA_VS | IOB33 | OUTPUT | LVCMOS33 | | 12 | SLOW | | |
| button | IOB33 | INPUT | LVCMOS33 | | | | | |
| clk | IOB33 | INPUT | LVCMOS33 | | | | | |
| reset | IOB33 | INPUT | LVCMOS33 | | | | | |

Section 7 - RPMs
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Section 8 - Guide Report
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Guide not run on this design.
Section 9 - Area Group and Partition Summary
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Partition Implementation Status
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  No Partitions were found in this design.
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Area Group Information
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  No area groups were found in this design.
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Section 10 - Timing Report
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A logic-level (pre-route) timing report can be generated by using Xilinx static
timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the
mapped NCD and PCF files. Please note that this timing report will be generated
using estimated delay information. For accurate numbers, please generate a
timing report with the post Place and Route NCD file.
For more information about the Timing Analyzer, consult the Xilinx Timing
Analyzer Reference Manual; for more information about TRCE, consult the Xilinx
Command Line Tools User Guide "TRACE" chapter.
Section 11 - Configuration String Details
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Use the "-detail" map option to print out Configuration Strings
Section 12 - Control Set Information
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Use the "-detail" map option to print out Control Set Information.
Section 13 - Utilization by Hierarchy
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Use the "-detail" map option to print out the Utilization by Hierarchy section.