SABARAGAMUWA UNIVERSITY OF SRI LANKA

Faculty of Applied Sciences

Declaration by Student for Online Examination

I do hereby undertake to submit without demur or protest to the decision of the Faculty of Applied Sciences as far as the online examination and its results are concerned. I will be strictly following the instruction listed below:

1. I will strictly follow the deadlines of the examinations including the starting date and time and ending date and time.
2. I will check the emails and/or LMS to get the necessary instructions and exam schedule from the department.
3. I will contact the department to check my eligibility to appear in the online examinations.
4. I will be responsible to ensure the availability of a suitable computer/device with stable Internet connectivity and a suitable location (a closed room with no external noise and sufficient lighting) in order to avoid any disturbance during the online examination.
5. I agree to switch on the video camera and/or microphone of my computer or any other device during the presentation and viva voce Examination and when requested to do so by the examination supervisor. I also agree to share my screen with the evaluation panel during such Examination. In the case of projects, I will also be aware of sharing relevant deliverables on the screen for discussions.
6. I will ensure the submission of answers to all attempted questions within the prescribed time in the required file format.
7. I am aware that in case of any examination misconduct, the examination supervisor has the authority to report to the relevant authorities of the Faculty/University and the prescribed procedure for examination malpractices and/or offenses will be followed.
8. I have read and understood the information in the Students' Guide for Online Examinations, Faculty of Applied Sciences, prior to the Online Examination.
9. I will compulsorily adhere to the conditions specified in the Honour code for open book examinations as follows:

I acknowledge the Faculty Honour Code and I hereby confirm that the submitted work is entirely my own and I have not (i) used the services of any agency or person(s) providing a specimen, model work in the preparation of the work I submit for this open book examination; (ii) given assistance in accessing this paper or in providing specimen, model to other candidates submitting for this open-book examination.

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Signature:  Location: Batticaloa Date: 14/10/2021

Task 1

1)

The RISC processors have a minor set of commands with limited addressing nodes. The CISC processors have a greater set of commands with many addressing nodes.

RISC is used in high-end applications similar video processing, telecommunications, and image processing. CISC is used in low-end applications such as security systems, home automation
RISC offers high performance per watt for battery functioned devices where energy proficiency is key. A RISC processor accomplishes one action per instruction. By taking just one cycle to complete, operation execution time is enhanced.

To improve the performance of RISC chips, for chip designers, RISC processors make simpler the design and deployment process and offer a lower per-chip cost due to the smaller mechanisms required. Because of the reduced instruction set and simple decoding logic, less chip space is used, fewer transistors are required, and more general-purpose registers can appropriate into the central processing unit.

To advance performance, CISC systems attempt to reduce the number of instructions programs must call. To do this, they have large sets of microcode instructions that cover a broad range of tasks. A single microcode instruction, in turn, when interpreted in the CPU, may become numerous tasks the processor performs. As a consequence, instructions are of variable length and often necessitate more than one clock cycle to complete.

2)

My favor computer design specification:

64-bit CPU, 8GB RAM with DDR3, 100 MHz bus speed, 512 bit data bus width.

Bit size of the CPU

The processor's architecture and instruction set determine how many cycles, or ticks, are needed to execute a given instruction. In other words, some instruction sets are more efficient than others, enabling the processor to do more useful work at a given speed.

Memory type

the faster the RAM, the faster the processing speed. With faster RAM, you surge the speed at which memory transmissions information to other components. Meaning, your fast processor now has an equally fast way of talking to the other components, making your computer much more efficient.

The bus speeds

The faster the bus, the more data it can move within a given amount of time. The system's "Front Side Bus" connects the CPU to the computer's "Northbridge," which knobs communication amid the computer's RAM and the processor. This is the reckless part of the bus and handles the computer's most energetic workload

The address and data bud widths

The width of the data bus controls the number of bits that can be shifted to or from in one operation. The greater the data bus, the better the processor performance. By increasing the data bus from 32-bit to 64-bit, the computer can transfer twice as much information at one time. Therefore, increasing the size of the data bus improves the system performance of the computer.

Memory mapping

Cache is a small amount of memory which is part of the CPU which is physically closer to the CPU than RAM is. The more cache there is, the more data can be stored closer to the CPU. The ability to share memory amid application, and additional efficient coding.

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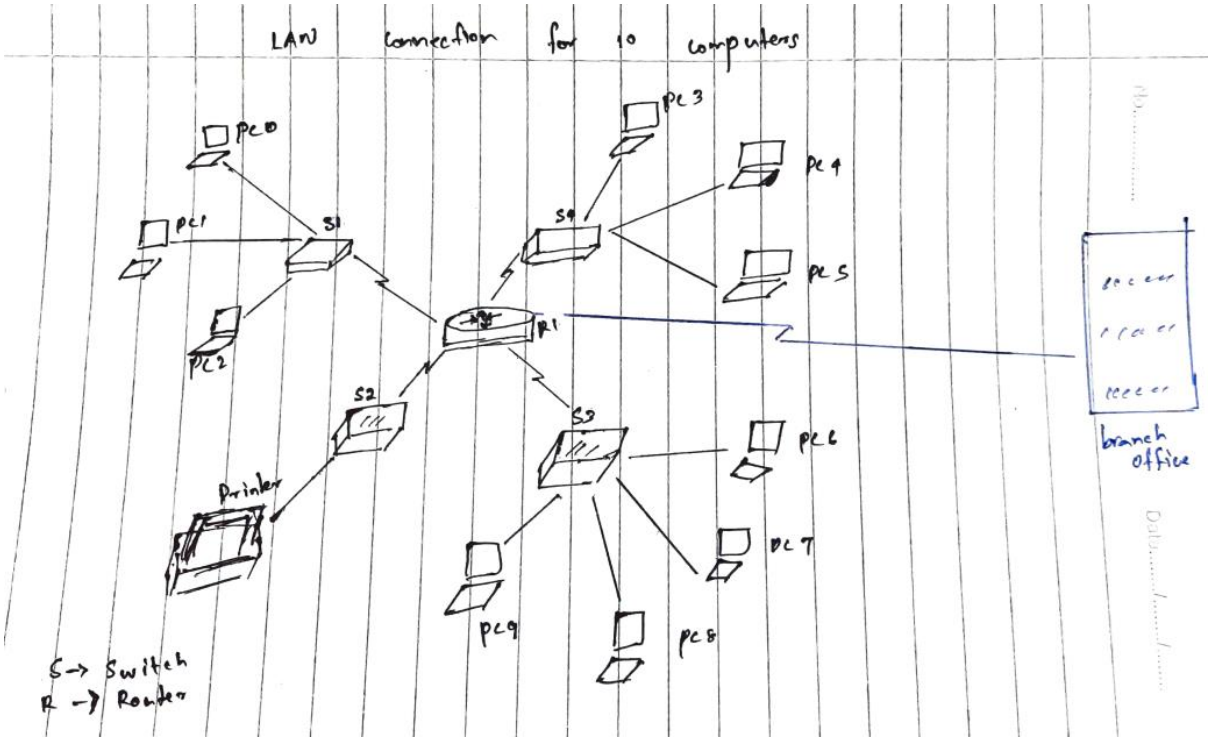
Task 2

1)



Explanation:

According to the scenario, the LAN connection contains three small LAN connections with ten PCs including a network printer. Therefore, a working office or something can implement a network system like this.

2)

The network devices are the following used here:
1. Switch
2.Router
3. Network cables.

Switch

Switch that filters and forwards network packets from one networking device. Switches are working under layer 2 datalink protocol. But there are some switches can be operate in layer 3.

Router
Router will pass the the network packet through different networks based on the routing table. They are work under network layer. they also provide traffic segmentation, multiple broadcast domains, and define network layer addressing subnets and networks.
No of collision domain: 16
No of broadcast domain: 1

3)

MAN – Metropolitan Area Network

A metropolitan area network (MAN) is a computer network that is bigger than a single building local area network (LAN) but is situated in a single geographic area that is smaller than a wide area network (WAN). Generally, it is several LANs interconnected by dedicated backbone connections. It may also refer to public use networking infrastructure in a municipality or region.

A metropolitan area network traditionally refers to a private data network used by a single organization in several buildings or by several organizations interconnected in the same geographic vicinity. It is larger than a LAN in a single building but not large enough to be measured a WAN. The size typically ranges from 5 kilometers to 50 km. If all the buildings are on a single piece of adjoining property, it may also be considered a campus network.

4)

Internet can be get through multiple ways. The main way to connect internet with cables. It is used for connect branches to branches.
Cable service connects to the Internet via cable TV, although you do not necessarily need to have cable TV in order to get it. It uses a broadband connection and can be faster than both dial-up and DSL service; however, it is only available where cable TV is available.

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Task 3

Why Machine Learning Needs Benchmarks

1)

There are now at least 45 hardware startups with $1.5 billion in investment targeting machine learning. The transfer from research to commercial deployment has been remarkably fast: the breakthrough Alex Net paper, which markedly improved image classification using deep learning, was published just six years ago. A good benchmark suite is both diverse and representative, where each workload in the suite has unique attributes. What might a good ML benchmark look like? Allow me some rhetorical indulgence, in grouping the attributes that I think are important under five "R"s:
They are Relevant, Representative, Recent, Repeatable, Reasonable. Choosing the set of workloads is probably best done with expert guidance. Rapid iteration makes for more work but also allows a benchmark suite to remain relevant.

2)

MFLOPS (millions of floating-point operations per second) can be a very deprived measure of a processor's performance because floating-point operations is not reliable across computers, and the number of definite floating-point operations performed may differ, or the MFLOPS evaluation changes according not only to the combination of integer and floating-point operations but to the mixture of fast and slow floating-point operations.

.It is a lawful quantity of performance, if we define a method of counting the number of floating-point operations in a high-level language program. This counting procedure can also weight the processes, giving more multifaceted operations larger weights, permitting a computer to attain a high MFLOPS rating even if the program covers many floating-point divides.

These MFLOPS might be called stabilized MFLOPS. Of course, because of the counting and weighting, these normalized MFLOPS may be very different from the real rate at which a computer executes floating-point operations.

References

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