Design and Optimization of Non-Volatile Latch using Resistive Memory Technology

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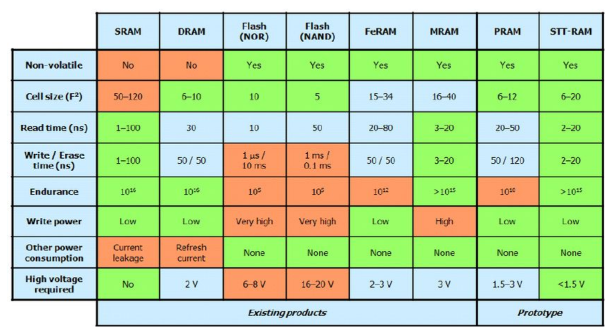
1. Introduction

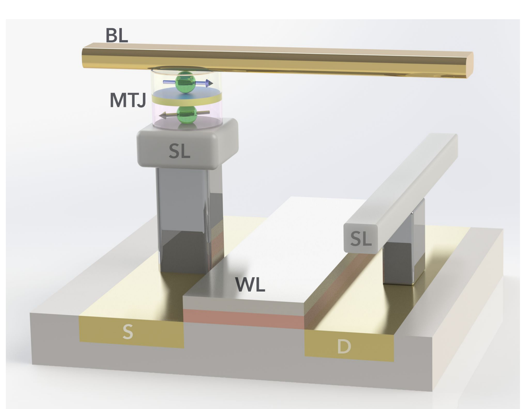
- Modern Semiconductor industry is vulnerable to IP fraud and reverse engineering due to low hardware security and IC fabrication foundries outsourcing semiconductor design.



- STT technology poses as a great potential solution. It can be used to improve hardware security by implementing fast, reconfigurable logic to IC design.

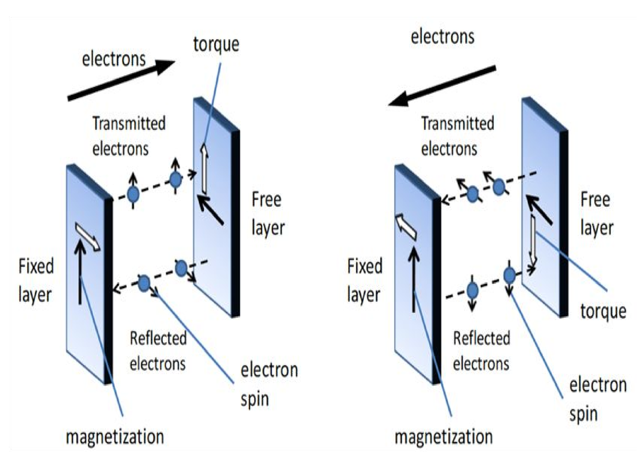
2. Spin Transfer Torque Random Access Memory (STTRAM)

- Resistive memory technology to replace traditional charge-based memory.
- Information storage by use of magnetic orientation.
- CMOS compatibility, scalability, non-volatility, low power



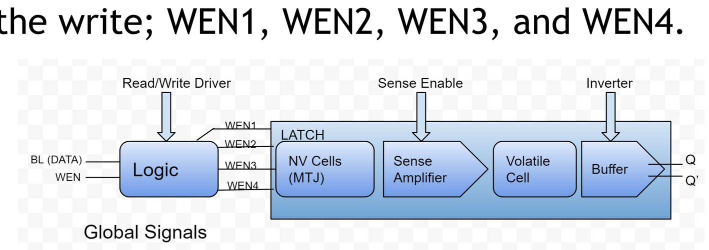
3. Magnetic Tunnel Junction (MTJ)

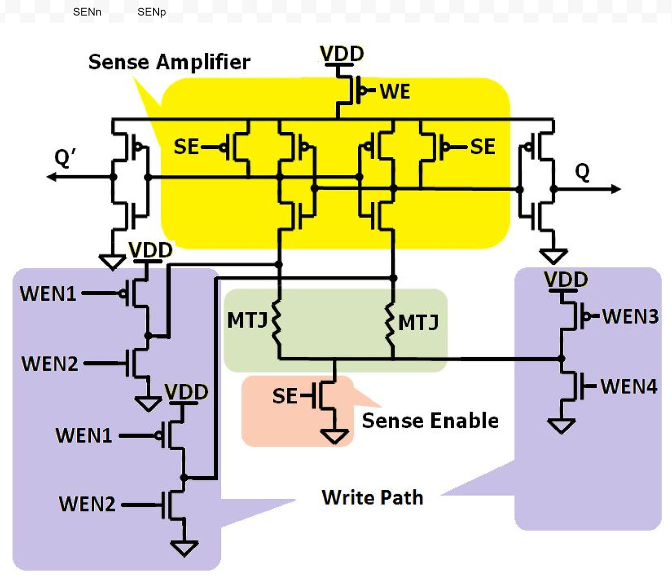
- Composed of an oxide layer in between two ferromagnetic layers; one free and one pinned.
- Used to store information as binary bit.
- Resistance is sensed by applying a current to MTJs layers.
- Information is sensed as resistances.
  - Low resistance is logic state 0 & High resistance is logic state 1.



4. Design and Parameters

- The precharge latch consists of two MTJs as resistive memory cells to hold our data as binary one or zero.
- The outputs are the voltage out referenced as Q for the left side of the circuit and Q' for the right side of the circuit. There are four inputs for the write; WEN1, WEN2, WEN3, and WEN4.





Logic

- The control logic is composed of two inverters and two nand gates, and it generates the signals to flip the MTJ.
- Depending on the direction of the current, values (either 0 or 1) are introduced for the Data and the Write Enable (1-4).

Bit-Line (Data)	Wen	WEN1	WEN2	WEN3	WEN4
0	0	1	0	1	0
0	1	1	1	0	0
1	0	1	0	1	0
1	1	0	0	1	1

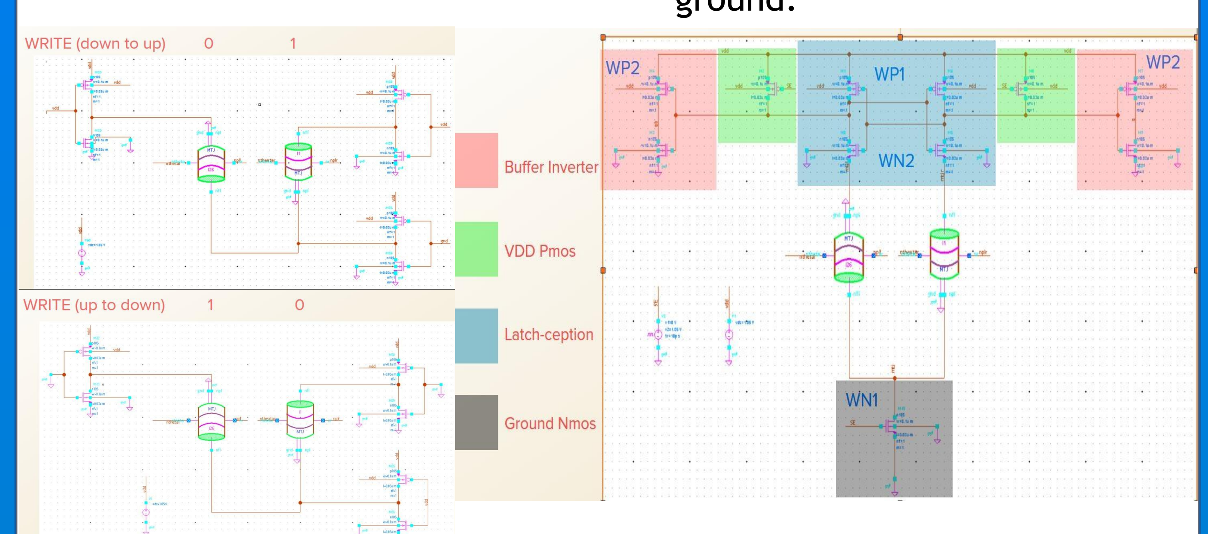
Write and Read Operations

Write Operations

- When writing a 0 1 to the pair of MTJs, WEN1 and WEN2 are low, the top NMOS transistors are on, and the top of the circuit is connected to ground while WEN3 allows the bottom PMOS to turn on.
- When writing 1 0 to the pair of MTJs, WEN1 and WEN2 are high which allows VDD to be present at the top of the circuit.

Read Operations

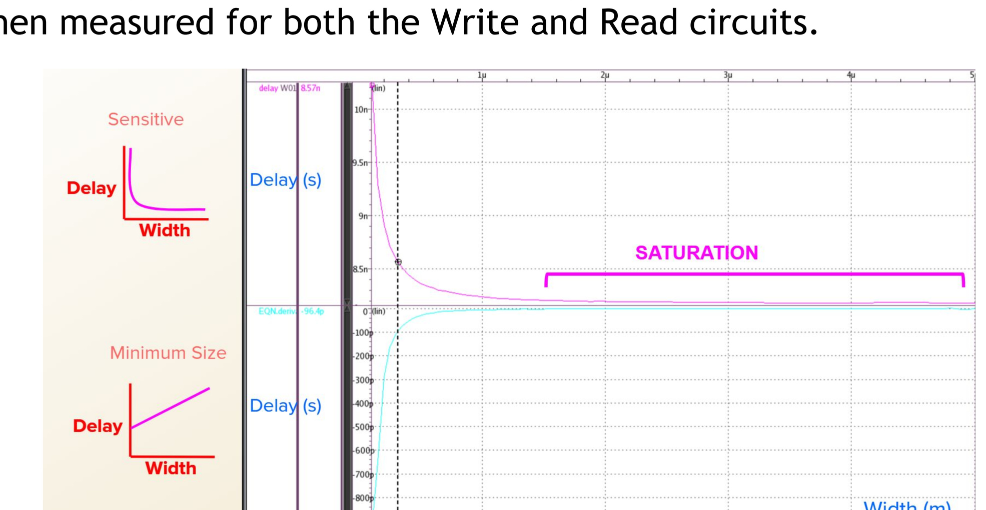
- During the pre-charge phase sense enable is low and the PMOS at the top of the circuit allows the circuit to be pre-charged with VDD while the NMOS that connects to ground is not active.
- During the evaluation phase sense enable is high and the VDD PMOS is inactive while the Grounding NMOS is active and allows the circuit to connect to ground.



5. Methodology

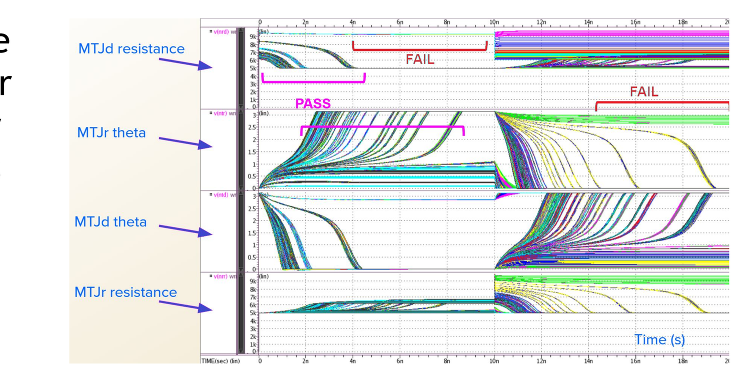
Delay Vs Width Sweeps

- Circuit first created as a schematic and exported as HSPICE netlist.
- Added lines of code to Netlist to measure delay, area, and MTJ orientation.
- Using the netlist, simulations were run of the full circuit where individual transistor widths were adjusted.
- The change in delay due to the changes in transistor widths was then measured for both the Write and Read circuits.



Optimization of write (6 Transistors)

- We ran multivariable simulations with four variables to see how the transistor values are affected and to find accurate width values.

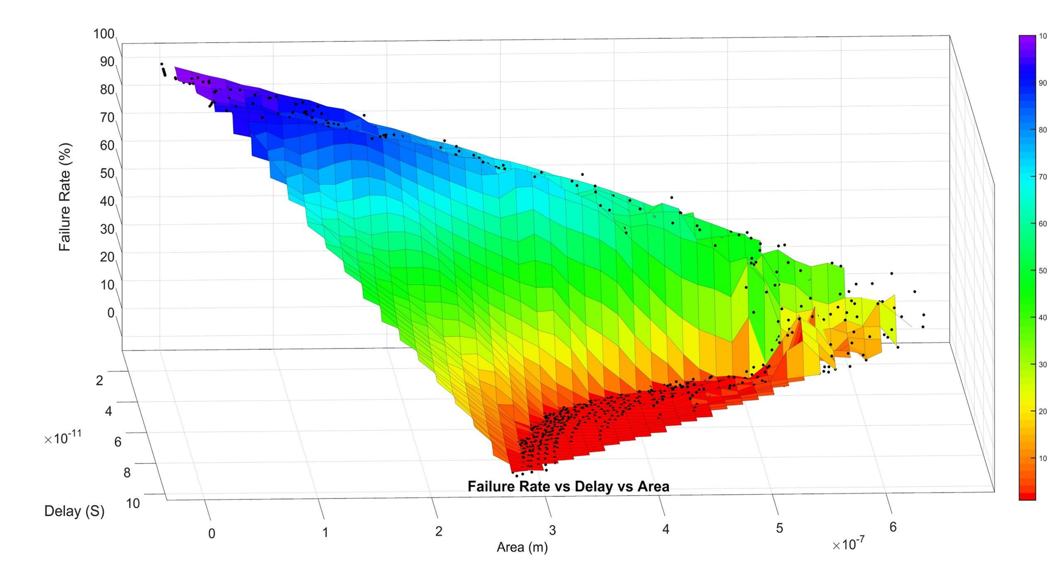


Optimization of read (12 Transistors)

- Optimization of the read cycle was performed by using HSpice and a netlist that allowed delay and area to be used as weighted goals.
- The netlist contained a parameter which allowed an area goal to be set so that HSpice would determine the best possible transistor size.

Monte Carlo Simulations

- A Monte Carlo failure rate netlist program was used to test each set of values recorded in the optimization process.
- Each set of our values was run at 1000 iterations to ensure reliability of the circuit to within 0.1% accuracy.
- We looked for values that passed simulations with 0% failure rate, which meant a minimum of 99.9% reliability.
- The optimization for 100 run Monte Carlo yielded best values that had higher delay, lower reliability, and lower area.



Layout

- The goal of the layout was to minimize the area the circuit would take up while still being able to perform as desired.
- The first test we ran once our layout was constructed was the Design Rules Checking (DRC), which checks to make sure our design follows the current rules and conventions used in manufacturing.
- All of the nmos and pmos layers must overlap each other and the *VDD* and *VSS* must all be formed into one bar across all instances respectively to create one continuous circuit.

6. Results

Write			Read		
Monte	100	1000	Monte	100	1000
topN	1.693u	1.871u	WN1	0.77u	1.3u
topP	2.103u	2.402u	WN2	0.35u	0.8u
SinkP	3.506u	3.702u	WP1	0.73u	1.5u
SinkN	2.601u	3.001u	WP2	0.1u	0.1u
Area	13.699u	15.249u	Area	4.05u	7.1u
Delay	3.2203n	2.999n	Delay	34.9678p	3.755p

- Write Cycle Transistor sizes; topN was 1.871μm, topP was 2.402μm, SinkP was 3.506μm, and SinkN was 3.001μm
- Read Cycle Transistor sizes; WN1 was 1.3μm, WN2 was 0.8μm, WP1 was 1.5μm, and WP2 was 0.1μm
- Post Layout write path was rerun with parasitics and results showed the unideal delay of 3.5ns
- Post Layout Read Path with parasitics had a delay of 168ps with sensing power of 42.4009 μW. Leakage Power was very low at 1.5594μW at SE frequency of 250 MHz
- Post-Layout 1000 iteration Monte Carlo run with parasitics yielded 100% pass rate for both Write and Read Operations

7. Conclusion

- Low delay corresponded with low failure rate and thus high reliability
- High area and high power consumption corresponded with low failure rate
- Optimized values of the read path transistors much smaller than those of the write path. Larger increases in width were needed in the write path than the read path for similar improvements in reliability.
- Focus of future research on this subject will be on the improvement of the write path in terms of area, power consumption, and delay

8. References

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9. Acknowledgements

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