Varun Khaneja

Contact Information

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About Me

I'm a versatile, seasoned developer, interested in opportunities in mobile application development, web development. I love to travel, and am fascinated by economics.

Areas of Interests

Mobile application development, Web development, Web browsers, Cloud services.

Programming Skills

C++, *bash* scripting, *JavaScript*, *CSS*, *C#*, *Java*, *XAML*.
Mobile: *Android*, *Windows Phone 7*, Familiarity with *iOS*.
Desktop: *Windows*, *Linux*.

Professional Experience

Microsoft Corporation, Redmond, USA. **July 2011 – present**

Software Development Engineer II

Developer on the *Expression Blend for HTML* team. Expression Blend is a user interface design tool for creating graphical interfaces for web and desktop applications. Previously, I worked on implementing support for JavaScript controls for Windows 8 applications, and currently on an unannounced feature related to CSS.
Experience gained: *C#*, *C++*, *CSS*, *JavaScript*, *XAML*.

Adobe Systems, Noida, India. **June 2007 – July 2011**

Computer Scientist

Mobile: Built Adobe Reader for *Android*, almost single-handedly for *Windows Phone 7*, lead the effort for some of the other platforms.
PDF Reader for Unix: Implemented *Flash Player* playback inside *Reader*; Owned the responsibility for a smooth installation experience.
Acrobat: Joint ownership of development of the legacy Multimedia playing solution.
Experience gained: *Android*, *C++*, *bash scripting*, *Java*, *Windows Phone 7*.

Advanced Micro Devices (AMD), Bangalore, India. **July 2006 – May 2007**

Design Engineer - II Pre-silicon functional verification

Complete ownership of functional verification of the instruction cache and the floating-point unit (FPU) of the first generation of quad-core processor family from AMD.
Joint ownership of the functional verification of the Data Cache.
Verification was performed using a variety of approaches such as directed tests, whacker environment, and coverage including FCOV.

IIT Kanpur, Kanpur, India. **Dec 2004 - July 2005 - Dec 2005**

Course Tutor Fundamentals of Computing

Delivered Java tutorials (three back-to-back terms) at the university.
Worked along with the instructor and fellow tutors in developing and adopting best techniques of imparting learning.

Education

IIT Kanpur **July 2004 – June 2006**
Master of Technology Advisor: Dr. Mainak Chaudhuri CPI: 9.14 (on 10)

Bharati Vidyapeeth College of Engineering, Delhi, India **July 2000 – June 2004**
Bachelor of Technology Score: 79.80%

Honours and Awards

Nominated for the "Good Work" award multiple times by teammates, 2010.

Spot award for diligence shown in working on security issues related to Multimedia playback for Acrobat 9, 2008.

Bagged 1^{st} prize in *Coderupt*, an International Online Hacking Competition, 2006.

Ranked 2^{nd} (99.98 percentile) in GATE examination, 2004.

Among top 0.1% scorers in Mathematics in AISSE, 1998.

COURSES TAKEN

Computer Architecture, Parallel Computer Architecture, Embedded Systems, VLSI Design for Parallel Architectures, Grid Computing, Computer System Security.

ACADEMIC PROJECTS

Masters Thesis: Selective optimizations and Evaluation of a Directory-less Protocol on Distributed Shared Memory Multiprocessors.

Distributed Shared Memory multiprocessors have been using directory based approaches to maintain the state of the cache lines at home node. This approach has a major memory access overhead, for reading the directory, in cases when the line is in the modified state. I worked on designing a protocol that circumvents this problem by broadcasting the incoming request to all nodes in the system. Broadcasting all incoming requests puts a large amount of load on the coherence controller, so techniques to reduce the average load on it were also evaluated.

Prediction of header and addresses in a packet in a Distributed Shared Memory System

The project dealt with the use of prediction algorithms for predicting the header and contents of request messages in a DSM system. This helps in reducing the effect of memory access latency and improves system performance considerably. To keep the hardware costs minimal, simple algorithms were used which needed to be finely configured. *[September - November 2004]*

REFEREES

Available on request.