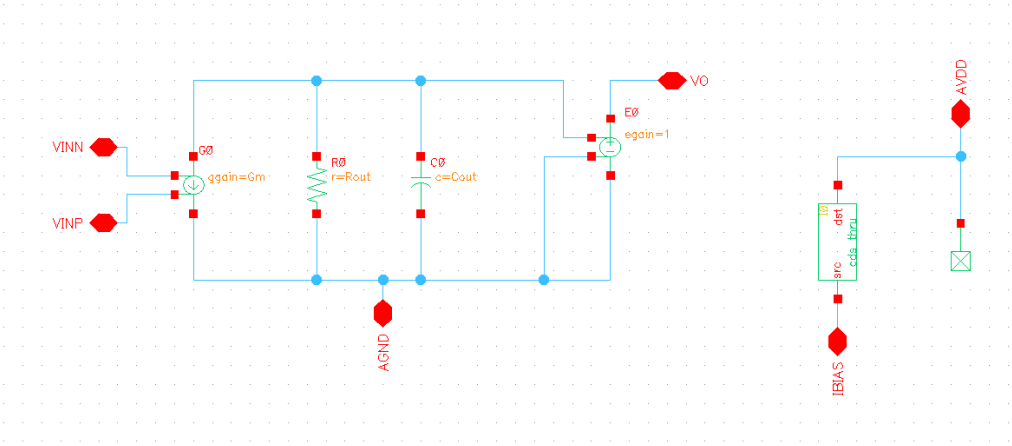
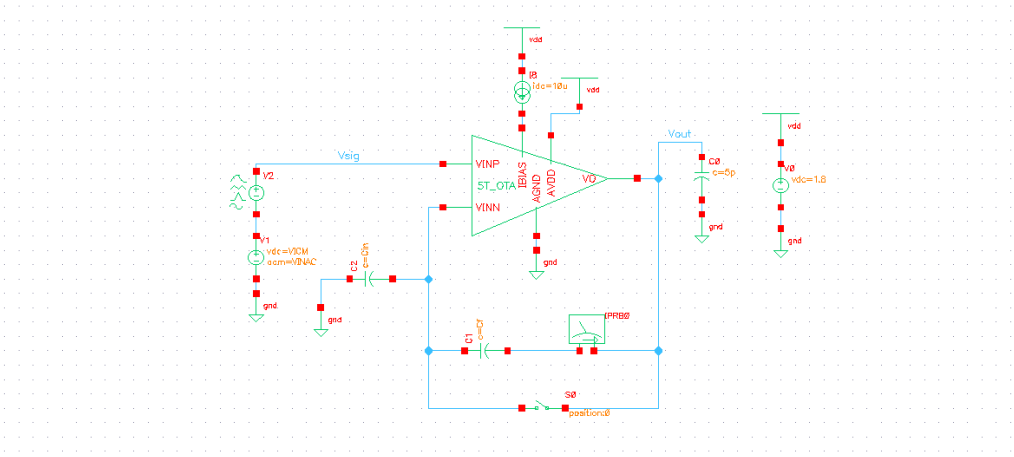
Lab 08

Negative Feedback

PART 1: Feedback with Behavioural OTA

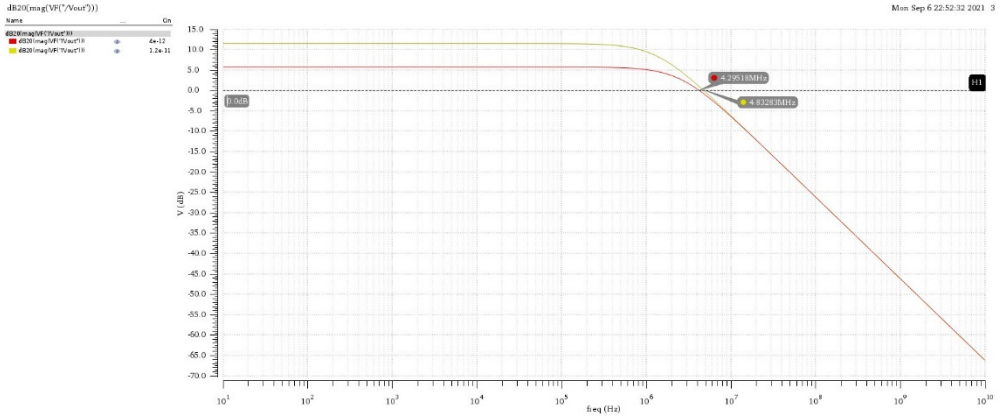


Schematic behavioural circuit schematic from cadence



Circuit testbench for schematic_behav with capacitive feedback

1) Closed loop-gain vs frequency.



Magnitude bode plot in dB for Vout in case of Cin=4p,12p

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Cin=4p						
1	TrainLAB:Lab08_TB:1	Av dB	5.76			
1	TrainLAB:Lab08_TB:1	Av Mag	1.941			
1	TrainLAB:Lab08_TB:1	BW	2.572M			
1	TrainLAB:Lab08_TB:1	GBW	5.005M			
1	TrainLAB:Lab08_TB:1	UGF	4.314M			
Parameters: Cin=12p						
2	TrainLAB:Lab08_TB:1	Av dB	11.53			
2	TrainLAB:Lab08_TB:1	Av Mag	3.771			
2	TrainLAB:Lab08_TB:1	BW	1.326M			
2	TrainLAB:Lab08_TB:1	GBW	5.011M			
2	TrainLAB:Lab08_TB:1	UGF	4.848M			

AC analysis results for two cases of Cin "DC gain | BW | GBW | UGF"

• Compare the DC gain, BW, and GBW with hand analysis in a table.

a. DC Gain Hand Analysis:

- $C_{in} = 4p \rightarrow \beta = \frac{C_F}{C_F + C_{in}} = 0.5, and\ we\ have\ A_{oL} = 65.72\ from\ previous\ lab\ so$

$$A_{cL} = \frac{A_{oL}}{1 + \beta A_{oL}} = 1.941 = 5.76dB.$$

- $C_{in} = 12p \rightarrow \beta = \frac{C_F}{C_F + C_{in}} = \frac{1}{4}, and\ we\ have\ A_{oL} = 65.72\ from\ previous\ lab\ so$

$$A_{cL} = \frac{A_{oL}}{1 + \beta A_{oL}} = 3.77 = 11.528dB.$$

b. Bandwidth and GBW Hand Analysis:

- $C_{in} = 4p \rightarrow \beta = \frac{C_F}{C_F + C_{in}} = 0.5, and\ we\ have\ A_{oL} = 65.72,$

$$\omega_{oL} = 76.22k\ from\ previous\ lab\ so\ \omega_{cL} = (1 + \beta A_{oL})\omega_{oL} = 2.58\ MHz$$
$$GBW = A_{vCL} * \omega_{cL} = 5.008MHz.$$

- $C_{in} = 4p \rightarrow \beta = \frac{C_F}{C_F + C_{in}} = 0.25, and\ we\ have\ A_{oL} = 65.72,$

$$\omega_{oL} = 76.22k\ from\ previous\ lab\ so\ \omega_{cL} = (1 + \beta A_{oL})\omega_{oL} = 1.328MHz$$
$$GBW = A_{vCL} * \omega_{cL} = 5.007MHz.$$

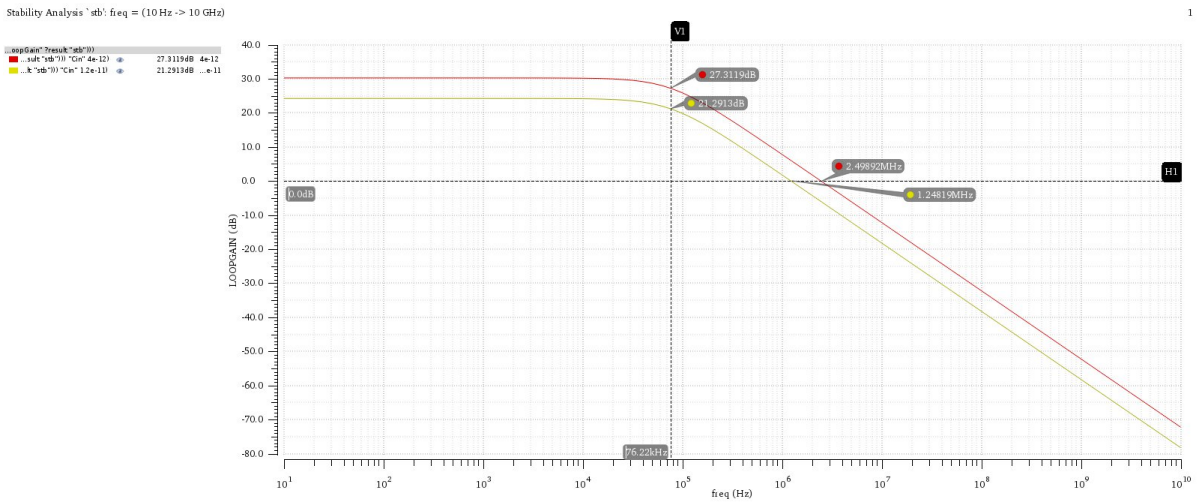
	Simulation results		Hand Analysis results	
	Cin=4p	Cin=12p	Cin=4p	Cin=12p
DC Gain	1.941	3.771	1.941	3.771
Bandwidth	2.572M	1.326M	2.58M	1.328M
GBW	5.005M	5.011M	5.008M	5.007M

• Comment on the difference between the results for the two values of CIN.

As shown from previous analysis that by increasing capacitance the value of feedback factor decreases due to capacitive divider which increases the value of closed-loop gain, but cannot reach to ideal value of closed-loop gain because open-loop gain is a finite gain, but GBW is the same in two cases because as gain decrease bandwidth increase by the same ratio which keep GBW constant.

2) Loop gain vs frequency.

• Plot loop gain in dB for the two values of CIN. Annotate the DC loop gain, the dominant pole, and the unity gain frequency in the plot.



Loop gain magnitude bode plot in dB with UGF and dominant pole annotated

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Cin=4p						
1	TrainLAB:Lab08_TB:1	UGF L	2.5M			
1	TrainLAB:Lab08_TB:1	Av Mag L	32.86			
1	TrainLAB:Lab08_TB:1	Av dB L	30.33			
1	TrainLAB:Lab08_TB:1	GBW L	2.503M			
Parameters: Cin=12p						
2	TrainLAB:Lab08_TB:1	UGF L	1.249M			
2	TrainLAB:Lab08_TB:1	Av Mag L	16.43			
2	TrainLAB:Lab08_TB:1	Av dB L	24.31			
2	TrainLAB:Lab08_TB:1	GBW L	1.251M			

Gain and UGF results from ADEXL for loop gain simulation

• Compare DC LG and GBW with hand analysis in a table.

a. DC LG Hand Analysis:

- $C_{in} = 4p \rightarrow \beta = \frac{C_F}{C_F + C_{in}} = 0.5, and\ we\ have\ A_{oL} = 65.72\ from\ previous\ lab\ so\ LG = \beta A_{oL} = 32.86.$
- $C_{in} = 12p \rightarrow \beta = \frac{C_F}{C_F + C_{in}} = 0.25, and\ we\ have\ A_{oL} = 65.72\ from\ previous\ lab\ so\ LG = \beta A_{oL} = 16.43.$

b. GBW LG Hand Analysis:

- $C_{in} = 4p \rightarrow GBW = LG * \omega_{oL} = 2.5\ MHz.$
- $C_{in} = 4p \rightarrow GBW = LG * \omega_{oL} = 1.25\ MHz.$

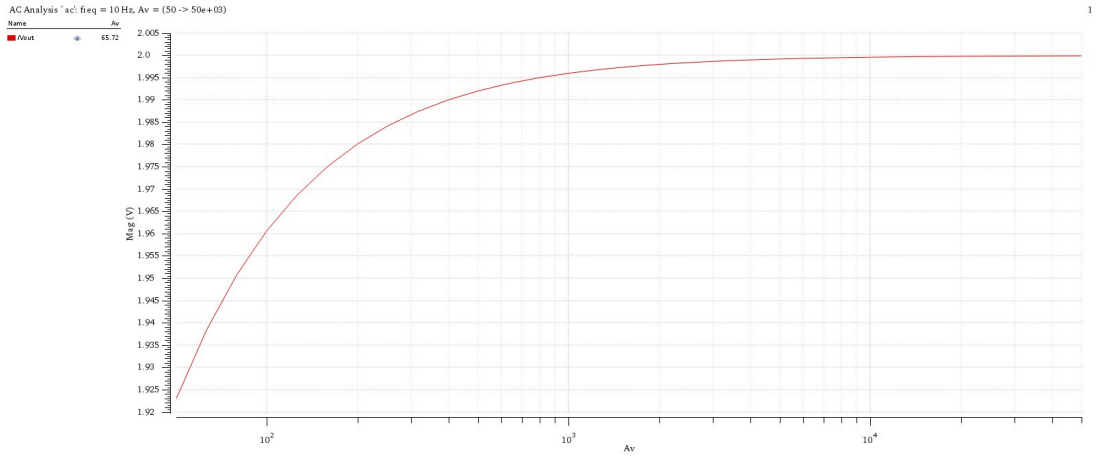
	Simulation results		Hand Analysis results	
	Cin=4p	Cin=12p	Cin=4p	Cin=12p
DC LG	32.86	16.43	32.86	16.43
GBW LG	2.503M	1.251M	2.5M	1.25M

• Comment on the differences between the results for the two values of CIN.

As shown from previous analysis that by increasing capacitance the value of feedback factor decreases due to capacitive divider which increases the value of closed-loop gain, but cannot reach to ideal value of closed-loop gain because open-loop gain is a finite gain, which increase GBW because BW of LG is constant as open-loop BW.

3) Gain Desensitization.

• Plot closed loop DC gain (magnitude at 10Hz, not dB) vs Av.



Closed-loop gain versus open-loop gain plot

• Calculate the percent change in closed loop gain (magnitude, not dB). Note that open loop gain (Av) changes by three orders of magnitude (60 dB). Comment.

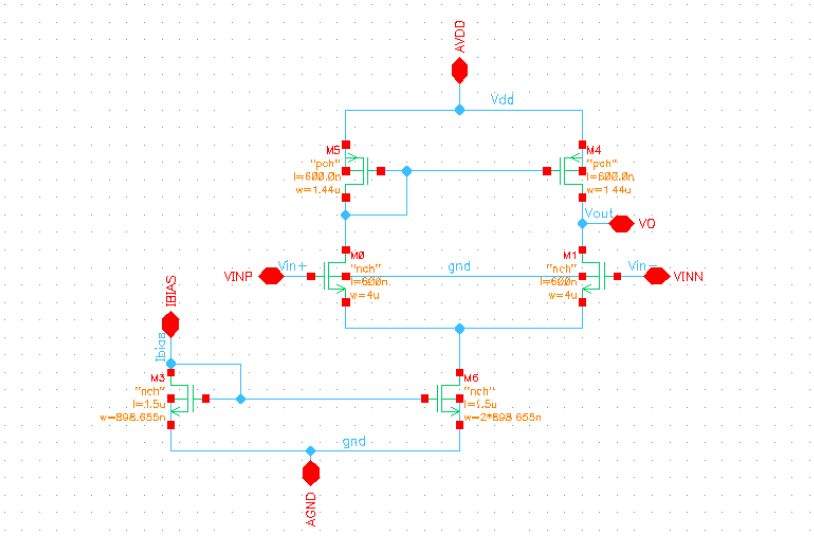
$$@A_{oL} = 50K \rightarrow A_{cL} = 2 \mid ideal\ closed - loop\ gain$$

$$@A_{oL} = 50 \rightarrow A_{cL} = 1.92 \mid Actual\ closed - loop\ gain$$

$$static\ gain\ error \mid \varepsilon_s = \frac{A_{cL-ideal} - A_{cL-actual}}{A_{cL-ideal}} = 4\%$$

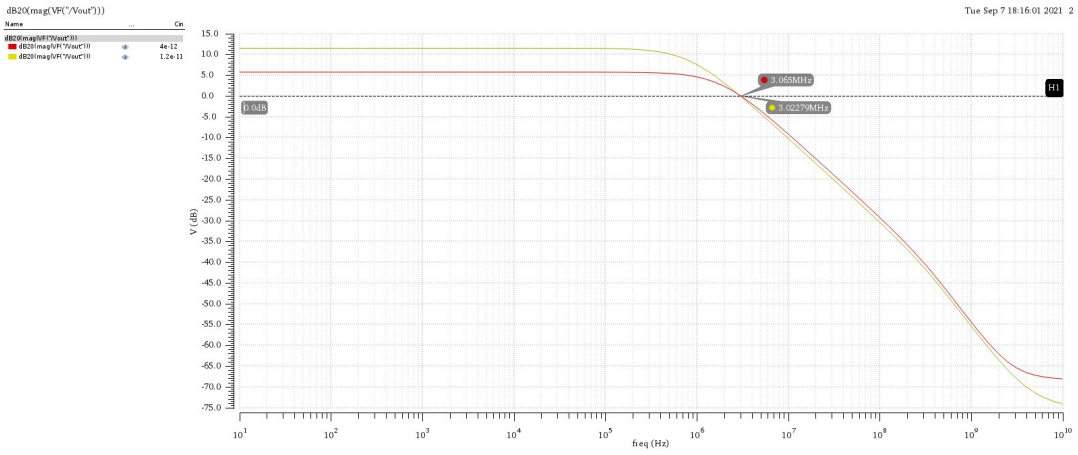
Comment. So from previous analysis as shown that closed-loop gain not affected by variations of open-loop gain, and only depend on capacitive divider loads so this give a stable gain with PVT variations.

PART 2: Feedback with Real 5T OTA



Circuit schematic for 5T-OTA with MOSFETs design from cadence

1) Closed loop-gain vs frequency.



Magnitude bode plot in dB for Vout in case of Cin=4p,12p

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Cin=4p						
1	TrainLAB:Lab08_TB:1	Av dB	5.755			
1	TrainLAB:Lab08_TB:1	Av Mag	1.94			
1	TrainLAB:Lab08_TB:1	BW	1.842M			
1	TrainLAB:Lab08_TB:1	GBW	3.582M			
1	TrainLAB:Lab08_TB:1	UGF	3.072M			
Parameters: Cin=12p						
2	TrainLAB:Lab08_TB:1	Av dB	11.52			
2	TrainLAB:Lab08_TB:1	Av Mag	3.766			
2	TrainLAB:Lab08_TB:1	BW	829.5k			
2	TrainLAB:Lab08_TB:1	GBW	3.132M			
2	TrainLAB:Lab08_TB:1	UGF	3.034M			

AC analysis results for two cases of Cin "DC gain | BW | GBW | UGF"

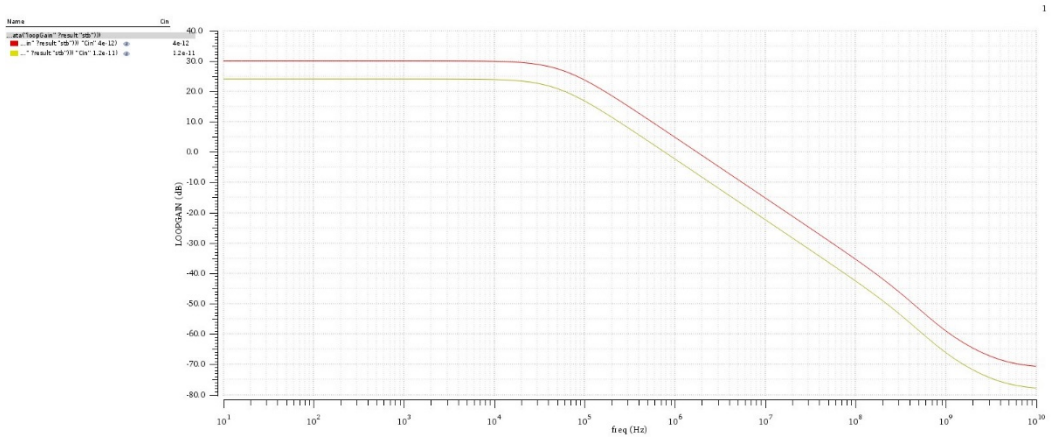
• Compare between the results you obtained here and the results in Part 1 in a table.

	Simulation Results Part 1		Simulation Results Part 2	
	Cin=4p	Cin=12p	Cin=4p	Cin=12p
DC Gain dB	1.941	3.771	1.94	3.766
Bandwidth	2.572M	1.326M	1.842M	829.5k
GBW	5.005M	5.011M	3.582M	3.132M
UGF	4.314M	4.848M	3.072M	3.034M

• You will notice that the bandwidth, and consequently the GBW are much smaller than Part 1. Why? Comment.

As shown that there is degradation in bandwidth and GBW due to introducing a drain capacitance of output node, and feedback capacitance also which contribute loading effect all this increase total capacitance and decrease BW.

2) Loop gain vs frequency.



Loop gain magnitude bode plot in dB with UGF and dominant pole annotated

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Cin=4p						
1	TrainLAB:Lab08_TB:1	UGF L	1.804M			
1	TrainLAB:Lab08_TB:1	Av Mag L	31.98			
1	TrainLAB:Lab08_TB:1	Av dB L	30.1			
1	TrainLAB:Lab08_TB:1	GBW L	1.787M			
1	TrainLAB:Lab08_TB:1	BW L	55.76k			
Parameters: Cin=12p						
2	TrainLAB:Lab08_TB:1	UGF L	781.7k			
2	TrainLAB:Lab08_TB:1	Av Mag L	16.13			
2	TrainLAB:Lab08_TB:1	Av dB L	24.15			
2	TrainLAB:Lab08_TB:1	GBW L	781.4k			
2	TrainLAB:Lab08_TB:1	BW L	48.34k			

Gain and UGF results from ADEXL for loop gain simulation

• Compare between the results you obtained here and the results in Part 1 in a table.

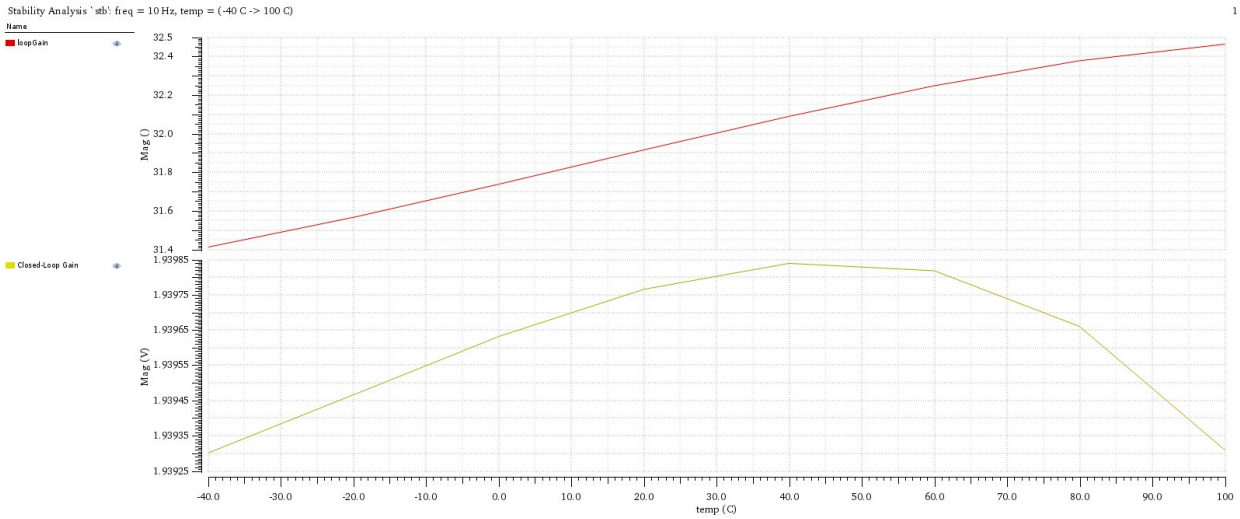
	Simulation Results Part 1		Simulation Results Part 2	
	Cin=4p	Cin=12p	Cin=4p	Cin=12p
DC Gain dB	30.33	24.31	30.1	24.15
Bandwidth	76.17k	76.14k	55.76k	48.34k
GBW	2.503M	1.251M	1.787M	781.4k
UGF	2.5M	1.249M	1.804M	781.7k

• You will notice that the unity gain frequency is much smaller than Part 1. Why? Comment.

As shown that there is degradation in bandwidth and GBW due to introducing a drain capacitance of output node, and feedback capacitance also which contribute loading effect all this increase total capacitance and decrease BW.

3) Gain Desensitization.

• Sweep the temperature from the parameters window. Set temperature = -40:20:100.



Loop-gain and closed-loop gain analysis results versus frequency from simulation

• Compare the percent change in the DC loop gain (from STB) and the DC closed loop gain (from AC) across temperature extremes.

Percent of error for closed-loop gain:

$$@T = 40 \rightarrow A_{cL} = 1.94 \mid Max\ closed - loop\ gain$$

$$@A_{oL} = -40 \rightarrow A_{cL} = 1.939 \mid Min\ closed - loop\ gain$$

$$static\ gain\ error \mid \varepsilon_s = \frac{A_{cL-ideal} - A_{cL-actual}}{A_{cL-ideal}} = 0.05\%$$

Percent of error for loop gain:

$$@T = 100 \rightarrow A_{cL} = 32.465 \mid Max\ loop\ gain$$

$$@A_{oL} = -40 \rightarrow A_{cL} = 31.41355 \mid Min\ loop\ gain$$

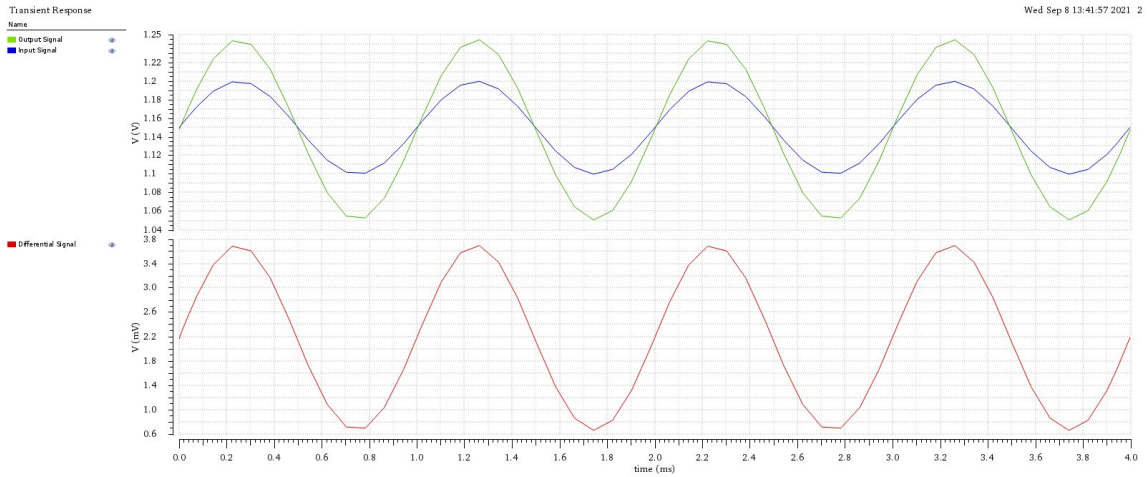
$$static\ gain\ error \mid \varepsilon_s = \frac{A_{cL-ideal} - A_{cL-actual}}{A_{cL-ideal}} = 4\%$$

Comment.

From previous analysis as shown that closed-loop gain is insensitive to temperature change as it depends on ratio of capacitive divider despite loop gain which affected by changing temperature as shown.

4) Transient analysis.

• Plot the input signal, the output signal, and the differential input signal of the OTA (VP – VN).



Transient analysis results for f=1K "input | output | Diff."

• Calculate the peak-to-peak voltage of the previous three signals. What is the relation between the output and (VP – VN)?

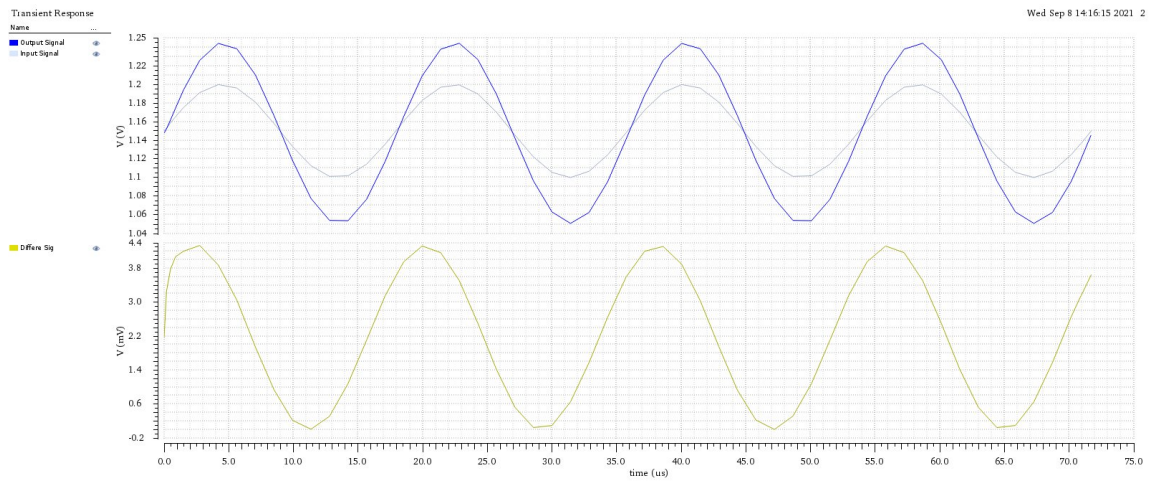
Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:Lab08_TB:1	Output Sig				
TrainLAB:Lab08_TB:1	Input Signal				
TrainLAB:Lab08_TB:1	Vin PP	99.78m			
TrainLAB:Lab08_TB:1	Vout PP	193.5m			
TrainLAB:Lab08_TB:1	Verr PP	3.038m			

Peak to peak voltages from ADXL simulation for input, output and differential voltages

Comment.

As shown that the ration between output voltage to differential voltage is nearly equivalent to open-loop gain $A_{vOL} = \frac{Vout}{Verr} = 63.7$ and we have AoL=65.72, which make a great agreement.

• Repeat the transient analysis with FIN exactly equal to the closed loop bandwidth. Plot the input signal, the output signal, and the differential input signal of the OTA (VP – VN).



Transient analysis results for f=1K “input | output | Diff.”

• Calculate the peak-to-peak voltage of the previous three signals. What is the relation between the output and the input signal? What is the relation between the output and (VP – VN)? Compare between this case and the case of 1kHz input.

Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:Lab08_TB:1	Output Signal				
TrainLAB:Lab08_TB:1	Input Signal				
TrainLAB:Lab08_TB:1	Vin PP	99.73m			
TrainLAB:Lab08_TB:1	Vout PP	193.2m			
TrainLAB:Lab08_TB:1	Verr PP	4.337m			

Peak to peak voltages from ADXL simulation for input, output and differential voltages

Comment.

As shown from previous figure that the relation between output signal and input signal is nearly equal to closed-loop gain Acl=2, and $\frac{Vout}{Vin} = 1.937$.