Lab 01

LPF Simulations and MOSFET Characteristics

Part 1: Low Pass Filter Simulation (LPF)

1.Transient Analysis:

1) Circuit design:

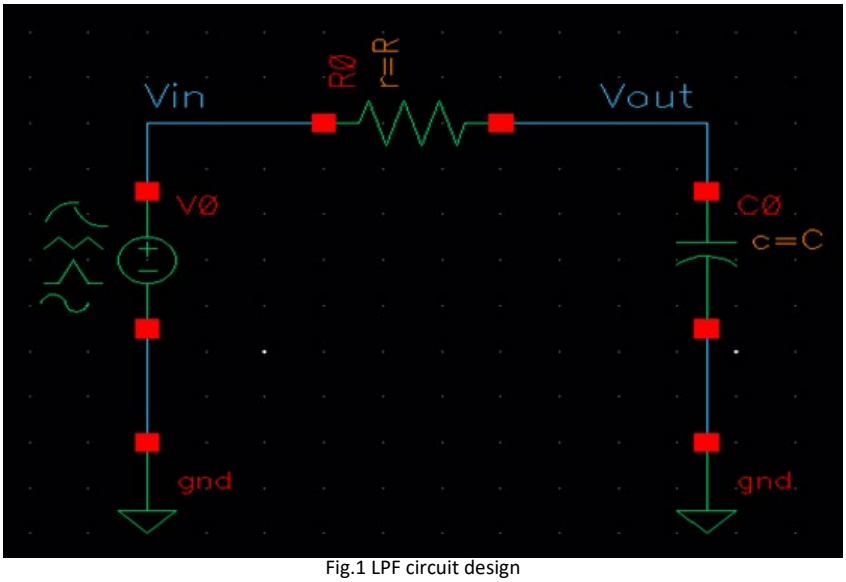

Fig.1 LPF circuit design

For time constant $\tau = 0.5ns$ and resistance of $R = 1k\Omega$,
I choose value of capacitor $C = 0.5pf$. $\therefore\ \tau = RC$

2) , 3) Transient analysis:

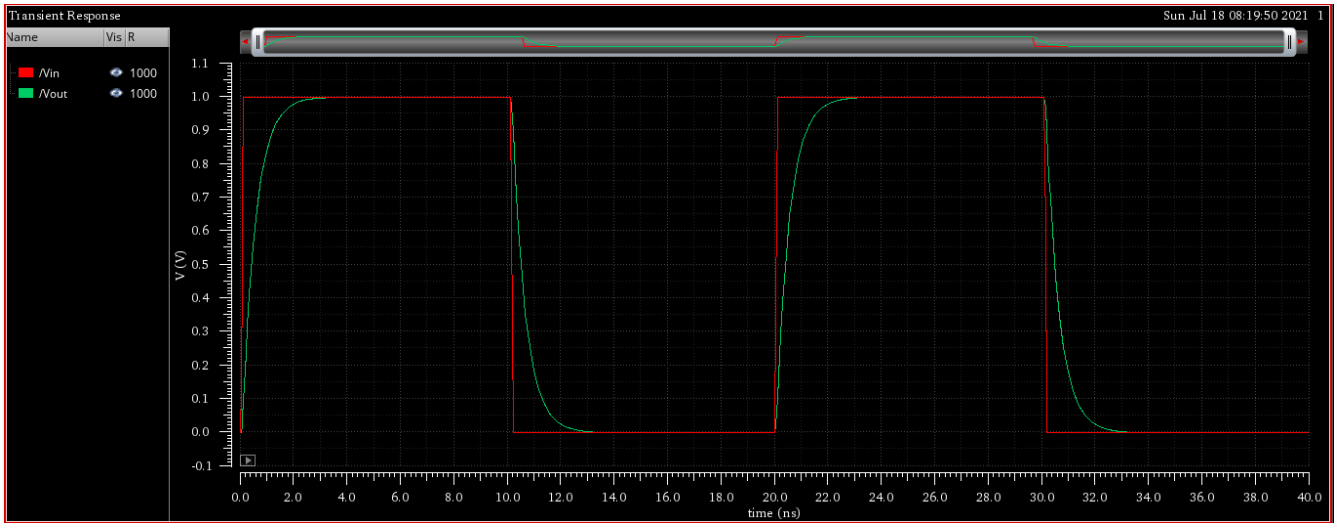

Fig.2 transient analysis by applying two square waves

4) Analytical analysis of fall time and rise time of V_{out}:

$$T_{rise} = T_{fall} = 2.2 * RC = 1.1ns$$

Simulation results for rise time and fall time:

	R	riseTime(... "time")	fallTime(... "time")
1	1.000E3	1.104E-9	1.104E-9

Fig.3 rise time and fall time simulation results

5)

	Simulation Results	Analytical Solution
Rise Time	1.104 ns	1.1 ns
Fall Time	1.104 ns	1.1 ns

And as shown in table that analytical solution is the same of simulation results.

6) Parametric sweep for resistance:

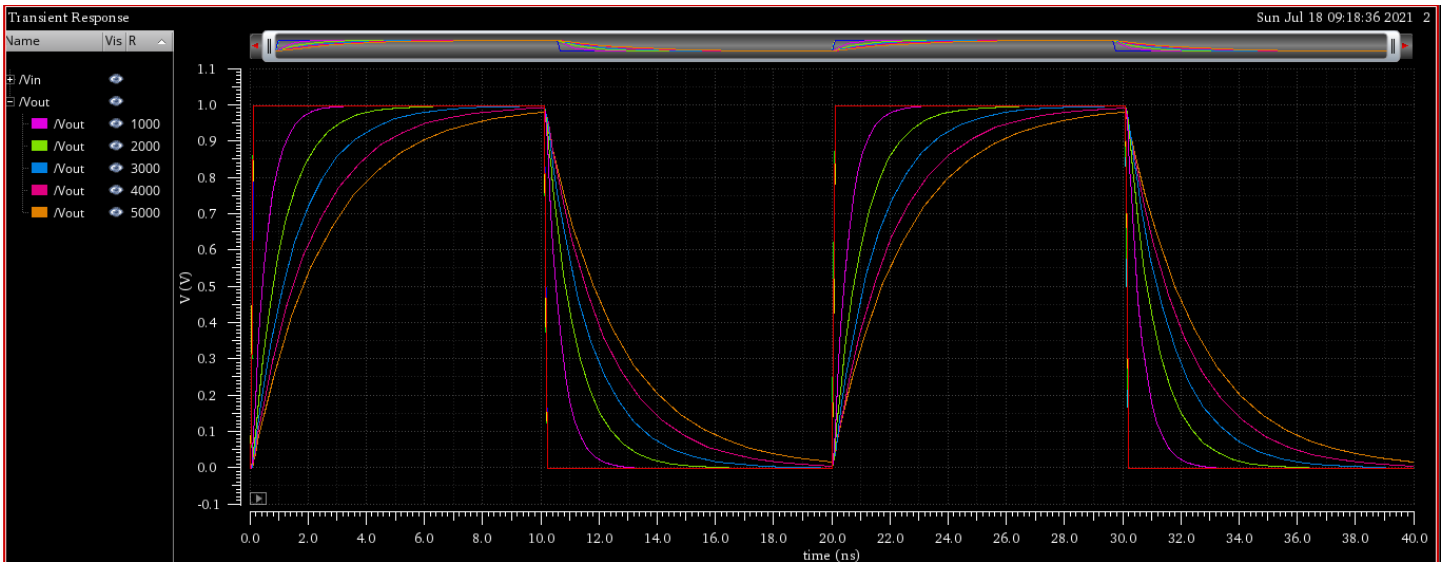

Fig.4 parametric sweep for resistance simulation results

Comment: as shown that by increasing resistance rise time and fall time increases also due to their relation $T_{rise} = T_{fall} = 2.2 * RC$, and also time constant of LPF increase so its cut off frequency decreases follows the relation $\omega_c = \frac{1}{RC}$, and by decreasing cut off frequency of LPF it act as an integrator at very high frequencies.

2.AC Analysis:

1) Bode plot for LPF from cadence:

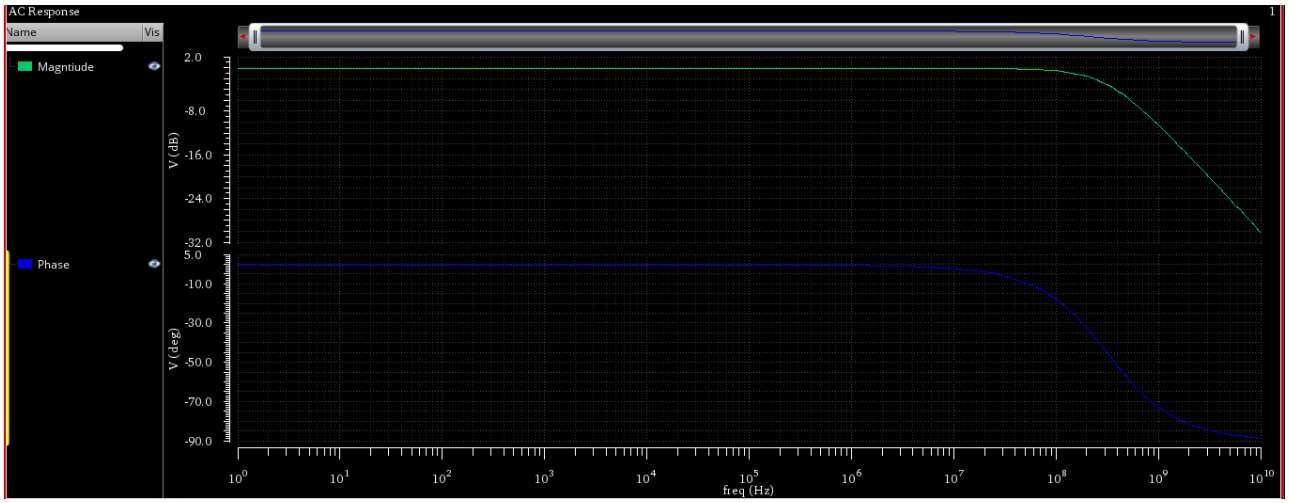

Fig.5 bode plot for LPF

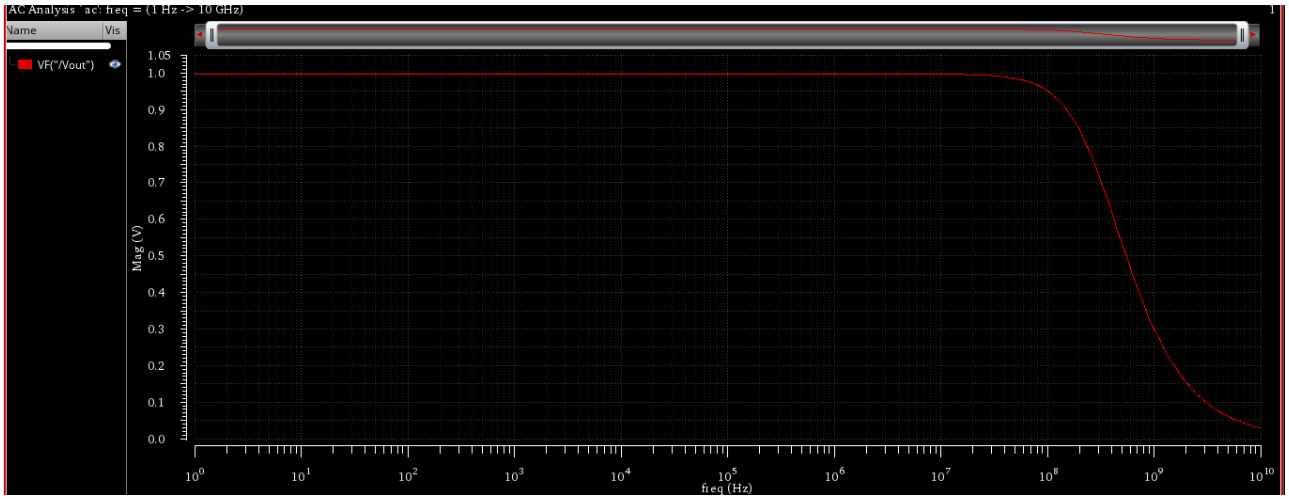

Fig.6 magnitude plot of LPF

2) DC gain and bandwidth from simulation:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Analog_IC_Design_Course:LPF_Simulation:1	/Vout				
Analog_IC_Design_Course:LPF_Simulation:1	DC Gain	1			
Analog_IC_Design_Course:LPF_Simulation:1	3dB-BW	317.6M			

Fig.7 ADXL simulation results for DC gain & BW

3) Analytical results:

- $\omega_c = \frac{1}{\tau} = \frac{1}{RC} \rightarrow F_c = \frac{1}{2\pi RC} = 318.3MHz.$
- DC gain: $A_v = \frac{1}{1+\omega RC} = 1 \ @(\ \omega = 0).$

	Simulation Results	Analytical Solution
3dB-Bandwidth	317.6M	318.3M
DC Gain	1	1

4) Parametric sweep for resistance:

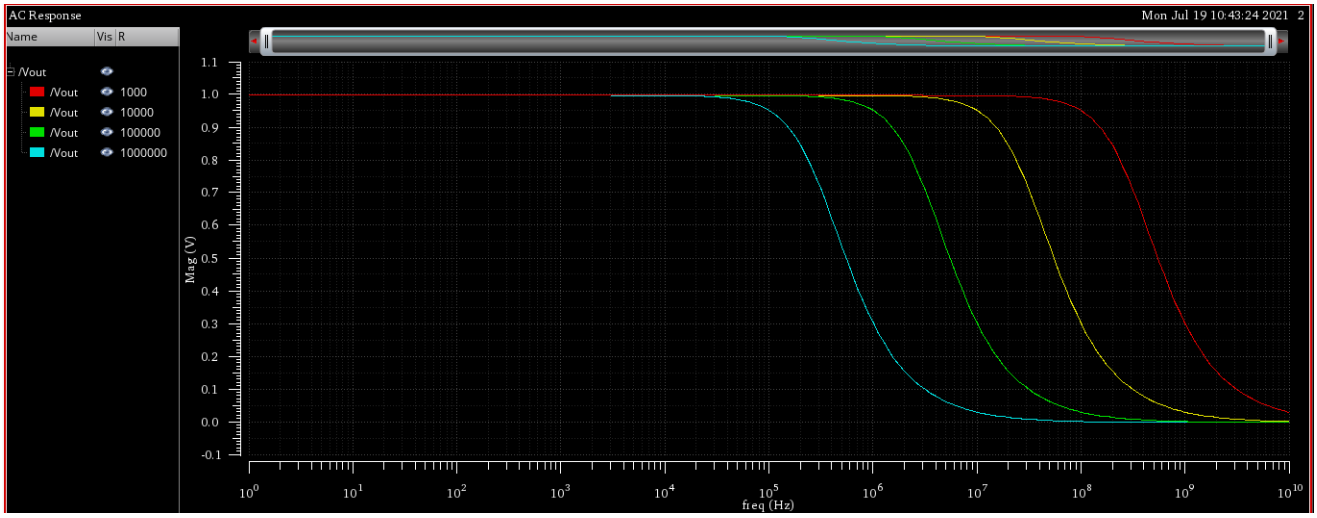

Fig.8 Parametric sweep for resistance at AC analysis

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: R=1k						
1	Analog_IC_...	DC Gain	1			
1	Analog_IC_...	Bandwidth	317.6M			
Parameters: R=10k						
2	Analog_IC_...	DC Gain	1			
2	Analog_IC_...	Bandwidth	31.76M			
Parameters: R=100k						
3	Analog_IC_...	DC Gain	1			
3	Analog_IC_...	Bandwidth	3.176M			
Parameters: R=1M						
4	Analog_IC_...	DC Gain	1			
4	Analog_IC_...	Bandwidth	317.6k			

Fig.9 calculator results for BW and DC gain

Comment: as shown in previous figure that by increasing the value of resistance cut off frequency of LPF decreases which follows this relation

$$F_c = \frac{1}{2\pi RC}.$$

Part 2: MOSFET Characteristics

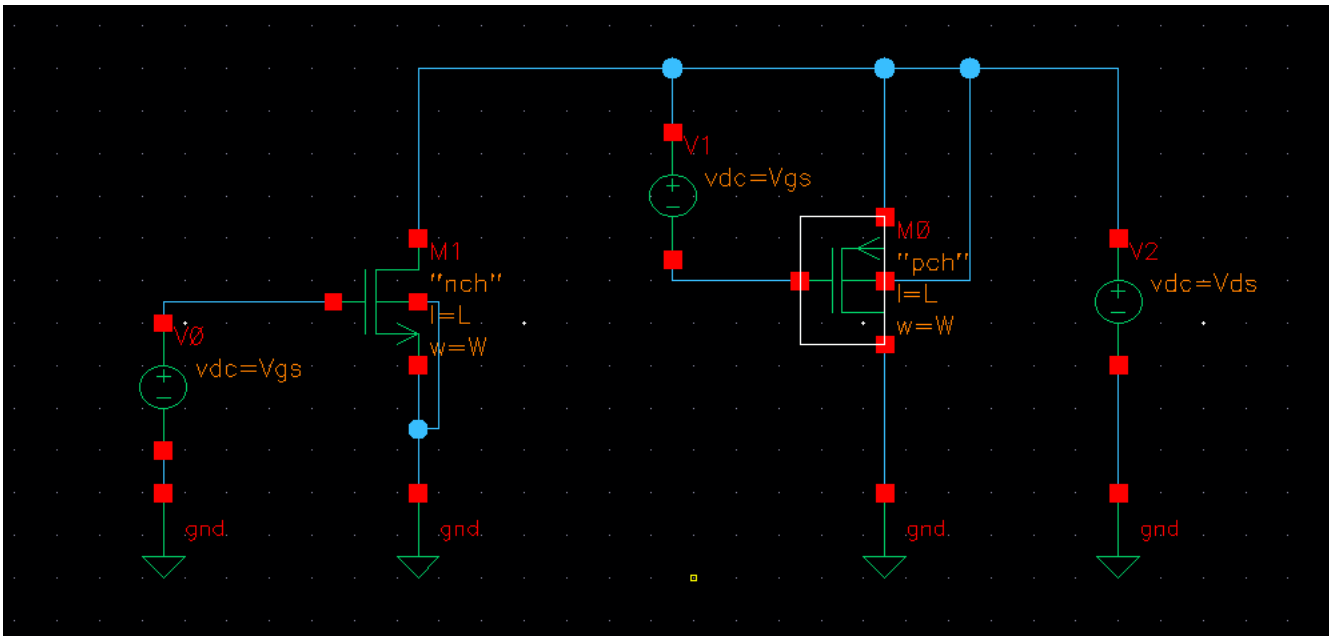

Fig.10 Circuit schematic from cadence

1.ID vs V_{gs} :

1) drain current versus V_{gs} for NMOS and PMOS short channel and long channel:

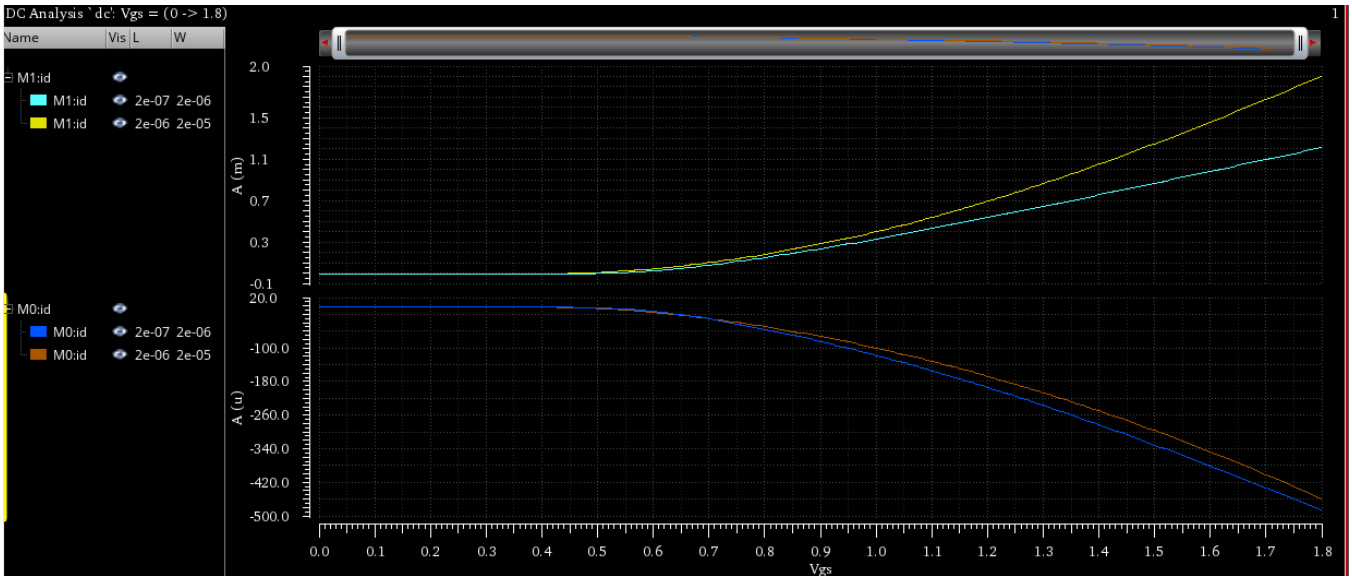

Fig.11 ID vs VGS characteristics for NMOS and PMOS

2) Long Channel vs Short Channel:

- The current of long channel is higher that that of short channel, because in long channel we assume 1D electric field as this field is only controlled by gate voltage, but in case of short channel electric

field is controlled by gate voltage and drain voltage so in this case we assume 2D electric field which decreases drain current.
Also due to wider depletion region in case of short channel than long channel MOSFET, which also affects on drain current by decreasing its value.

- Short channel drain current is considered as linear relation but long channel current considered as quadratic relation, and this because short channel drain current is determined by velocity saturation so drain current become proportional to VGS following realation: $I_D = WC_{ox}(V_{gs} - V_{th})v_{sat}$, but in case of long channel drain current is proportional V_{gs}^2 following relation: $I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_{gs} - V_{th})^2$.

3) NMOS vs PMOS:

- The current of NMOS is higher than current of PMOS due to the effect of mobility as the mobility of electrons is higher than mobility of holes so NMOS has higher current as the following realtion: $I_D = \frac{1}{2}\frac{W}{L}\mu C_{ox}(V_{gs} - V_{th})^2$.
- The ratio between current of NMOS to current of PMOS will depend totally on mobility of electrons and holes, as they have the same channel length, width and same bais VGS so ratio will be as following: $\frac{I_{Dn}}{I_{Dp}} = \frac{\mu_n}{\mu_p} = 2\sim4$.
- As shown in the previous figure that short channel effect appears strongly in case of NMOS more than case of PMOS.

2. g_m vs V_{gs} :

1) g_m of PMOS and NMOS versus bias voltage VGS of short channel and long channel overlaid:

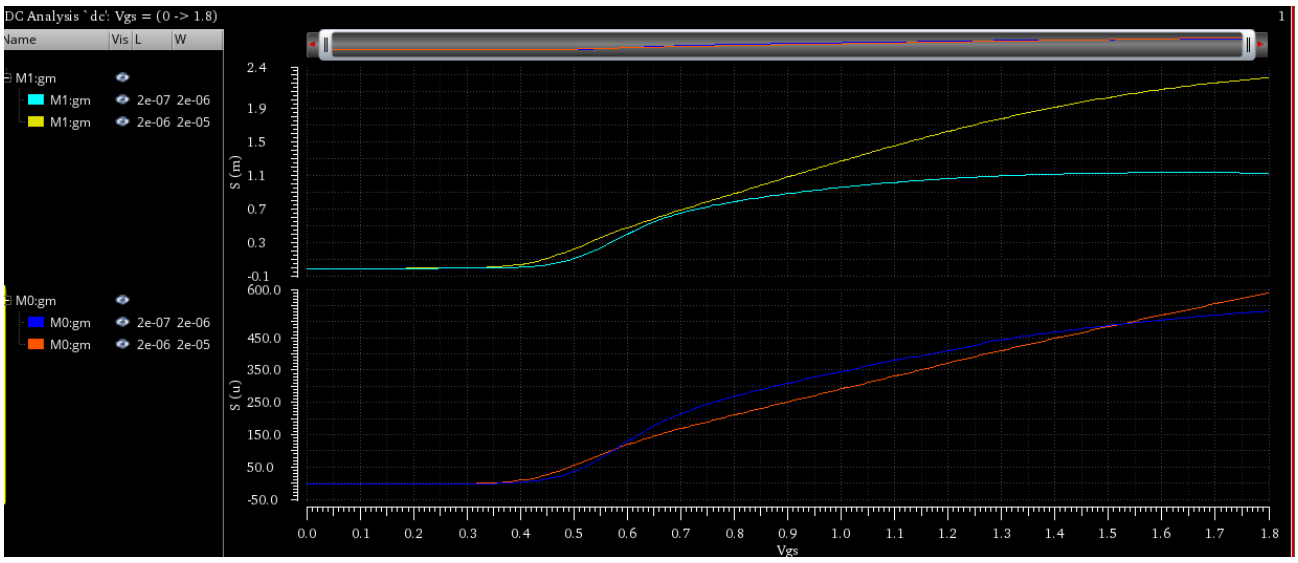

Fig.12 gm vs VGS plot from cadence

2) Long Channel vs Short Channel:

- As we know that g_m is the change of drain current to change of gate current $g_m = \frac{\Delta I_D}{\Delta V_{gs}}$, so g_m is linear in case of long channel effect as $g_m \propto V_{gs}$, and in case of short channel it can be considered as step function as $g_m = const$, this due to linear relation between drain current and V_{gs} .
- As shown in above figure that g_m saturates in case of short channel MOSFET only as it considered as a step function, but in case of long channel g_m increases by increasing the value of V_{gs} as we set $\frac{W}{L}$ to be constant in case of our lab.

3.I_D vs V_{ds}:

1) drain current versus VDS for NMOS short channel and long channel and sweeping VGS from 0:0.2:1.8v by parmetric sweep:

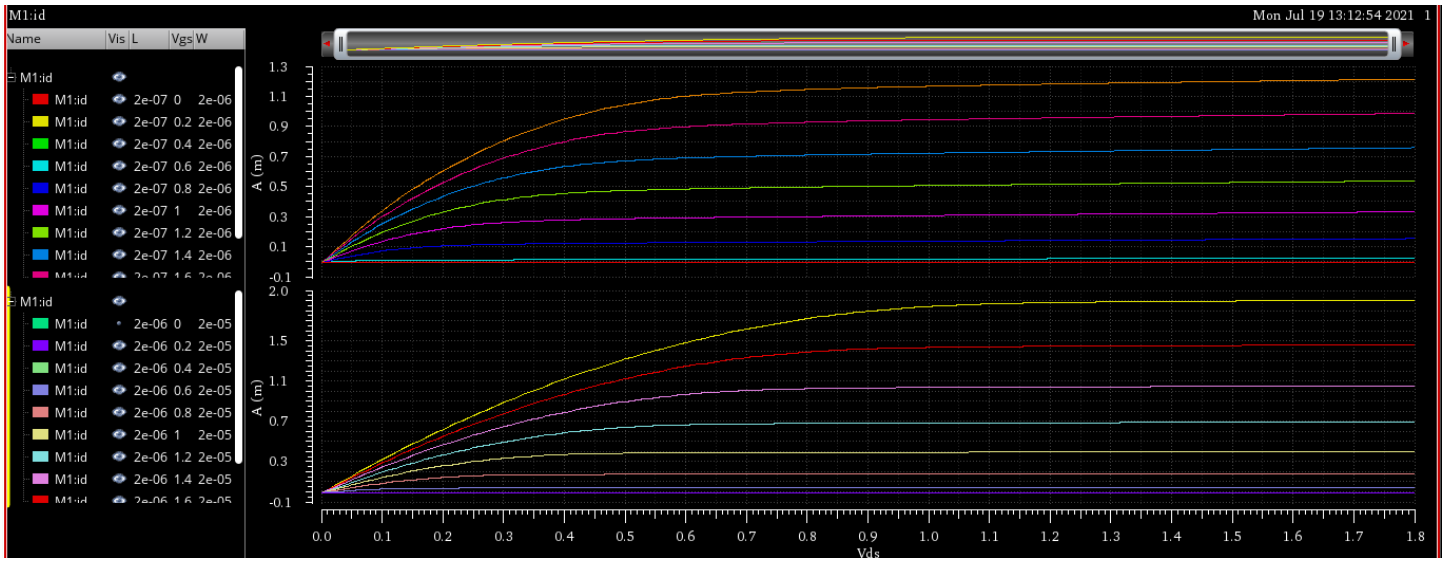

Fig.13 ID vs VDS for long channel NMOS

2) Long Channel vs Short Channel:

- As shown in above figure that long channel MOSFET have higher current than short channel MOSFET, this due to the depletion region width which is higher in case of short channel than case of long channel, and also due to drain induced barriar lowering effect, and also gate voltage lose control on drain current.
- Long channel MOSFET has higher slope in saturation region than short channel MOSFET, because as we see that the steps between different curves of sweeping gate voltage in case of long channel is quadrtic but linear steps in case of short channel due to velocity saturation effect which dominant in case of short channel MOSFET.