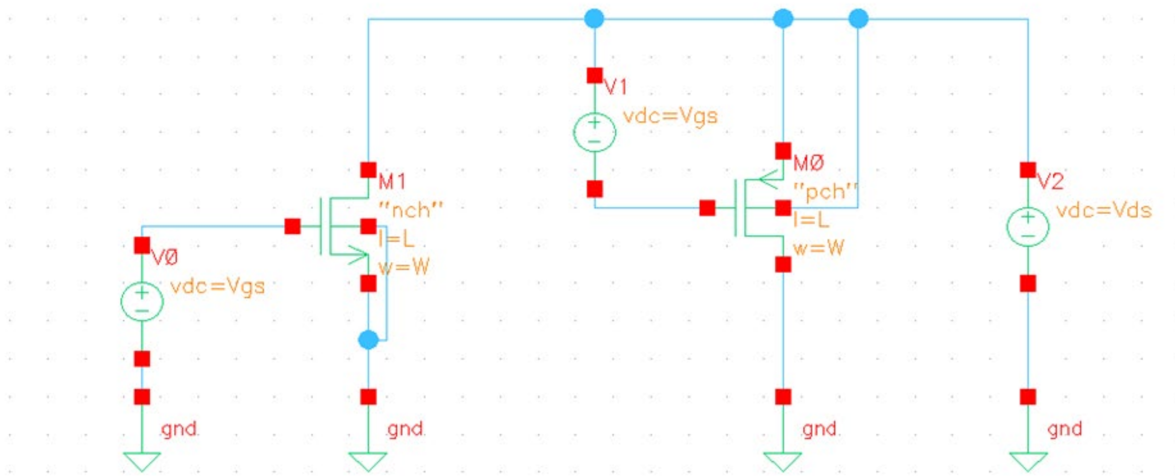
Lab 06

Differential Amplifier

Part 1: Sizing Chart

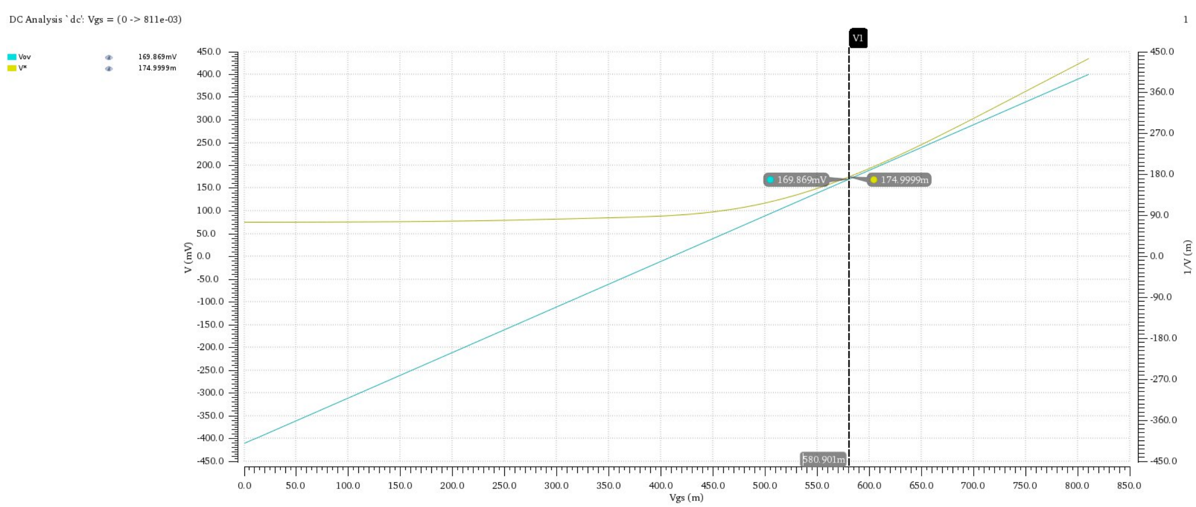
- Given Parameters in this Lab:

MOSFET Length L	1um
Supply Voltage V_{ds}	1.8V
Tail Current I_{ss}	40uA
Differential Gain	8
Common Mode Output Level	0.7



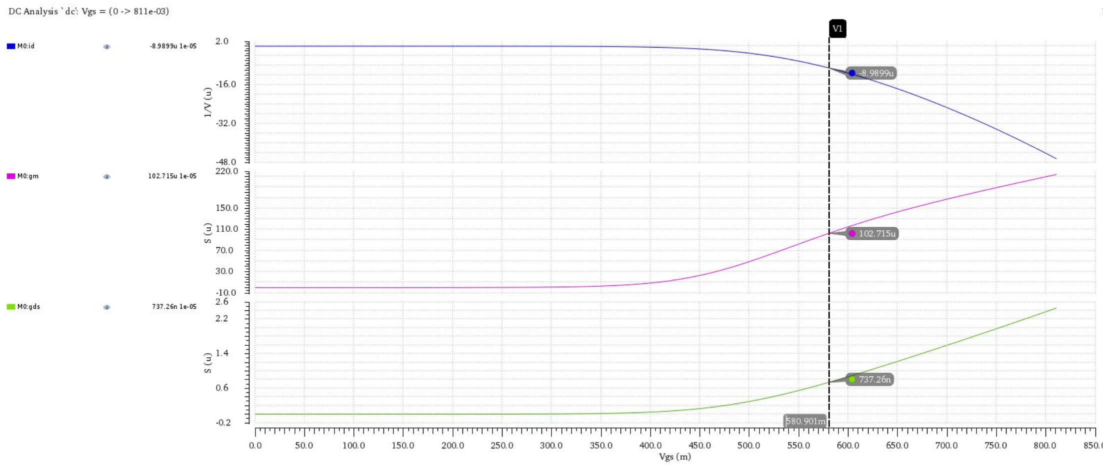
Schematic used in sizing

As $A_V = \frac{2*V_{RD}}{V^*} \rightarrow V^* = \frac{2*V_{RD}}{A_V} = 0.175v.$



Vov & V* versus Vgs sweep

From previous graphs we find at $V_Q^* = 175mV \rightarrow V_{gsQ} = 580.901mV\ and\ V_{ovQ} = 169.896mV.$



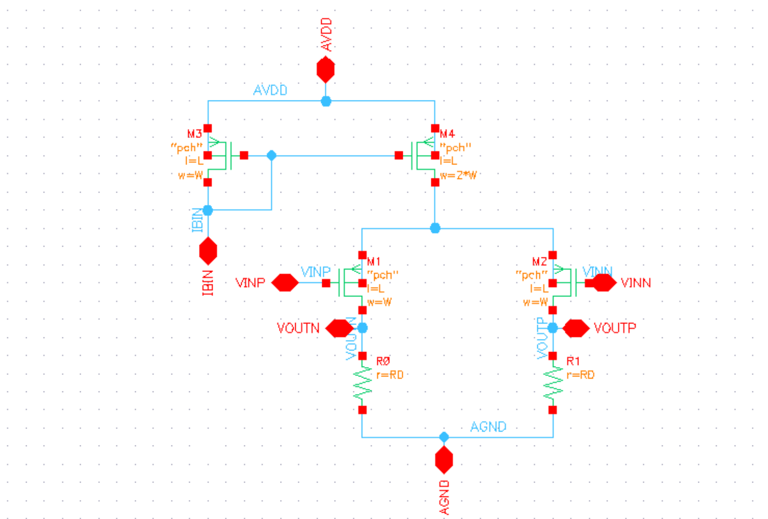
I_D, g_m and g_{ds}versus V_{gs}

From previous graph at $V_{gs} = 580.901mV$, we have $I_{dX} = 8.9899uA, g_{mX} = 102.715uS$ and $g_{dsX} = 737.26nS$.

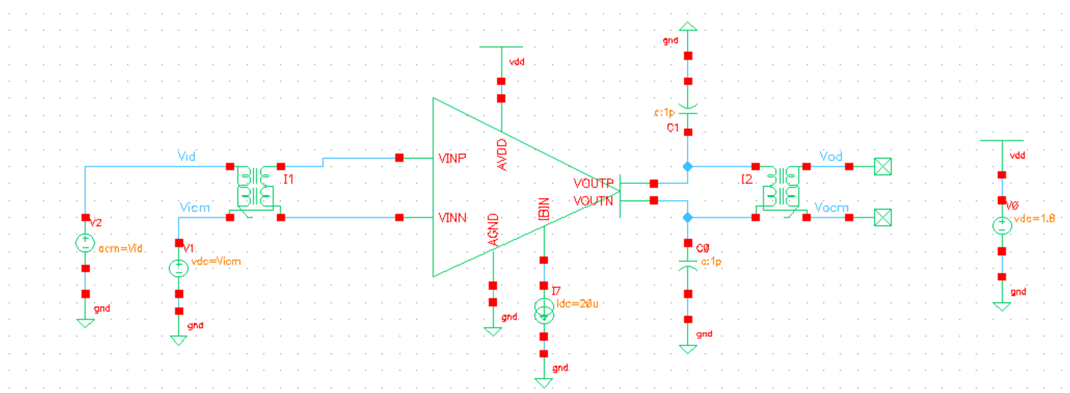
Using cross multiplication as $I_d \propto W$, we find that W=11.126um.

Also $g_m = 114.28uS, and$ $g_{ds} = 820.275nS$ @ W=11.126um.

Part 2: Differential Amplifier



Differential pair schematic

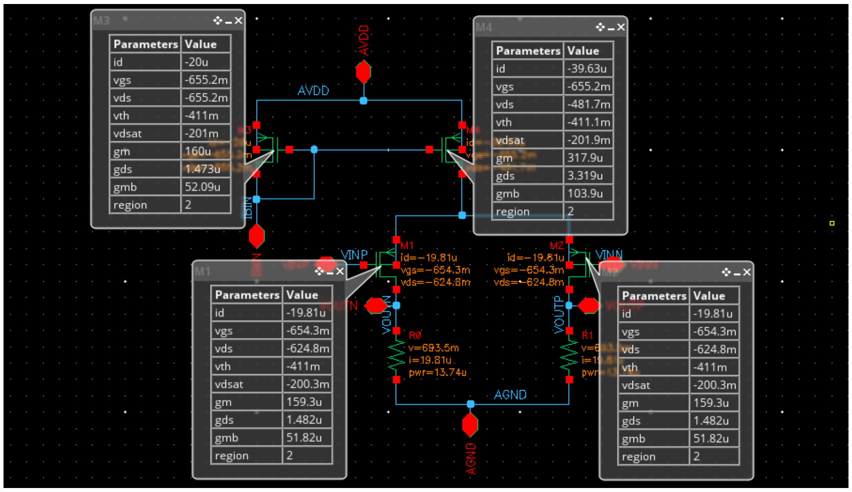


Differential pair symbol + testbench

- Input Common Mode Calculations:

$$V_{icmMAX} = -V_{gs} - V^{*} + V_{dd} = -580.901m - 175m + 1.8 = 1.044\ V$$
$$V_{icmMIN} = -V_{th} + V_{RD} = -411m + 0.7 = 0.289\ V$$
$$V_{icm} = \frac{V_{icmMAX} + V_{icmMIN}}{2} = 0.664\ V$$

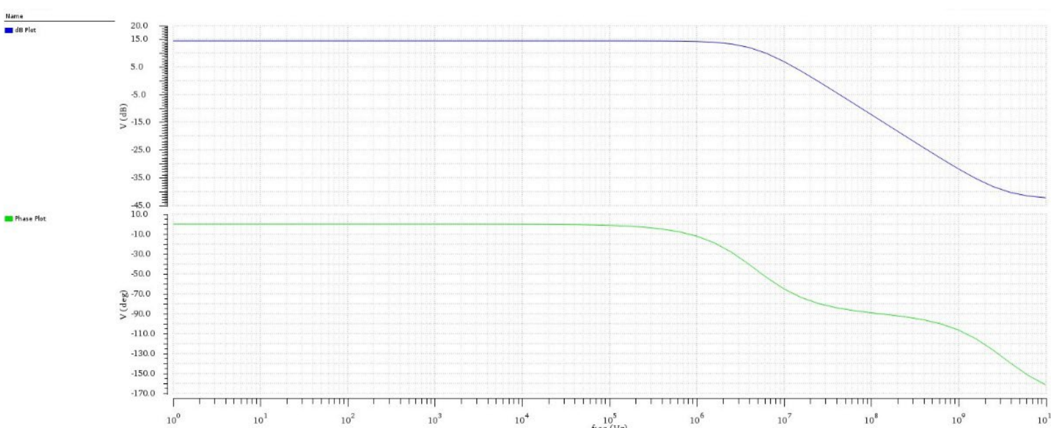
1) OP Simulation:



Op analysis results from cadence simulation

As shown that all MOSFET's regions equal 2 which mean that all transistors in saturation.

2) Diff Small Signal css:



Bode plot of small signal differential gain

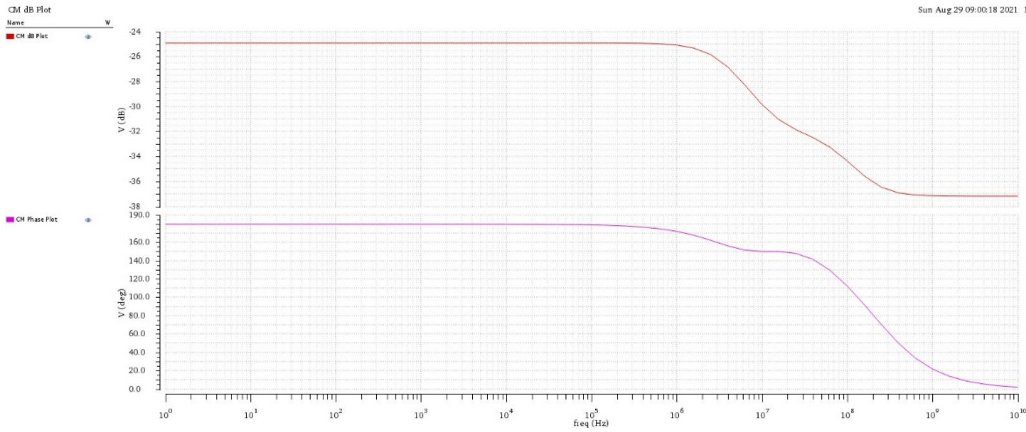
Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:lab06_Diff_testbench:1	Mag Plot				
TrainLAB:lab06_Diff_testbench:1	Gain Mag	5.299			
TrainLAB:lab06_Diff_testbench:1	Phase Plot				
TrainLAB:lab06_Diff_testbench:1	Gain dB	14.48			
TrainLAB:lab06_Diff_testbench:1	BW	4.763M			

DC gain and bandwidth from simulation results

- Analyitical Results:

$$V_{RD} = I_D * R_D \rightarrow R_D = \frac{V_{RD}}{I_D} = \frac{0.7}{20u} = 35k\Omega$$
$$|A_V| = g_m * R_D = 159.3u * 35k = 5.5755$$
$$BW = \frac{1}{2\pi * RD * CL} = 4.547MHz$$

3) CM Small Signal css:



Bode plot of CM small signal gain

Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:lab06_Diff_testbench:1	CM Gain	56.93m			
TrainLAB:lab06_Diff_testbench:1	CM Gain dB	-24.89			
TrainLAB:lab06_Diff_testbench:1	CM BW	5.764M			
TrainLAB:lab06_Diff_testbench:1	CM dB Plot				
TrainLAB:lab06_Diff_testbench:1	CM Phase Plot				
TrainLAB:lab06_Diff_testbench:1	CM Mag Plot				

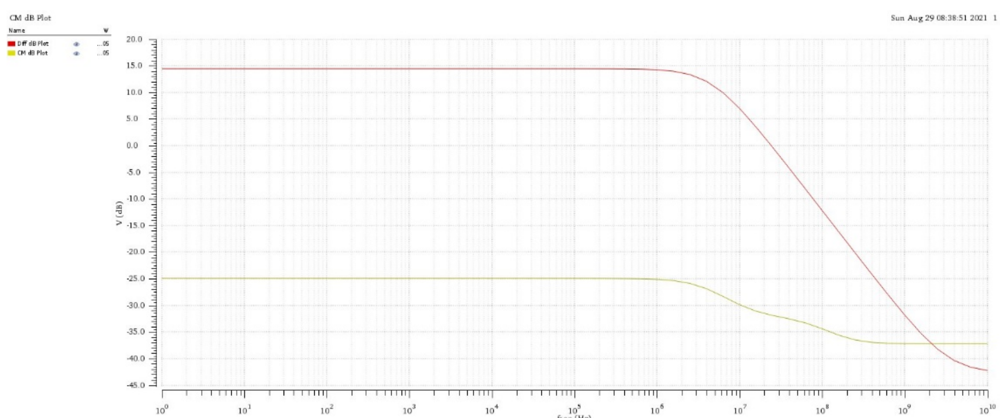
DC gain and bandwidth from simulation results

- Analytical Results:

$$|A_V| = \frac{g_m * R_D}{1 + 2(g_m + g_{mb})R_{ss}} = 43.4m$$

CM small signal gain is less than 1 as the common mode is partially rejected, and not affect on the output due to degeneration by large resistance Rss.

- The variations in Avcm at high frequency gain because tail current source is shunted by capacitance so at high frequency another pole due to this capacitance come to action which affects on bode plot and also impedance increases.



Avd & Avcm dB Plots

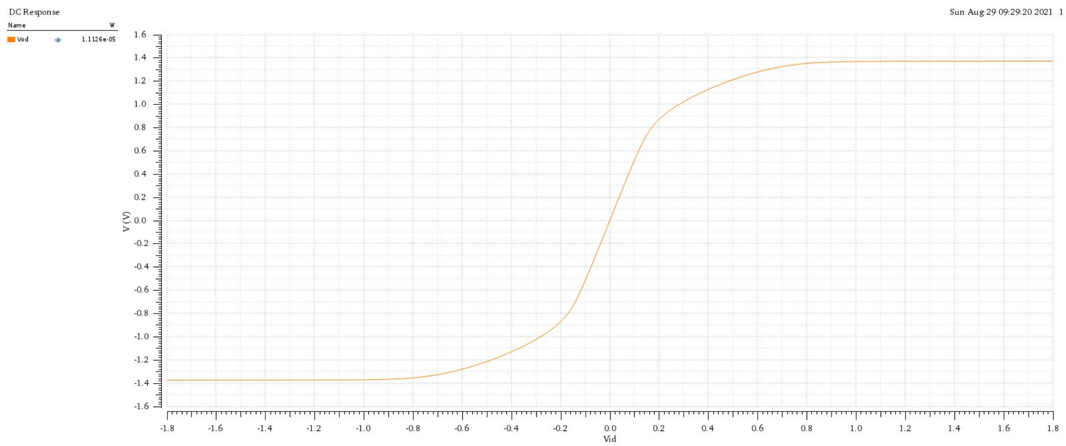
As shown simulation results will be 93.07

- Analytical Results:

$$CMRR = \frac{A_{vd}}{A_{vCM}} = 2(g_m + g_{mb})R_{SS} = 127.8$$

- Variation at high frequency due to capacitance which shunt Rss and decrease impedance and come into action with pole.

4) Diff Large Signal css:

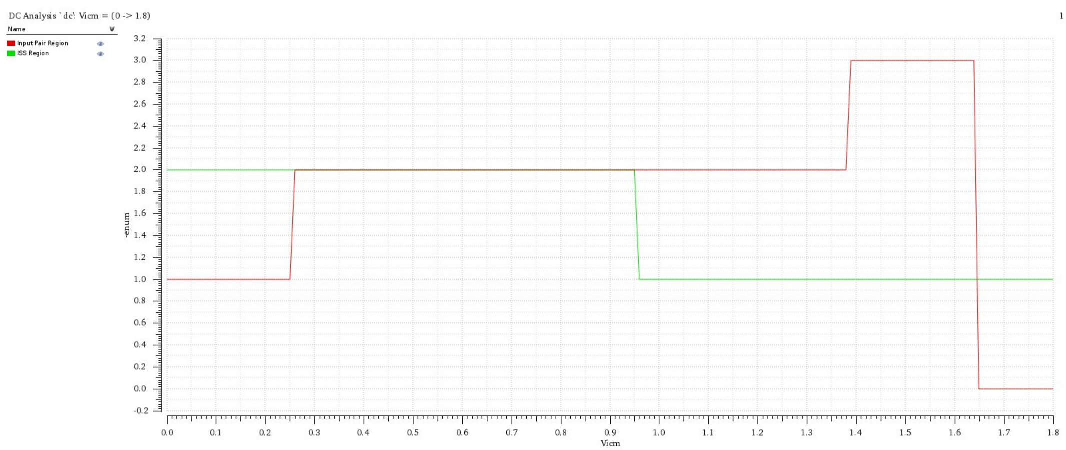


Vid versus sweep Vod

- Analytical solution for valid range:

$$-R_D * I_{SS} \rightarrow R_D * I_{SS} = -1.4 \rightarrow 1.4$$

5) CM Larg Signal css:



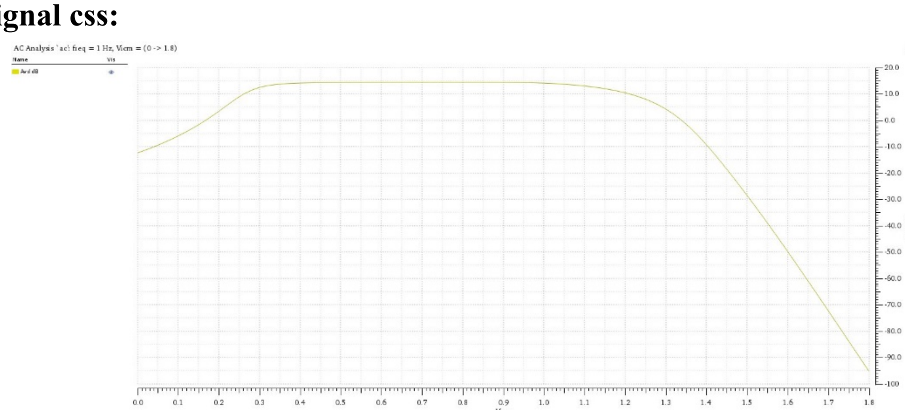
Region versus Vicm sweep

- Input common mode range from simulation as shown from 0.29 to 0.98 which meet with hand analysis results for CMIR

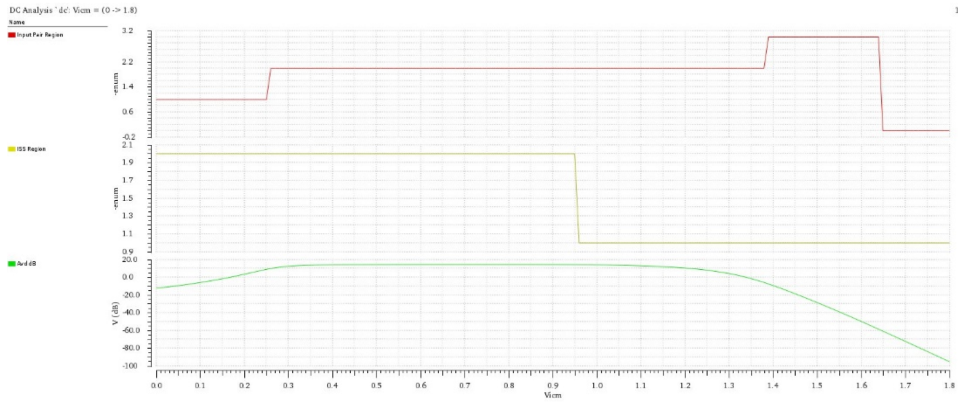
$$V_{icmMAX} = -V_{gs} - V^* + V_{dd} = -580.901m - 175m + 1.8 = 1.044\ V$$

$$V_{icmMIN} = -V_{th} + V_{RD} = -411m + 0.7 = 0.289\ V$$

6) CM Larg Signal css:



Vid versus Vicm sweep @ f=1Hz



Regions and Vid versus CM at certain frequency