Lab 04

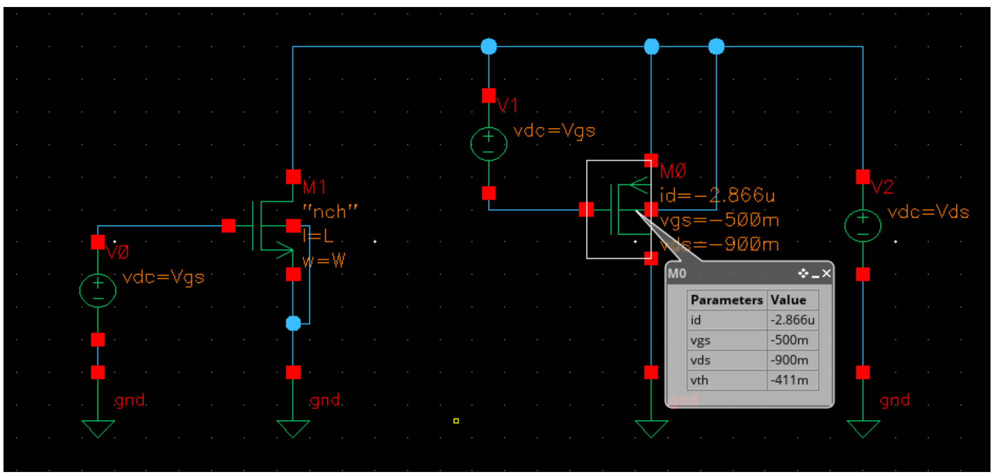
Common Drain Frequency Response

Part 1: Sizing Chart

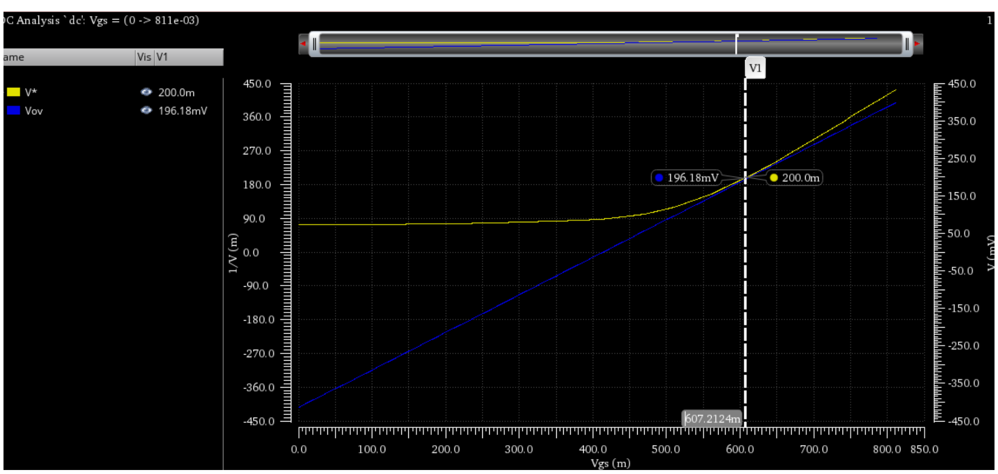
- Given Parameters in this Lab:

MOSFET Length L	1um
Supply Voltage V_{ds}	1.8V
Drain Current I_D	10uA
Real MOSFET Overdrive Voltage V^*	0.2V

- Determine PMOS Width Value (W):

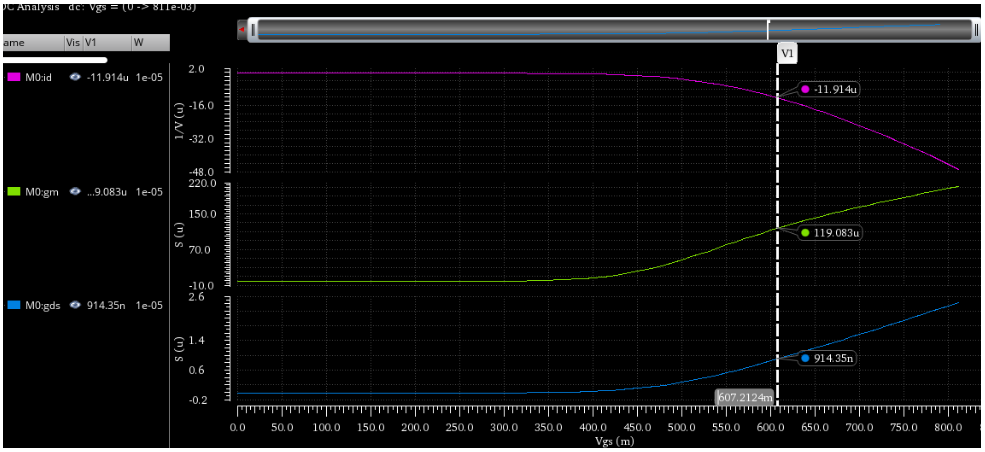


Design used for determine PMOS width



Vov & V* versus Vgs sweep

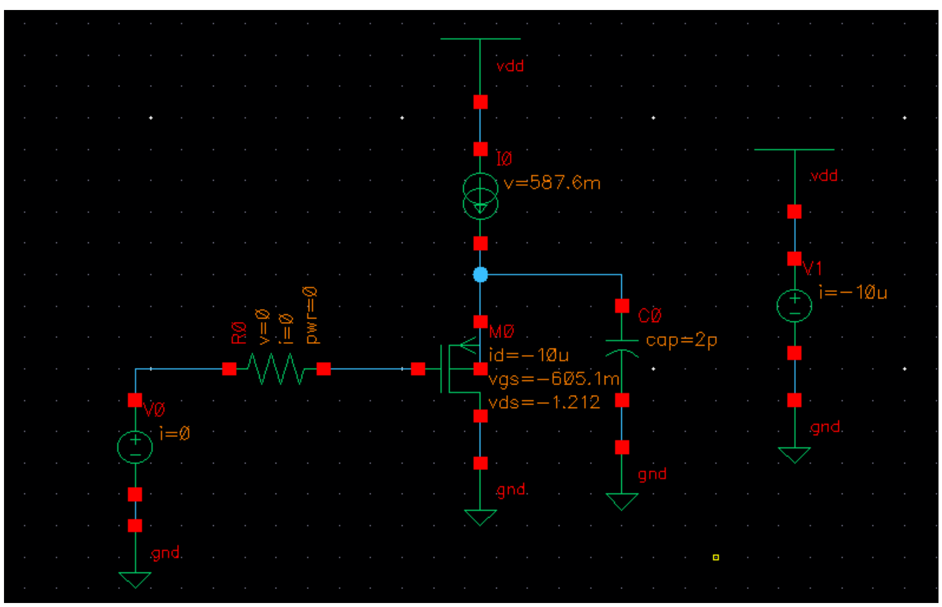
From previous graphs we find at $V_Q^* = 200mV \rightarrow V_{gsQ} = 607.2124mV\ and\ V_{ovQ} = 196.18mV$.



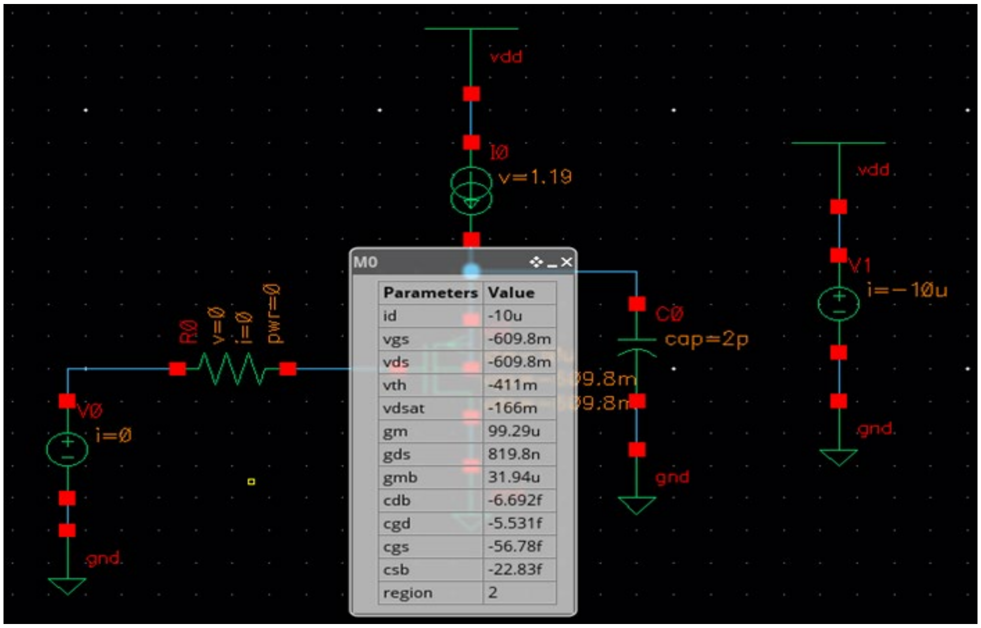
From previous graph at $V_{gs} = 607.2124mV$, we have $I_{dX} = 11.914uA, g_{mX} = 119.083uS\ and\ g_{dsX} = 914.35nS$.
Using cross multiplication as $I_d \propto W$, we find that W=8.39um.
Also $g_m = 100uS, and\ g_{ds} = 767.14nS$ @ W=8.39um.

Part 2: CD Amplifier

1. OP Analysis:



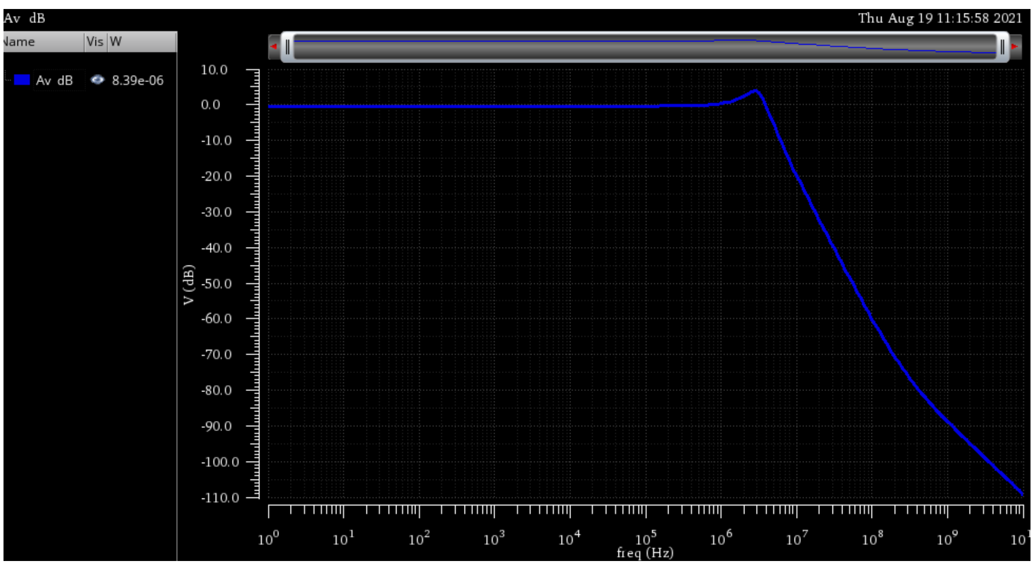
Circuit schematic for common drain amplifier



OP parameters for PMOS used in CD

- As shown region =2 so it operates in saturation

2. AC Analysis:



Bode plot magnitude for CD gain

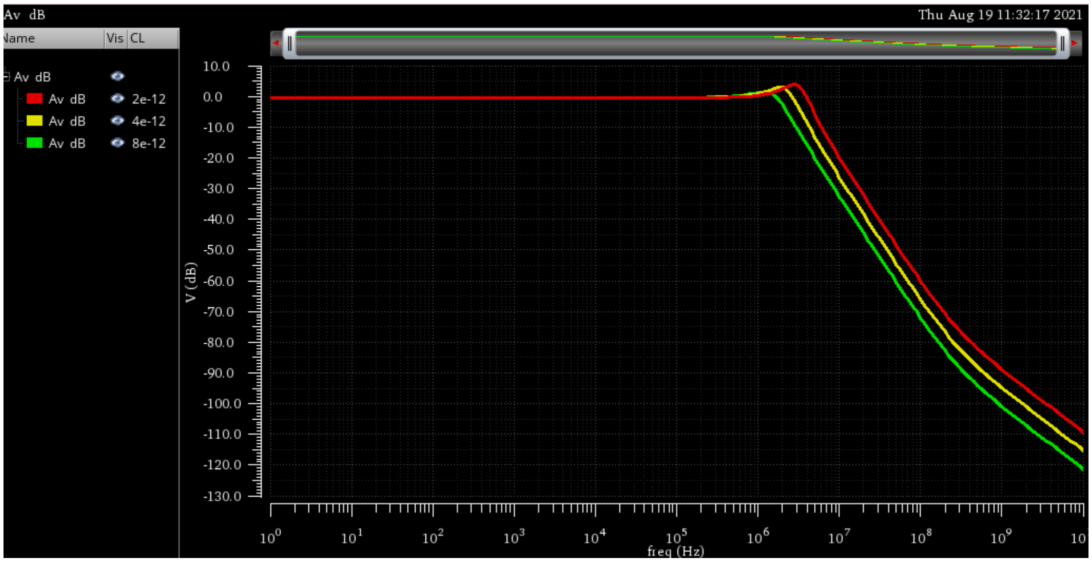
- As shown from previous figure that there is a peaking in frequency domain which equals 4.288 dB.
- Quality Factor Calculations:

$Q = \sqrt{\frac{g_m(C_{gs}+C_{gd})R_{sig}}{C_L}}$=2.487, and hence Q>0.707 so system is underdamped system which proves peaking happens in frequency domain.

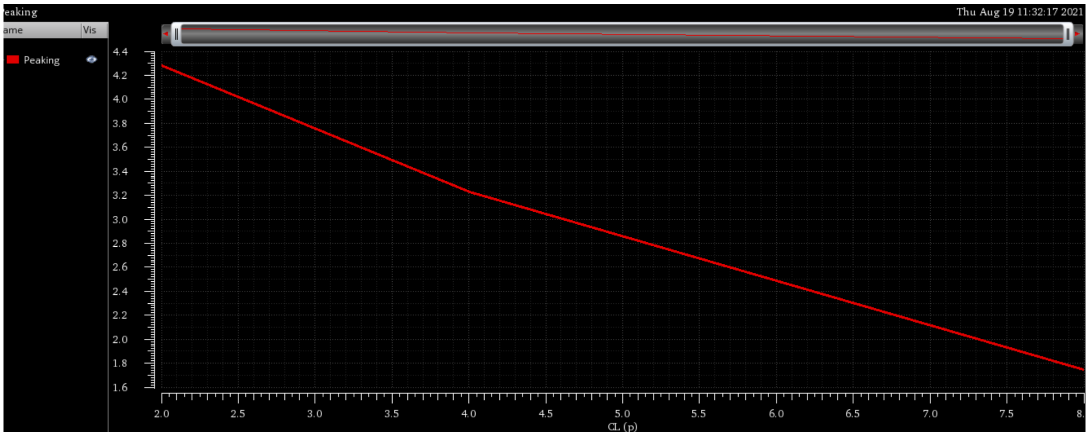
- Parametric Sweep for C_L:

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: CL=2p						
1	TrainLAB:CD_Lab4:1	Av dB				
1	TrainLAB:CD_Lab4:1	Peaking	4.288			
Parameters: CL=4p						
2	TrainLAB:CD_Lab4:1	Av dB				
2	TrainLAB:CD_Lab4:1	Peaking	3.237			
Parameters: CL=8p						
3	TrainLAB:CD_Lab4:1	Av dB				
3	TrainLAB:CD_Lab4:1	Peaking	1.753			

CL parametric sweep results for CD



Bode plot magnitude of gain after sweep load capacitance CL

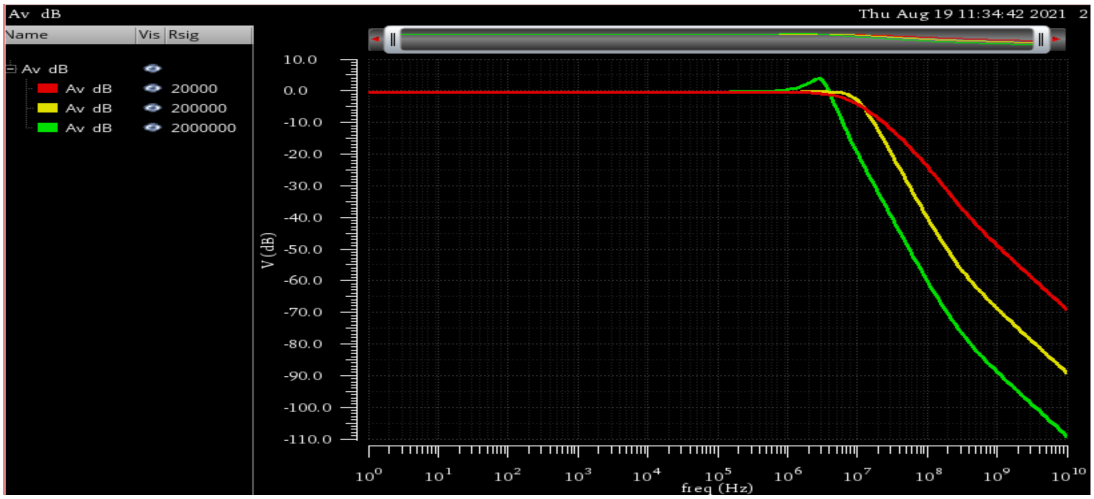


Peaking versus load capacitance CL

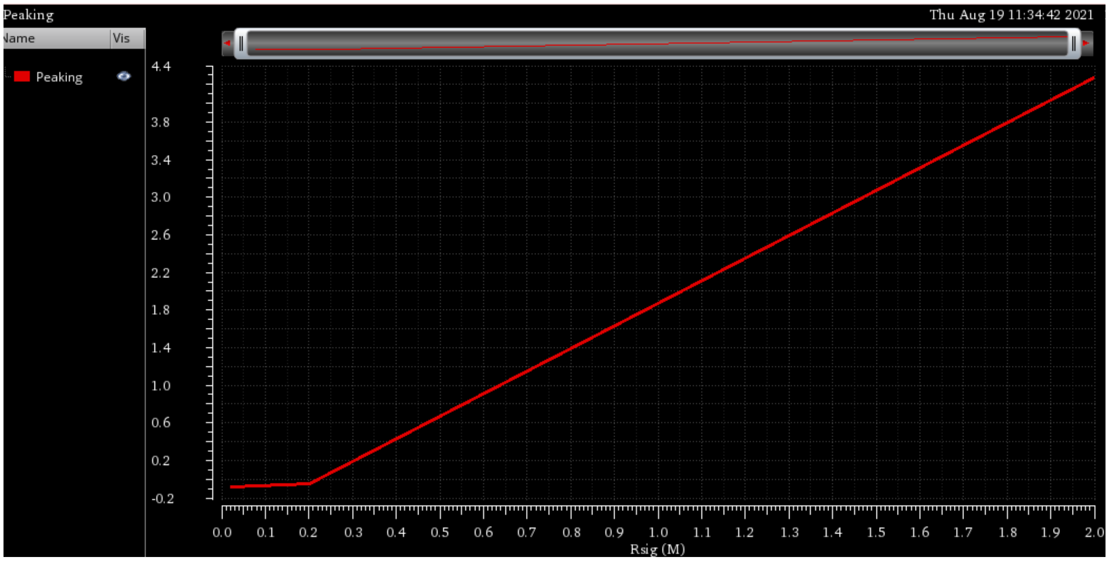
Comment:

From previous results as shown that by increasing CL peaking decrease because that quality factor decreases also so it doesn't become underdamped anymore.

- Parametric Sweep for R_{sig}:



Bode plot magnitude of gain after sweep Rsig

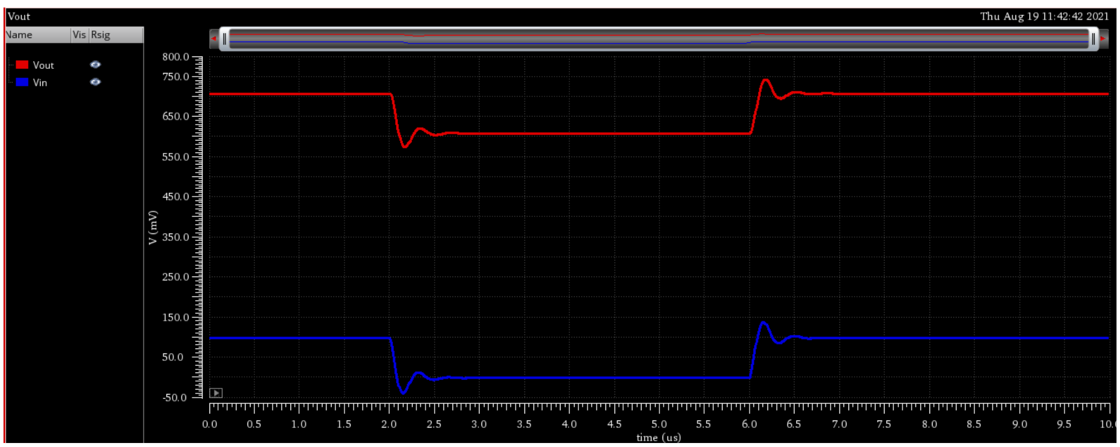


Peaking versus Rsig

Comment:

As shown that by increasing Rsig quality factor increases and also peaking increases.

3. Transient Analysis:



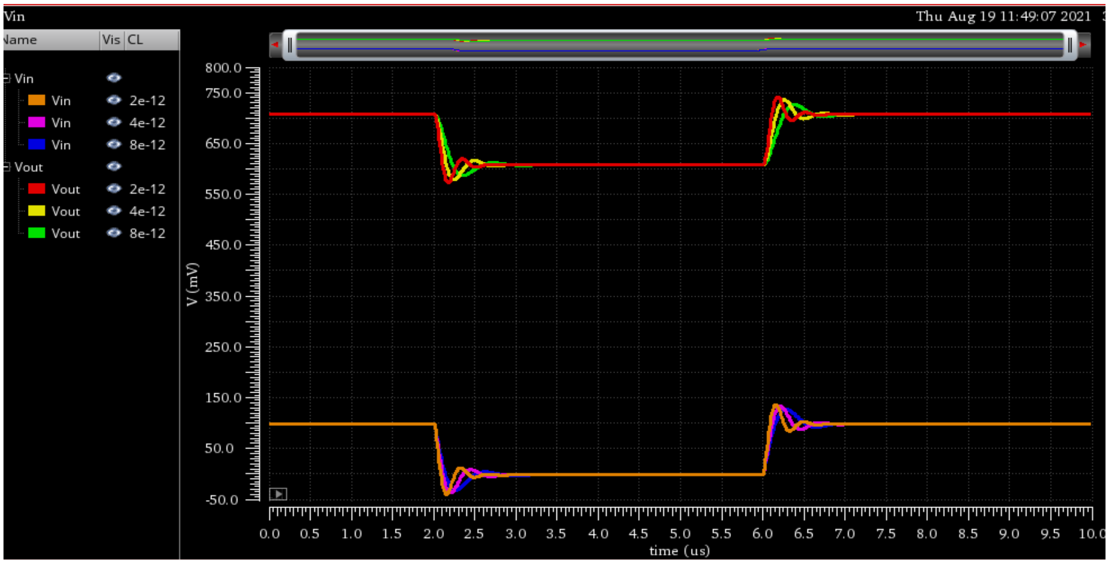
Vin & Vout versus time

- DC Shift between Vout&Vin:
  1) DC shift between Vin and Vout equals Vgs because common drain amplifier considered as voltage buffer (source follower), so it doesn't affect on gain but only shift DC level for input signal.
  2) If we want to shift signal down use NMOS common drain stage.
- As shown from previous figure that there is ringing in time domain because our system is underdamped system as have been proved in previous part from quality factor calculations.
- Overshoot equals from cadence 34.83%

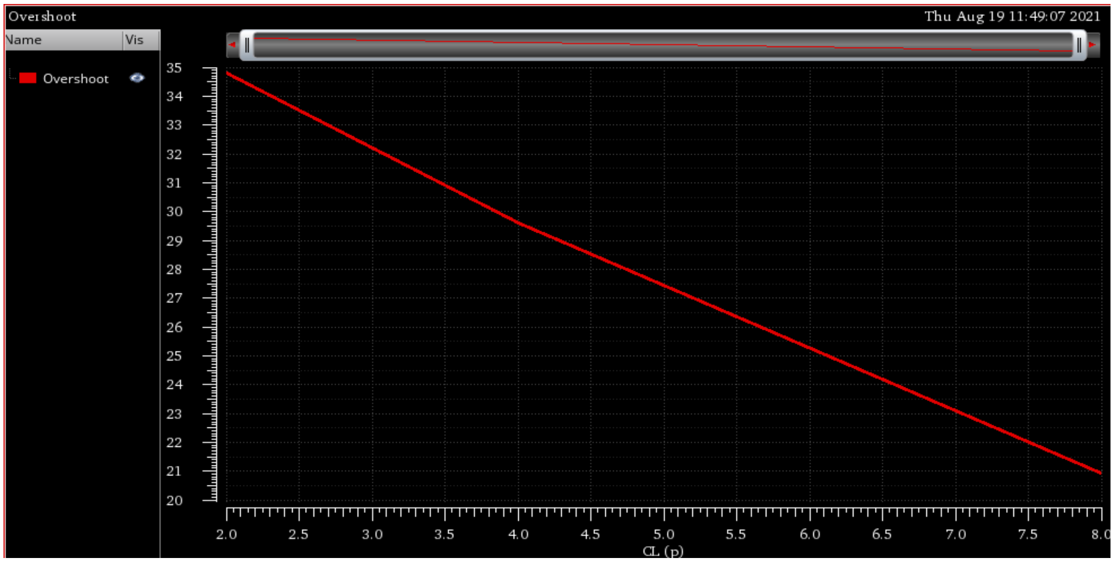
Parameters: CL=2p						
1	TrainLAB:CD_Lab4:1	Vout				
1	TrainLAB:CD_Lab4:1	Vin				
1	TrainLAB:CD_Lab4:1	Overshoot	34.83			

Overshoot results from ADXL cadence

- Parametric Sweep for CL:



Vout & Vin versus time after CL parametric sweep



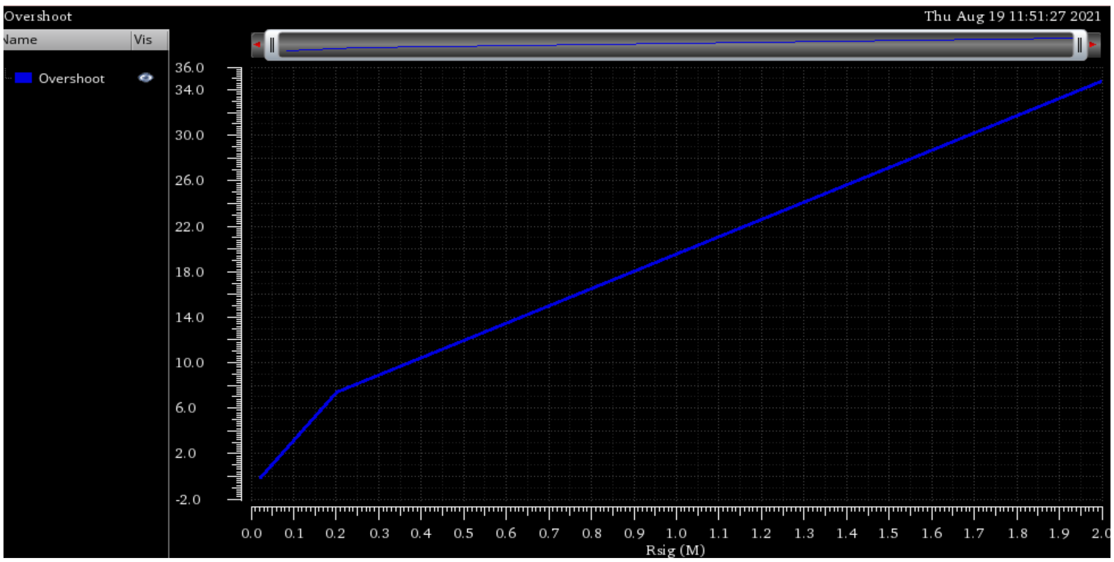
Overshoot versus CL sweep

Comment:

From previous results as shown that by increasing CL overshoot decrease because that quality factor decreases also so it doesn't become underdamped anymore.

- Parametric Sweep for R_{sig}:

Vout & Vin versus time after Rsig parametric sweep

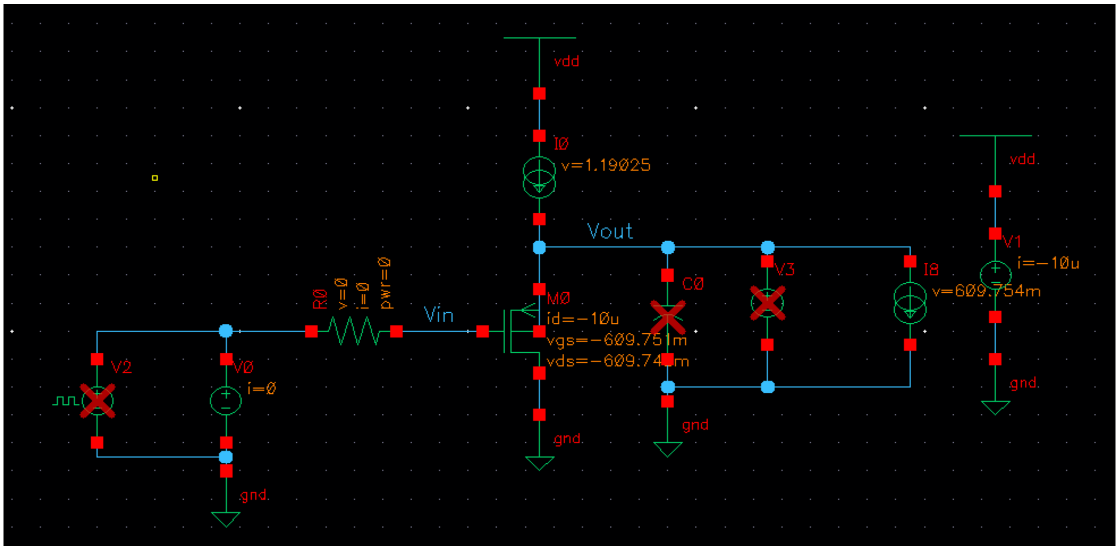


Overshoot versus CL sweep

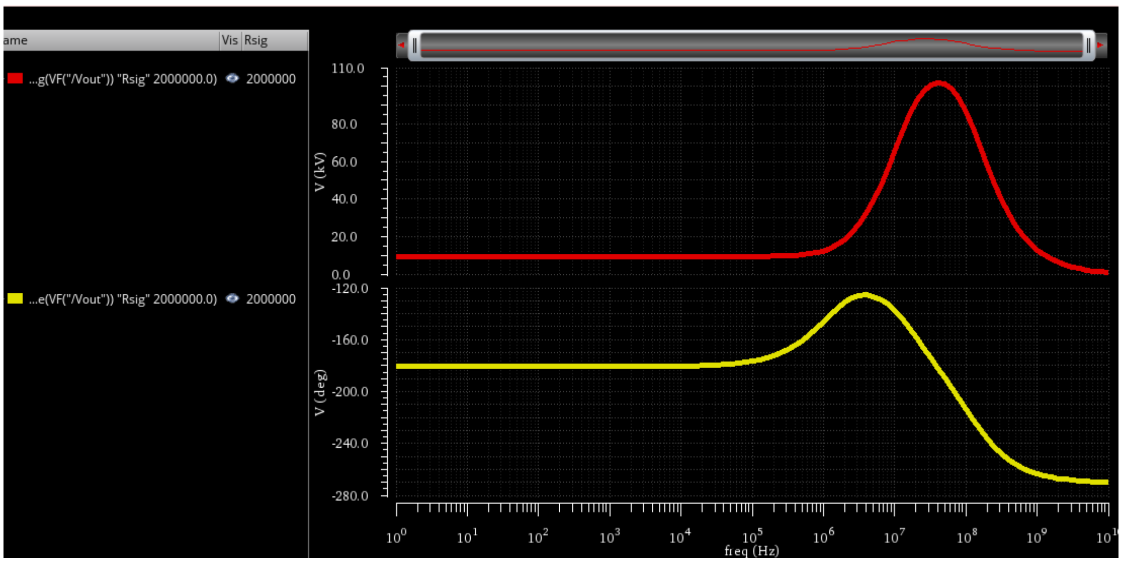
Comment:

As shown that by increasing Rsig quality factor increases and also overshoot increases.

4. Z_{out} (Inductive Rise):



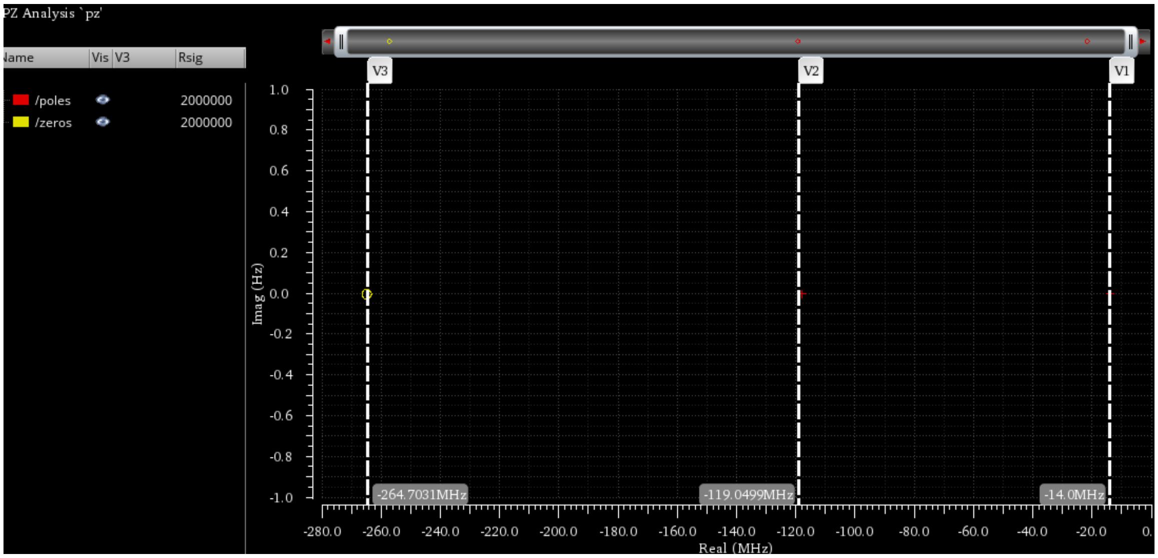
Circuit schematic for Zout calculations



Zout magnitude and phase versus frequency

- From previous analysis there is an inductive rise in output impedance because Rsig get into action at certain frequency and become greater than 1/gm.
- Yes, output impedance falls at high frequency as shown because of Cgd which become effective at high frequencies.

- Pole Zero Analysis:



s-plan for pole zero analysis Zout results