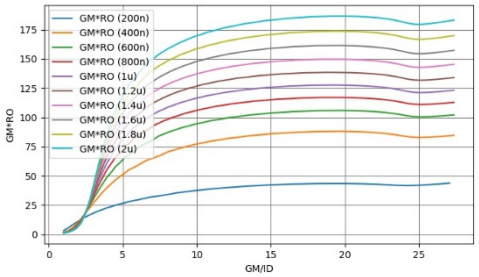
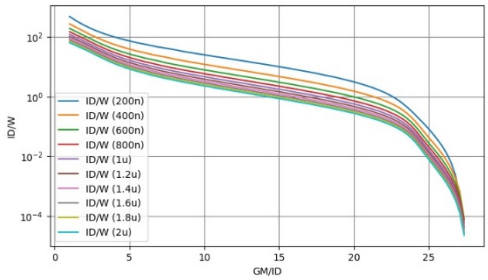
Lab 07

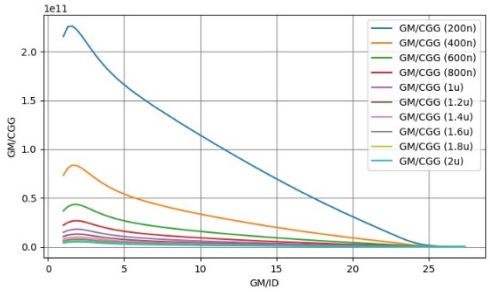
gm/ID Design Methodology

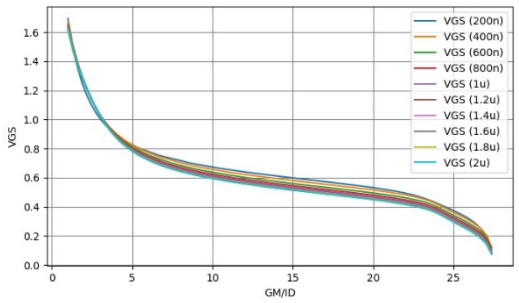
Part 1: gm/ID Design Curves

- NMOS Design Charts from ADT:

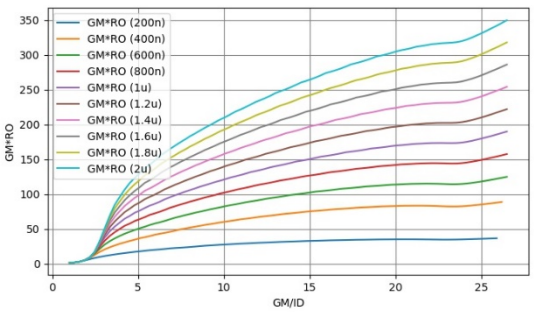


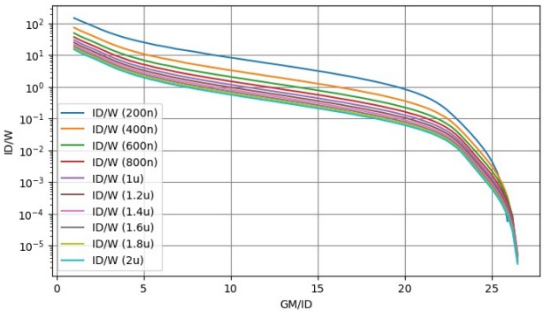


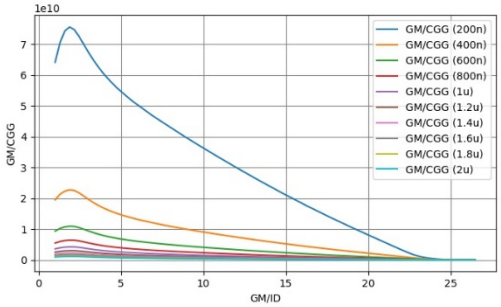


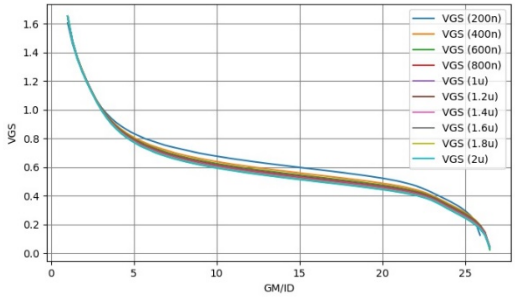


- PMOS Design Charts from ADT:



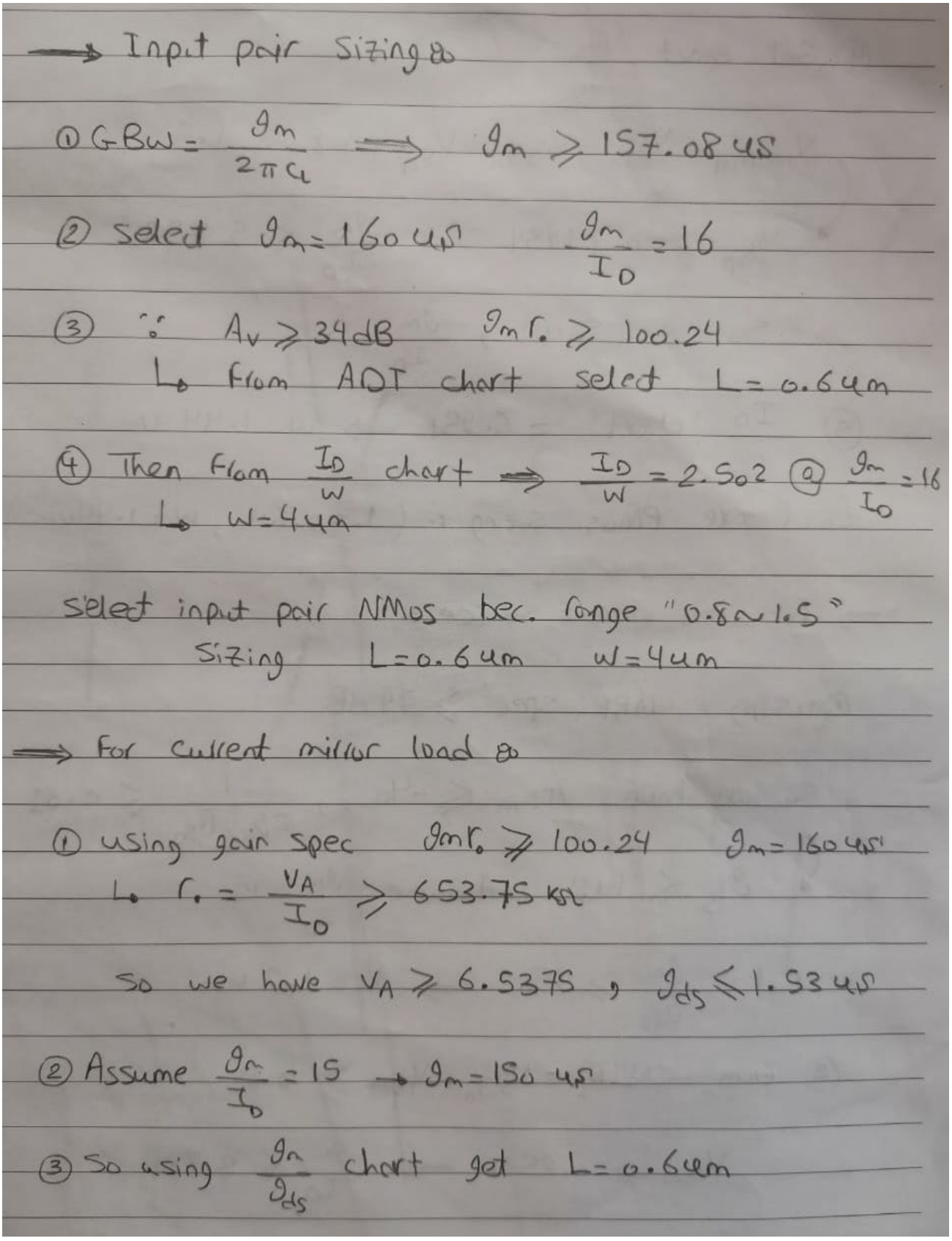






Part 2: OTA Design

- Hand Analysis and Design Procedure:



→ Input pair Sizing ⇒

① $GBW = \frac{g_m}{2\pi C_L} \Rightarrow g_m \geq 157.08\,\mu S$

② select $g_m = 160\,\mu S$ $\quad \frac{g_m}{I_D} = 16$

③ ∵ $A_V \geq 34dB$ $\quad g_m r_o \geq 100.24$
L⇒ From AOT chart select $L = 0.6\mu m$

④ Then From $\frac{I_D}{W}$ chart $\Rightarrow \frac{I_D}{W} = 2.502$ ⑤ $\frac{g_m}{I_D} = 16$
L⇒ $W = 4\mu m$

select input pair NMOS bec. range "0.8~1.5"
Sizing $L = 0.6\mu m$ $\quad W = 4\mu m$

→ For current mirror load ⇒

① using gain spec $g_m r_o \geq 100.24$ $\quad g_m = 160\,\mu S$
L⇒ $r_o = \frac{V_A}{I_D} \geq 653.75\,K\Omega$

So we have $V_A \geq 6.5375$, $g_{ds} \leq 1.53\,\mu S$

② Assume $\frac{g_m}{I_D} = 15 \rightarrow g_m = 150\,\mu S$

③ So using $\frac{g_m}{g_{ds}}$ chart get $L = 0.6\mu m$

④ Get exact $\frac{g_m}{I_D}$

$V_{incm_H} = V_{gs_n} - V_{Dsat_n} - V_{gs_p} + 1.8 \le 1.5$

→ $V_{gs_p} \ge 0.74934 \Rightarrow \frac{g_m}{I_D} \le 5.852$

So $g_m = 50\mu S$, $\frac{g_m}{I_D} = 5$

⑤ $\frac{I_D}{W}$ "chart" $= 6.951 \Rightarrow W = 1.44\mu m$

Load are PMOS sizing :- ($L = 0.6\mu$, $W = 1.44\mu m$)

⟹ for tail current source :

① using CMRR spec $\ge 74\,dB$

So we have $A_{cm} \le -40$, $\frac{1}{2 g_{m_{3,4}} R_{SS}} \le 0.01$

→ $g_{ds} \le 1\mu S$ Assume $\frac{g_m}{I_D} = 15$

Get $\frac{g_m}{g_{ds}} \ge 150 \rightarrow L = 1.5\mu m$

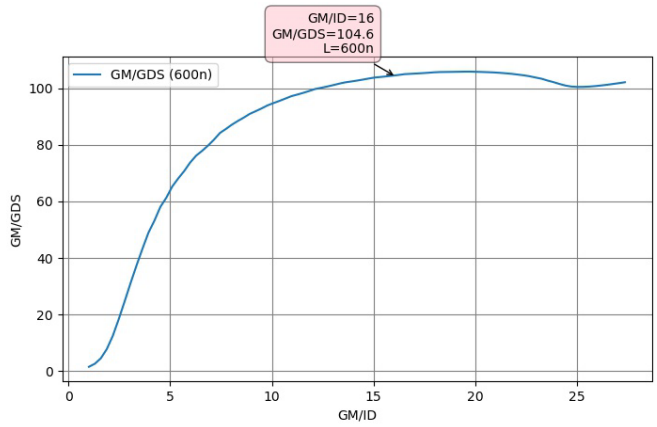
② From $CMIR_L = V_{gs_n} + V_{dsat} \ge 0.8$

$V_{dsat} \ge 0.2531 \rightarrow \frac{g_m}{I_D} \le 5.781$

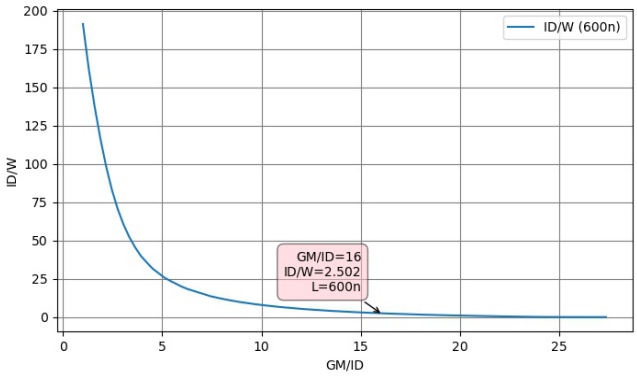
select $g_m/I_D = 5$ $g_m = 50\mu S \Rightarrow W = 898.655nm$

- Charts from ADT to Design:

1) Input Pair Sizing

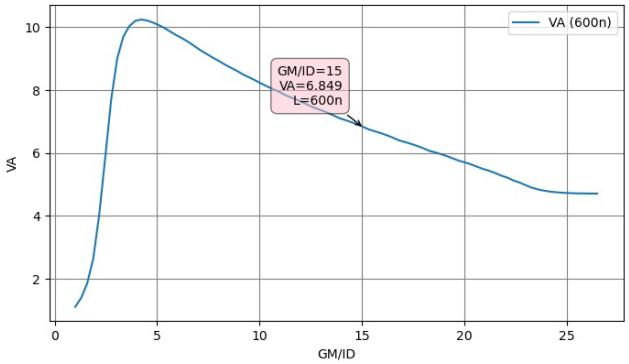


Length determination from gain chart

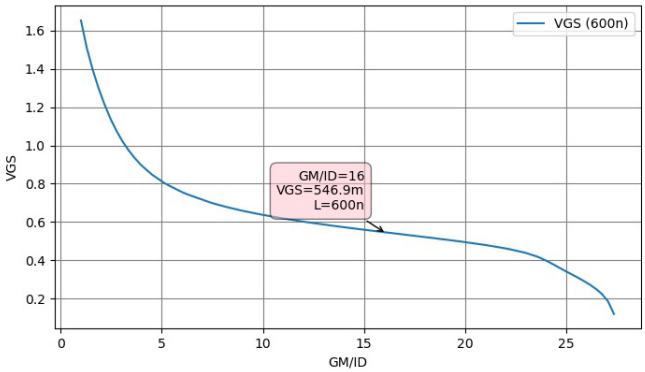


width determination from driven current capability chart

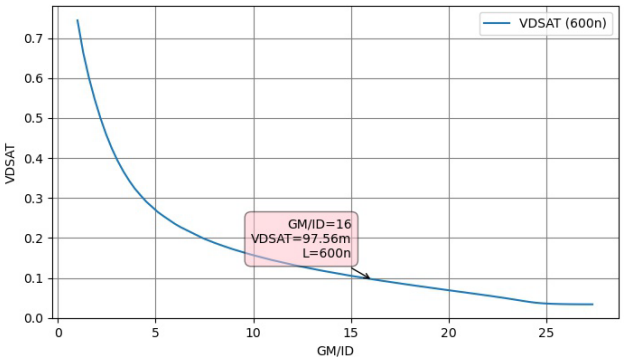
2) Current Mirror Load Sizing



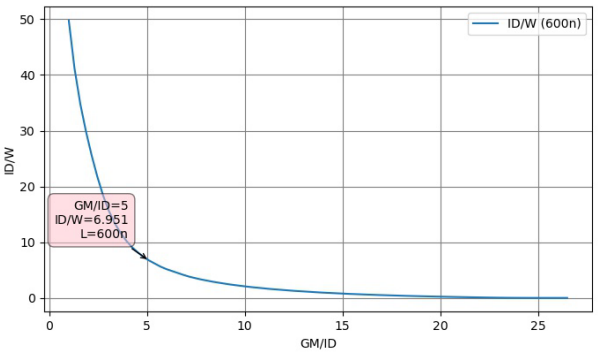
Length determination of current mirror load from early voltage chart at assumed gm/id



Vgs of input pair for common mode range calculations

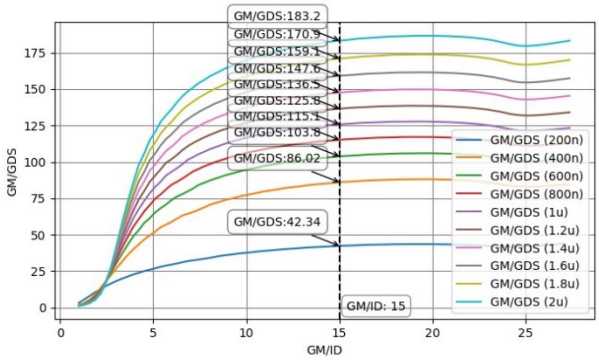


VDSAT of input pair for common mode range calculations

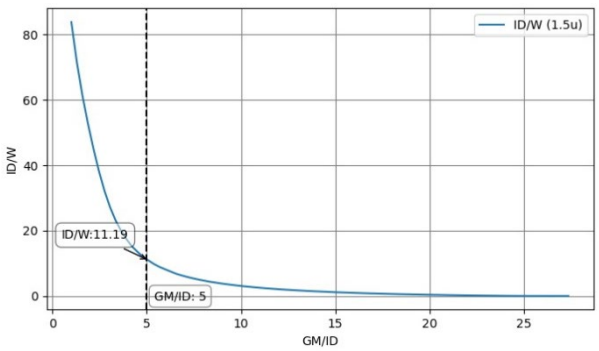


width determination of PMOS load from driven current capability chart

3) Tail Current Source Sizing



Length determination for tail current source from CMRR spec



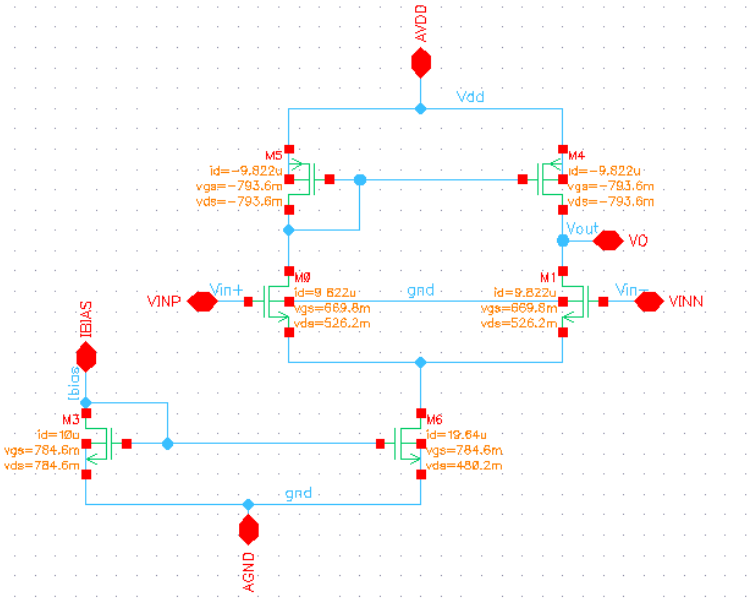
width determination from driven current capability chart

- Sizing Table:

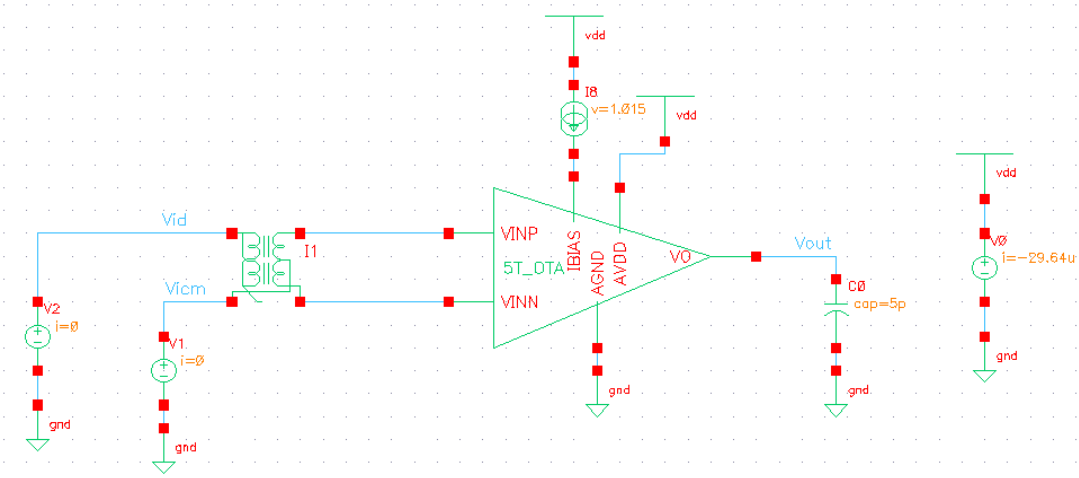
	Input Pair NMOS	Current Mirror Load PMOS	Magic Battery - Tail Current Source
Width	4um	1.44um	898.655nm – 2*898.655nm
Length	0.6um	0.6um	1.5um
ID	10uA	10uA	10uA – 20uA
GM	160uS	50uS	50uS – 100uS
GM/ID	16	5	5
Vdsat	97.56mV	296.9mV	299.1mV
Vov	114.3mV	368.1mV	395.4mV
V*	125.9mV	402.7mV	403.4mV

Part 3: Open-Loop OTA Simulation

1) Schematic of the OTA with DC node voltages clearly annotated.



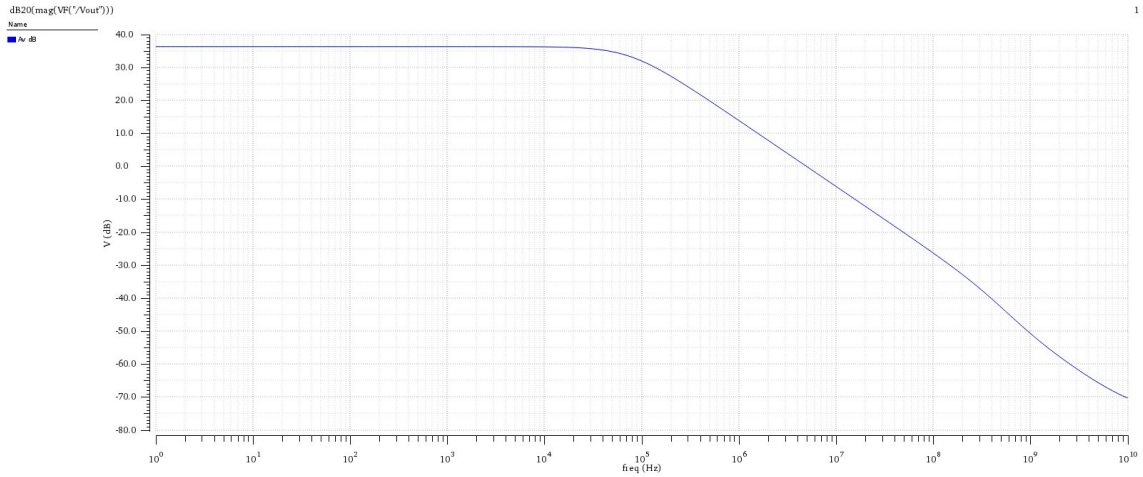
OTA circuit schematic with voltages annotated



OTA circuit testbench after symbol design

- Is the current (and gm) in the input pair **exactly** equal? Yes
- What is DC voltage at VOUT? Why?
  DC voltage at VOUT equal 1V, because of voltage drop on current mirror load as shown which will be $V_{out} = V_{DD} - V_{DS} = 1.8 - 793.5m = 1V$.

2) Diff small signal ccs:



Magnitude bode plot dB for differential gain

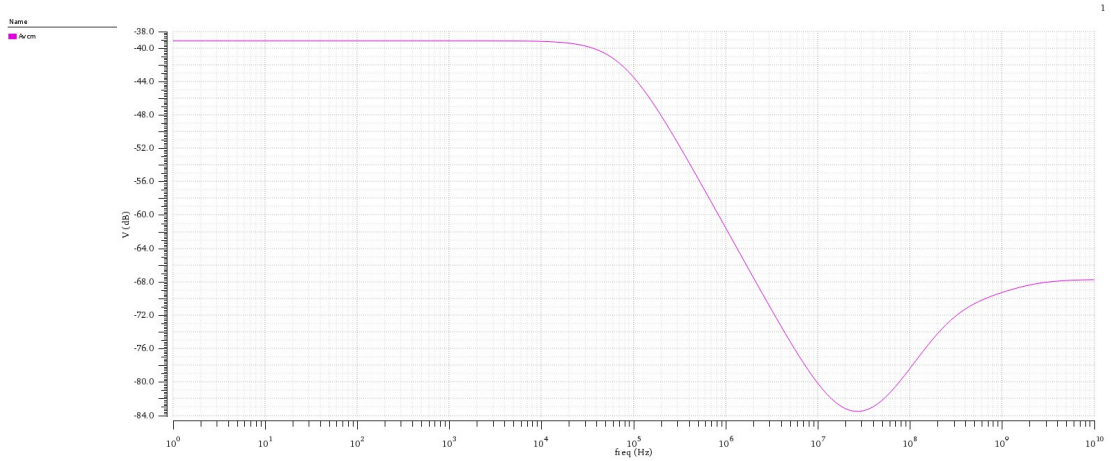
Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:lab07_OTA_testbench:1	Av Mag	65.72			
TrainLAB:lab07_OTA_testbench:1	Av dB	36.35			
TrainLAB:lab07_OTA_testbench:1	BW	76.22k			
TrainLAB:lab07_OTA_testbench:1	UGF	5.016M			
TrainLAB:lab07_OTA_testbench:1	GBW	5.02M			

AC simulation results from ADEXL for differential gain

• Compare simulation results with hand calculations in a table.

Circuit Parameter	Hand Analysis Results	Simulation Results
DC Gain MAG	66.24	65.72
DC Gain dB	36.42 dB	36.35 dB
Bandwidth	77.7kHz	76.22kHz
GBW	5.15MHz	5.02MHz
UGF	5.15MHz	5.016MHz

3) CM small signal ccs:



Magnitude bode plot dB for common mode gain

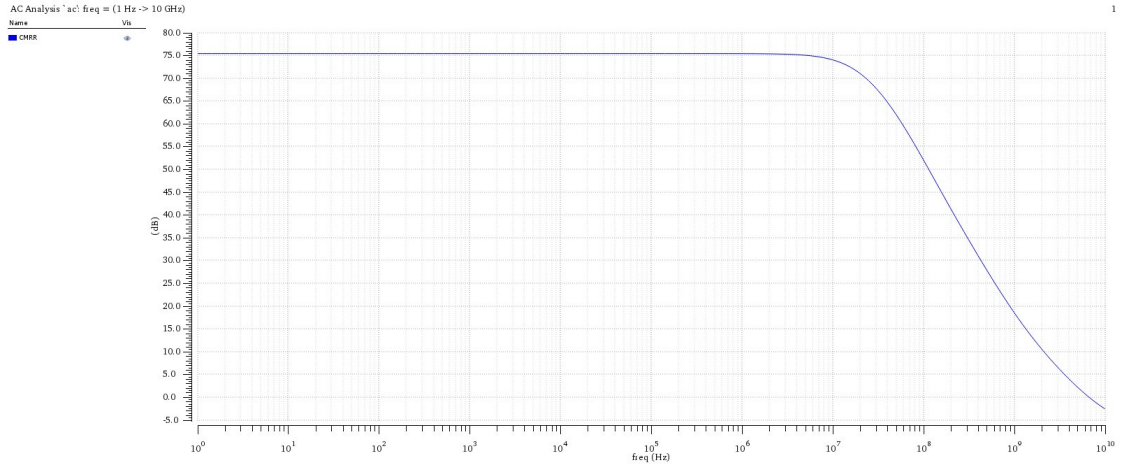
Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:lab07_OTA_testbench:1	Av Mag	11.09m			
TrainLAB:lab07_OTA_testbench:1	Av dB	-39.1			
TrainLAB:lab07_OTA_testbench:1	BW	76.22k			
TrainLAB:lab07_OTA_testbench:1	GBW	847.1			

AC simulation results from ADEXL for differential gain

• Compare simulation results with hand calculations in a table.

Circuit Parameter	Hand Analysis Results	Simulation Results
DC Gain MAG	14.09m	11.09m
DC Gain dB	-37 dB	-39.1 dB
Bandwidth	77.7kHz	76.22kHz
GBW	1.09kHz	847.1Hz

4) CMRR:

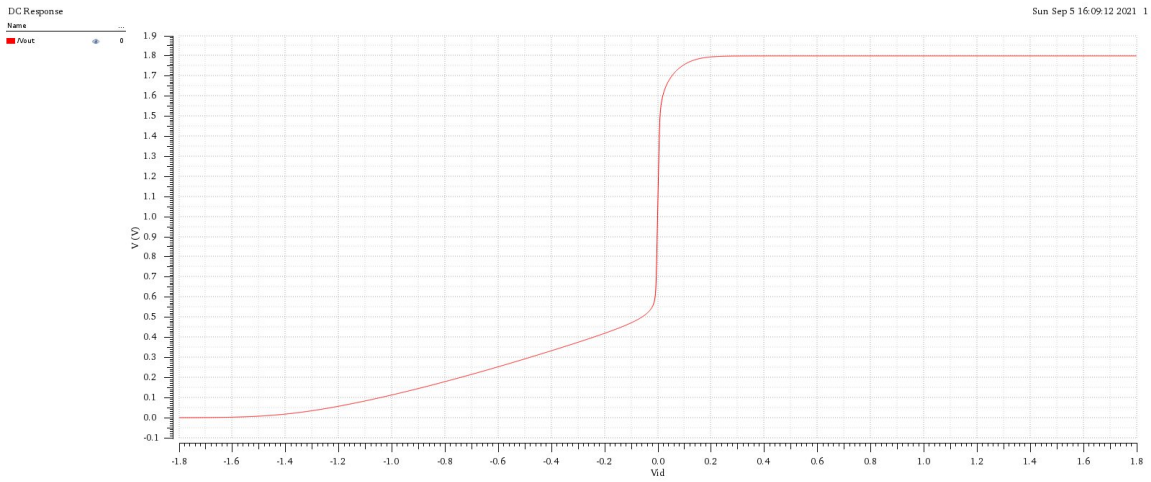


CMRR dB plot

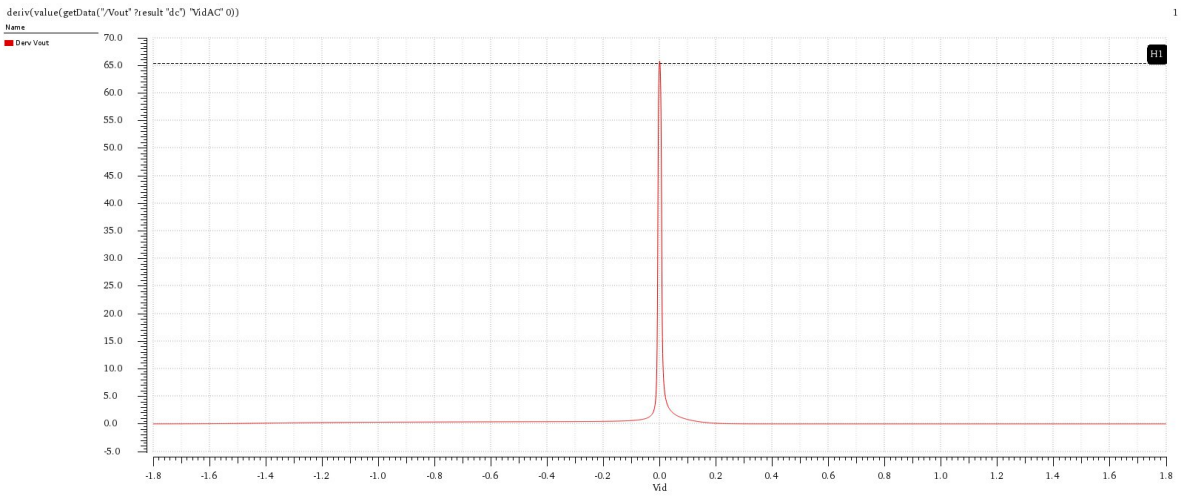
Analytical Analysis:

CMRR=gm1*(ro1//ro3)*2*gm3*Rss=161.7u*409.653k*2*49.41u*718.2k=4701.25=74dB

5) Diff large signal ccs:



Vout versus Vid

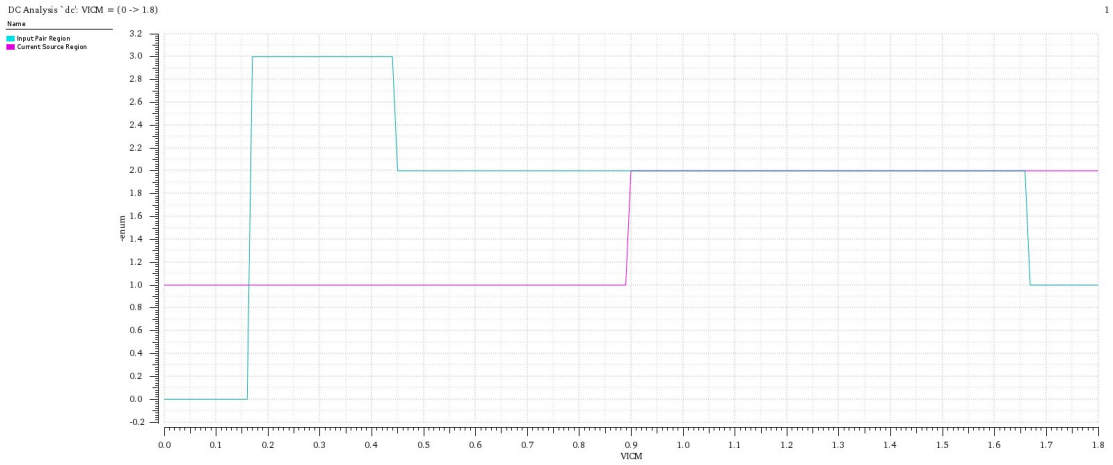


Derivative of Vout versus Vid

• Compare the peak with Avd:

As shown from previous graph that differential gain Avd is exact the peak of derivative.

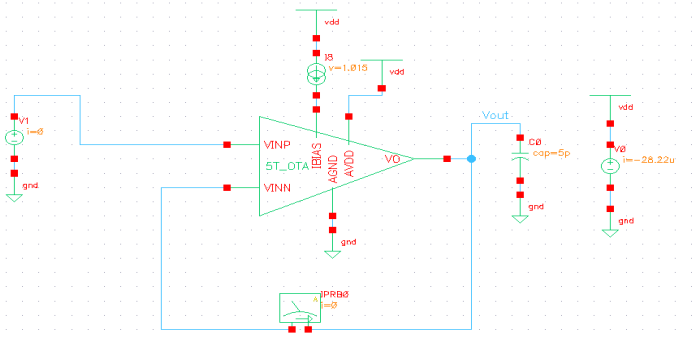
6) CM large signal ccs (region vs VICM):



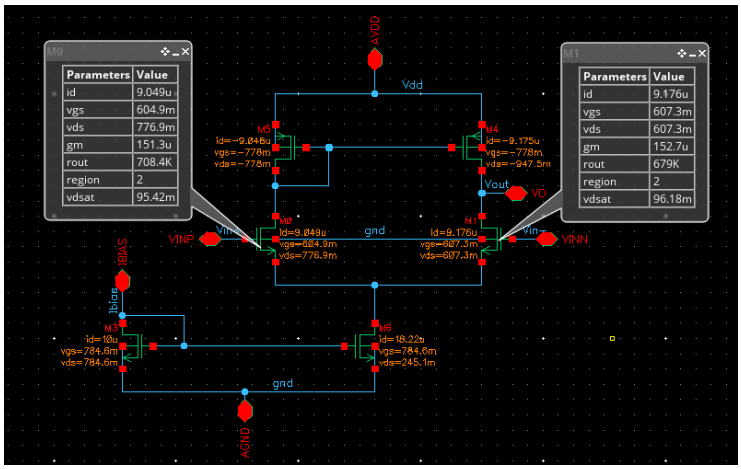
Region of tail current source and input pair versus Vicm Sweep

As shown from previous graph that common mode input range equal 0.85:1.5 which meet nearly the specs which equal 0.8:1.5.

Part 4: Closed-Loop OTA Simulation



Closed loop OTA schematic



OP parameters of input pair after applying feedback

- Is the current (and gm) in the input pair exactly equal? Why?

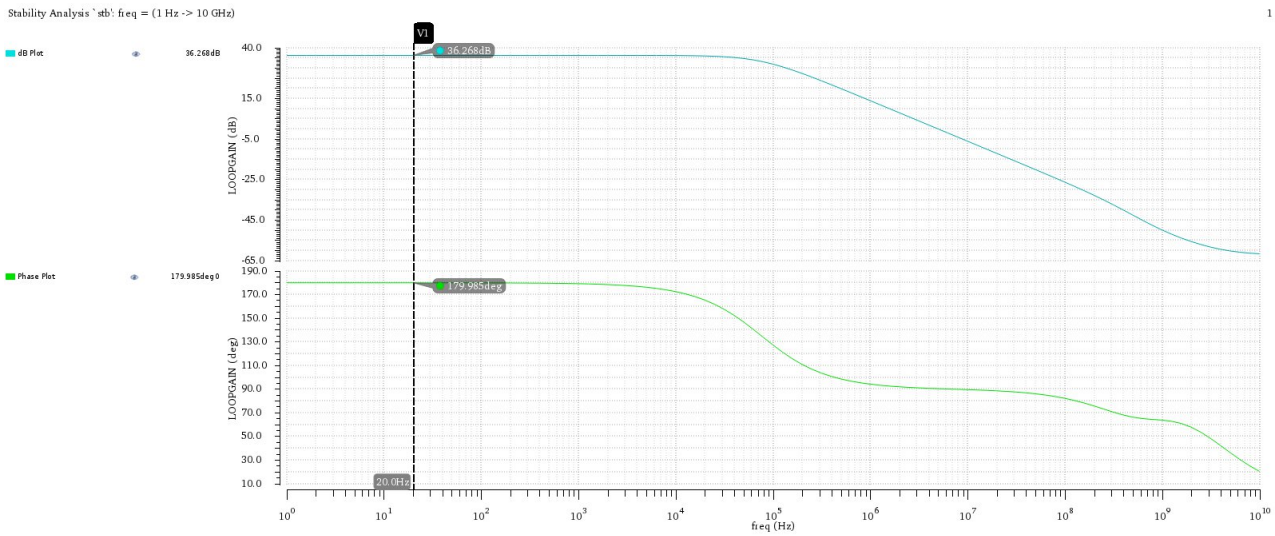
  As shown from previous schematic that Id and gm of input pair aren't equal, this because unity gain feedback which gives a finite value for gain so differential inputs don't become zero anymore and there is a slight difference between Vin+ and Vin- which make mismatch.

- Calculate the mismatch in I_D and gm.

  ΔID=0.127uA

  ΔGm=1.4uS

Loop gain:



Loop gain bode plot from simulation

	Expression	Value
1	gainBwProd(value(mag(getData("loopGain" ?result "...	4.990E6

GBW of loop gain from cadence

- Compare DC gain and GBW with those obtained from open-loop simulation. Comment

  As shown from previous results that there is no difference between loop gain and open OTA gain this because of unity feedback which make value of β=1 so open loop OTA is the same gain of loop gain.