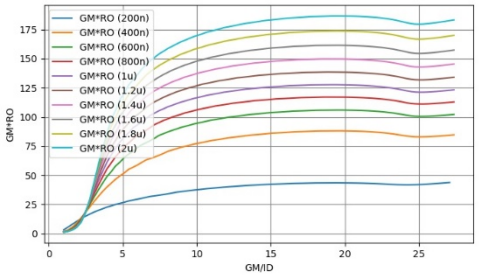
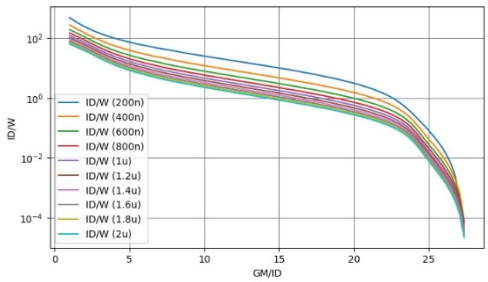
Lab 09 (Mini-Project 1)

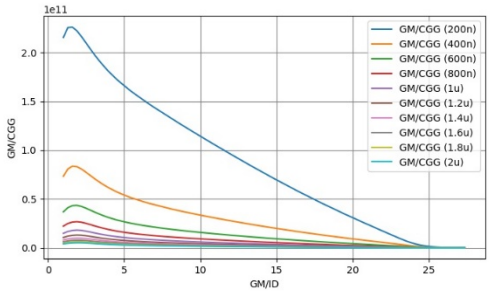
Two-Stage Miller OTA

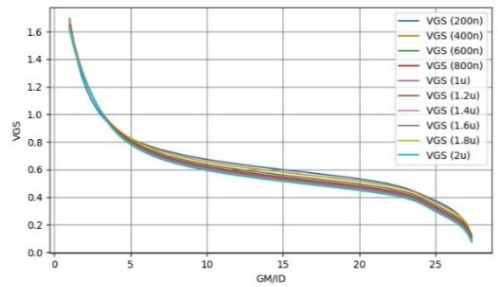
Part 1: gm/ID Design Curves

- NMOS Design Charts from ADT:

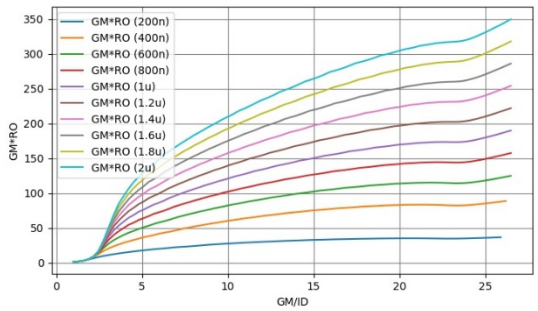


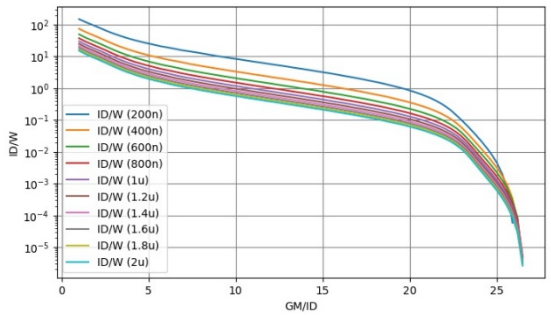


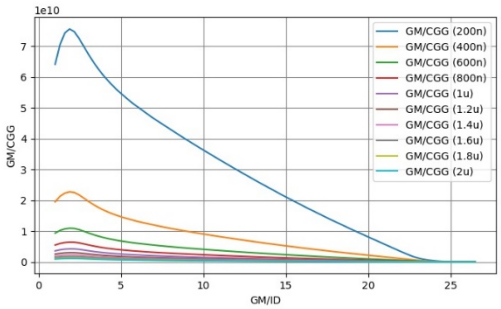


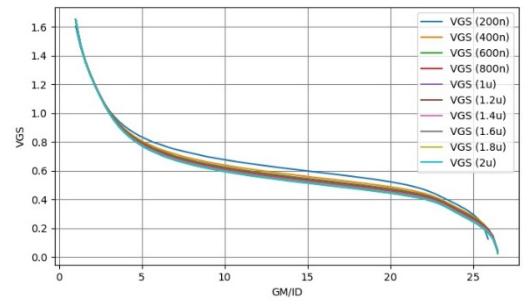


- PMOS Design Charts from ADT:









Part 2: OTA Design

- **Topology Selection:**

  Input Pair | Tail Current Source → PMOS, because of CM input range which is 0.2-1 near to GND rail.

  Current Mirror Load | 2nd Stage Input MOS → NMOS.

- **Input Pair Sizing 1st Stage:**

$$T_{riseCL} = 2.2\tau_{CL} \leq 70ns \rightarrow \tau_{CL} = \frac{A_{cl}}{\omega_u} \leq 31.82ns, and\ A_{cl} = 1 \text{ unity gain buffer.}$$

$$\omega_u = \frac{g_{m1}}{C_c} \geq 31.43\, Mrad/sec\,, let\ C_c = 0.5 * C_l = 2.5pf \rightarrow g_{m1} \geq 78.57uS.$$

$$Slew\ Rate\ SR = \frac{I_{B1}}{C_c} = 5\, V/us \rightarrow I_{B1} = 12.5uA, so\ for\ one\ pair\ I_{B1} = 6.25uA.$$

$$\left(\frac{g_m}{I_D}\right)_{ip1} \geq 12.572 \rightarrow choose\ \left(\frac{g_m}{I_D}\right)_{ip1} = 13\ and\ g_m{\sim}81.25uS.$$

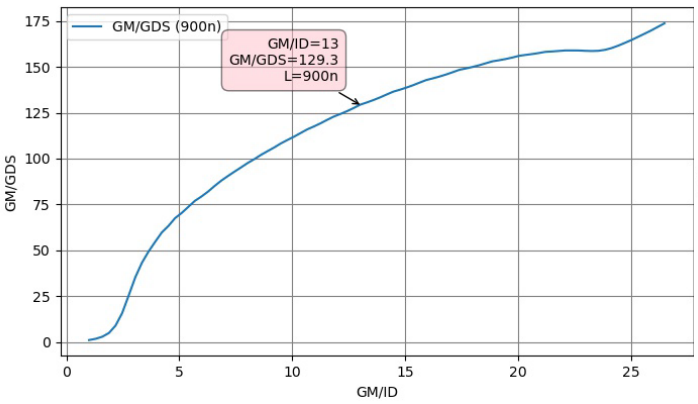
$$we\ have\ \varepsilon_s = \frac{1}{\beta A_{ol}} \leq 0.05\% \rightarrow A_{ol} = A_{v1} * A_{v2} \geq 2000.$$

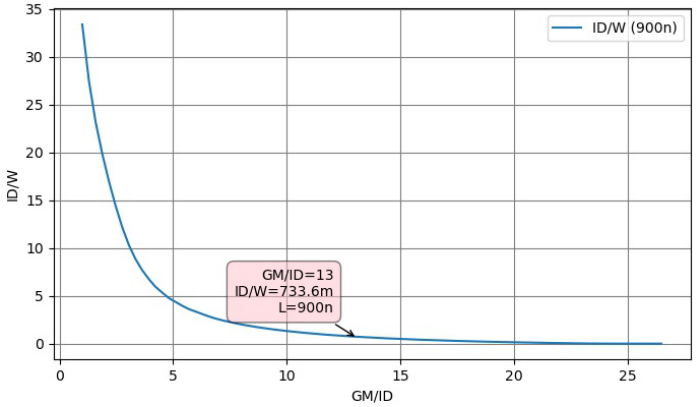
Choose $A_{v1} = 2 * A_{v2}$, because we design 1st stage for gain and 2nd stage for swing.

$$A_{v1} \geq 63.24\ and\ A_{v2} \geq 31.62 \rightarrow \frac{g_{m1} * r_{o1}}{2} \geq 63.24 \rightarrow \frac{g_{m1}}{g_{ds1}} \geq 126.48.$$

Using $\frac{g_m}{g_{ds}}$ chart from ADT to determine length of input pair MOS, which will be as shown L=0.9um.

Then using $\frac{I_D}{W}$ chart at $\frac{g_m}{I_D} = 13$ we can determine width of input pair MOS which will be W=8.52um.





Charts from ADT to determine width and length for input pair PMOS

- **Current Mirrors Design:**

For tail current source OTA we have $CMRR = \frac{A_{vd}}{A_{vCM}} \geq 74dB \rightarrow A_{vCM} = \frac{1}{2g_m R_{SS}} \leq 12.62m$

$$g_{ds} \leq 2.051uS, assume\ \frac{g_m}{I_D} = 15 \rightarrow g_m = 187.5uS \rightarrow \frac{g_m}{g_{ds}} \geq 91.43.$$

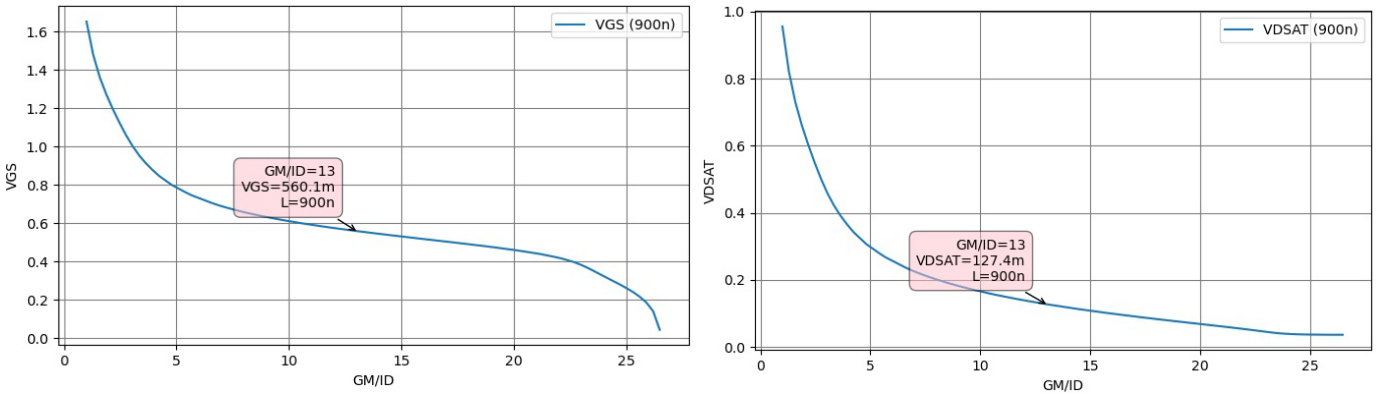
Using $\frac{g_m}{g_{ds}}$ chart from ADT to determine length current mirrors PMOS, which will be as shown L=0.6um.

To get exact $\frac{g_m}{I_D}$ for current mirrors, $V_{icmH} = -V_{gsIN} - V_{dsat} + 1.8 \geq 1 \rightarrow V_{dsat} \leq 0.2399 \rightarrow$

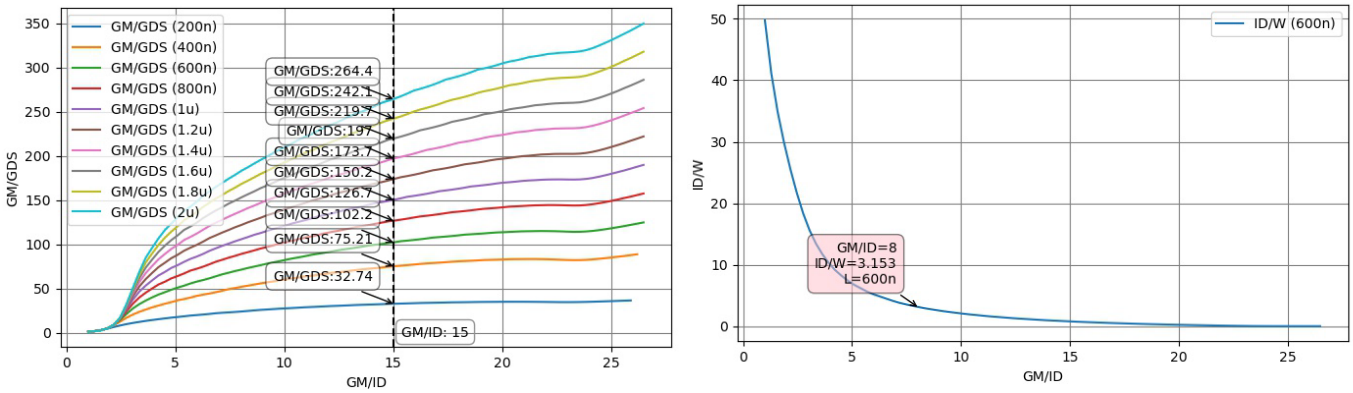
$$\frac{g_m}{I_D} \geq 6.521 \; as \; shown \; in \; V_{dsat} \; charts \; for \; current \; mirrors,$$

$$choose \; \frac{g_m}{I_D} = 8 \; for \; all \; curent \; mirrors.$$

Then using $\frac{I_D}{W}$ chart at $\frac{g_m}{I_D} = 8$ we can determine width of each current mirror PMOS which will be W1=3.17um, W2=3.964um and W3=153065um.



Vgs and Vdsat for input pair to determine CMIRH and exact gm/id for current mirror



Charts from ADT to determine width and length for current mirrors PMOS

- **Input NMOS 2nd Stage:**

$$To \; set \; phase \; margin \; PM \geq 70° \rightarrow \omega_{pnd} = \frac{g_{m2}}{C_l} \geq 4 * \omega_u \rightarrow g_{m2} \geq 628.6uS.$$

$$Current \; consumption = 60uA \rightarrow I_{B2} = 47.5uA \rightarrow \left(\frac{g_m}{I_D}\right)_{ip2} \geq 13.233 \rightarrow$$

$$choose \; \left(\frac{g_m}{I_D}\right)_{ip2} = 14, and \; g_{m2} \sim 665uS.$$

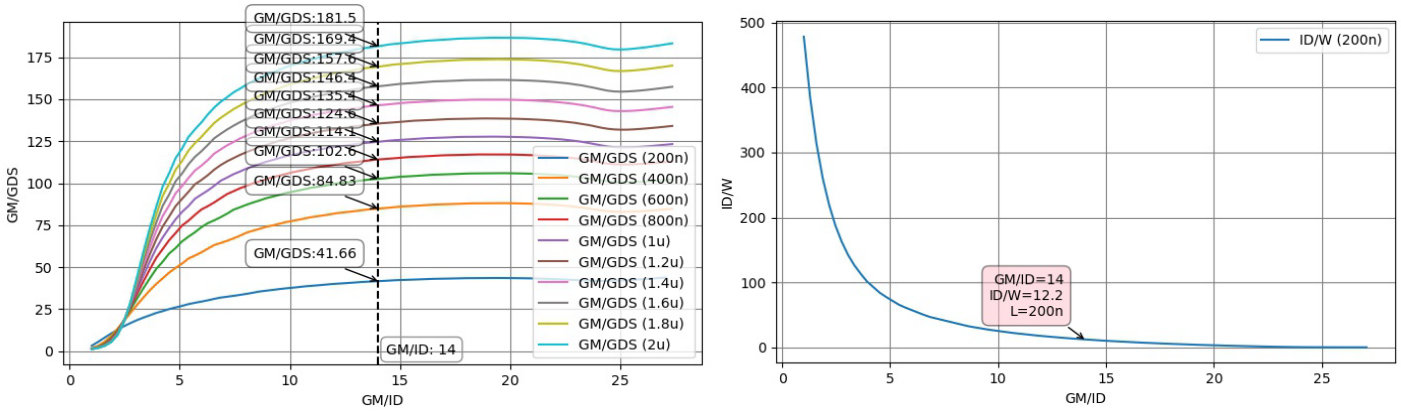
$$A_{v2} \geq 31.62 \rightarrow g_{m2} * (r_{on} || r_{op}) \geq 31.62 \rightarrow g_{dsp} = 2.051us \; from \; CMRR \; calculation.$$

$$g_{dsn} \leq 17.83uS \rightarrow \frac{g_m}{g_{ds}} \geq 37.29 \rightarrow L = 0.2um \; from \; \frac{g_m}{g_{ds}} \; chart,$$

$$and \; V_{gs} = 611.7mV \; from \; Vgs \; chart.$$

Then using $\frac{I_D}{W}$ chart at $\frac{g_m}{I_D} = 14$ we can determine width of 2nd stage input NMOS which will be W=3.89um.

And miller resistance $R_Z = \frac{1}{g_{m2}} = 1.504k\Omega.$



Charts from ADT to determine width and length for current mirrors PMOS

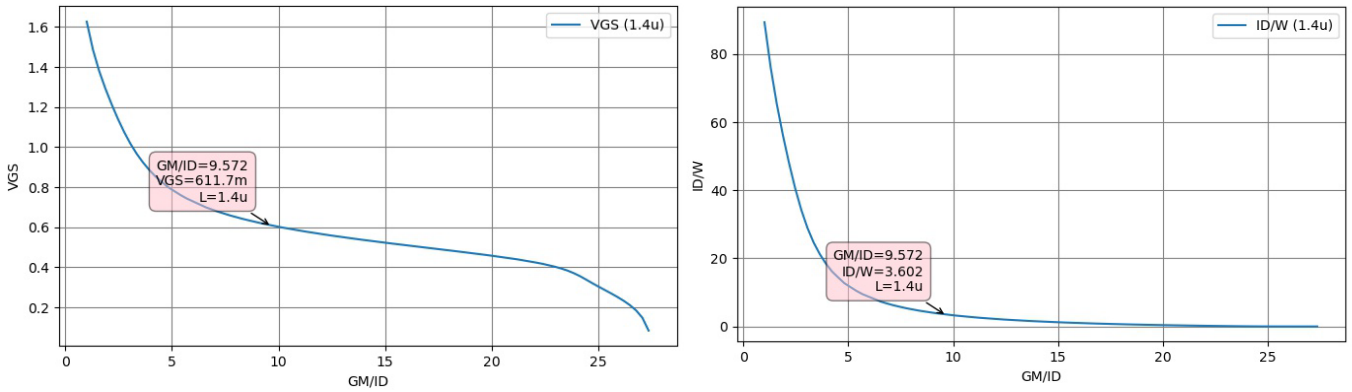
- **Current Mirror Load of OTA Design:**

Using gain spec of 1st stage $A_{v1} \geq 63.24 \rightarrow \frac{g_{m1} * r_{o1}}{2} \geq 63.24 \rightarrow \frac{g_{m1}}{g_{ds1}} \geq 126.48 \rightarrow g_{ds1} \leq 642.4nS.$

And assume $\frac{g_m}{I_D} = 15 \rightarrow g_m = 93.75uS \rightarrow \frac{g_m}{g_{ds}} \geq 145.94$, from $\frac{g_m}{g_{ds}}$ chart get L=1.4um.

To avoid systematic offset set Vgs of load current mirror as Vgs of 2nd stage input Vgs=611.7mV, so from Vgs chart we get exact gm/id=9.572.

Then using $\frac{I_D}{W}$ chart at $\frac{g_m}{I_D} = 9.572$ we can determine width of current mirror load NMOS which will be W=1.74um.



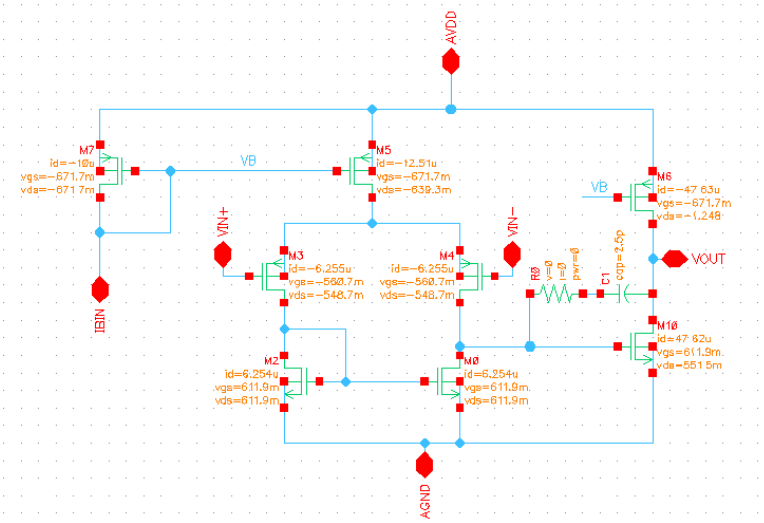
Charts from ADT to determine width, length and gm/id for current mirror load NMOS

- **Sizing Summary:**

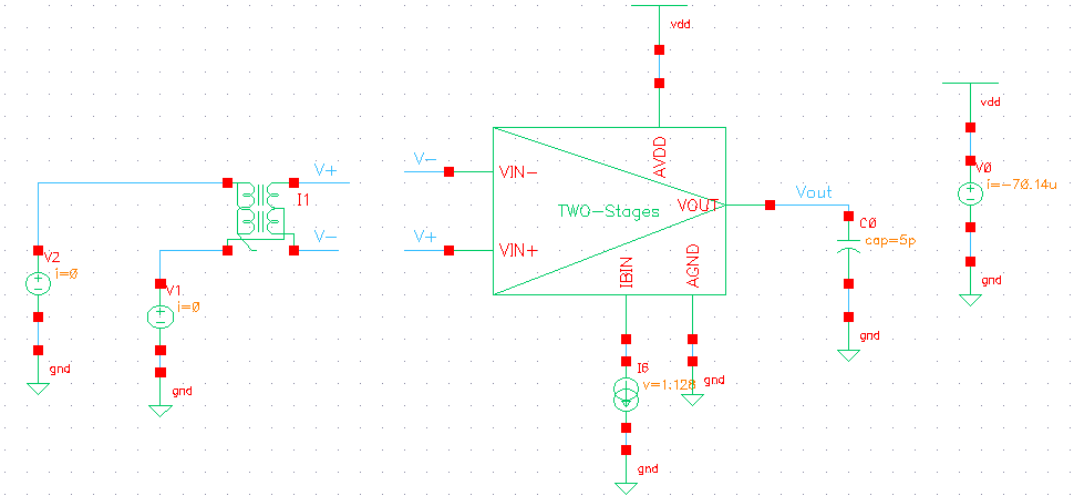
	Input Pair 1st Stage (PMOS)	CM Load NMOS	Input Pair 2nd Stage (NMOS)	Magic Battery - Tail CM OTA – Tail CM 2nd Stage (PMOS)
Width	8.52um	1.74um	3.89um	3.17um – 3.964um – 15.065um
Length	0.9um	1.4um	0.2um	0.6um
ID	6.25uA	6.25uA	47.5uA	10uA – 12.5uA – 47.5uA
GM	81.25uS	59.825uS	665uS	80uS – 100uS – 380uS
GM/ID	13	9.572	14	8

PART 3: Open-Loop OTA Simulation

1) Schematic of the OTA and bias circuit with DC node voltages clearly annotated.



Tw-stages OTA circuit schematic with voltages annotated



OTA circuit testbench after symbol design

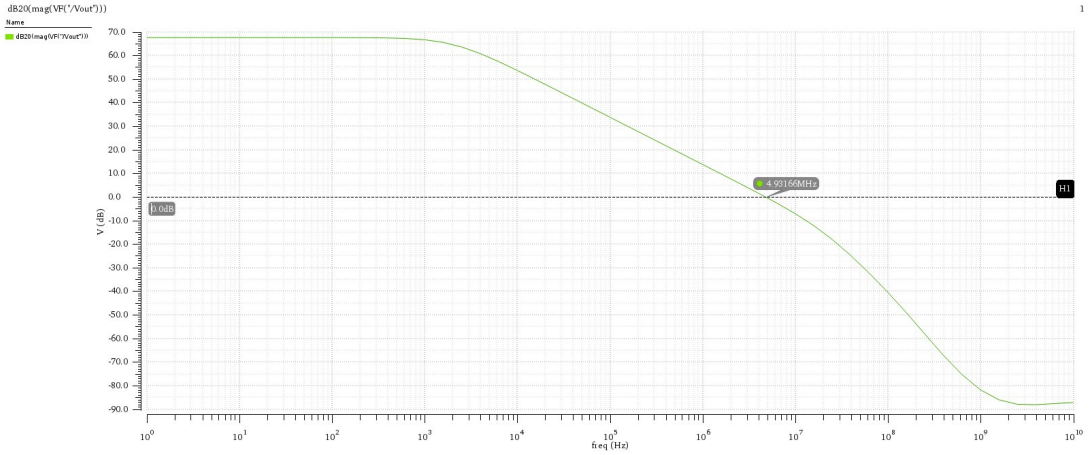
- Is the current (and gm) in the input pair exactly equal? Yes, as shown in schematic.
- What is DC voltage at the output of the first stage? Why?
  Dc voltage at output of 1st stage equals Vgs of current mirror load and Vgs of 2nd stage NMOS, and they must equal each other to avoid systematic offset and keep all MOSFETs in saturation.
- What is DC voltage at the output of the second stage? Why?
  Dc voltage at output of 2nd stage equals Vds of input NMOS which is 0.552V, this due to voltage drop on current mirror PMOS as shown in schematic which equal VDD-Vds=1.8-1.248=0.552V.

2) Diff small signal ccs:

Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:Lab09-TB:1	Av	2.41k			
TrainLAB:Lab09-TB:1	Av_dB	67.64			
TrainLAB:Lab09-TB:1	BW	2.069k			
TrainLAB:Lab09-TB:1	UGF	5.07M			
TrainLAB:Lab09-TB:1	GBW	4.998M			

AC simulation results from ADEXL for differential gain

- Plot diff gain (in dB) vs frequency.



Magnitude bode plot dB for differential gain

- Compare simulation results with hand calculations in a table.

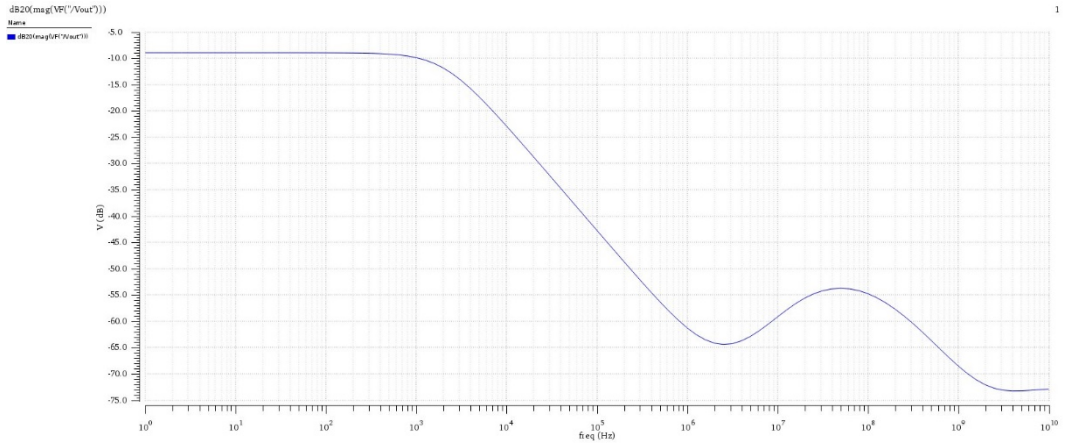
Circuit Parameter	Hand Analysis Results	Simulation Results
DC Gain MAG	2418	2410
DC Gain dB	67.67 dB	67.64 dB
Bandwidth	2.136kHz	2.069 kHz
GBW	5.17MHz	5.07MHz
UGF	5.17MHz	5MHz

3) CM small signal ccs:

Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:Lab09-TB:1	Av	358.7m			
TrainLAB:Lab09-TB:1	Av_dB	-8.905			

AC simulation results from ADEXL for common mode gain

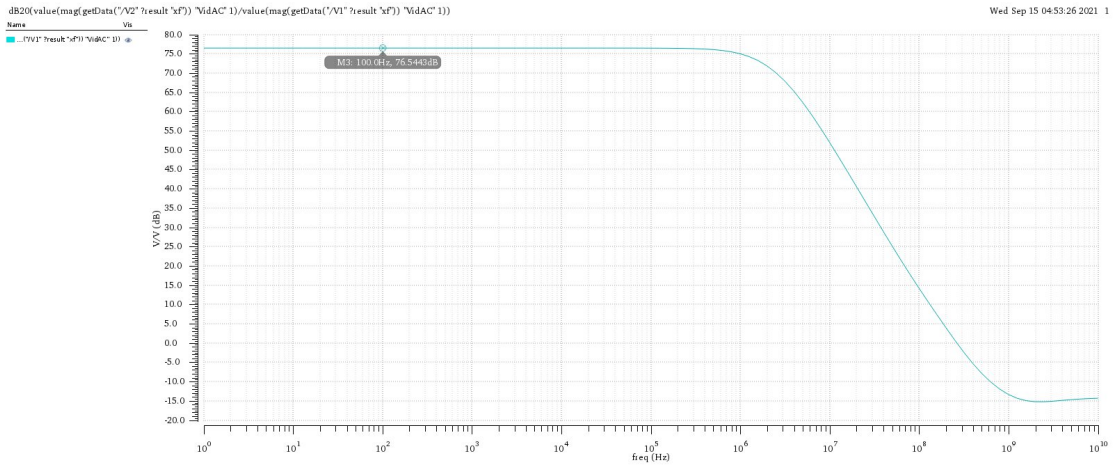
- Plot CM gain in dB vs frequency.



- Compare simulation results with hand calculations in a table.

Circuit Parameter	Hand Analysis Results	Simulation Results
DC Gain MAG	367.27m	358.7m
DC Gain dB	-8.7 dB	-8.905 dB

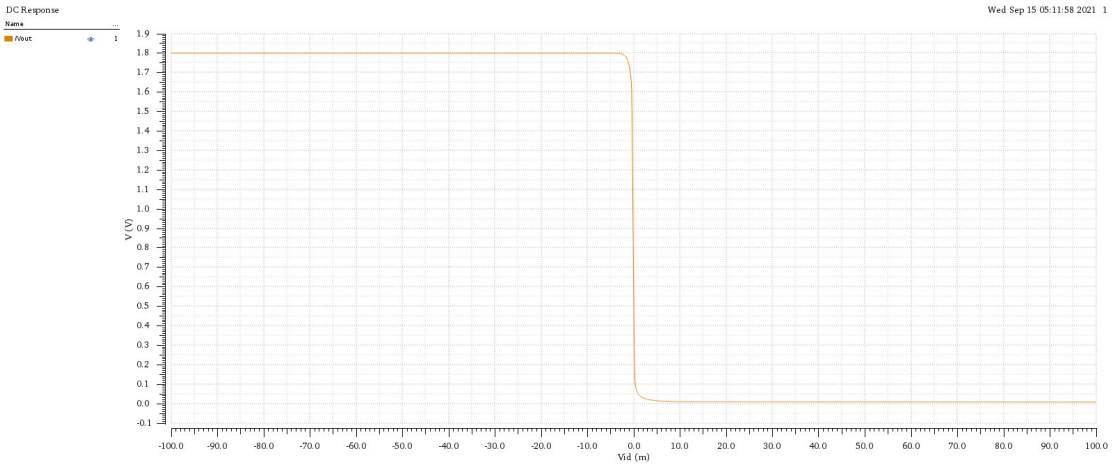
4) (Optional) CMRR:
   - Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.



CMRR dB plot

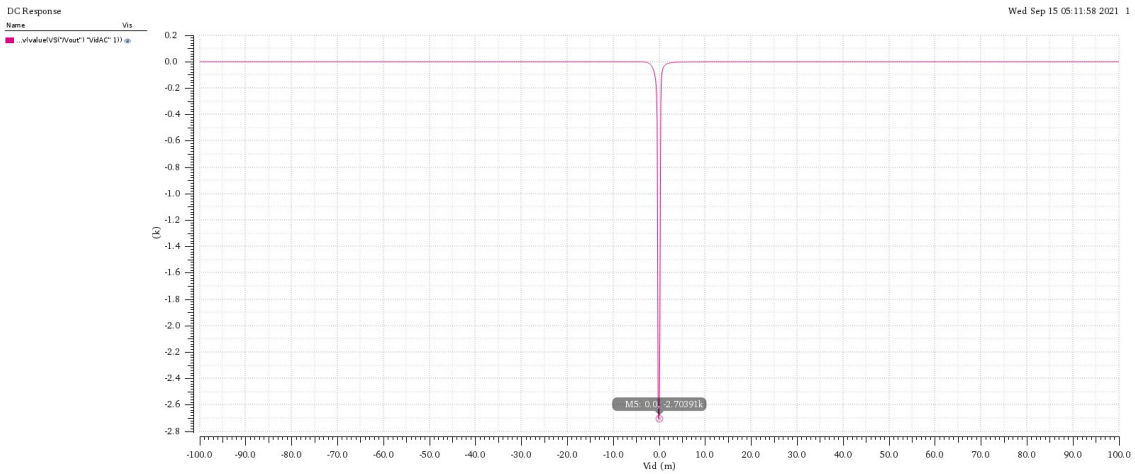
   - Compare simulation results with hand calculations in a table.
     Hand Analysis: CMRR=gm1*(ro1//ro3)*2*gm3*Rss=6583.558=76.37dB

5) (Optional) Diff large signal ccs:
   - Plot VOUT vs VID.



Vout versus Vid

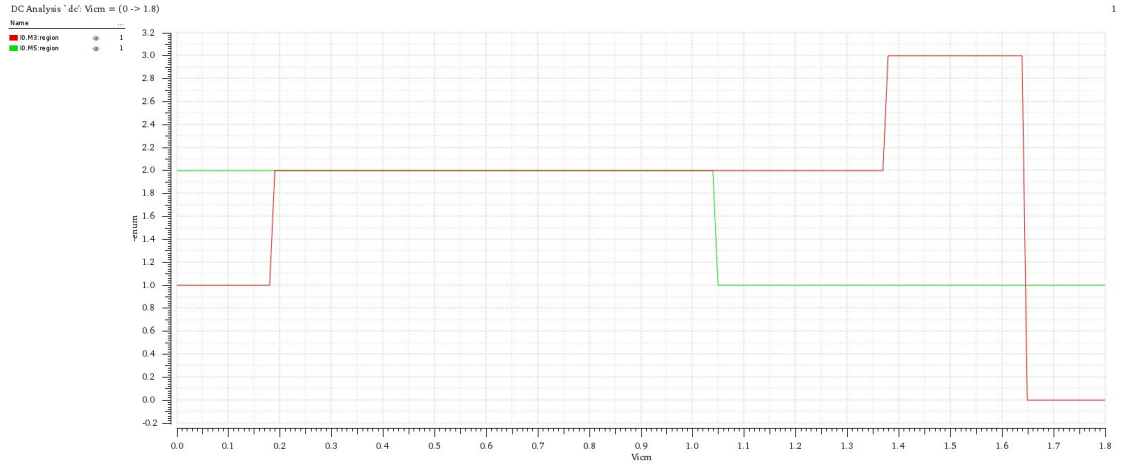
   - Plot the derivative of VOUT vs VID. Compare the peak with Avd from ac analysis. Comment on the result.



Derivative of Vout versus Vid

Comment: as shown from previous analysis that peak of derivative equals 2.7k which is nearly to value differential gain but it has -ve value because of inversion in 2nd stage as it's a common source stage.

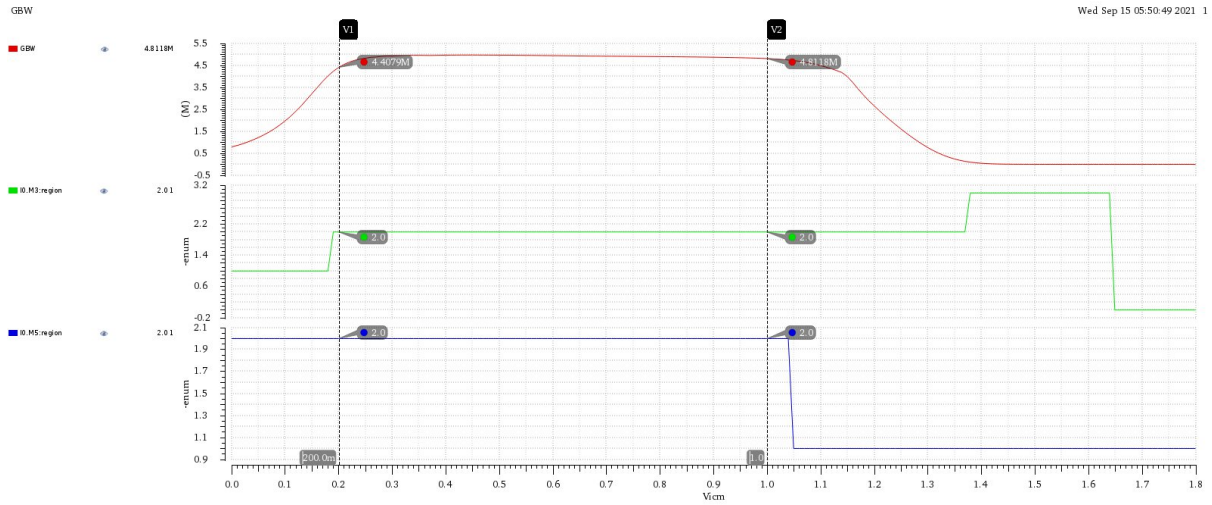
6) CM large signal ccs (region vs VICM):
   - Plot "region" OP parameter vs VICM for the input pair and the tail current source.



Region of tail current source and input pair versus Vicm Sweep

As shown from previous graph that common mode input range equal 0.2:1.05 which meet nearly the specs which equal 0.2:1.

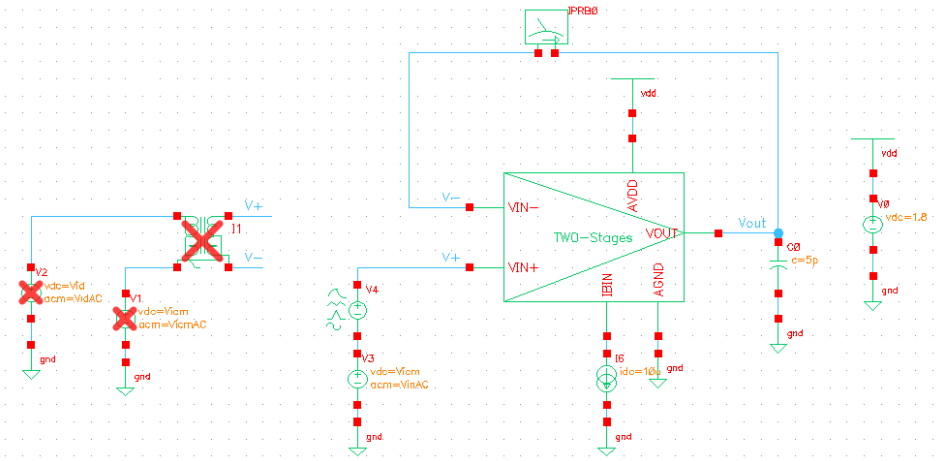
7) (Optional) CM large signal ccs (GBW vs VICM):
   - Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).



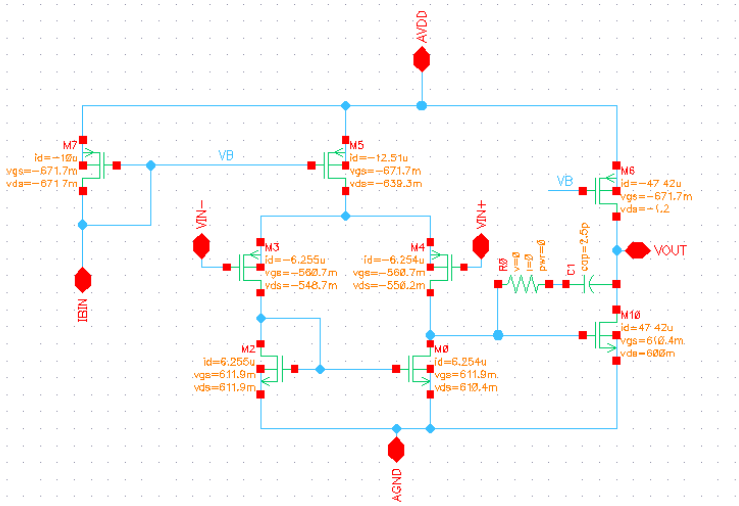
GBW and region overlaid versus Vicm DC sweep

PART 4: Closed-Loop OTA Simulation

1) Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.



Closed-loop OTA schematic testbench



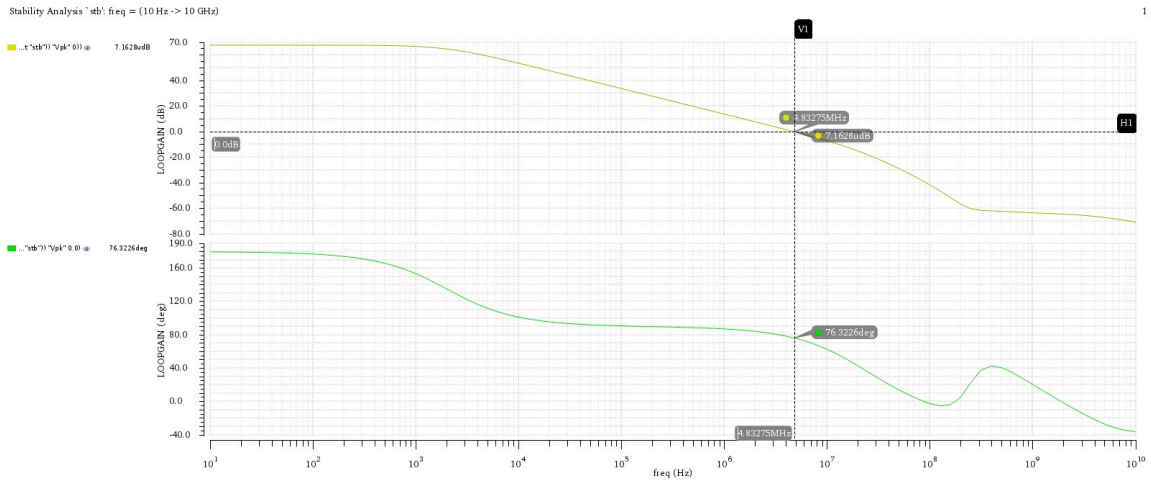
OP parameters of input pair after applying feedback

- Are the DC voltages at the input terminals of the op-amp exactly equal? Why?
  No, there is some difference in Vds voltage due to Verr between two inputs of OTA.

- Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?
  DC output voltage equals 0.6V which is more slightly than DC output voltage in case of open-loop.

- Is the current (and gm) in the input pair exactly equal? Why?
  No, because there is some error in DC biasing voltage of input pair which make a small difference in drain current and gm.

2) Loop gain:
   - Plot loop gain in dB and phase vs frequency.



Bode plot of loop gain simulation

Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:Lab09-TB:1	UGF LG	4.85M			
TrainLAB:Lab09-TB:1	DC Gain LG	67.77			
TrainLAB:Lab09-TB:1	GBW LG	4.945M			
TrainLAB:Lab09-TB:1	PM	76.36			

AC simulation results from ADEXL for loop gain

- Compare DC gain, fu, and GBW with those obtained from open-loop simulation.

Circuit Parameter	Simulation Results closed-loop	Simulation Results open-loop
DC Gain dB	67.77 dB	67.64 dB
GBW	4.954MHz	5.07MHz
UGF	4.85MHz	5MHz

Comment: the gain of closed loop is nearly the same of loop gain due to unity gain frequency but there some degradation in bandwidth of closed-loop due to the decrease in phase margin and decrease gain crossover Gx by compensating capacitor Cc.

- Report PM. Compare with hand calculations. Comment.
  As we set $\omega_{pnd} = 4 * \omega_u$ so the system is critical damped system and its phase margin nearly around 76° which meet simulation result.

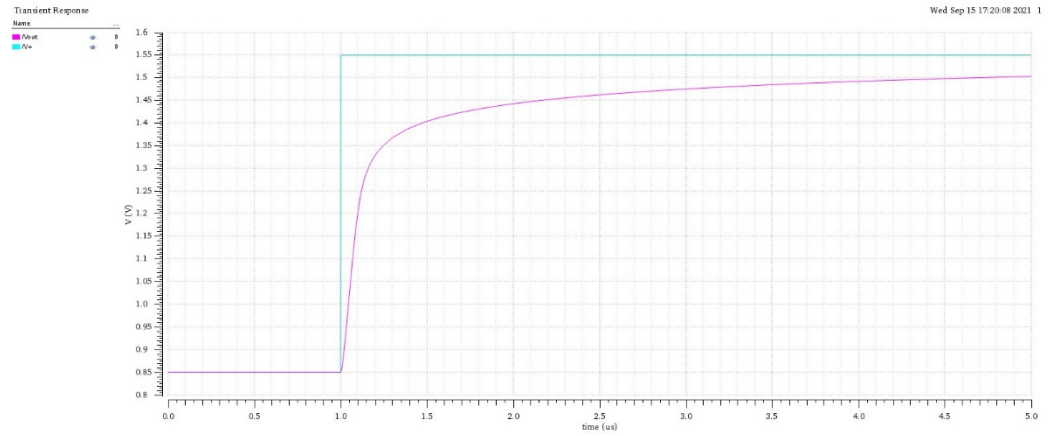
3) Slew rate:
   - Note that we want a single step input, which is why we selected very large period and width for the pulse.
     Choose a very large period and width for pulse to see the settle time of output voltage.

   - Report the slew rate.

slewRate(VT("/Vout") 1u t 5u t 10 9...

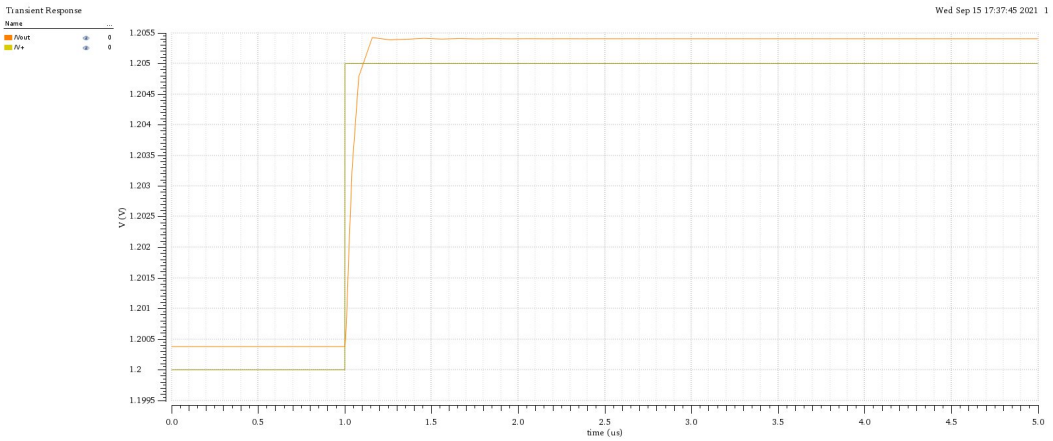
	Vpk	slewRat...time")
1	0.000	590.2E3

- Report Vin and Vout overlaid.



Vout & Vin overlaid after transient analysis

4) Settling time:



Vout & Vin overlaid after small signal transient analysis

- Do you see any ringing? Why?
  No there is no ringing in system because this system is a critical damped system with no ringing in time domain.