

Lab 12

Two-Stages Miller OTA

Design With ADT:

I have start design with optimize button in ADT as following

The screenshot shows the ADT interface with the following sections:

- Optimization Settings:**
 - DOB: A020005_1MEG.dbb
 - Initial Point: Best DOB Point
 - Corner: Nominal
 - Max No. of Iterations: 20
 - Constraints Strictness: Moderate
- DOFs (Degrees of Freedom):**

Name	Min	Max	Active
1 M1(L)	180n	2u	<input type="checkbox"/>
2 M2(L)	180n	2u	<input type="checkbox"/>
3 M3(L)	180n	2u	<input type="checkbox"/>
4 M4(L)	180n	2u	<input type="checkbox"/>
5 M5(L)	180n	2u	<input type="checkbox"/>
- Constraints:**

Name	Min	Max	Weight	Active
1 DC Gain	1k	3k	1	<input checked="" type="checkbox"/>
2 DC PSR	-24.45	-446m	1	<input type="checkbox"/>
3 DC CMR	-25.29	12.06	1	<input type="checkbox"/>
4 Total Inp...	951.8n	104.7u	1	<input type="checkbox"/>
5 Thermal...	2.406a	3.41f	1	<input type="checkbox"/>
- Objectives:**

Name	Operation	Weight	Active
1 M1(L)	Minimize	1	<input checked="" type="checkbox"/>
2 M2(L)	Minimize	1	<input checked="" type="checkbox"/>
3 M3(L)	Minimize	1	<input checked="" type="checkbox"/>
4 M4(L)	Minimize	1	<input checked="" type="checkbox"/>
- Optimization Results:**

DOF	Value
1 M5(GM/ID)	11.07
2 M4(GM/ID)	11.14
3 M1(GM/ID)	14.62
4 M5(L)	345.7n
5 M4(L)	232.1n
6 M3(L)	1.199u

Output Variable	Nominal
1 DC Gain	1.004k
2 UGF	201.8MEG
3 PM	70.66
4 DC PSR (dB)	-3.771
5 DC CMR (dB)	-16.16
6 Total Input Integrated Noise (Vrms)	11.78u
- Circuit Diagram:** A schematic of a Two-Stages Miller OTA with transistors M1a, M1b, M2a, M2b, M3, M4, and M5. It includes biasing nodes like IB1, IB2, and Vbiasn, and a compensation network with RZ and CC.

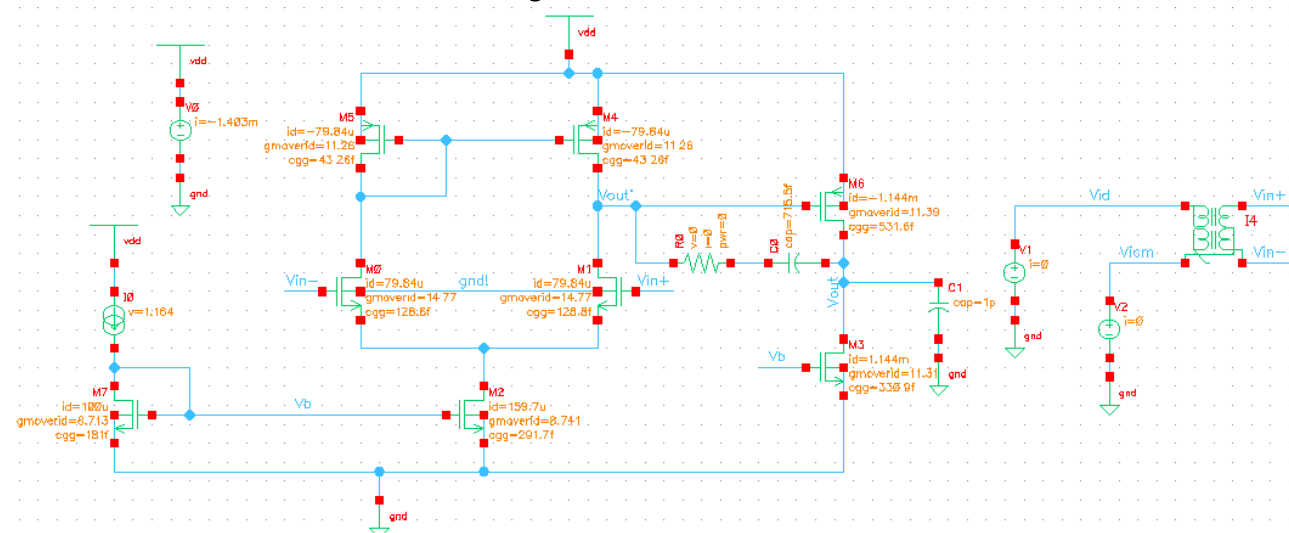
Initial design points from ADT

DOF	Value
1 M5(GM/ID)	11.07
2 M4(GM/ID)	11.14
3 M1(GM/ID)	14.62
4 M5(L)	345.7n
5 M4(L)	232.1n
6 M3(L)	1.199u

DOF	Value
6 M3(L)	1.199u
7 M2(L)	249.2n
8 M1(L)	641n
9 IB_Nominal	1.362m
10 CC_Nominal	715.6f
11 IB2/IB1	7.235

Output Variable	Nominal
17 M1(W)	25.21u
18 M2(W)	16.38u
19 M3(W)	31.87u
20 M4(W)	210.9u
21 M5(W)	103.1u
22 Rz	89.48

Cadence OP simulation with initial sizing



Results of initial sizing

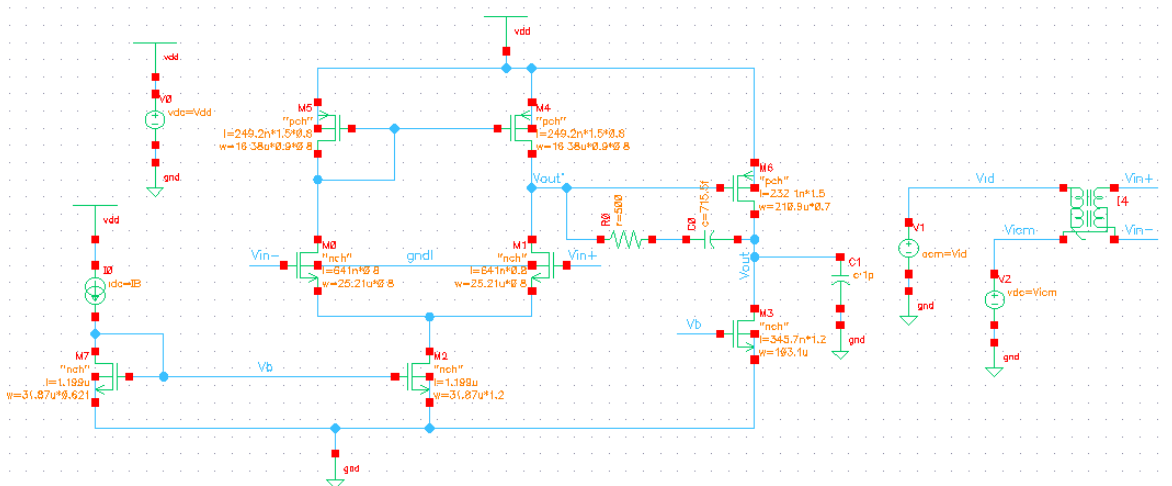
Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:session_15:1	Av Mag	1.014k			
TrainLAB:session_15:1	Av dB	60.12			
TrainLAB:session_15:1	BW	200.7k			
TrainLAB:session_15:1	UGF	190.9M			
TrainLAB:session_15:1	GBW	204M			
TrainLAB:session 15:1	PM	70.4			

Tuning Process:

As shown from previous results that all specs are achieved except gate capacitance spec so I have take the following design decision

- Decrease width of input pair to decrease capacitance but this will affect gain as I decreased length by the same ratio to save OP of input pair.
- To increase gain and GBW of OTA I have increased current in both 1st and 2nd stage.
- Then increase the Gm of 2nd stage and decrease Gm of 1st stage as UGF and PM of OTA have dropped.
- And also to increase PM I have increased length of 1st stage current mirror load to increase Rout.
- And finally to tune UGF with PM increase compensation resistor to make zero come in action with pole and increase PM without affecting UGF.

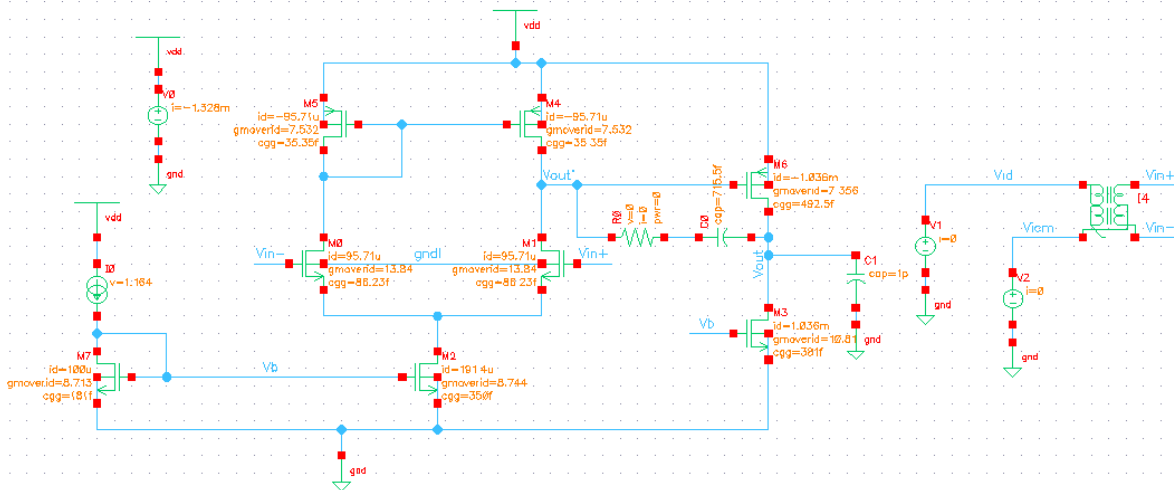
Schematic with final sizing:



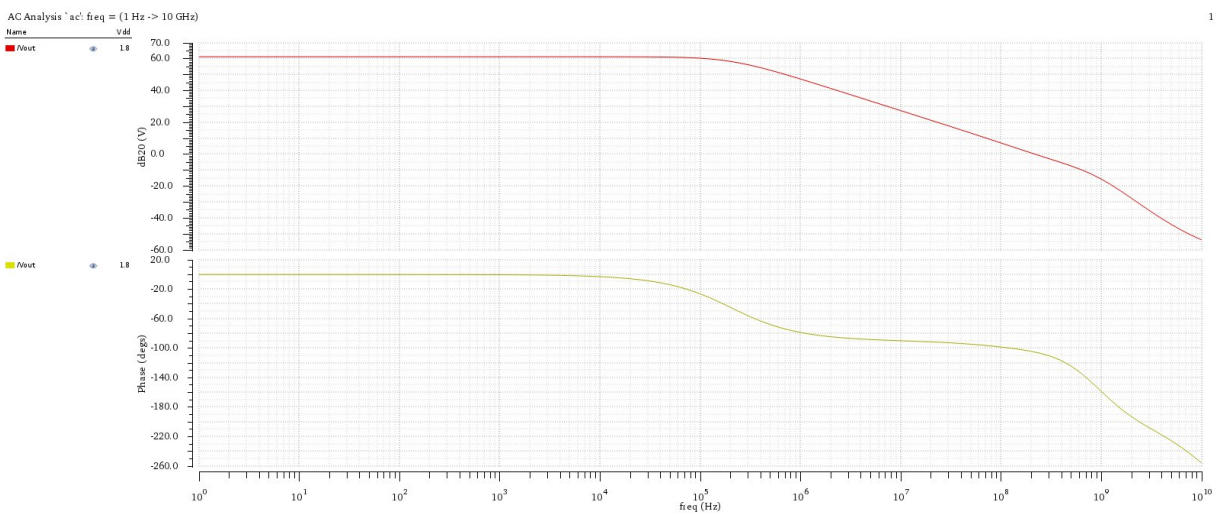
Results from ADEXL after tuning:

Test	Output	Nominal	Spec	Weight	Pass/Fail
TrainLAB:session_15:1	Av Mag	1.163k			
TrainLAB:session_15:1	Av dB	61.31			
TrainLAB:session_15:1	BW	204.8k			
TrainLAB:session_15:1	UGF	226.7M			
TrainLAB:session_15:1	GBW	238.7M			
TrainLAB:session_15:1	PM	74.62			

OP parameters from schematic after tuning:



Bode Plot



Results with Corners

		Parameter	Nominal					C0	C1
		IB	100u					90u	110u
		Vdd	1.8					1.6	2

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0	C1
TrainLAB:session_15:1	Av Mag	1.163k				1.005k	1.246k	1.005k	1.246k
TrainLAB:session_15:1	Av dB	61.31				60.04	61.91	60.04	61.91
TrainLAB:session_15:1	BW	204.8k				202.7k	220.5k	220.5k	202.7k
TrainLAB:session_15:1	UGF	226.7M				207M	241.8M	207M	241.8M
TrainLAB:session_15:1	GBW	238.7M				222M	253.2M	222M	253.2M
TrainLAB:session_15:1	PM	74.62				73.66	75.54	73.66	75.54

From previous results it's clear that all specs have been achieved with all corners for IB and VDD.