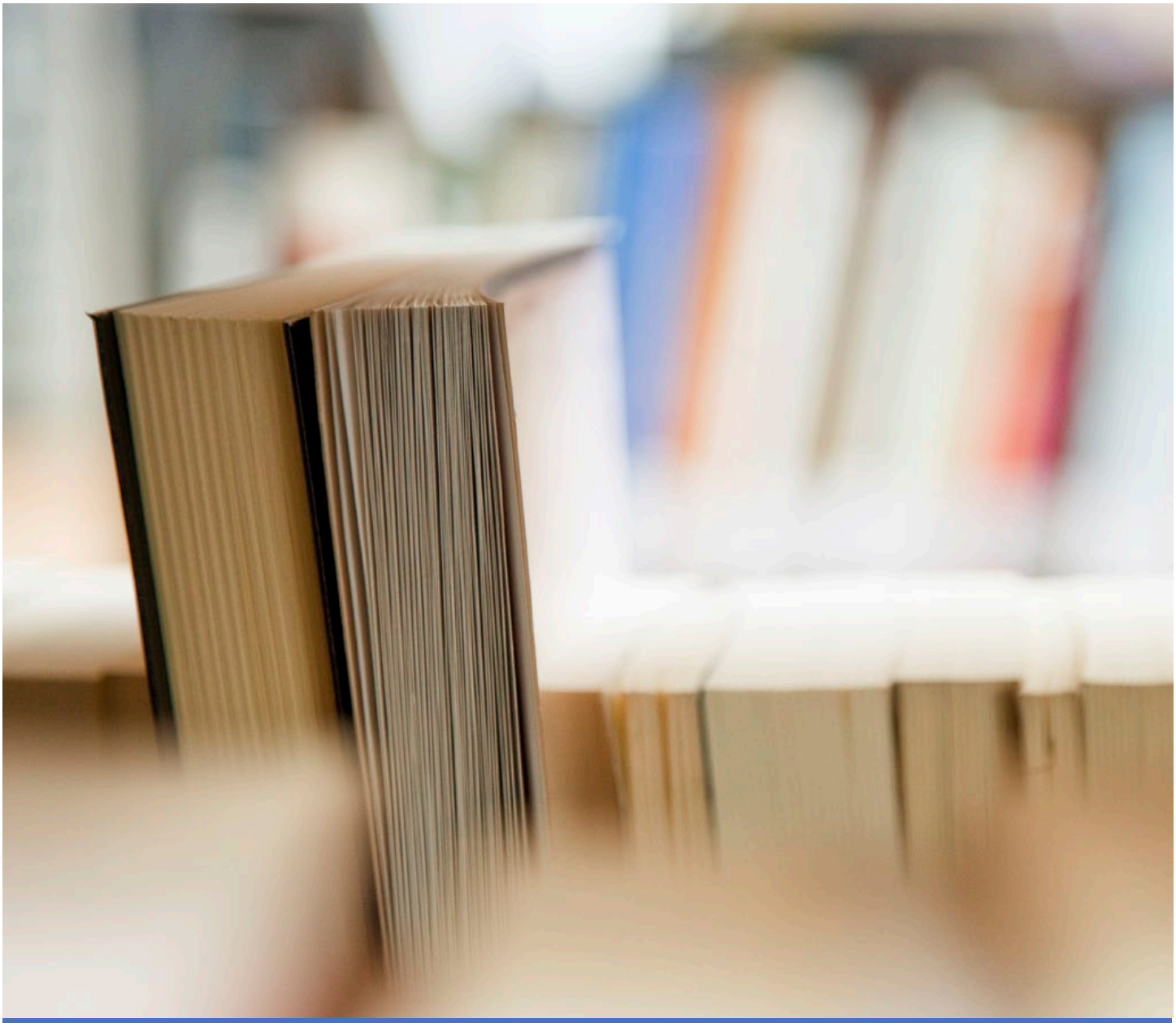

# Analog IC Design

## Labs Simulations & Results

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# Lab 01

LPF Simulations and MOSFET Characteristics

## Part 1: Low Pass Filter Simulation (LPF)

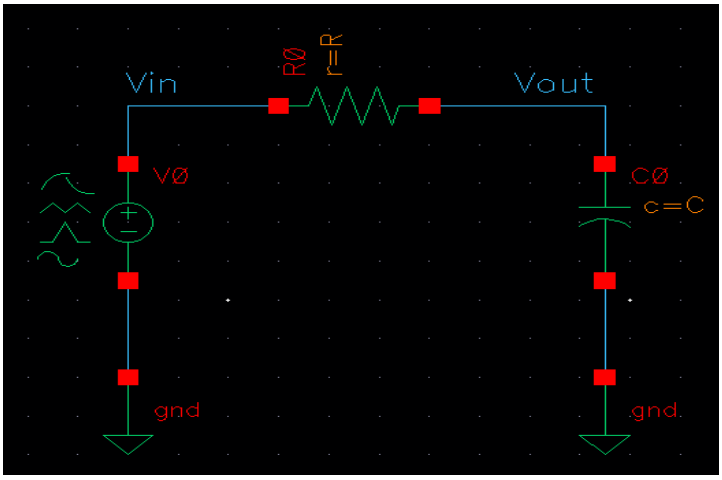


Fig.1 circuit schematic

# 1. Transient Analysis:

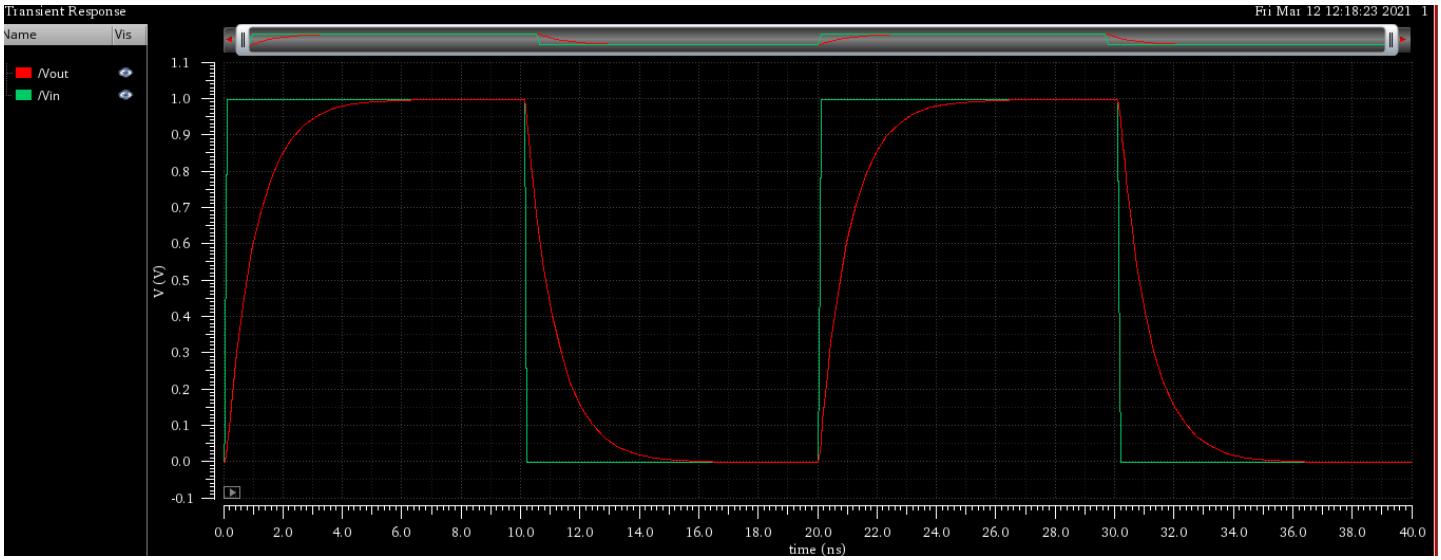


Fig.2 transient analysis with 2 CLK periods

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R=1 kΩ, C=1 pF, ℂ=1 ns.

The analytical results of fall time and rise time calculations are evaluated by the following relation: $T_R = T_F = 2.2RC \approx 2.2ns$.

Comment: on high values of R LPF begin to act as integrator as shown in the following figure.

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | /Vout | | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | /Vin | | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | rise time | 2.196n | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | fall time | 2.189n | | | |

Fig.3 rise time and fall time calculations

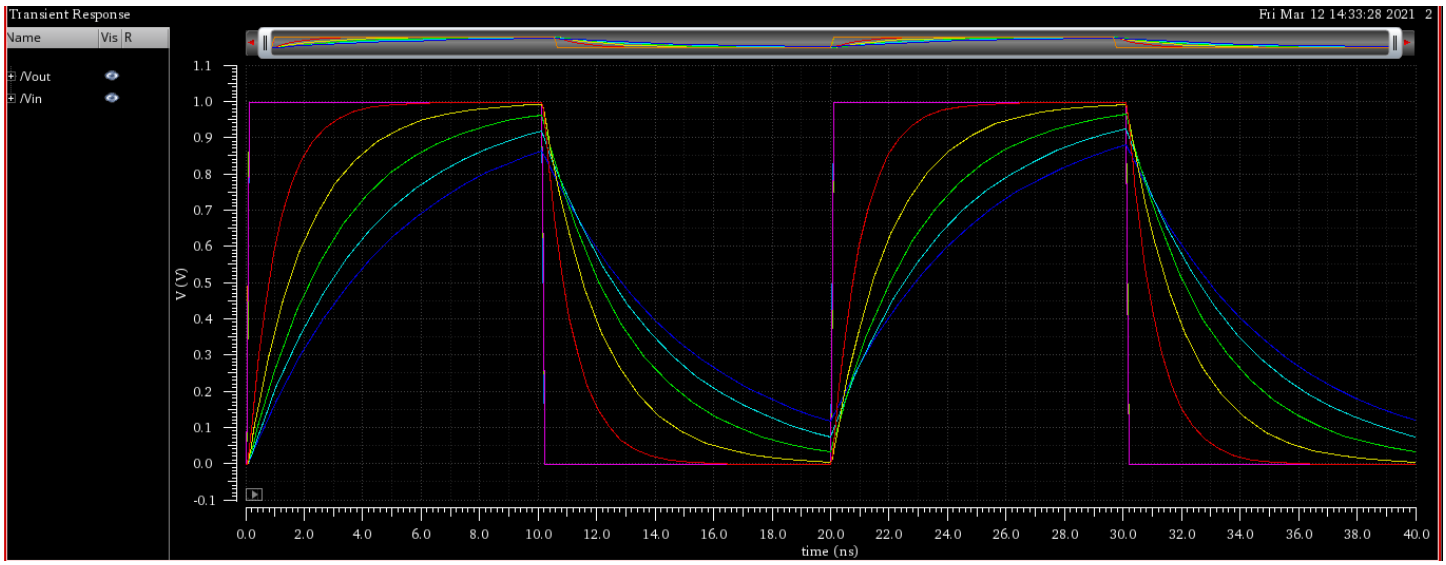


Fig.4 parametric sweep for different values of R

| Point | Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|---|
| Parameters: R=1k | | | | | | |
| 1 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vout | | | | |
| 1 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vin | | | | |
| 1 | Analog_IC_Design_Course:LPF_Simulation:1 | rise time | 2.196n | | | |
| 1 | Analog_IC_Design_Course:LPF_Simulation:1 | fall time | 2.189n | | | |
| Parameters: R=2k | | | | | | |
| 2 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vout | | | | |
| 2 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vin | | | | |
| 2 | Analog_IC_Design_Course:LPF_Simulation:1 | rise time | 4.387n | | | |
| 2 | Analog_IC_Design_Course:LPF_Simulation:1 | fall time | 4.39n | | | |
| Parameters: R=3k | | | | | | |
| 3 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vout | | | | |
| 3 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vin | | | | |
| 3 | Analog_IC_Design_Course:LPF_Simulation:1 | rise time | 6.582n | | | |
| 3 | Analog_IC_Design_Course:LPF_Simulation:1 | fall time | 6.562n | | | |
| Parameters: R=4k | | | | | | |
| 4 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vout | | | | |
| 4 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vin | | | | |
| 4 | Analog_IC_Design_Course:LPF_Simulation:1 | rise time | 8.769n | | | |
| 4 | Analog_IC_Design_Course:LPF_Simulation:1 | fall time | 8.787n | | | |
| Parameters: R=5k | | | | | | |
| 5 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vout | | | | |
| 5 | Analog_IC_Design_Course:LPF_Simulation:1 | /Vin | | | | |

Fig.5 different results of rise time and fall time after parametric sweep

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# 2. AC Analysis:

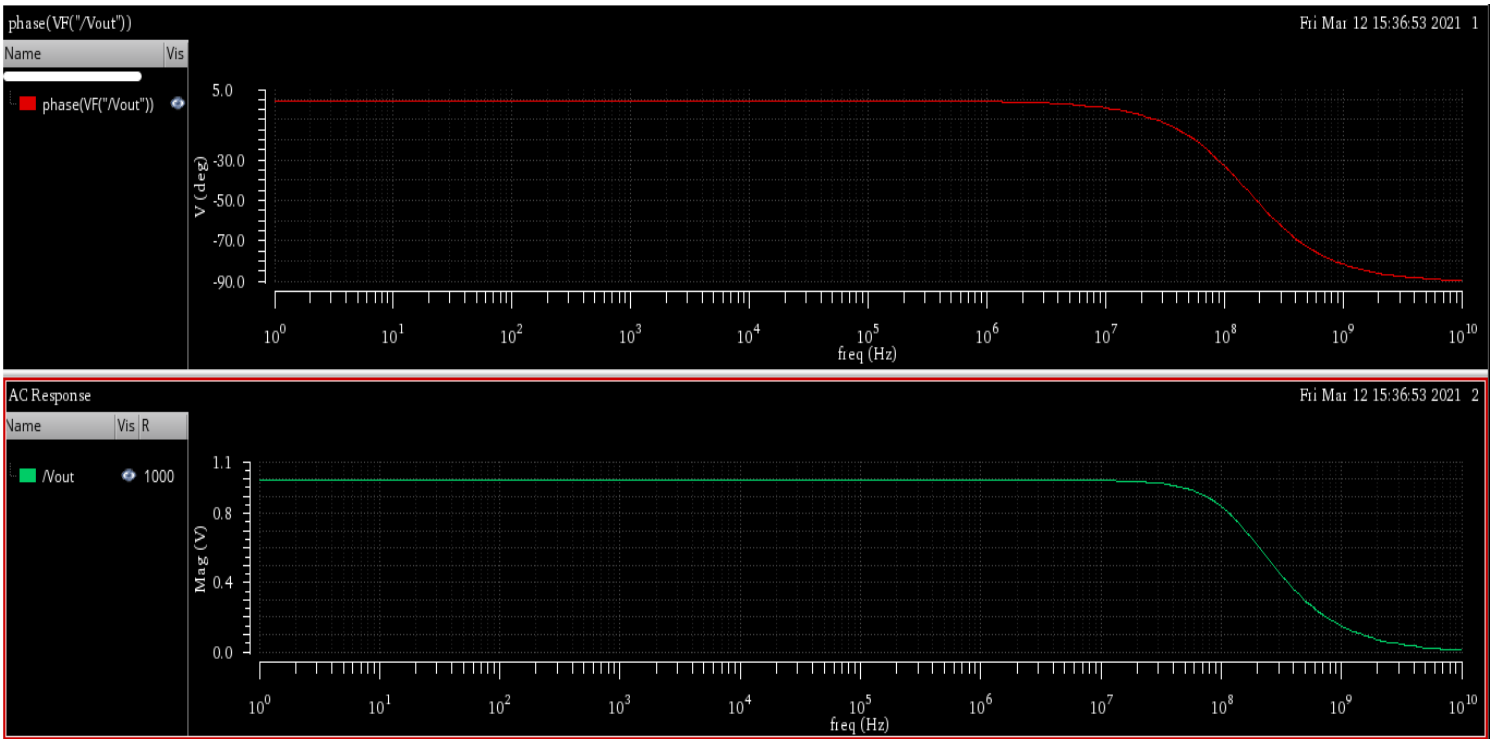


Fig.6 bode plot of LPF circuit simulation

Comment: as the resistance value increase time constant ƭ increase and the cut off frequency decreases and also the bandwidth and this shown in the following figure from parametric sweep simulation. $w_c = \frac{1}{\tau} = \frac{1}{RC}$

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| Analog_IC_Design_Course:LPF_Simulation:1 | /Vout | | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | gain | 1 | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | bandwidth | 158.8M | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | dc gain | 0 | | | |
| Analog_IC_Design_Course:LPF_Simulation:1 | phase(VF("/Vout")) | | | | |

Fig.7 bandwidth and gain calculations from LPF

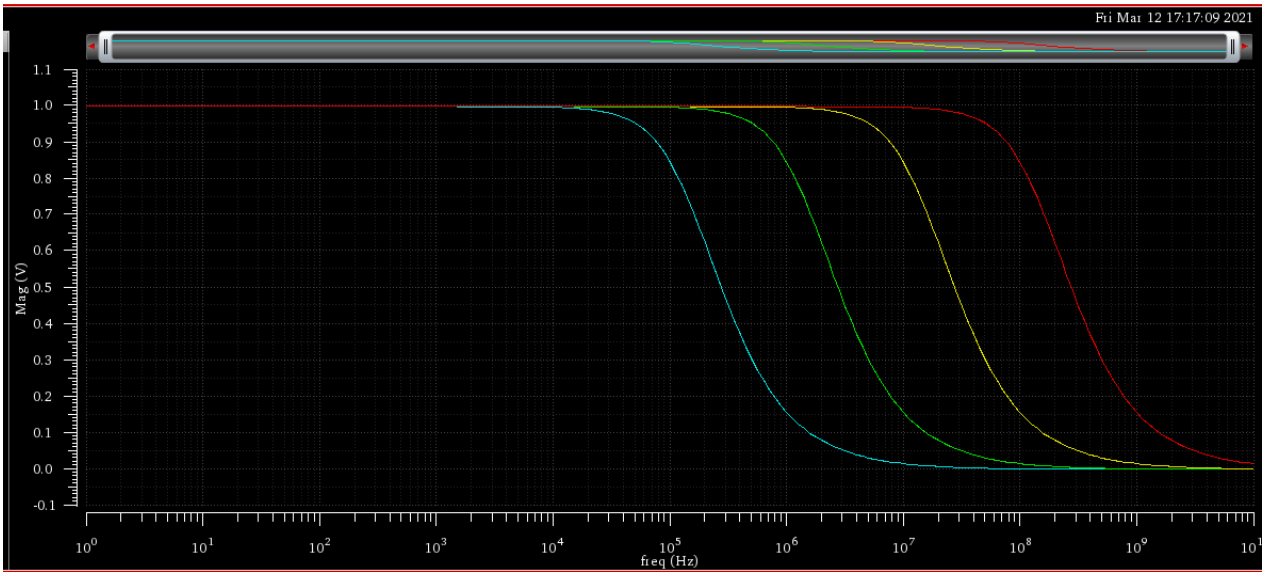

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Fig.8 parametric sweep AC analysis

| Point | Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|---|
| Parameters: R=1k | | | | | | |
| 1 | Analog_IC_Design_Course:LPF_Simulation:1 | mag plot | | | | |
| 1 | Analog_IC_Design_Course:LPF_Simulation:1 | bandwidth | 158.8M | | | |
| Parameters: R=10k | | | | | | |
| 2 | Analog_IC_Design_Course:LPF_Simulation:1 | mag plot | | | | |
| 2 | Analog_IC_Design_Course:LPF_Simulation:1 | bandwidth | 15.88M | | | |
| Parameters: R=100k | | | | | | |
| 3 | Analog_IC_Design_Course:LPF_Simulation:1 | mag plot | | | | |
| 3 | Analog_IC_Design_Course:LPF_Simulation:1 | bandwidth | 1.588M | | | |
| Parameters: R=1M | | | | | | |
| 4 | Analog_IC_Design_Course:LPF_Simulation:1 | mag plot | | | | |
| 4 | Analog_IC_Design_Course:LPF_Simulation:1 | bandwidth | 158.8k | | | |

Fig.9 bandwidth values after parametric sweep analysis

# 3. Pole Zero Analysis:

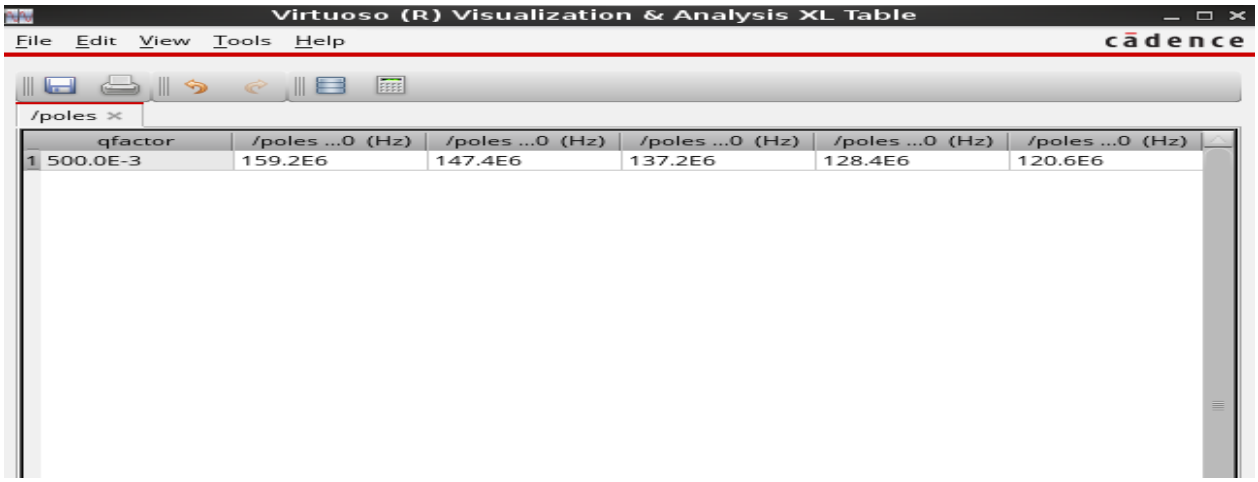


Fig.10 pole frequency of different values of resistance

Comment: pole frequency analysis is very near to values of different bandwidth in AC analysis above.

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# Part 2: MOSFET Characteristics

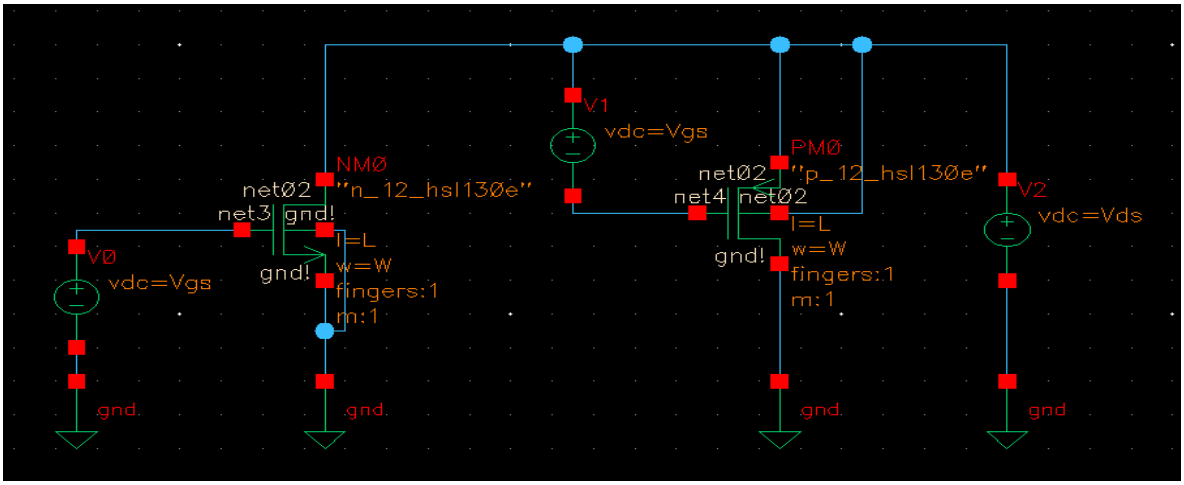


Fig.1 circuit schematic

# 1. ID vs VGS:

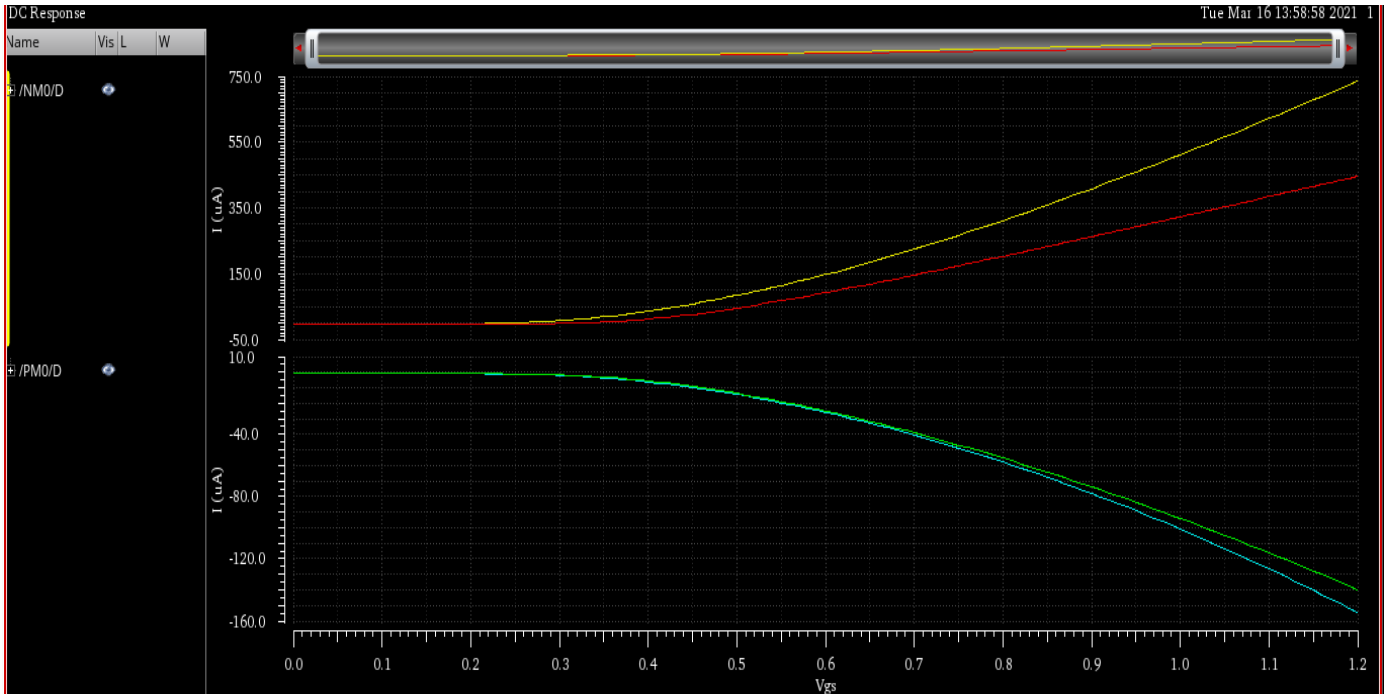


Fig.2 ID vs VGS characteristics for NMOS and PMOS

Comment: as it shown in the previous figure that drain current ID in long channel MOSFET is higher than the current in short channel MOSFET, and also the current relation in long channel is a quadratic relation but in short channel it's a linear relation and this happen because in short channel drain current is determined by velocity saturation so drain current become proportional to VGS not to $VGS^2$ as it in long channel MOSFET, and this which affect on current value as that the drain current in short channel is affected by both vertical electric field VGS and lateral electric field VDS which cause velocity saturation in drain current at short channel MOSFET.

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Comment: also as it shown in above figure the current in NMOS is higher than that in PMOS this is due to the mobility effect as the mobility of electrons is higher than the mobility of holes so the ratio between drain current in NMOS to that at PMOS equal to ratio between the mobility in electrons to that of holes $\frac{ID_n}{ID_p} = \frac{\mu_n}{\mu_p} = 2\sim4$, and also as it appear that the short channel MOSFET act as long channel MOSFET in case of PMOS short channel only affect in case of NMOS.

# 2. gm vs VGS:

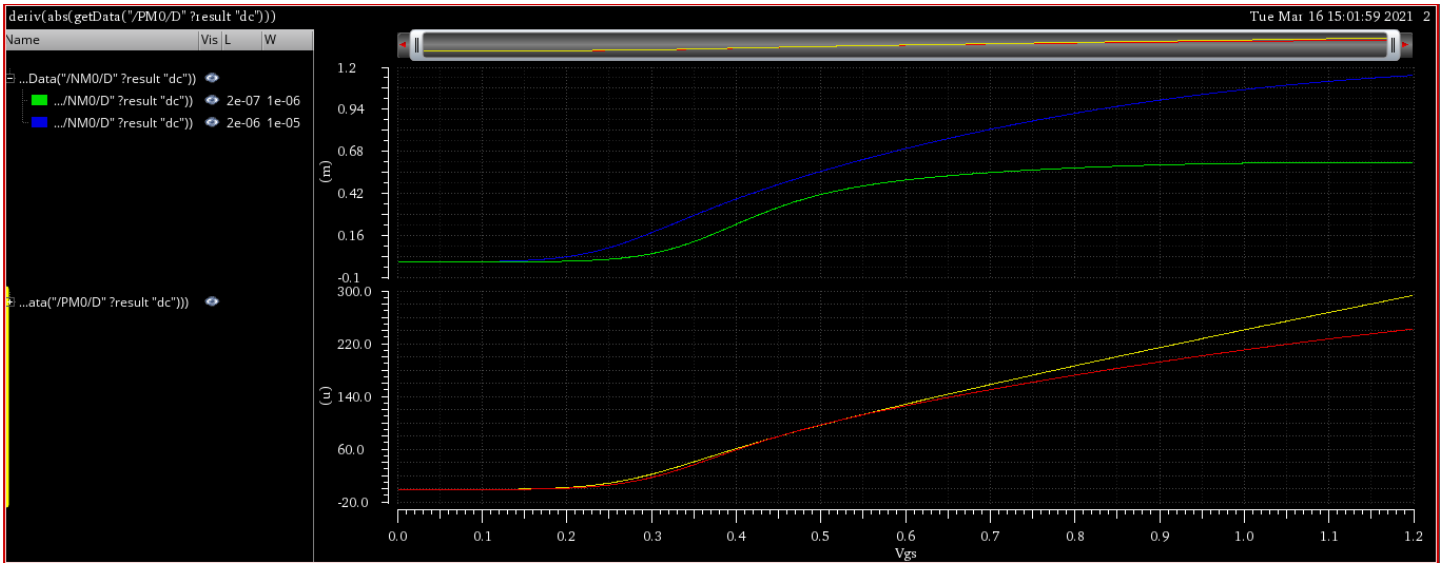


Fig.3 gm vs VGS plot from cadence

Comment: as it shown in above figure that gm increases approx. linearly with VGS in long channel as the relation between ID and VGS is a quadratic relation and gm is the change of drain current to change of VGS: $gm = \frac{\partial ID}{\partial VGS}$, and at short channel it can be considered as a step constant change as the relation between ID and VGS is a linear relation due to velocity saturation.

# 3. ID vs VDS:

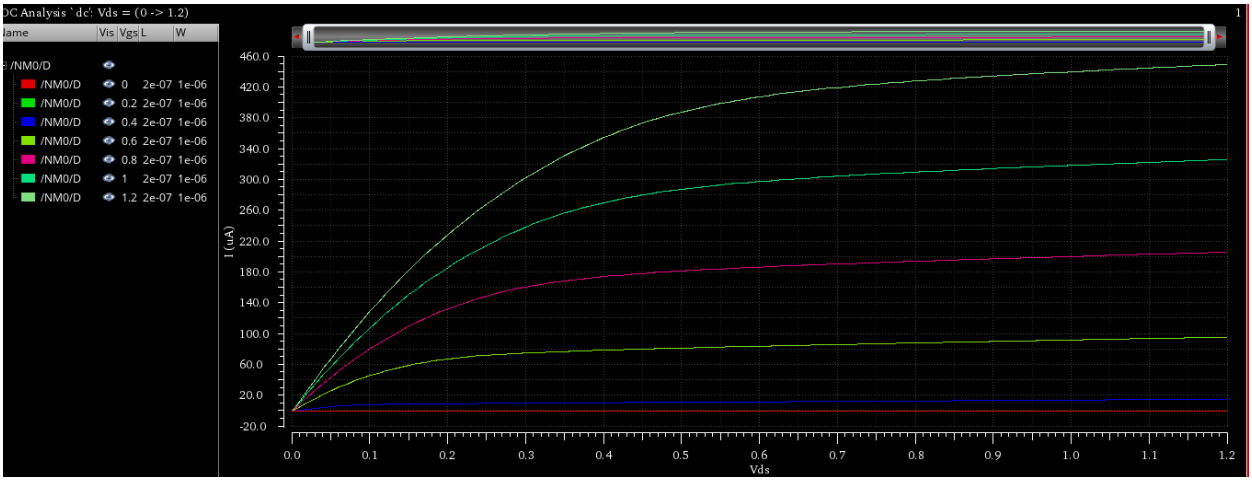

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Fig.4 ID vs VDS for short channel NMOS

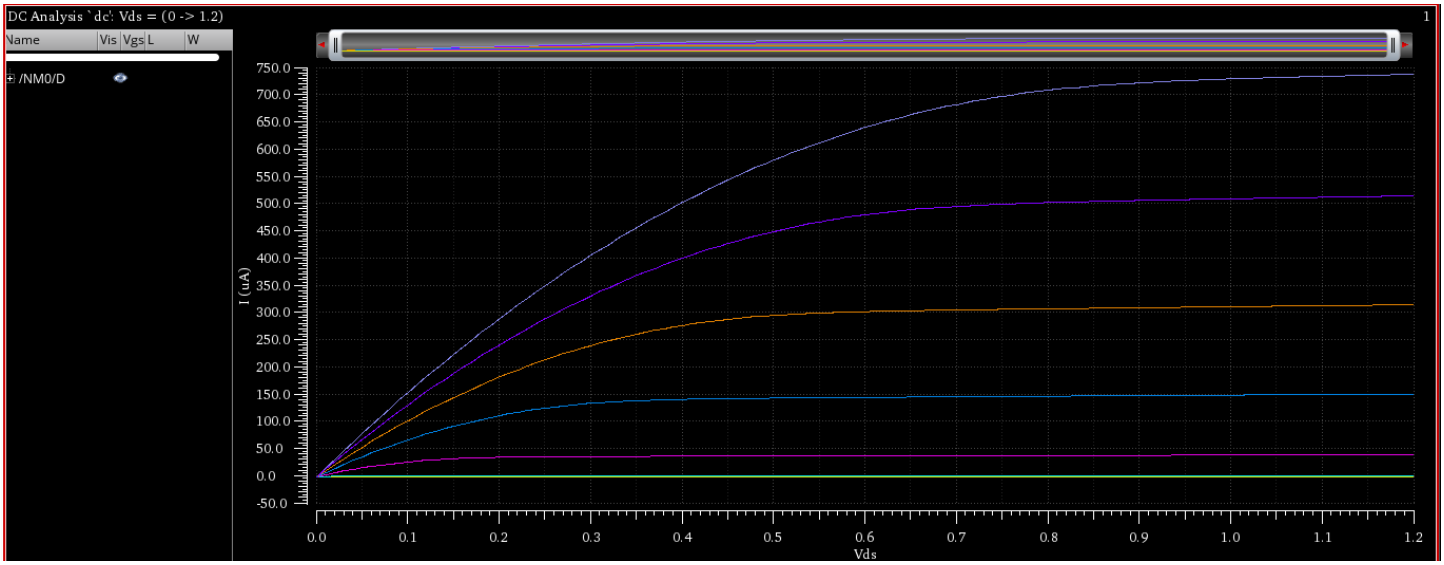


Fig.5 ID vs VDS for long channel NMOS

Comment: as it shown in above figures that the difference between short channel and long channel NMOS that the steps between different VGS voltage is a quadratic step in long channel and linear steps in short channel due to velocity saturation effect, and we notice that as the value of VGS increase the slope of saturation curve become higher as that the value of $VDS_{sat}$ increase.

# 4. Gm & $r_o$ vs VDS:

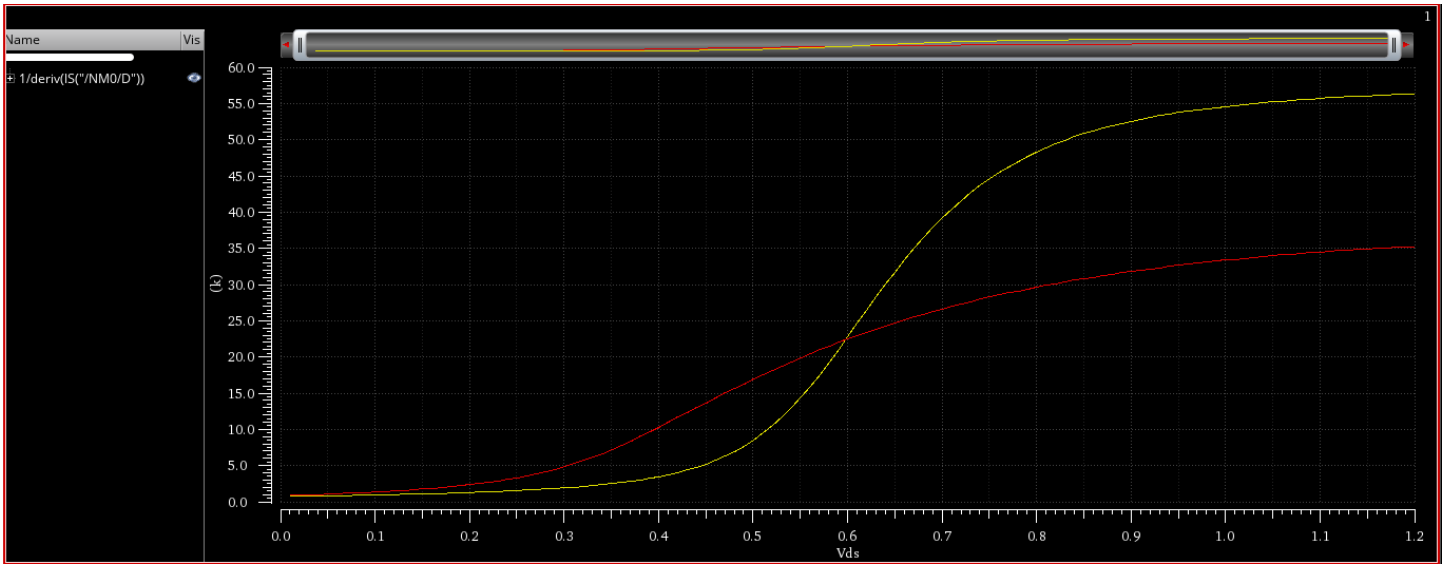


Fig.6 $r_o$ vs VDS for short and long channel NMOS

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# Lab 02

## Common Source Amplifier

## Part 1: Sizing Chart

For common mode output level we choose: $V_{RD} = \frac{VDD}{2} = 0.6$, so drain resistance will be $R_D = \frac{V_{RD}}{I_D} = \frac{0.6}{100u} = 6kohms.$

We have a new parameter which is $V^*$as for real MOSFET case $V_{ov} \neq 2I_D/g_m$, so we have $V^* = \frac{2I_D}{g_m}$, so the desired voltage gain will be $A_v = \frac{2V_{RD}}{V^*} = 5$, so operating amplifier voltage will be $V^* = V_Q^* = \frac{2V_{RD}}{A_v} = 0.24$.

Now we want to determine the width (W) of MOSFET from the following simulation:

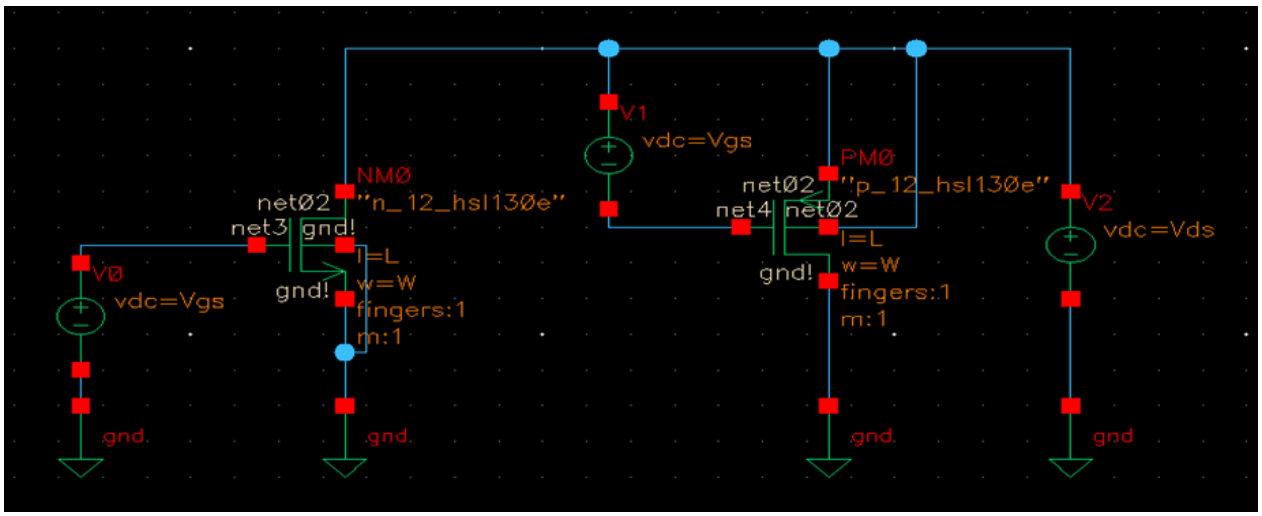


Fig.1 circuit schematic of NMOS and PMOS

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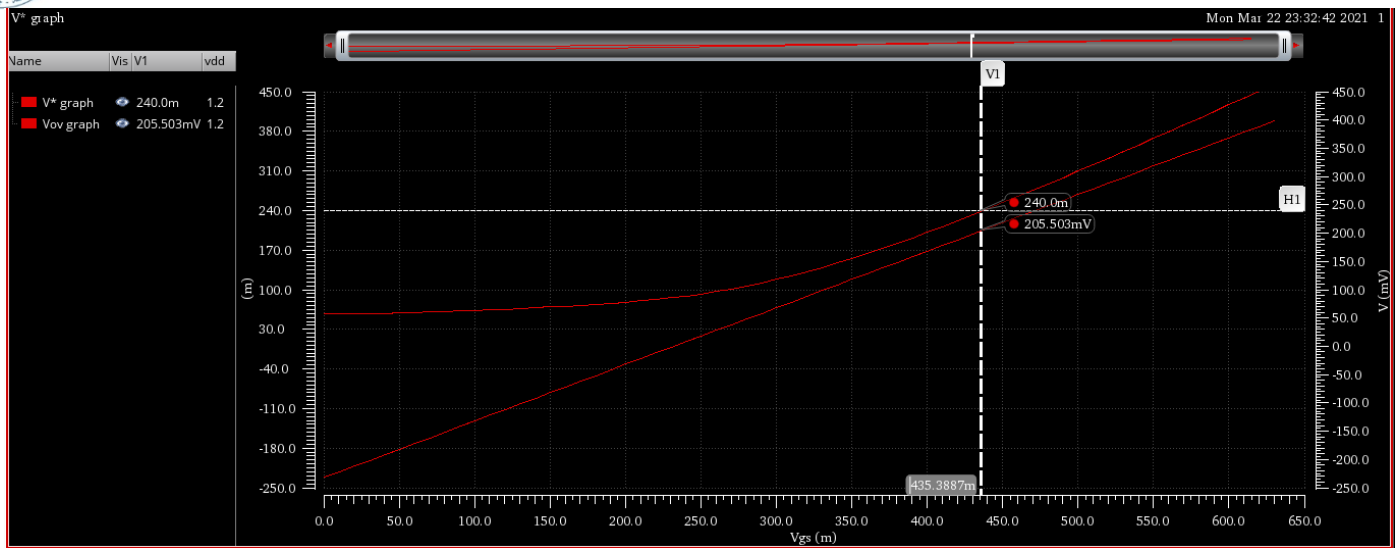


Fig.2 $V^*$and $V_{ov}$ curves versus $V_{gs}$

From the previous figure we notice that at the operating voltage of amplifier $V_Q^* = 240mV$,the actual overdrive voltage will be $V_{ovQ} = 205.503mV$, and $V_{GSQ} = 435.3887mV$.

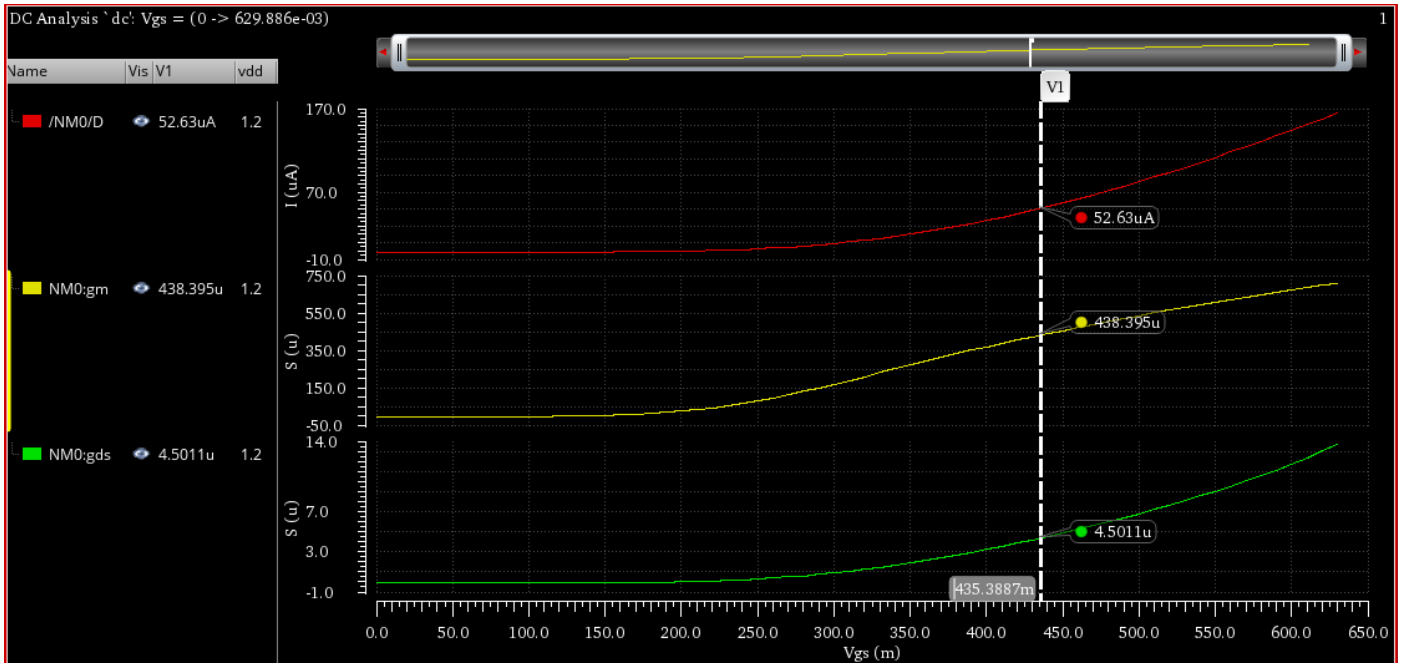


Fig.3 $I_D, g_m$ *and* $g_{ds}$versus VGS

Now from operating VGS value we get the following operating parameters: $I_{DX} = 52.63uA,$ $g_{mX} = 438.395um \text{ and } g_{sdX} = 8.55209um.$

As $I_D \propto W$ and we have at our assumed width in previous simulation: $W = 10um \rightarrow I_{DX} = 52.63uA$, so using cross multiplication and get width at desired operating current $I_D = 100um \rightarrow W \cong 20um$.

Now another check as $g_m \propto W$ at constant overdrive voltage so we get $g_{ds} = 8.974um \text{ and } g_m = 875.458um \text{ @ } W = 20um.$

And we have $r_o = \frac{1}{g_{ds}} = 116.96kohms$. so now we could calculate voltage gain $A_v = g_m * \left(\frac{R_D * r_o}{R_D + r_o}\right) = 4.9.$

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# Part 2: CS Amplifier

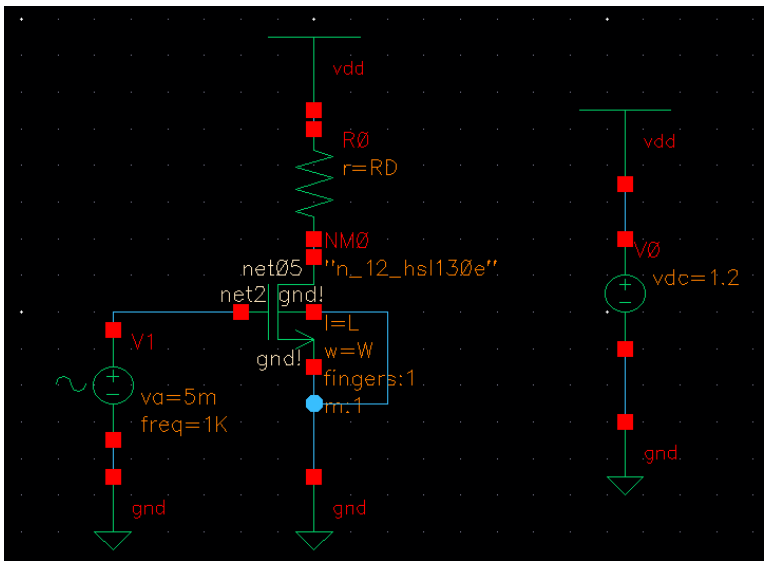


Fig.1 CS Amplifier circuit schematic

# 1. OP and AC analysis:

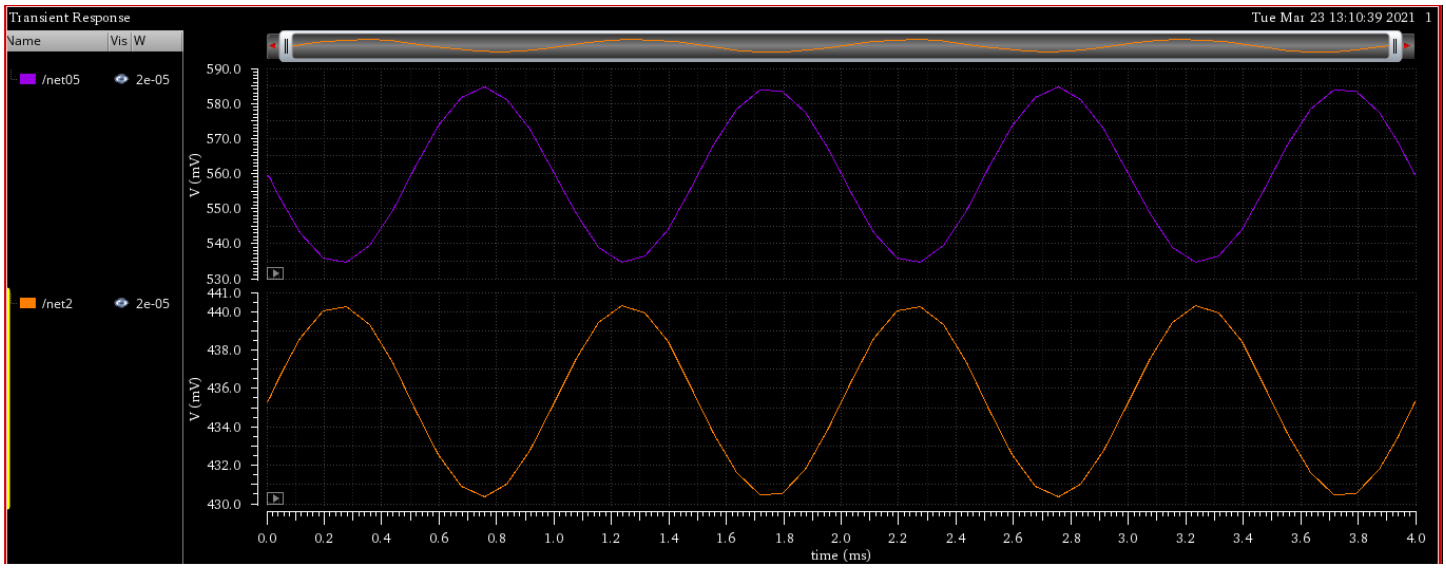


Fig.2 input signal and output signal after amplification

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| Analog_IC_Design_Course:CS_Amp:1 | output | | | | |
| Analog_IC_Design_Course:CS_Amp:1 | input | | | | |
| Analog_IC_Design_Course:CS_Amp:1 | NM0:gm | 883.6u | | | |
| Analog_IC_Design_Course:CS_Amp:1 | NM0:gds | 9.319u | | | |
| Analog_IC_Design_Course:CS_Amp:1 | NM0:id | 106.7u | | | |
| Analog_IC_Design_Course:CS_Amp:1 | NM0:vth | 228.4m | | | |
| Analog_IC_Design_Course:CS_Amp:1 | ro | 107.3k | | | |
| Analog_IC_Design_Course:CS_Amp:1 | gm*ro | 94.81 | | | |
| Analog_IC_Design_Course:CS_Amp:1 | amp-gain | 5.301 | | | |

Fig.3 results from simulation for operating parameters

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As shown in above figure that the results from CS simulation is nearly to our actual values from simulation in part 1.

- We see that $r_o$ is much larger than $R_D$ so assumption of ignoring $r_o$ is justified in this case as this is a parallel connection of resistors, but in case of short channel $r_o$ become more controlled by VDS so the value of $r_o$ decrease and the assumption not justified in this case.
- Intrinsic gain will be: $g_m * r_o = 94.81$.
- Amplifier gain will be: $A_v = 5.3$.
- As it shown that the intrinsic gain of single transistor is much larger than the amplifier gain.

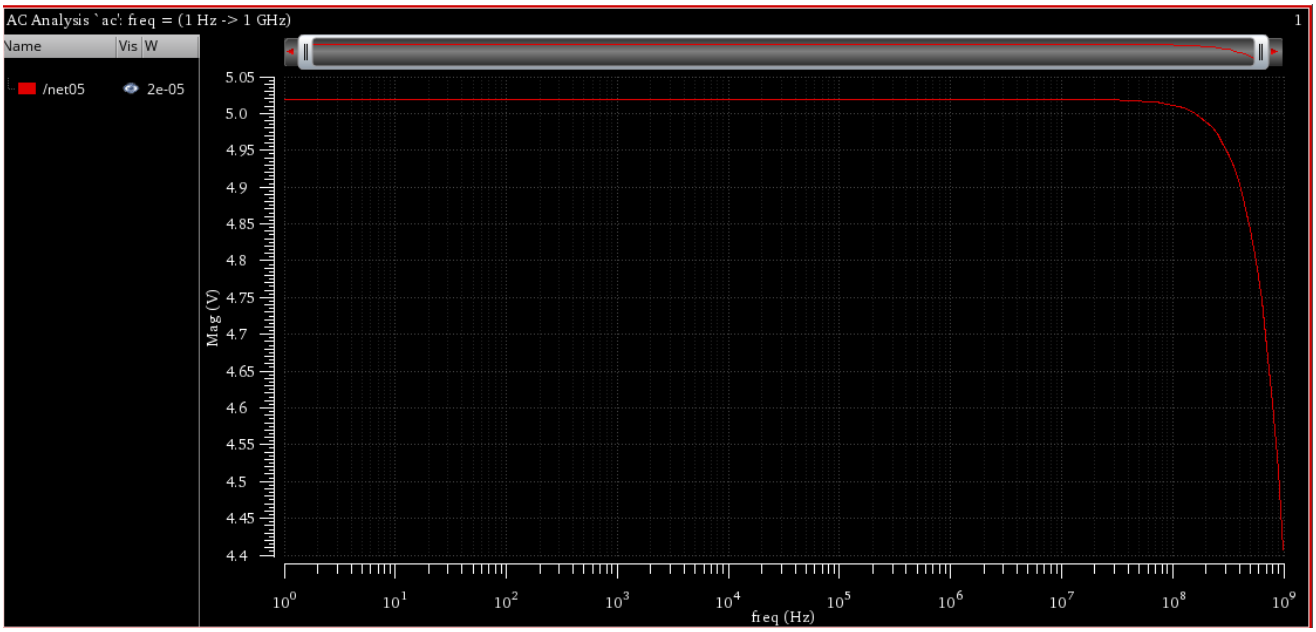


Fig.4 amplifier gain versus frequency from AC analysis

# 2. Gain Non-Linearity:

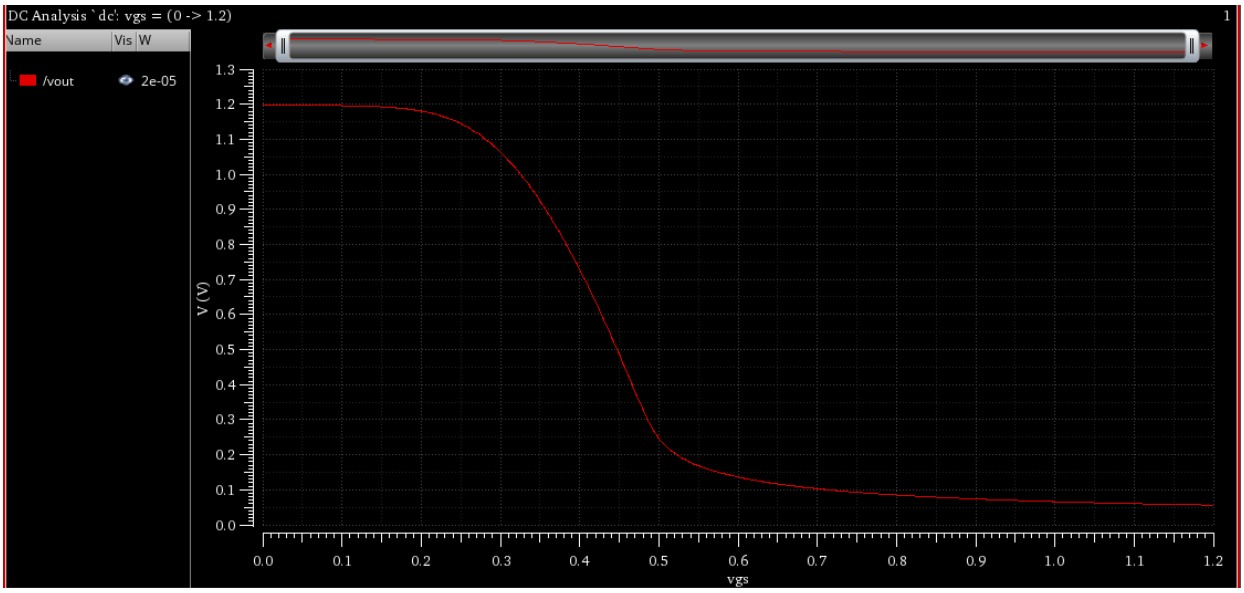


Fig.5 static characterization of the amplifier VOUT vs VIN

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Comment: as shown in the previous figure that the static gain isn't linear and this because of $g_m$ as that the gain equation is: $A_v \cong g_m * R_D$ and $g_m$ is a strong function of input voltage VGS which cause non-linearity.

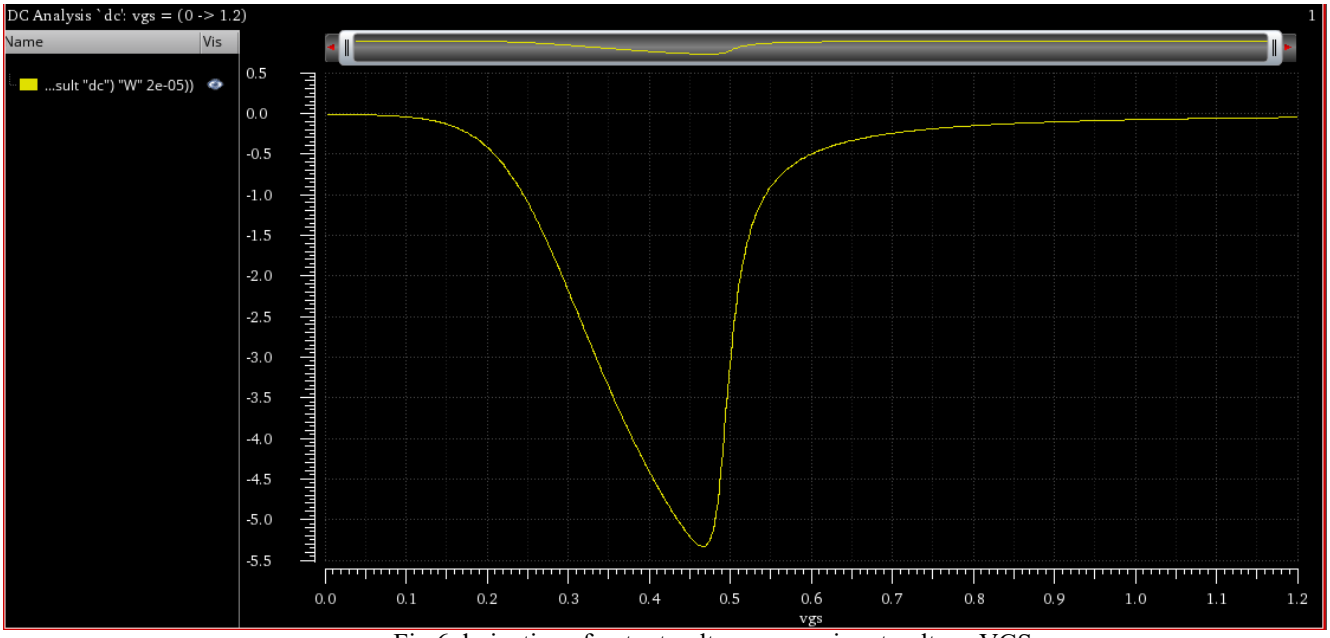


Fig.6 derivative of output voltage versus input voltage VGS

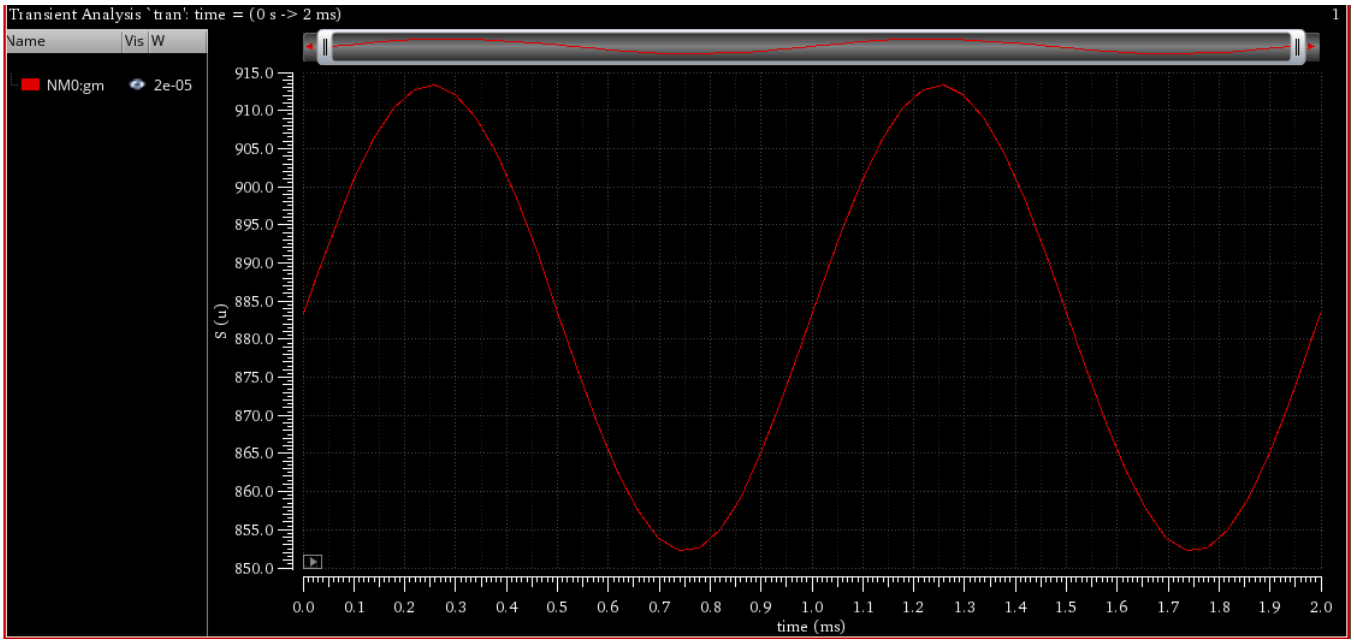


Fig.7 $g_m$ versus time after transient analysis

Comment: from above simulations it's clear that the gain is not linear as it is function in $g_m$ which is function in its turn in input voltage VIN "VGS" and it shown in the transient analysis of $g_m$ as it changes with time as shown in above figure.

# 3. Maximum Gain:

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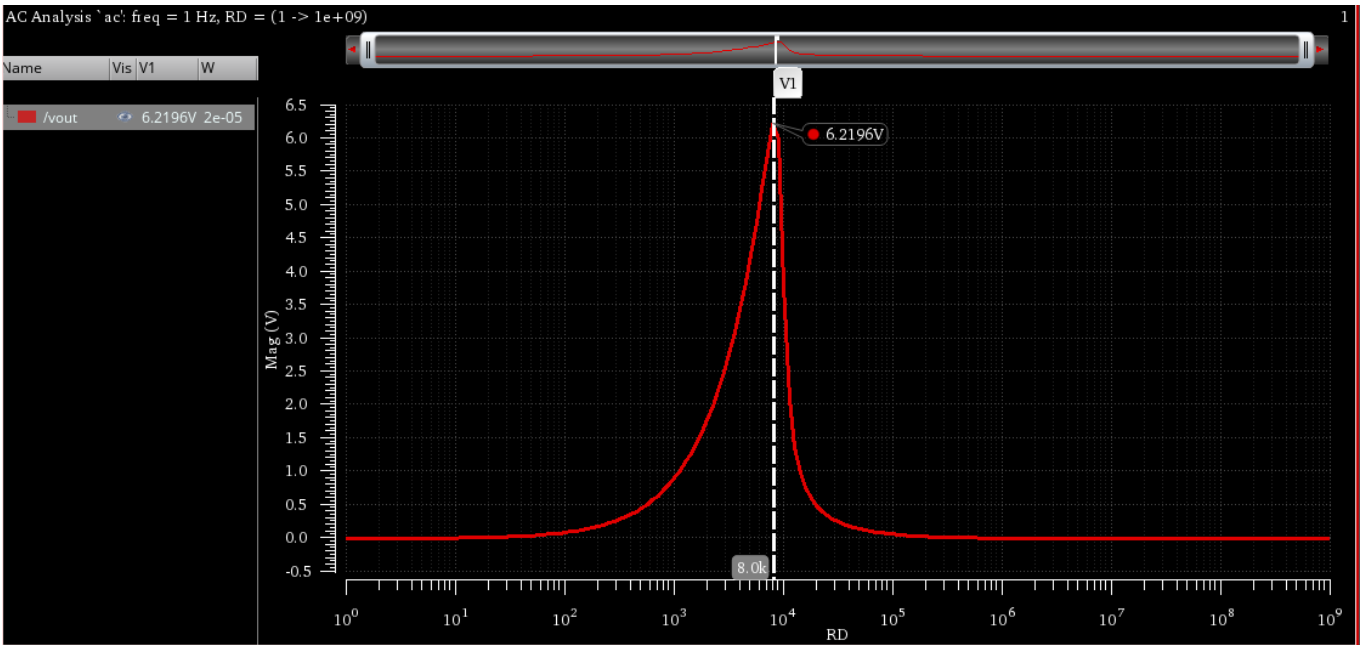


Fig.8 voltage gain $A_v$ versus RD AC analysis

Comment: as shown in above figure that the gain increase with change of RD but then decrease and this happen because of the increase of value of RD as the actual relation of voltage gain: $A_v = g_m * (R_D \parallel r_o)$ so by increasing the value of RD it becomes more comparable with $r_o$ so this parallel connection decreases the value of total resistance which decrease the gain as shown in above figure.

So as shown that the highest gain will be: $A_v = 6.2$ and the value of drain resistance which give this gain will be: $R_D = 8K$.

Max gain calculated in part 1: $A_v = 4.9 = g_m * R_D$ and the value of $g_m = 883.5uS$, so $R_D = 5.5kohms$.

The available swing of output maximum gain will equal: $Vdd - V_{RD} - V_{ov} = 1.2 - 106u * 8k - 435.38m + 228.4m = 0.145\ volts.$

From previous conclusions the scaling down of supply voltage VDD affects on output swing which also affect on gain.

# Lab 03

## Cascode Amplifier

## Part 1: Sizing Chart

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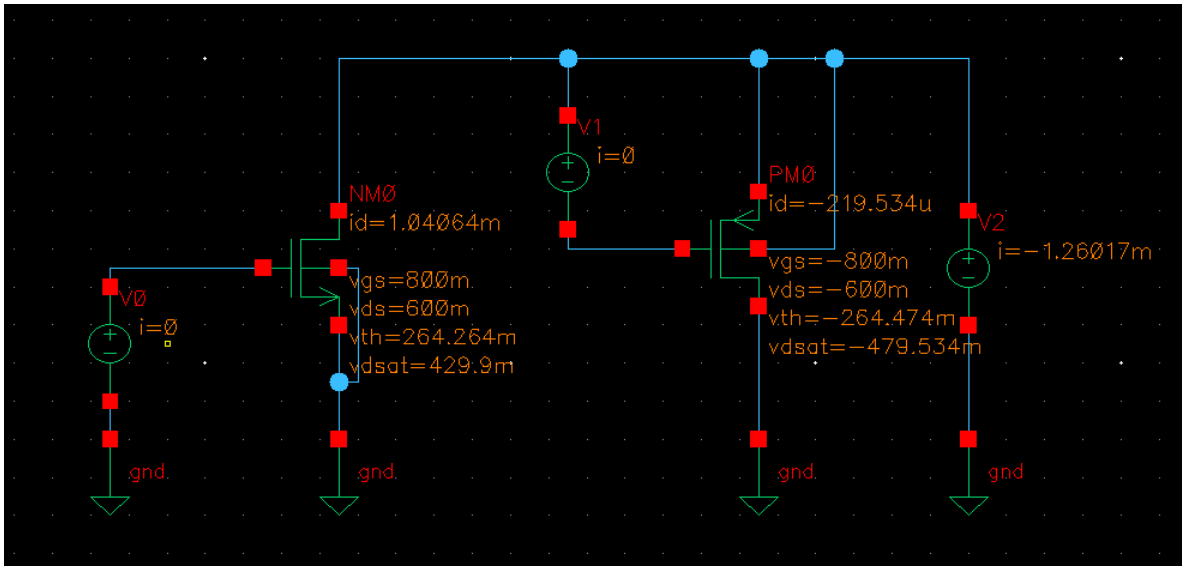


Fig.1 testbench circuit for NMOS OP parameters

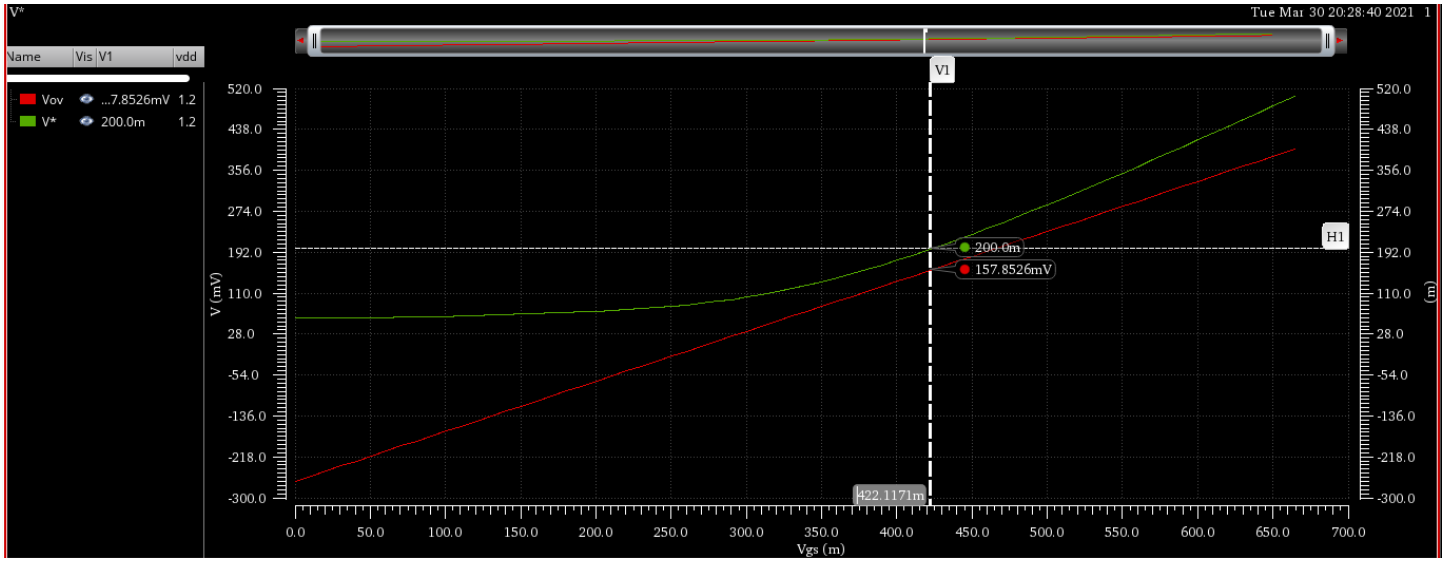


Fig.2 V* and Vov versus VGS

Comment: we find from the previous figure's simulation the following results at $V_Q^* = 200mV \rightarrow V_{ovQ} = 157.8526mV, V_{GSQ} = 422.1171mV.$

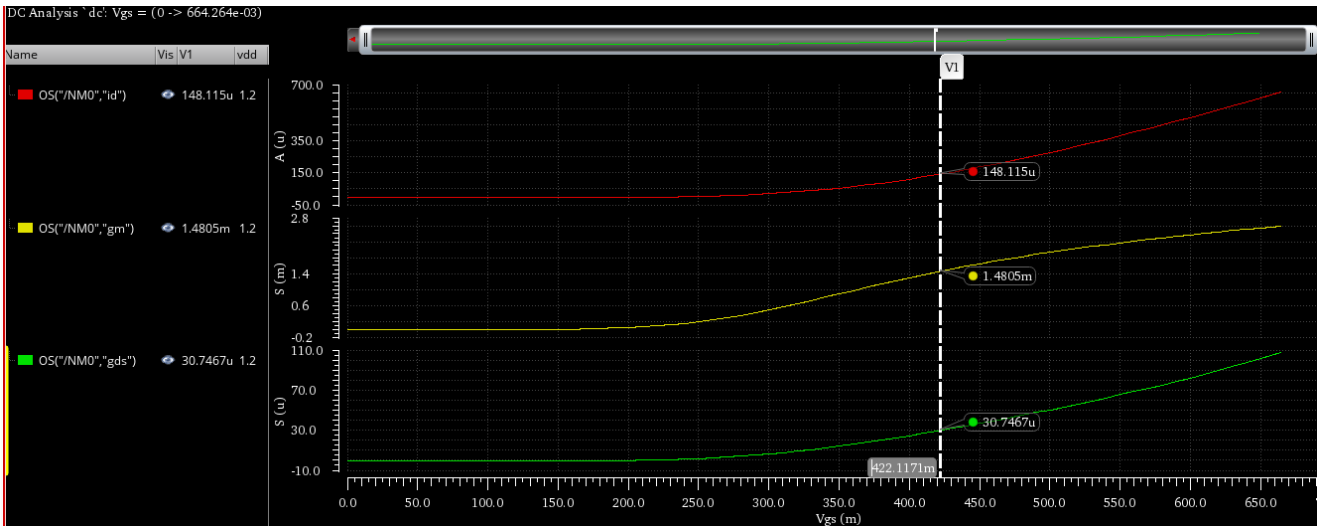

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Fig.3 gm, id and gds versus VGS

Comment: we get values at $V_{gsQ} = 422.1171mV \rightarrow g_m = 1.408m, g_{ds} = 30.7468u \; and \; I_D = 148.115uA.$

As current is proportional to width use cross multiplication to get actual width at $I_D = 20uA \rightarrow W = 1.35um$.

# Part 2: CASCODE for Gain

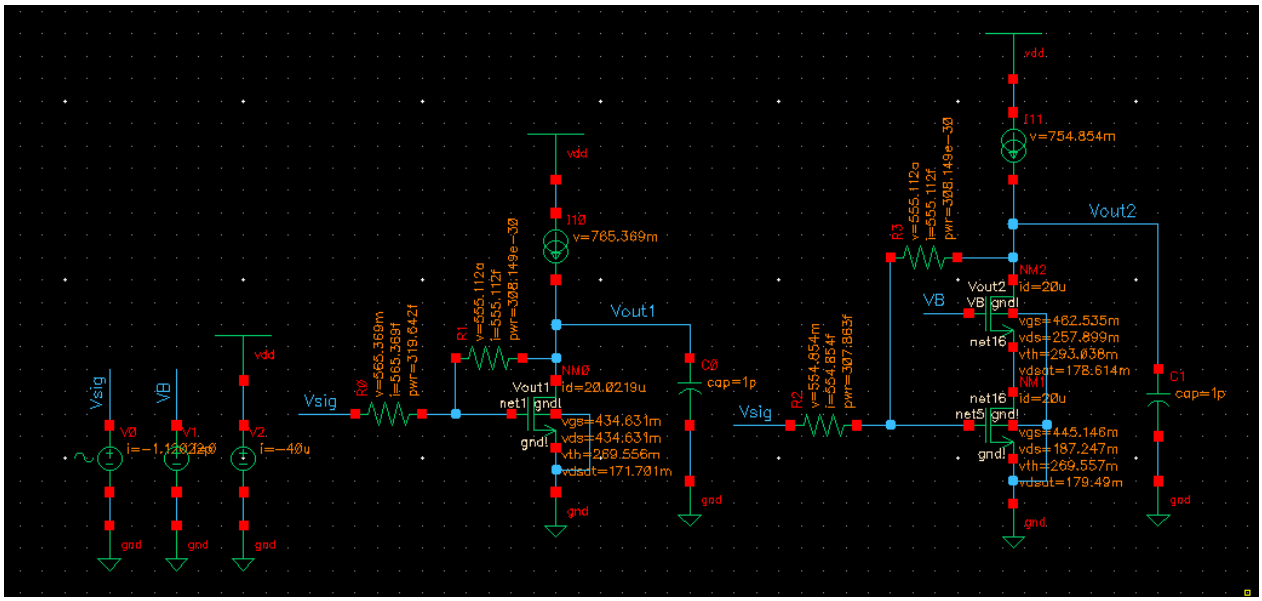


Fig.1 Circuit schematic for cascode and CS amplifiers with OP parameters

## 1. OP Analysis:

Now we want to choose the value of cascode bias voltage VB at $VDS = V_{ovQ} + 100m = 257.8526m$ so from the following figure we choose $VB = 649.782mV$.

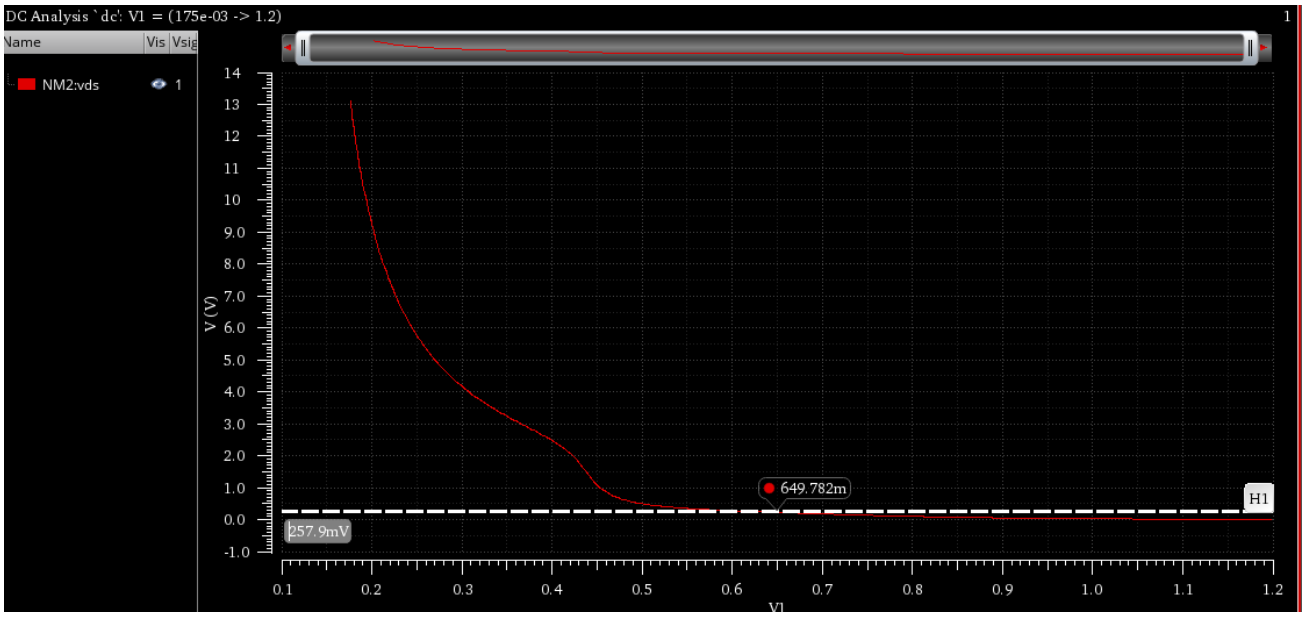


Fig.2 DC sweep for cascode bias voltage versus VDS to get suitable VB

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| Test | Output | Nominal | Spec |
|---|---|---|---|
| | | | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:id | 20.02u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:vgs | 434.6m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:vds | 434.6m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:vth | 269.6m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:vdsat | 171.7m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:gm | 194u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:gds | 4.519u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:gmb | 25.15u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:cdb | -689.3a | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:cgd | -398.1a | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:cgs | -5.166f | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:csb | -1.449f | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM0:region | 2 | |

Fig.3 OP parameters of MOSFET at CS amplifier NM0

| Test | Output | Nominal | Spec |
|---|---|---|---|
| | | | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:id | 20u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:vgs | 445.1m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:vds | 187.2m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:vth | 269.6m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:vdsat | 179.5m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:gm | 173.7u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:gds | 24.03u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:gmb | 22.86u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:cdb | -811.2a | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:cgd | -528.8a | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:cgs | -5.19f | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:csb | -1.442f | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM1:region | 2 | |

Fig.4 OP parameters of cascode MOSFET NM1

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| Test | Output | Nominal | Spec |
|---|---|---|---|
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:id | 20u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:vgs | 462.5m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:vds | 257.9m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:vth | 293m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:vdsat | 178.6m | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:gm | 187.1u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:gds | 8.633u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:gmb | 21.39u | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:cdb | -695.3a | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:cgd | -435.2a | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:cgs | -5.164f | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:csb | -1.266f | |
| Analog_IC_Design_Course:Cascode_Amp:1 | NM2:region | 2 | |

Fig.5 OP parameters of cascode MOSFET NM2

Comment.1: VTH of MOSFET NM0 and NM1 are the same and not suffer from body effect as the source and bulk are directly connected to GND, but the value of VTH of NM2 is different as it's suffer from body effect as the source isn't connected to GND so there is value foe VBS which increase threshold voltage of NM2.

Comment.2: as it shown that all MOSFETs are in saturation region which is equivalent to value 2 at region simulation in cadence.

Comment.3: a) $G_m > G_{ds}$ b) $G_m > G_{mb}$ c) $|C_{gs}| \gg |C_{gd}|$ d) $|C_{sb}| \gg |C_{db}|$

## 2. AC Analysis:

| Test | Output | Nominal | Spec |
|---|---|---|---|
| Analog_IC_Design_Course:Cascode_Amp:1 | dB20(VF("/Vout1")) | | |
| Analog_IC_Design_Course:Cascode_Amp:1 | ymax(dB20(VF("/Vout1"))) | 32.65 | |
| Analog_IC_Design_Course:Cascode_Amp:1 | ymax(mag(VF("/Vout1"))) | 42.93 | |
| Analog_IC_Design_Course:Cascode_Amp:1 | bandwidth(VF("/Vout1") 3 "lo... | 718.9k | |
| Analog_IC_Design_Course:Cascode_Amp:1 | gainBwProd(VF("/Vout1")) | 30.93M | |
| Analog_IC_Design_Course:Cascode_Amp:1 | dB20(VF("/Vout2")) | | |
| Analog_IC_Design_Course:Cascode_Amp:1 | ymax(dB20(VF("/Vout2"))) | 45.19 | |
| Analog_IC_Design_Course:Cascode_Amp:1 | ymax(mag(VF("/Vout2"))) | 181.8 | |
| Analog_IC_Design_Course:Cascode_Amp:1 | bandwidth(VF("/Vout2") 3 "lo... | 136.8k | |
| Analog_IC_Design_Course:Cascode_Amp:1 | gainBwProd(VF("/Vout2")) | 24.94M | |

Fig.6 simulation results of AC analysis for CS amplifier and CASCODE amplifier

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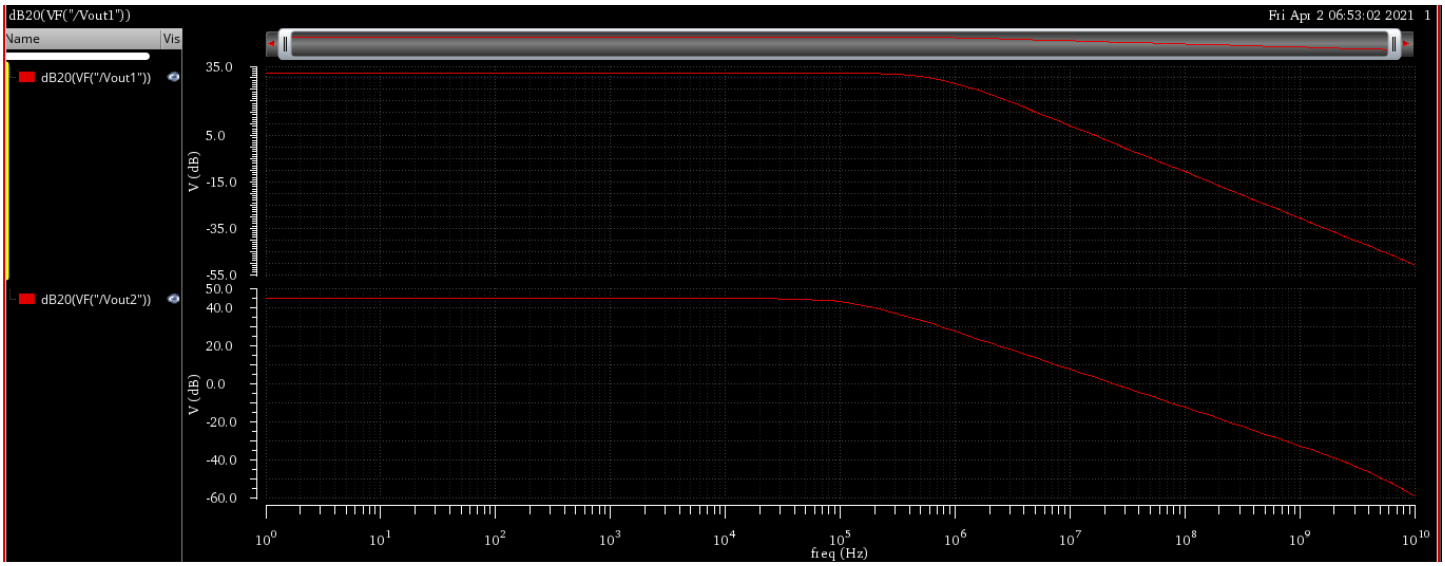


Fig.7 CS and CASCODE amplifiers gain in DB

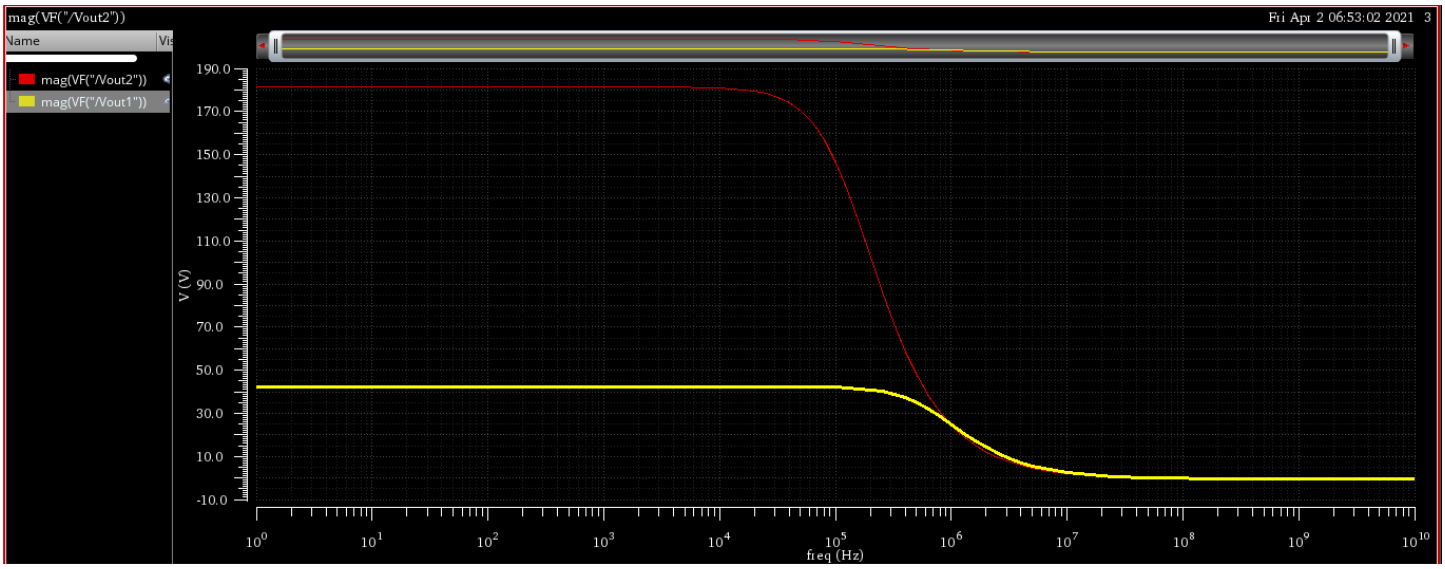


Fig.8 CS and CASCODE gain magnitude

# Part 3: CASCODE for BW

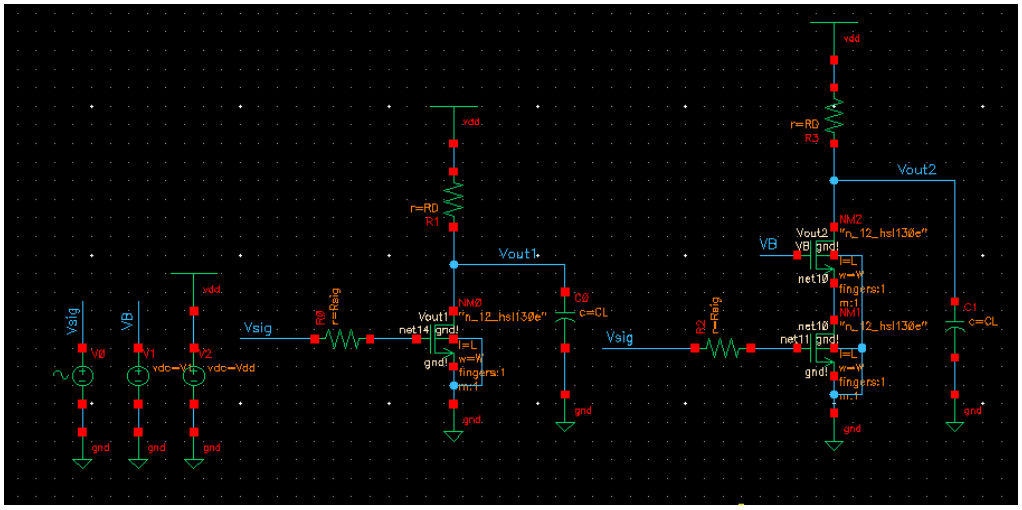

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Fig.1 Circuit schematic for CASCODE and CS amplifier after replacing current source by RD

# 1.OP Analysis:

Hint: as we want voltage drop on RD as following $V_{RD} = {Vdd}/{2} = 0.6$ and the value of current is $I_d \cong 20uA$ so we will set the value of resistance $R_D = \frac{V_{RD}}{I_D} = 30Kohms$.

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| Analog_Course:Cascode_BW:1 | NM0:id | 18.48u | | | |
| Analog_Course:Cascode_BW:1 | NM0:vgs | 422.1m | | | |
| Analog_Course:Cascode_BW:1 | NM0:vds | 645.6m | | | |
| Analog_Course:Cascode_BW:1 | NM0:vth | 269.6m | | | |
| Analog_Course:Cascode_BW:1 | NM0:vdsat | 162.5m | | | |
| Analog_Course:Cascode_BW:1 | NM0:gm | 189.7u | | | |
| Analog_Course:Cascode_BW:1 | NM0:gds | 3.751u | | | |
| Analog_Course:Cascode_BW:1 | NM0:gmb | 24.48u | | | |
| Analog_Course:Cascode_BW:1 | NM0:cdb | -635.8a | | | |
| Analog_Course:Cascode_BW:1 | NM0:cgd | -393.1a | | | |
| Analog_Course:Cascode_BW:1 | NM0:cgs | -5.117f | | | |
| Analog_Course:Cascode_BW:1 | NM0:csb | -1.446f | | | |
| Analog_Course:Cascode_BW:1 | NM0:region | 2 | | | |

Fig.2 OP parameters of MOSFET of CS amplifier

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| Analog_Course:Cascode_BW:1 | NM1:id | 18.29u | | | |
| Analog_Course:Cascode_BW:1 | NM1:vgs | 422.1m | | | |
| Analog_Course:Cascode_BW:1 | NM1:vds | 209.4m | | | |
| Analog_Course:Cascode_BW:1 | NM1:vth | 269.6m | | | |
| Analog_Course:Cascode_BW:1 | NM1:vdsat | 162.3m | | | |
| Analog_Course:Cascode_BW:1 | NM1:gm | 185.9u | | | |
| Analog_Course:Cascode_BW:1 | NM1:gds | 12.09u | | | |
| Analog_Course:Cascode_BW:1 | NM1:gmb | 24.31u | | | |
| Analog_Course:Cascode_BW:1 | NM1:cdb | -868a | | | |
| Analog_Course:Cascode_BW:1 | NM1:cgd | -512a | | | |
| Analog_Course:Cascode_BW:1 | NM1:cgs | -5.692f | | | |
| Analog_Course:Cascode_BW:1 | NM1:csb | -1.594f | | | |
| Analog_Course:Cascode_BW:1 | NM1:region | 2 | | | |

Fig.3 OP parameters of 1st MOSFET of CASCODE amplifier

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| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| Analog_Course:Cascode_BW:1 | NM2:id | 18.3u | | | |
| Analog_Course:Cascode_BW:1 | NM2:vgs | 440.4m | | | |
| Analog_Course:Cascode_BW:1 | NM2:vds | 442m | | | |
| Analog_Course:Cascode_BW:1 | NM2:vth | 295.8m | | | |
| Analog_Course:Cascode_BW:1 | NM2:vdsat | 160.2m | | | |
| Analog_Course:Cascode_BW:1 | NM2:gm | 196.5u | | | |
| Analog_Course:Cascode_BW:1 | NM2:gds | 4.303u | | | |
| Analog_Course:Cascode_BW:1 | NM2:gmb | 22.08u | | | |
| Analog_Course:Cascode_BW:1 | NM2:cdb | -699.9a | | | |
| Analog_Course:Cascode_BW:1 | NM2:cgd | -440.9a | | | |
| Analog_Course:Cascode_BW:1 | NM2:cgs | -5.632f | | | |
| Analog_Course:Cascode_BW:1 | NM2:csb | -1.378f | | | |
| Analog_Course:Cascode_BW:1 | NM2:region | 2 | | | |

Fig.4 OP parameters of 2nd CASCODE amplifier

Comment: as shown from above simulation results the MOSFETs of CS and CASCODE amplifier are been set at saturation region (region=2).

## 2. AC Analysis:

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| Analog_Course:Cascode_BW:1 | CS DC gain | 5.573 | | | |
| Analog_Course:Cascode_BW:1 | CS BW | 1.78M | | | |
| Analog_Course:Cascode_BW:1 | CS GBW | 9.944M | | | |
| Analog_Course:Cascode_BW:1 | CS UGF | 9.794M | | | |
| Analog_Course:Cascode_BW:1 | Cascode DC gain | 5.253 | | | |
| Analog_Course:Cascode_BW:1 | Cascode BW | 2.264M | | | |
| Analog_Course:Cascode_BW:1 | Cascode GBW | 11.92M | | | |
| Analog_Course:Cascode_BW:1 | Cascode UGF | 11.79M | | | |

Fig.5 AC simulation results of CS and CASCODE amplifiers

Comment: as shown from above results that the gain of CASCODE is the same gain of CS amplifier and this is due to the effect of RD value, but CASCODE in this case is very useful for bandwidth as shown in above figure.

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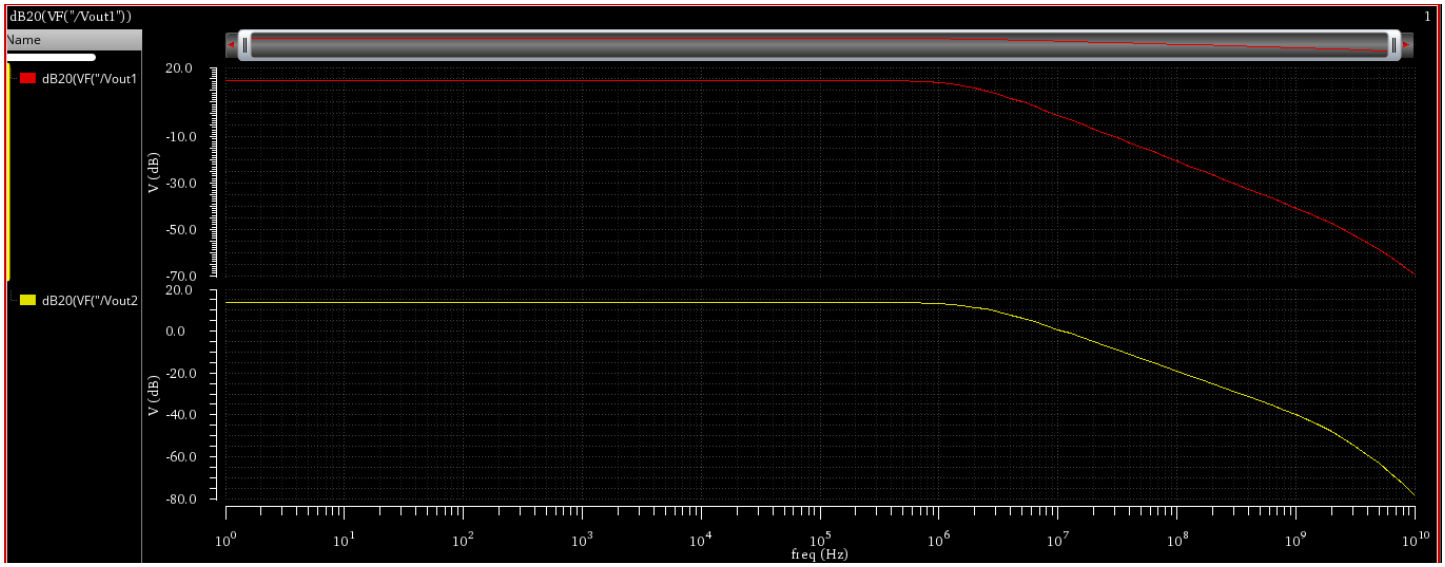


Fig.6 magnitude bode plot for CS and CASCODE amplifiers

# Lab 04

## Common Drain Frequency Response

## Part 1: Sizing Chart

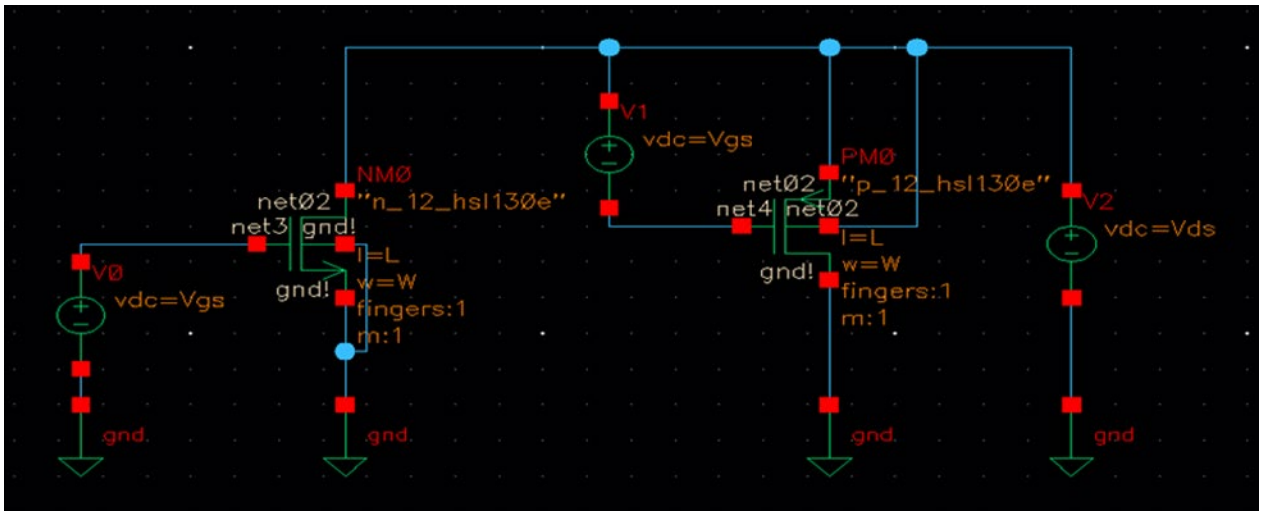


Fig.1 PMOS and NMOS circuit schematic for sizing

From simulations results we see that the value of PMOS threshold voltage: $V_{th} = -256.638mv$, so now set the value of VGS at $V_{GS} = -0.656638\ v$, and as we have $|V_Q^*| = 200mv$, so now from the following graph set $|V_{GSQ}| = 428.3391mv$ and $|V_{ovQ}| = 171.7014mv$.

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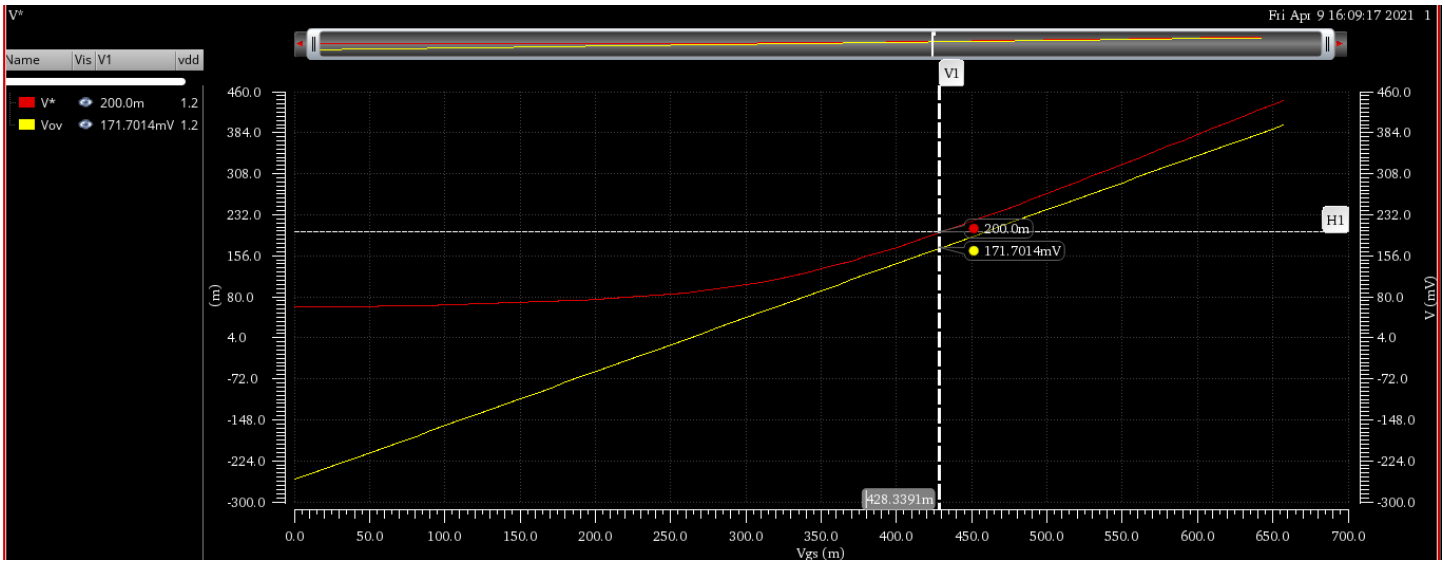


Fig.2 VGS and VOV results from simulation at V*=200mv

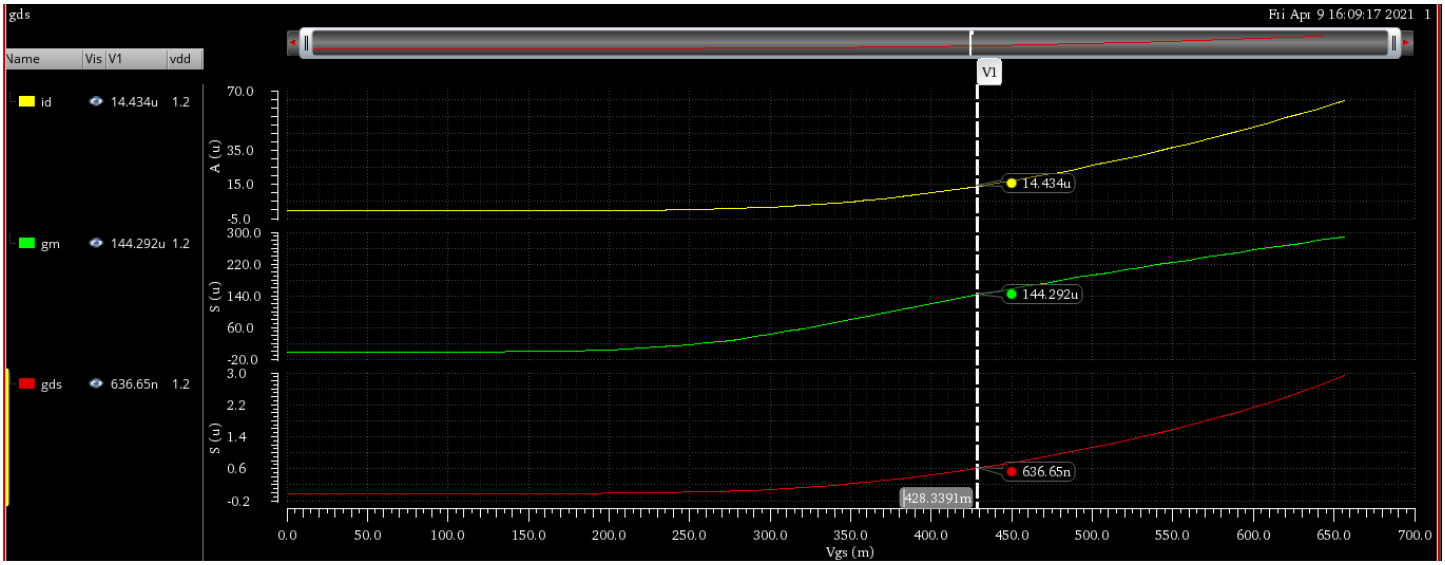


Fig.3 the actual values of ID, gm and gds at VGSQ

It's known that at constant $V_{ov} \rightarrow I_D \alpha W$ and we have assumed W=10um which gives $I_D = 14.434uA$, so by using cross multiplication at $I_D = 10uA \rightarrow W = 6.93um$.

And we have $g_m, g_{ds} \alpha \, {}^{1}/_{W}$, so using cross multiplication we get the values of gm and gds at W=6.93um which are $g_m = 100u \; and \; g_{ds} = 441.2n$.

# Part 2: CD Amplifier

## 1. OP (Operating Point) Analysis:

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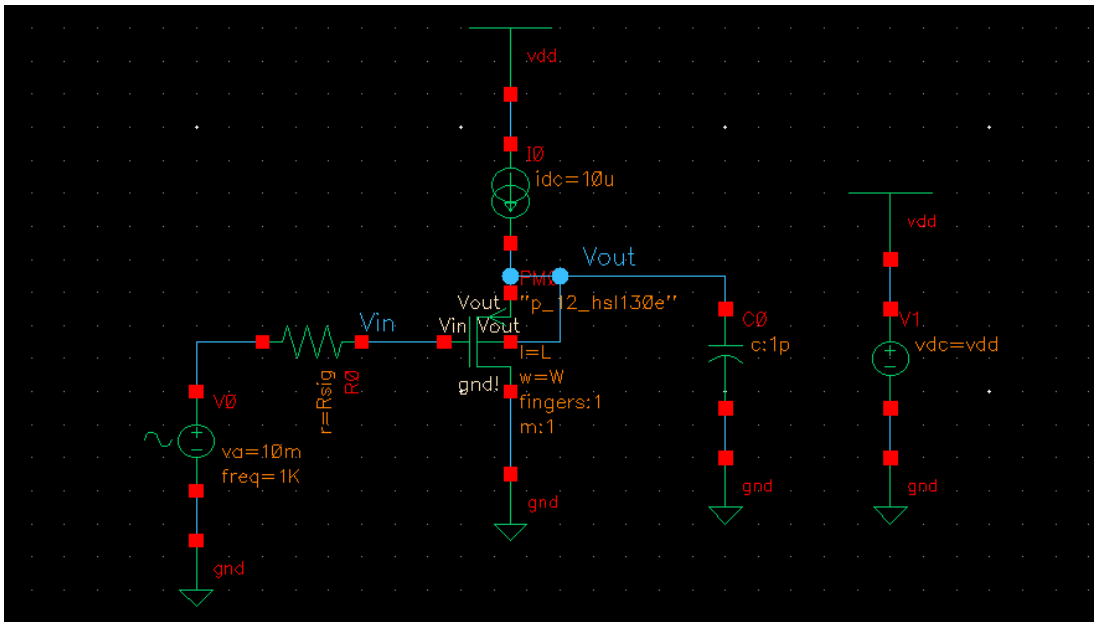


Fig.1 Common Drain Circuit schematic

| Test | Output | Nominal | Spec |
|---|---|---|---|
| | | | |
| Analog_IC_Design_Course:CD_Freq:1 | id | -10u | |
| Analog_IC_Design_Course:CD_Freq:1 | vgs | -427.5m | |
| Analog_IC_Design_Course:CD_Freq:1 | vds | -855.8m | |
| Analog_IC_Design_Course:CD_Freq:1 | vth | -256.6m | |
| Analog_IC_Design_Course:CD_Freq:1 | vdsat | -164.4m | |
| Analog_IC_Design_Course:CD_Freq:1 | gm | 100.3u | |
| Analog_IC_Design_Course:CD_Freq:1 | gds | 422.1n | |
| Analog_IC_Design_Course:CD_Freq:1 | gmb | 20.95u | |
| Analog_IC_Design_Course:CD_Freq:1 | cdb | -4.42f | |
| Analog_IC_Design_Course:CD_Freq:1 | cgd | -2.154f | |
| Analog_IC_Design_Course:CD_Freq:1 | cgs | -52.57f | |
| Analog_IC_Design_Course:CD_Freq:1 | csb | -15.01f | |
| Analog_IC_Design_Course:CD_Freq:1 | region | 2 | |

Fig.2 OP parameters of CD amplifier

Comment: as shown in above figure that common drain in region 2 which mean that it's in saturation case.

## 2. AC Analysis:

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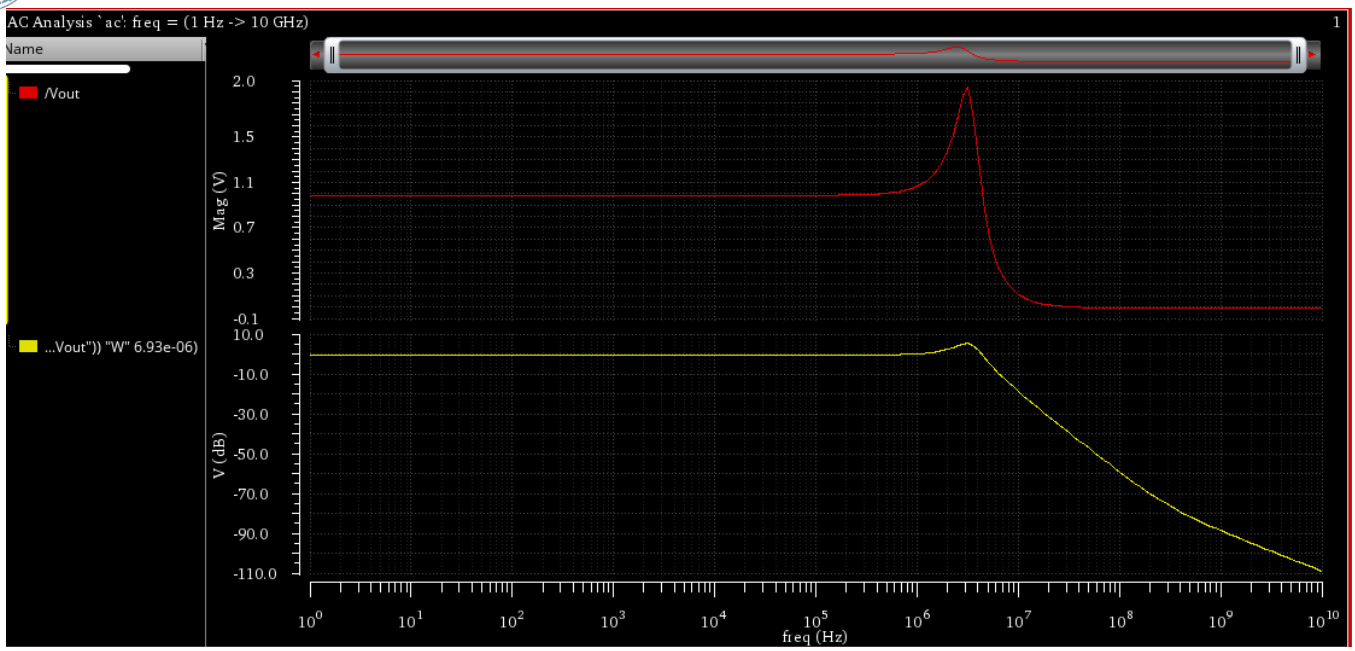


Fig.3 bode plot magnitude of VOUT at CD amplifier

Comment: as shown on above figure that there is a peaking in frequency domain in case of CD amplifier, so the value of maximum gain in this case will be: $A_v = 5.798$.

Analytical solution for quality factor Q for CD amplifier: as we know that we can't use miller approximations and OCTC techniques because it doesn't give dominant and non-dominant poles but only give us all poles at high frequency so we us exact solution in this case with some special cases that as we use IDC so $R_s$ will be very high and can be neglected and as we use PMOS so there is no body effect and can neglect CLM also.

Now we have $b_1 = \left(\frac{(c_{gs}+c_{gd})c_{L+c_{gs}c_{gd}}}{g_m}\right)R_{sig} = 2.18f, b_2 = c_{gd}R_{sig} + \frac{c_{gs}+c_L}{g_m} = 24.77n$ *and* $Q = \frac{\sqrt{b_1}}{b_2} = 1.88$, so from previous analysis we have $Q > 0.5$ which mean underdamped case which cause peaking in frequency domain and ringing in time domain.

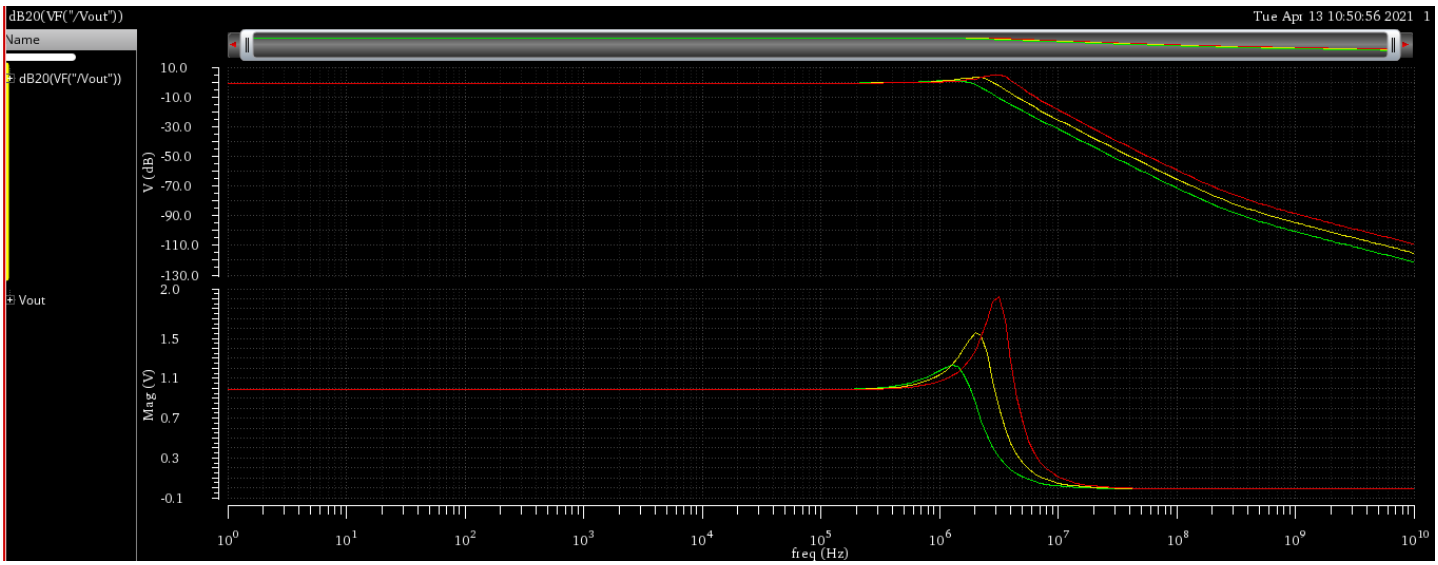

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Fig.2 bode plot magnitude after sweep of CL

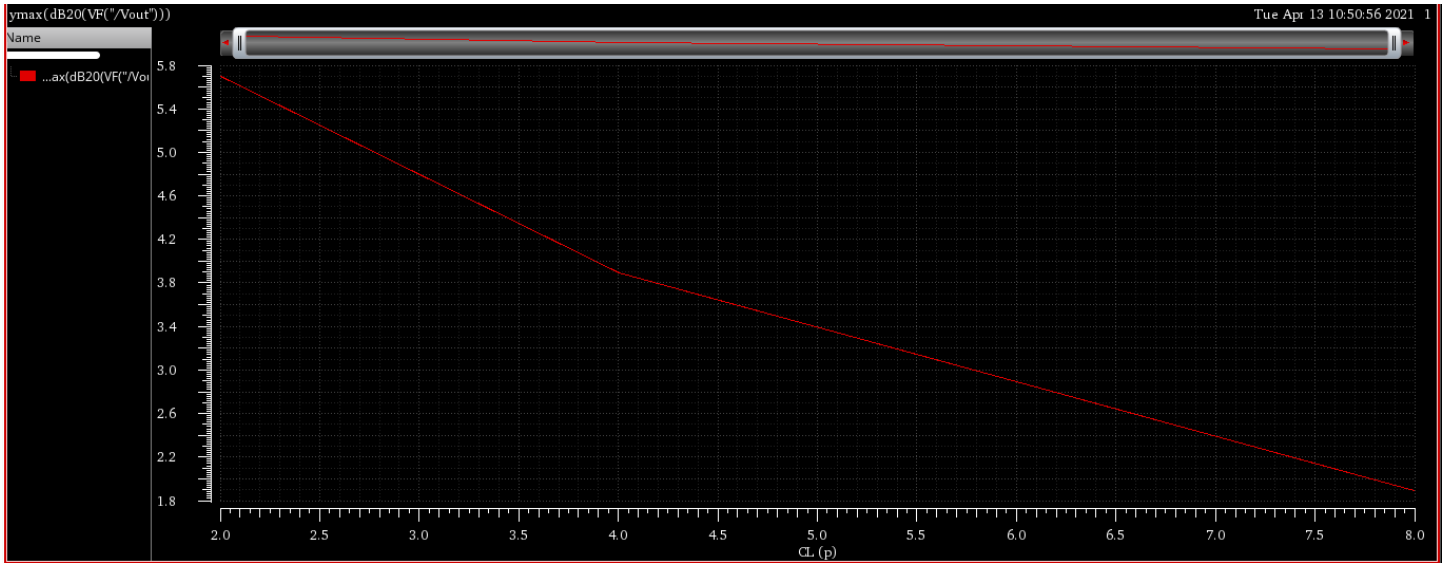


Fig.3 peaking versus CL sweep

Comment: as shown from previous simulation results that as the load capacitance increases the peaking value decreases as the quality factor is inverse proportional to load capacitance.

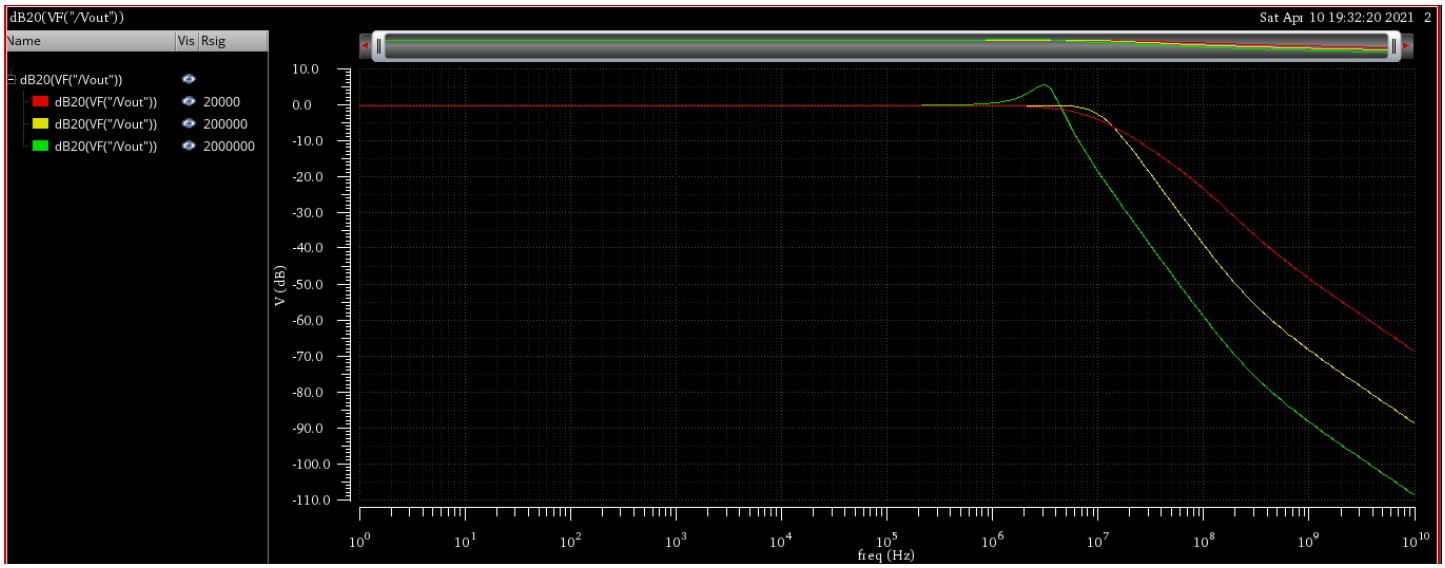


Fig.4 bode plot magnitude after sweep of RSIG

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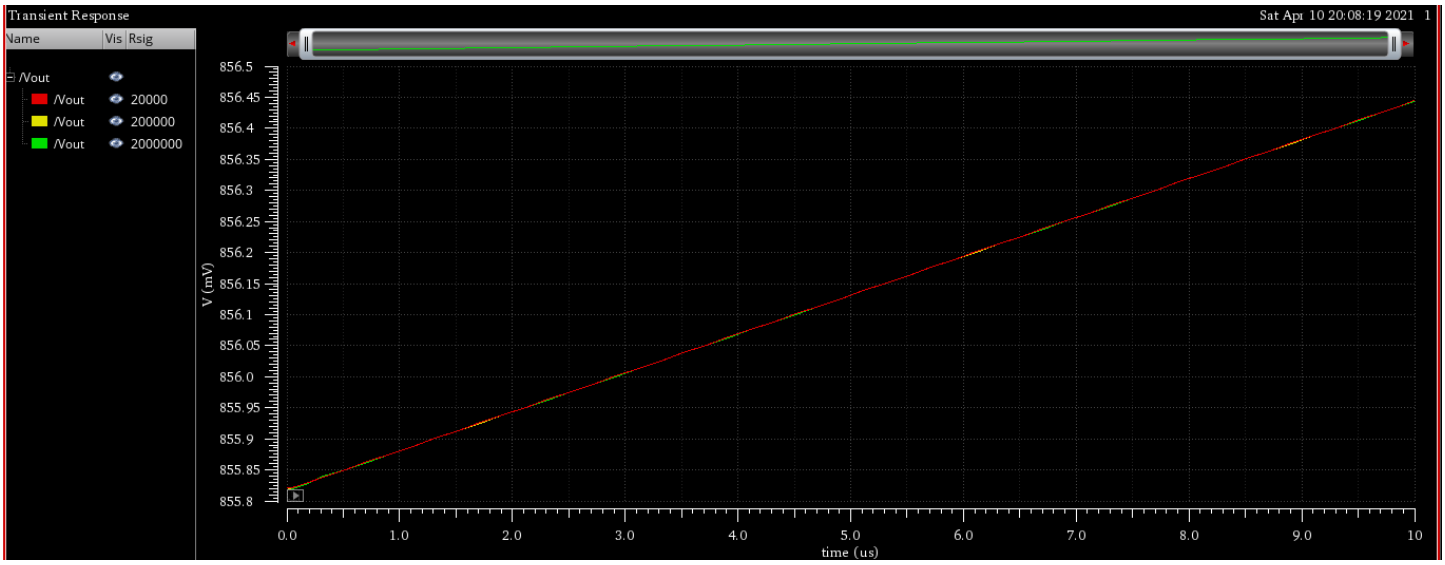


Fig.5 peaking versus RSIG sweep

Comment: from previous figure as it shown that as we increase RSIG the value of peaking increase as the quality factor Q is directly proportional with RSIG.

## 3. Transient Analysis:

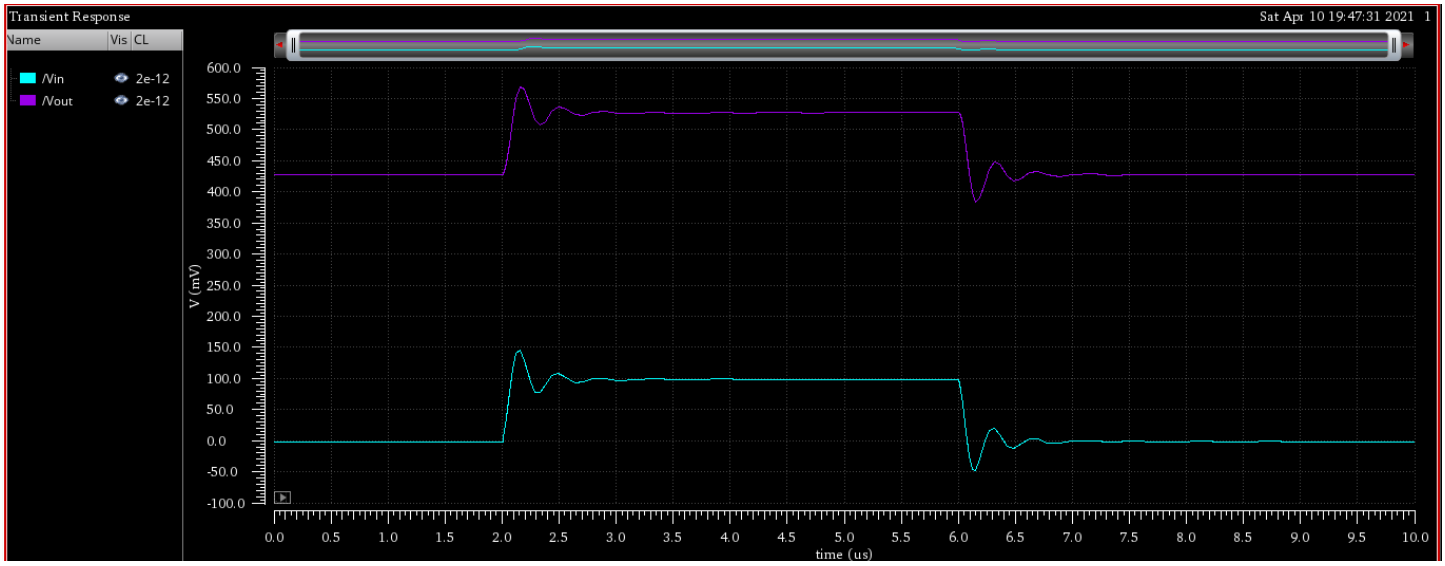


Fig.6 VIN & VOUT versus time at transient analysis

DC shift between input signal and output signal is equal to VGS which is equal: $DC\ shift = VGS = 428.3391mV$, and the output signal is shifted up as we use PMOS if we want to shift output signal down we can use NMOS CD amplifier.

It's clear the effect of ringing on input and output signals and using cadence calculator, we evaluate the value of overshoot in percentage which will be 41.2%.

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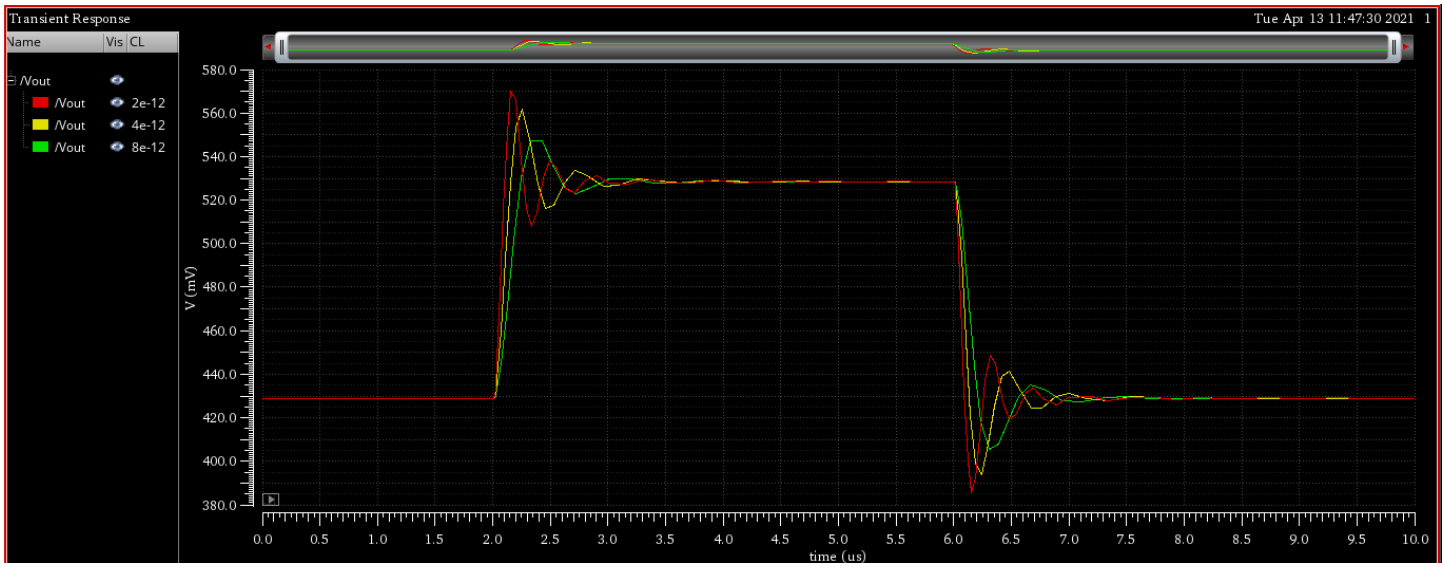


Fig.7 VOUT transient analysis versus sweep pf CL

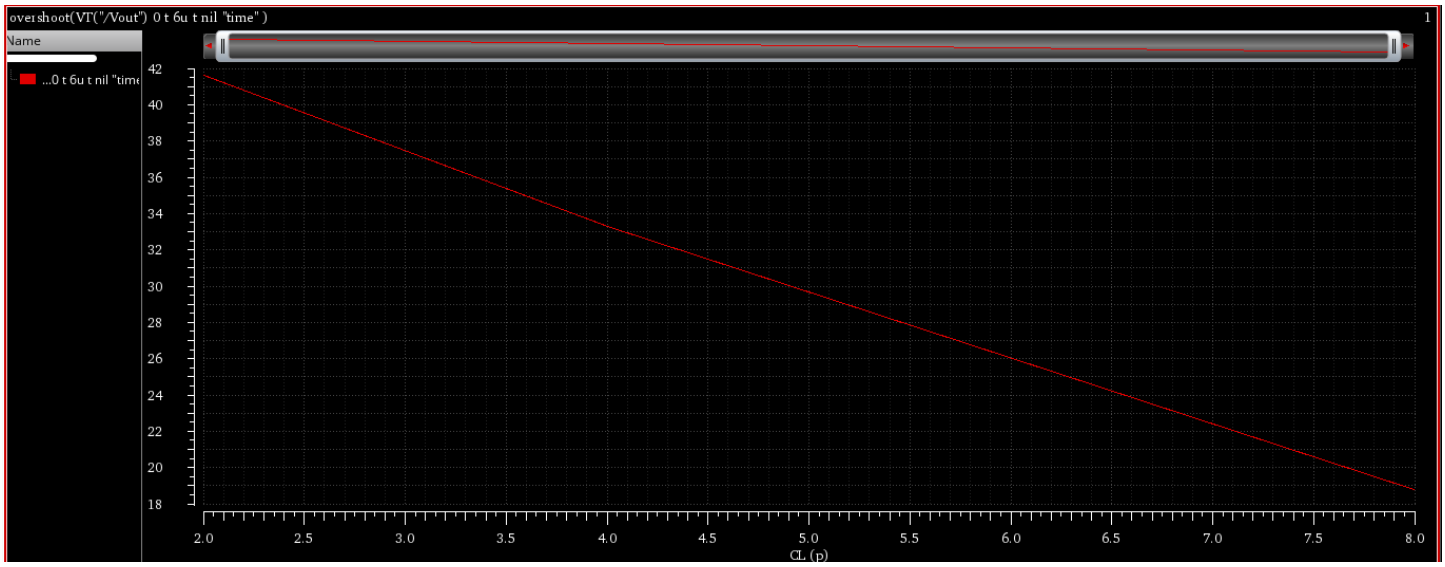


Fig.8 overshoot versus CL

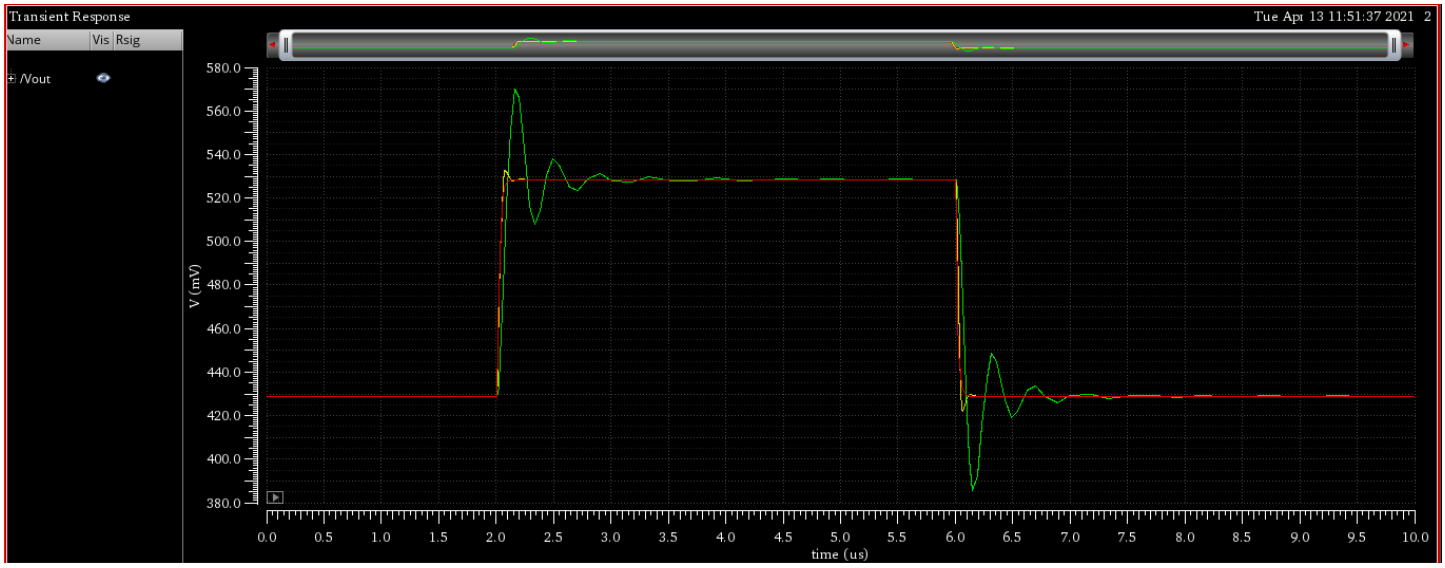


Fig.9 VOUT transient analysis versus sweep of RSIG

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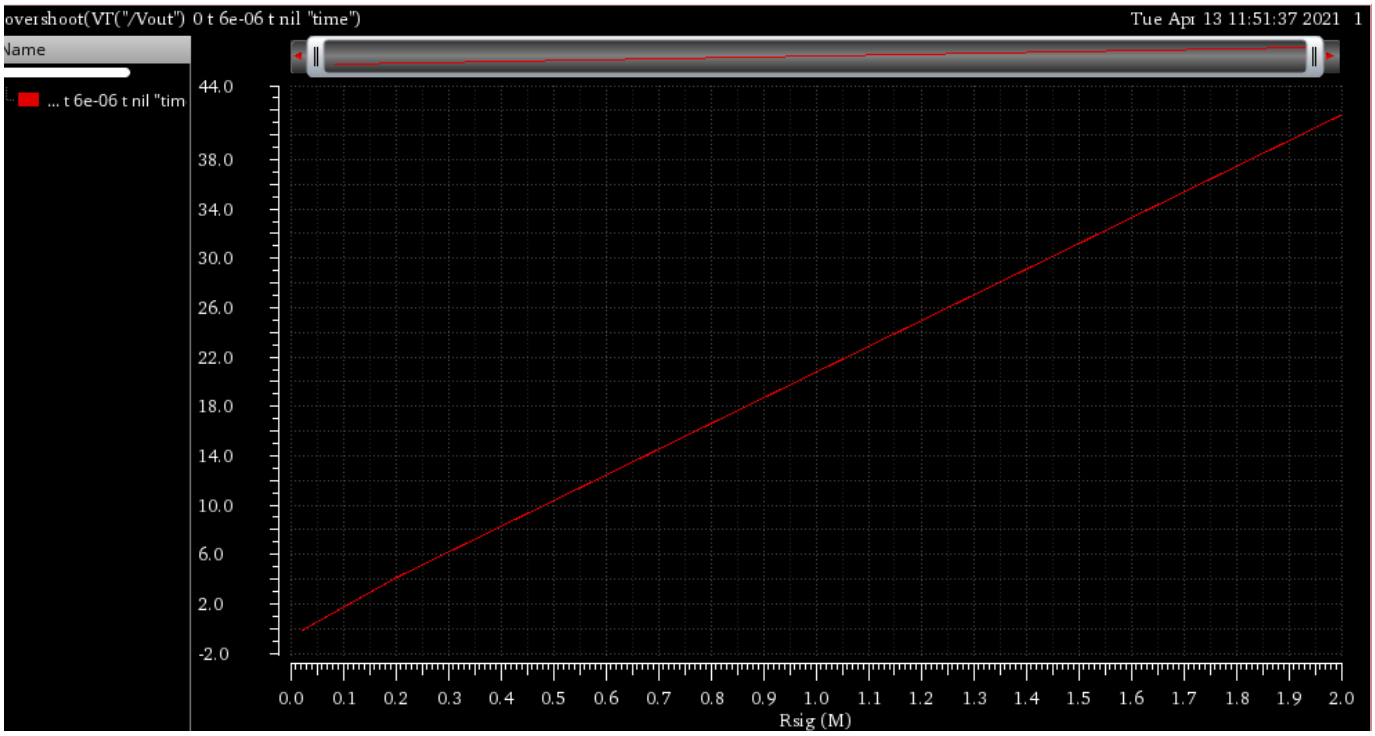


Fig.10 overshoot versus sweep of RSIG

# Lab 05

## Simple VS Low Compliance Cascode Current Mirror

## Part 1: Sizing Chart

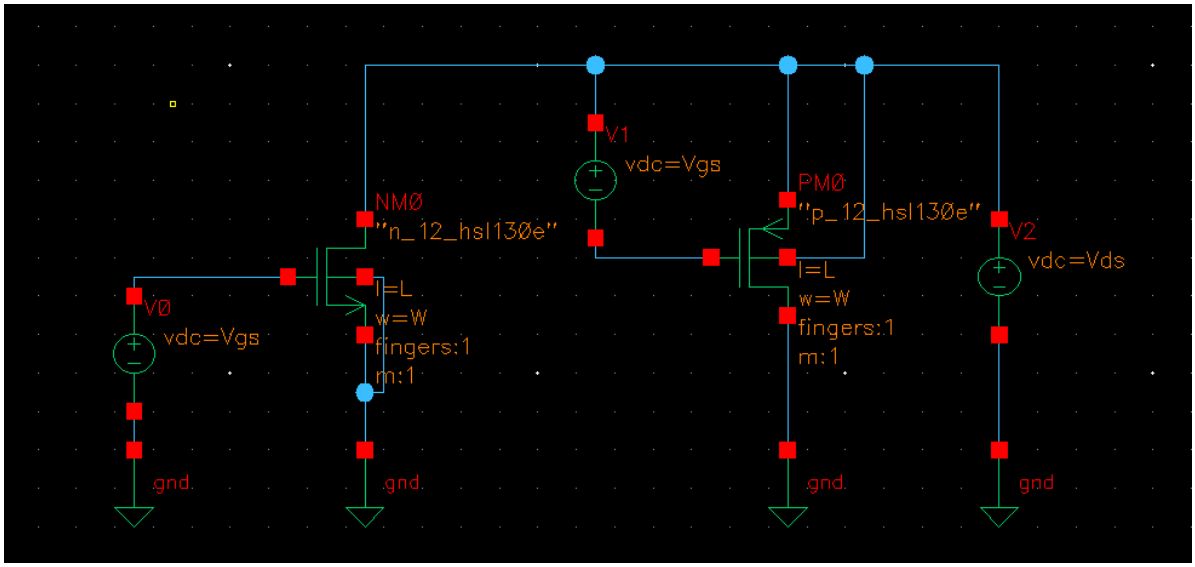


Fig.1 PMOS and NMOS circuit schematic for sizing

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We have set the real MOSFET overdrive voltage as following: $V^* = 200mV$.

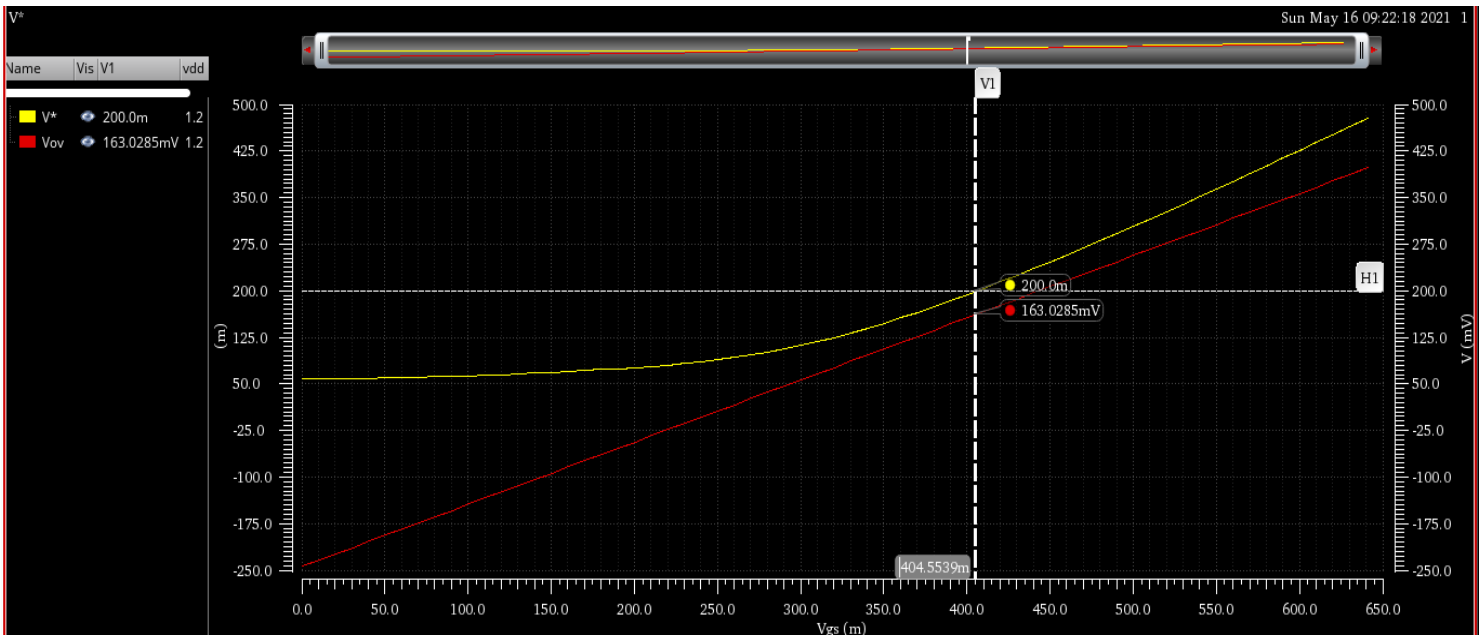


Fig.2 VGS and VOV results from simulation at V*=200mv

So as the previous figure we get the following: $V_{gsQ} = 404.5539mV, V_{ovQ} = 163.0285mV$.

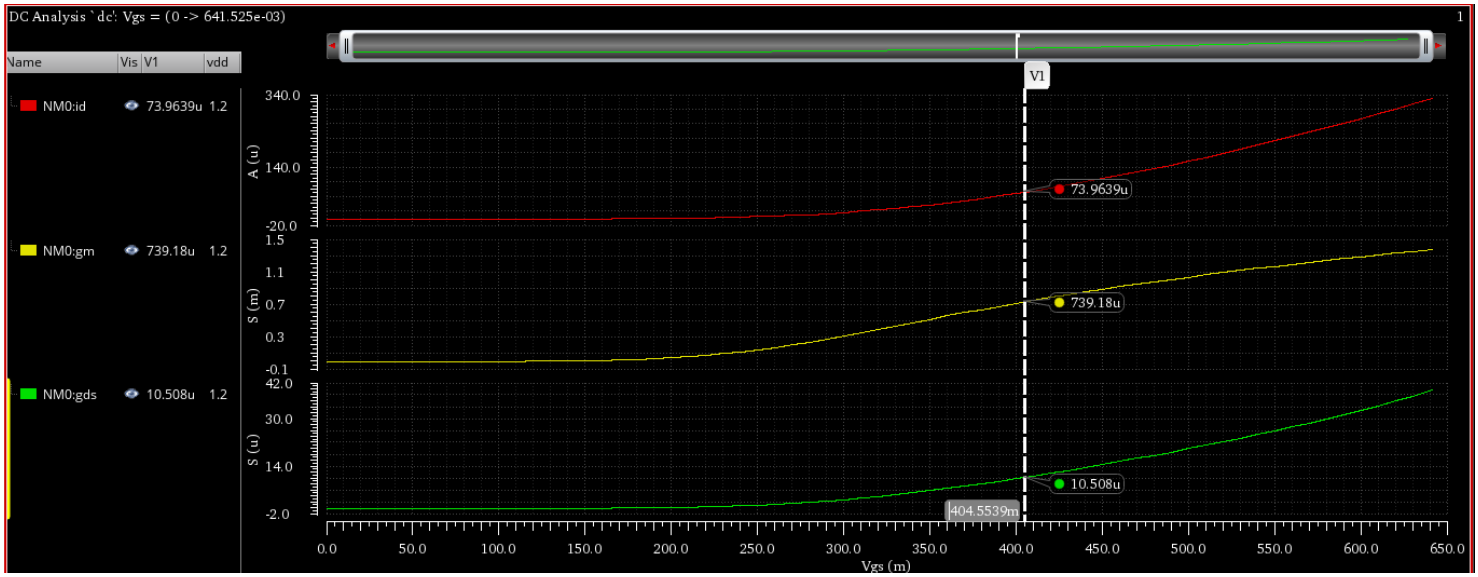


Fig.3 the actual values of ID, gm and gds at VGSQ

So we get now the actual value of drain current at assumed width (W=10um) which will be ID=73.9639uA and as the current is always proportional to width of MOSFET so we can get the actual width at ID=20uA which will be W=2.7um.

# Part 2: Current Mirror

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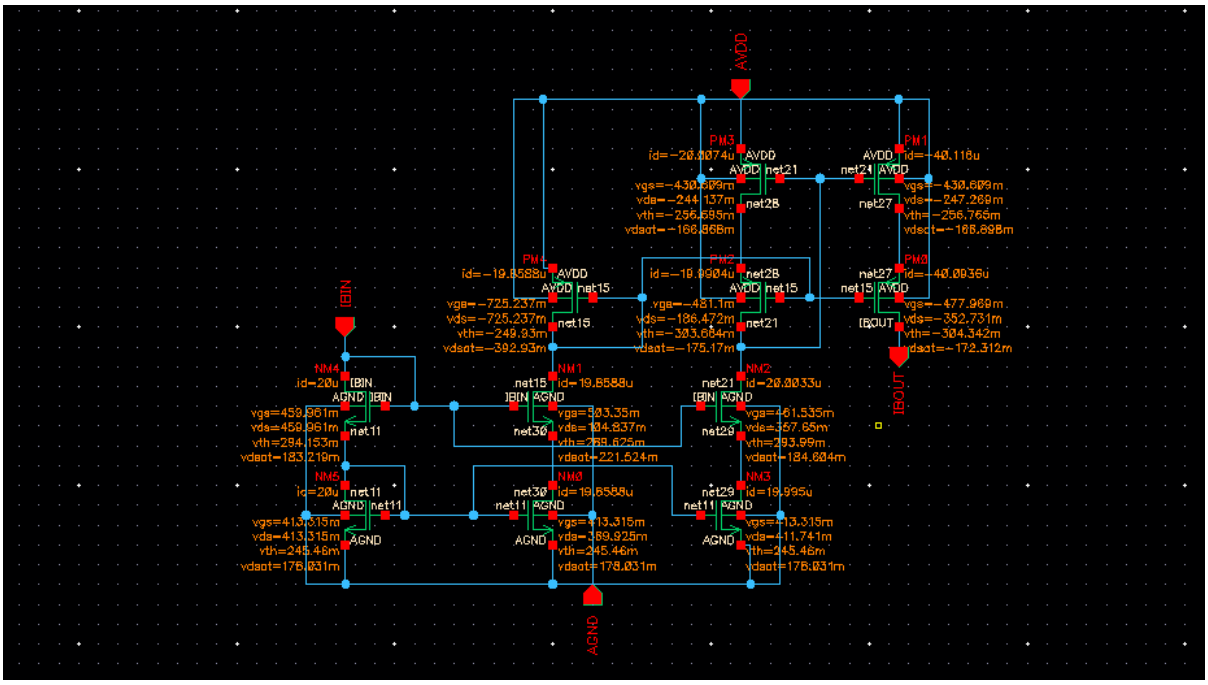


Fig.1 wide sense current mirror circuit schematic

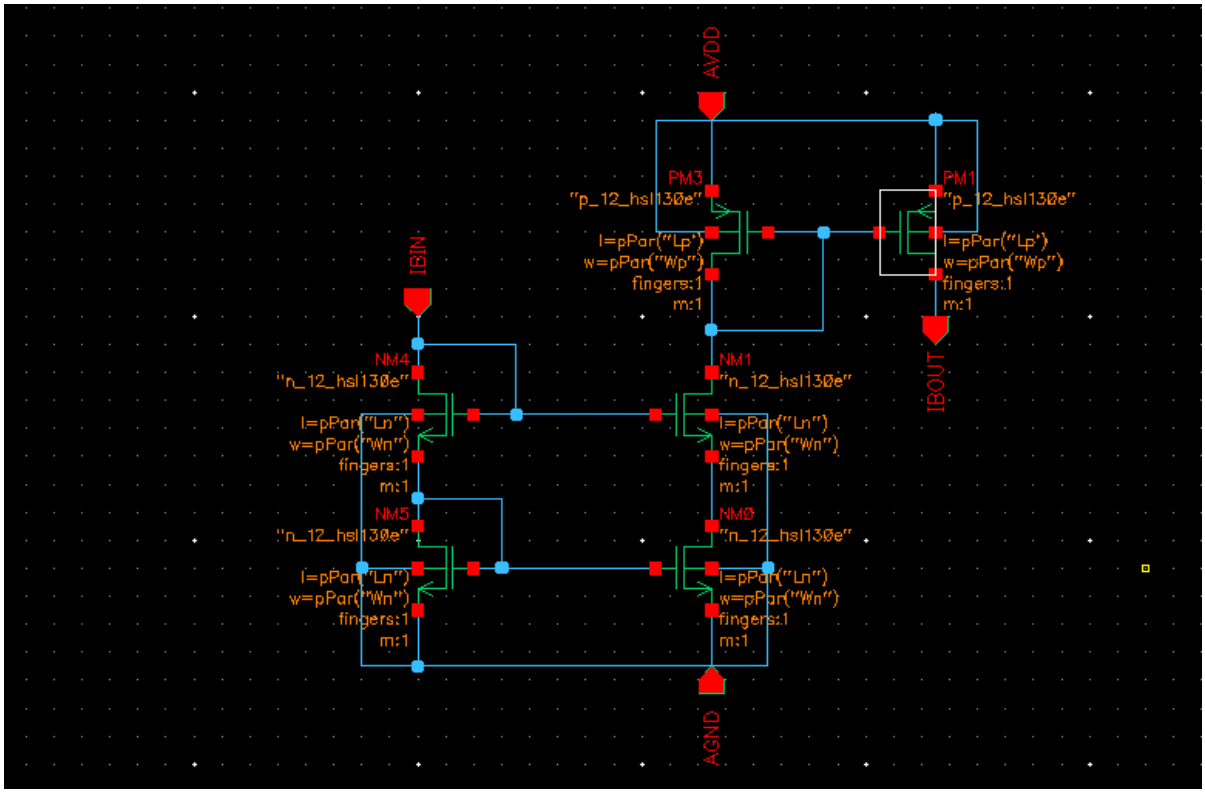


Fig.2 simple current mirror circuit schematic

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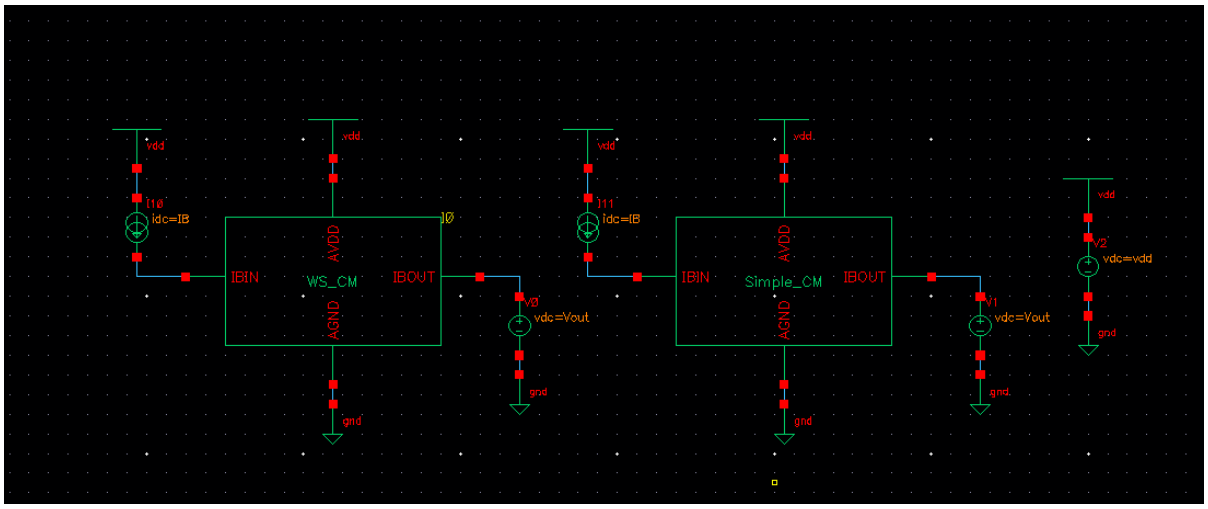


Fig.3 testbench for CMs circuit schematic

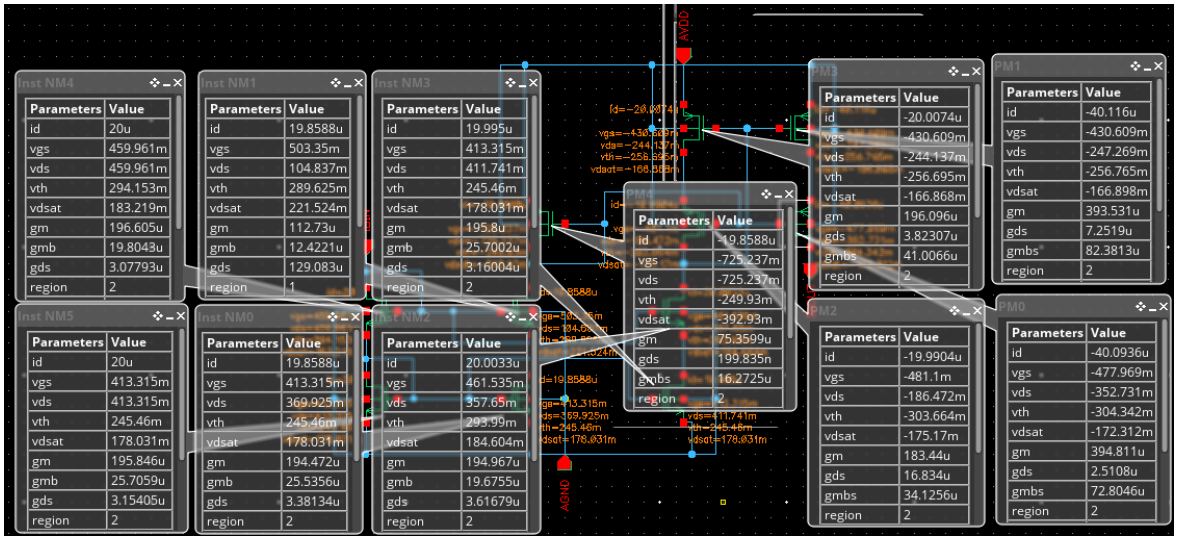


Fig.4 operating point parameters of WS CM MOSFETs

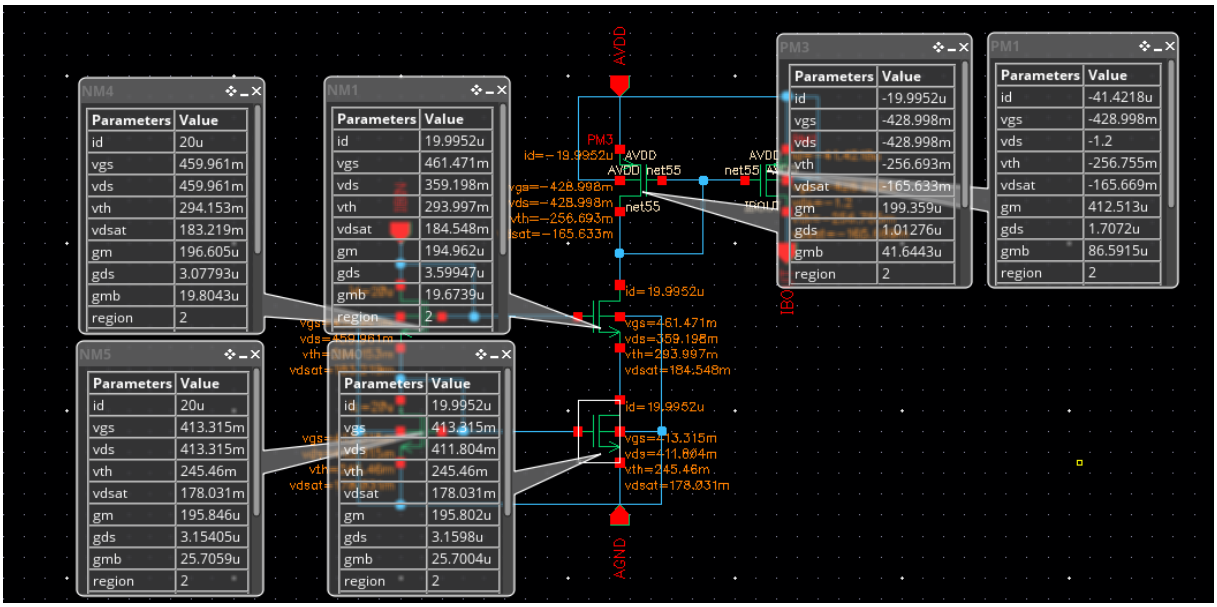

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Fig.5 operating point parameters of simple CM MOSFETs

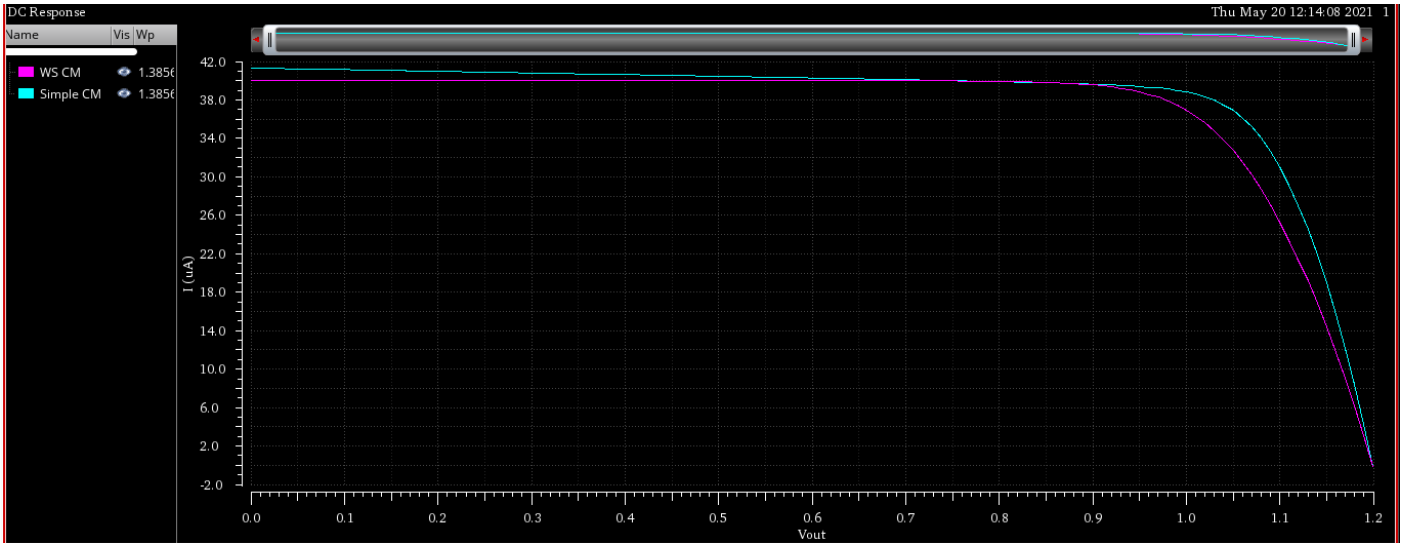


Fig.6 IB out versus VOUT from two CMs

Comment: the difference between two CMs that simple cascode CM wastes the headroom of supply voltage due to extra VTH in the 2nd MOSFET but at wide sense CM there is no wasting of supply voltage as diode connected over two MOSFETs.

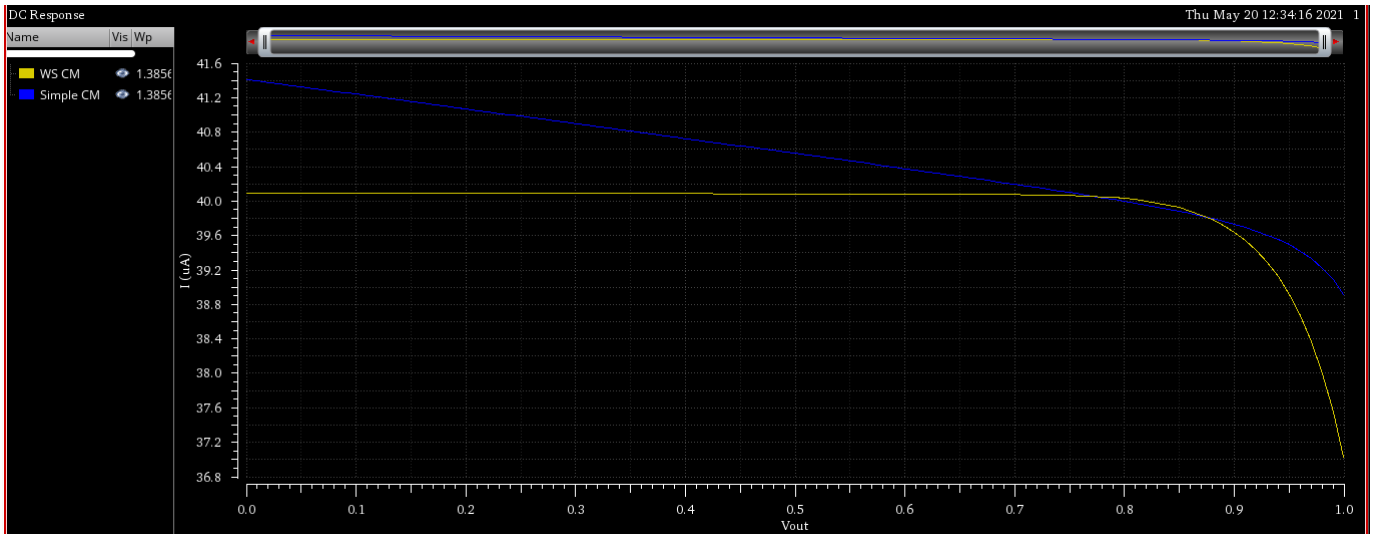


Fig.7 IB out versus VOUT at 1 volt for two CMs

Comment: from the shown figure error percentage of WS CM will be 7.4%, and error percentage of simple CM will be 3.33%.

So simple cascode CM is more accurate but it wastes a lot from supply voltage.

| Test | Output | Nominal | Spec |
|---|---|---|---|
| | | | |
| Analog_IC_Design_Course:lab_05_cm_tb:1 | WS | | |
| Analog_IC_Design_Course:lab_05_cm_tb:1 | Simple | | |
| Analog_IC_Design_Course:lab_05_cm_tb:1 | Simple CM | 97.33 | |
| Analog_IC_Design_Course:lab_05_cm_tb:1 | WS CM | 92.68 | |

Fig.8 error results of two CMs from ADL simulation

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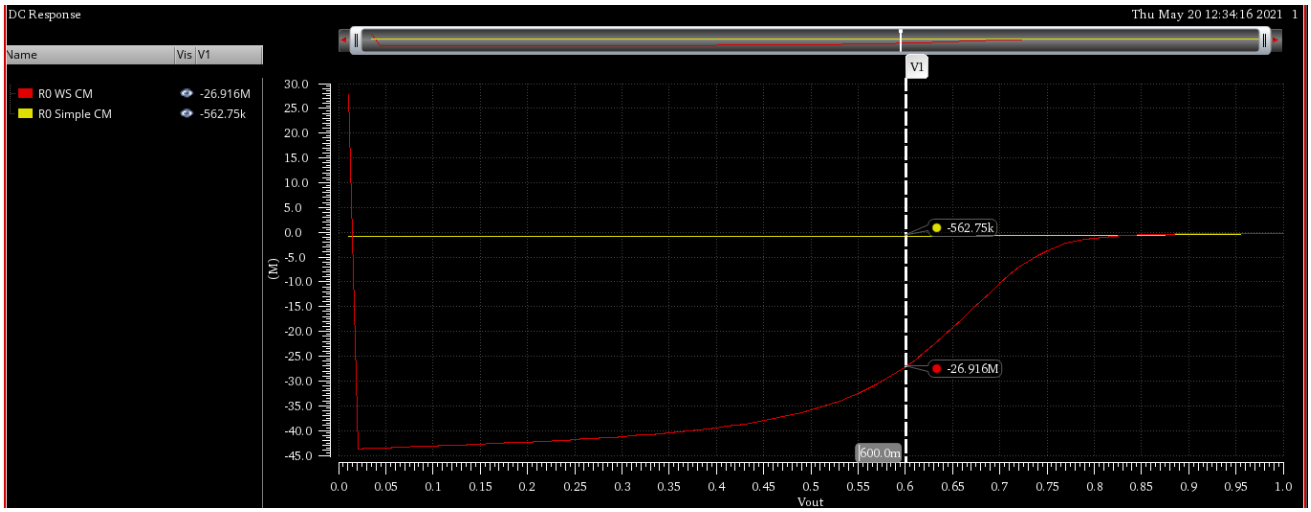


Fig.9 Rout versus VOUT of two CMs

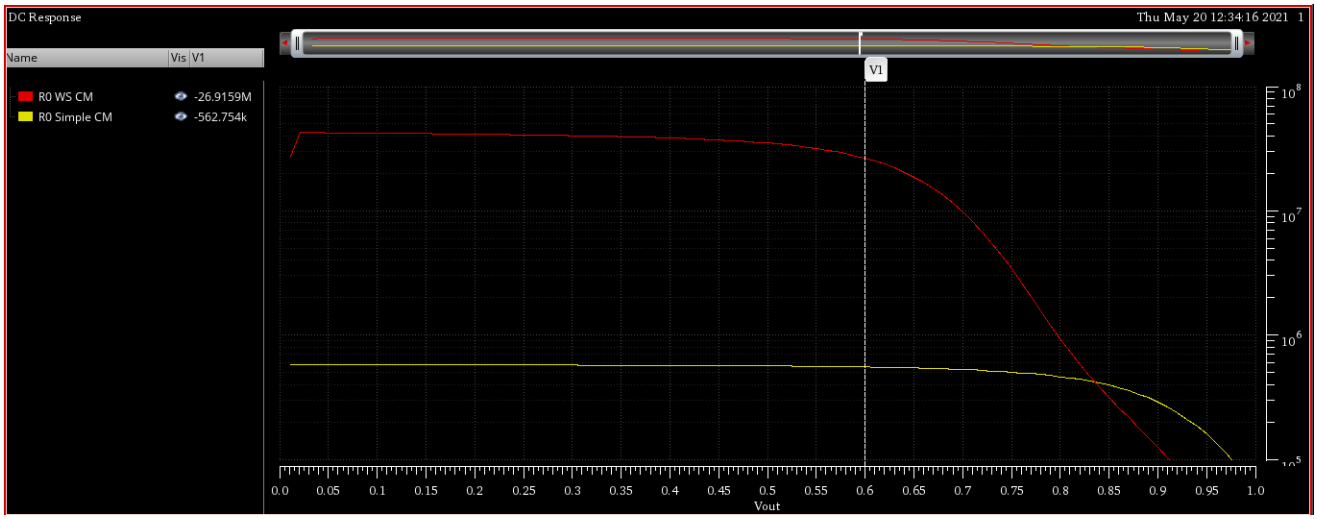


Fig.10 Rout versus VOUT of two CMs log scale