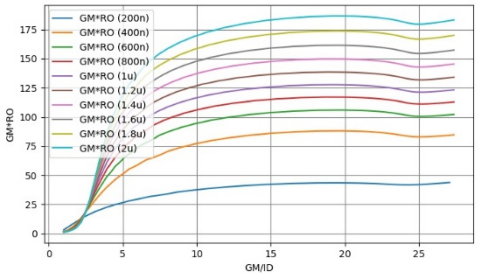
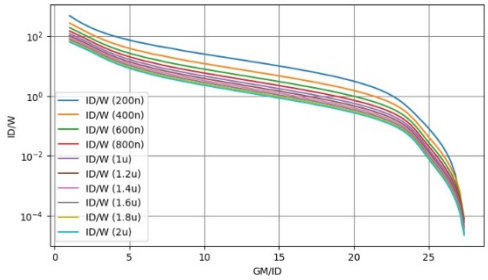
# Lab 11 (Mini-Project 02)

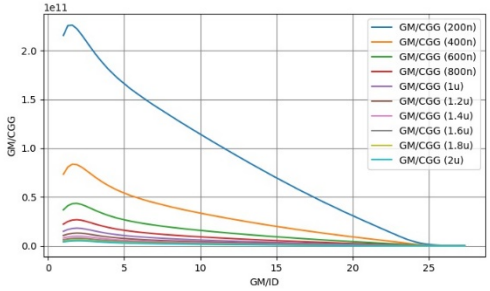
## Fully-Differential Folded Cascode OTA

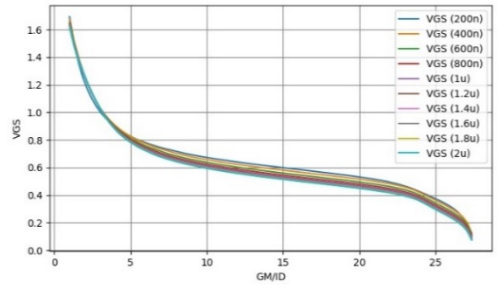
## Part 1: gm/ID Design Charts

- NMOS Design Charts from ADT:

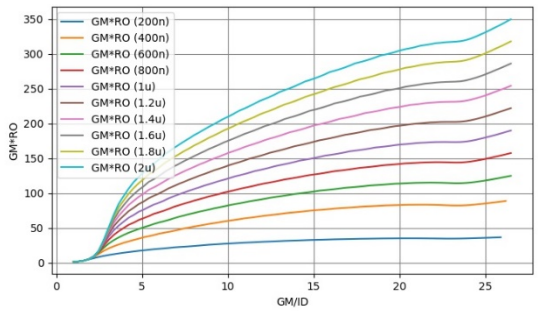


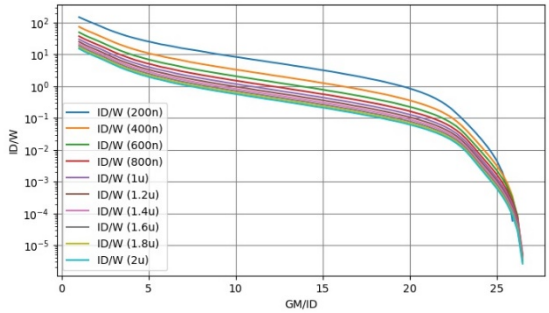



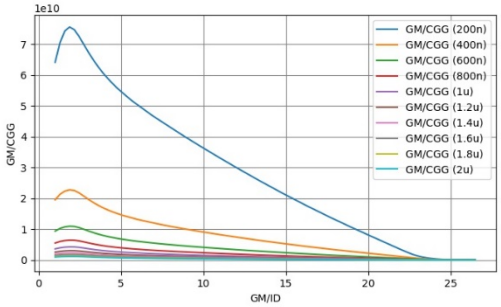



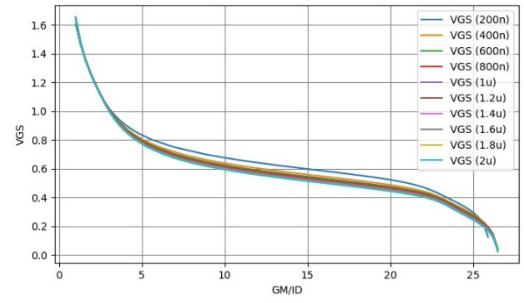




- PMOS Design Charts from ADT:



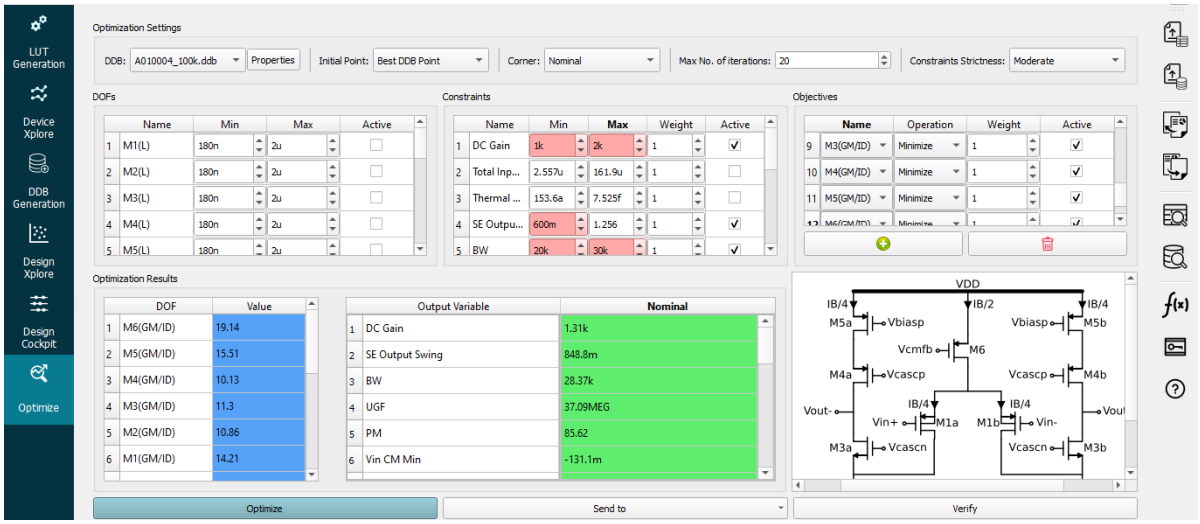



# Part 2: OTA Design

- **Topology Selection:**
  Input Pair | Tail Current Source → PMOS, because of CM input range which is 0-1.1 near to GND rail.
- **Sizing using ADT:**
  Used optimize bottom in ADT to get initial design points for lengths and gm/id for different MOSFETs in folded cascode OTA and get the following results.




ADT interface for sizing using optimize bottom

| | | | |
|---|---|---|---|
| M1(L) | 1.011u | M1(W) | 34.26u |
| M2(L) | 259.2n | M2(W) | 2.31u |
| M3(L) | 385.2n | M3(W) | 1.747u |
| M4(L) | 417.4n | M4(W) | 5.77u |
| M5(L) | 1.013u | M5(W) | 46.29u |
| M6(L) | 692.1n | M6(W) | 141.5u |

initial sizing results for MOSFETs of folded cascode OTA

| | | | |
|---|---|---|---|
| M1(GM/ID) | 14.21 | DC Gain | 1.31k |
| M2(GM/ID) | 10.86 | Total Input Integrated Noise (Vrms) | 46.79u |
| M3(GM/ID) | 11.3 | Thermal Input Noise Density (V^2/Hz) | 431.2a |
| M4(GM/ID) | 10.13 | SE Output Swing | 848.6m |
| M5(GM/ID) | 16.51 | BW | 28.37k |
| M6(GM/ID) | 19.14 | UGF | 37.09MEG |
| M2(VDsat_margin) | 82.23m | PM | 85.62 |
| M5(VDsat_margin) | 149.3m | Vin CM Min | -131.1m |
| IB_Nominal | 70.74u | Vin CM Max | 1.117 |
| | | ΣW*L | 268.4p |

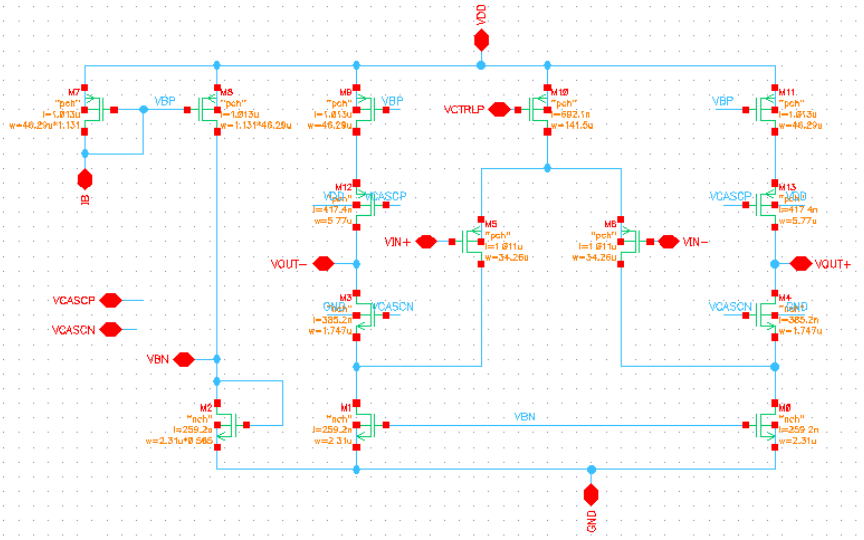
gm/id and current consumption results with achieved specs from ADT

| | |
|---|---|
| VBN | 657.1m |
| VBP | 522.2m |
| VCASCN | 971.7m |
| VCASCP | 993.6m |
| VCMFB | 482.8m |

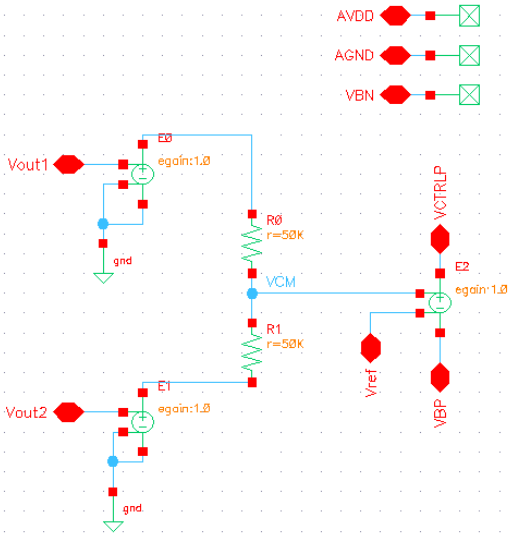
biasing for cascode MOSFETs and current mirrors

- **Simulation and Sizing using Cadence:**

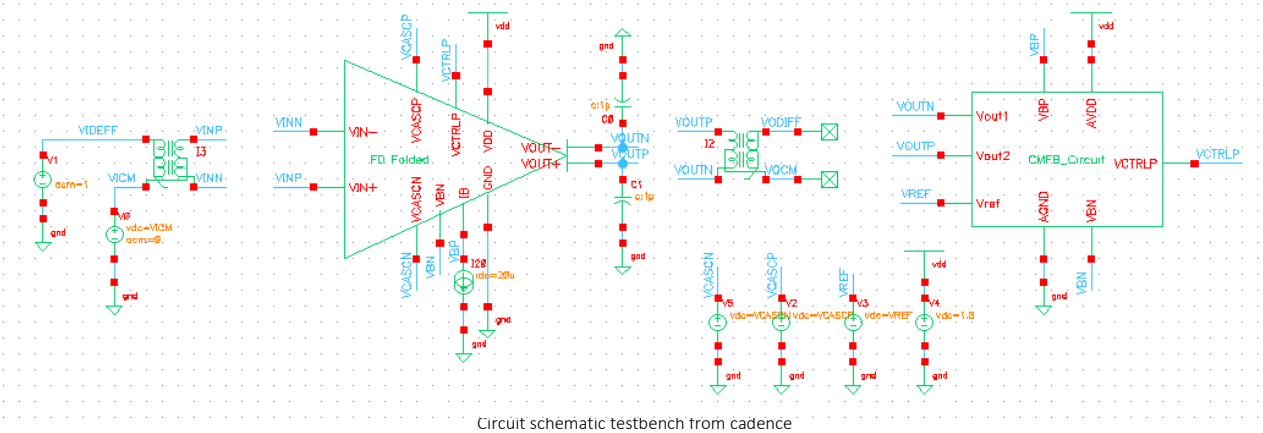
  Set the current mirror branch to have the same gm/id and same length by adjusting width of each MOSFET and from current consumption $I_B = 70.74uA$, which will be divided equally on each branch of CG and CS branches.




Circuit schematic for folded cascode from cadence with sizing




Circuit schematic for behavioural model




Circuit schematic testbench from cadence

Set Vicm=0.55, and set VREF=1.1 to maximize output signal swing.

- **Specs Verification and Tuning by Cadence:**

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| TrainLAB:Lab11_TB:1 | Av Mag | 784.5 | | | |
| TrainLAB:Lab11_TB:1 | Av dB | 57.89 | | | |
| TrainLAB:Lab11_TB:1 | BW | 45.67k | | | |
| TrainLAB:Lab11_TB:1 | GBW | 35.91M | | | |
| TrainLAB:Lab11_TB:1 | UGF | 36.24M | | | |
| TrainLAB:Lab11_TB:1 | PM | 85.97 | | | |

AC simulation results for folded cascode from ADXL

As shown from previous results that all specs have been achieved except DC gain spec, so the selection for tuning to increase width of cascode MOSFETs “M3 | M4” which will increase gm of NMOS and PMOS cascode and also will decrease Vdsat of each MOSFET which give a good output signal swing, this may affect on bandwidth of OTA but we have margin in bandwidth which be accepted tune.

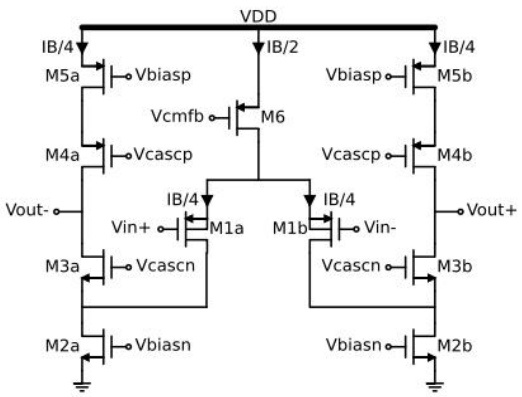
| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| TrainLAB:Lab11_TB:1 | Av Mag | 1.401k | | | |
| TrainLAB:Lab11_TB:1 | Av dB | 62.93 | | | |
| TrainLAB:Lab11_TB:1 | BW | 25.83k | | | |
| TrainLAB:Lab11_TB:1 | GBW | 36.28M | | | |
| TrainLAB:Lab11_TB:1 | UGF | 36.65M | | | |
| TrainLAB:Lab11_TB:1 | PM | 86.33 | | | |

Achived specs results after tuning

From previous results it’s clear that all specs have been achieved by increasing width of M3 and M4 by factor of two.

- **Sizing Summary:**

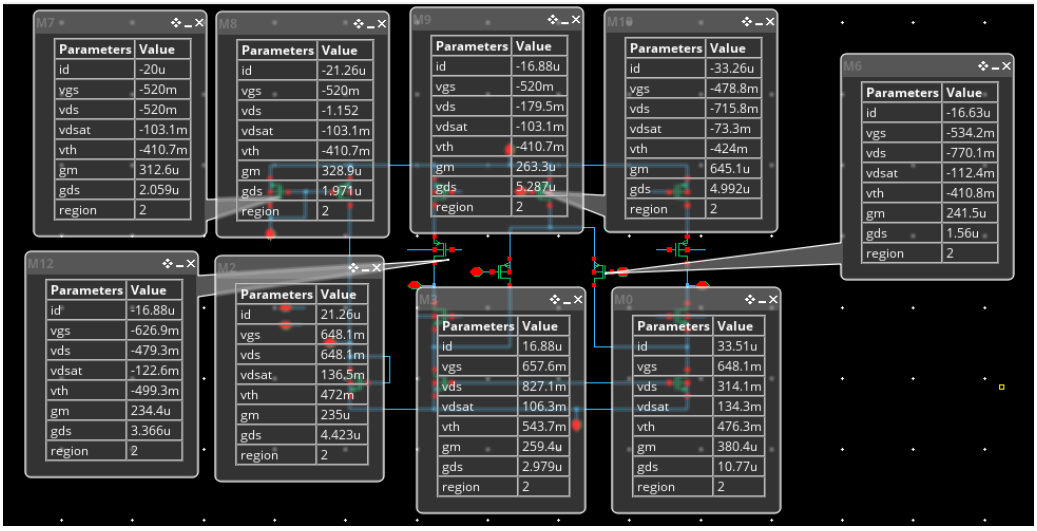
| | Length | Width | Current ID | Gm | Gm/ID |
|---|---|---|---|---|---|
| Input Pair M1 | 1.011um | 34.26u | 17.685uA | 251.304uS | 14.21 |
| Folded NMOS Current Mirror M2 | 259.2nm | 2.31um | 35.37uA | 384.1182uS | 10.86 |
| Cascode NMOS M3 | 385.2nm | 1.747um*2 | 17.685uA | 199.8405uS*2 | 11.3*2 |
| Cascode PMOS M4 | 417.4nm | 5.77um*2 | 17.685uA | 182.155uS*2 | 10.13*2 |
| PMOS Current Mirror in CG Branch M5 | 1.013um | 46.29um | 17.685uA | 291.98uS | 16.51 |
| Tail Current Source ISS PMOS M6 | 692.1nm | 141.5um | 35.37uA | 676.98uS | 19.14 |
| NMOS Mirror | 259.2nm | 2.31um*0.5655 | 20uA | 217.2uS | 10.86 |
| PMOS Source Mirror | 1.013um | 46.29um*1.131 | 20uA | 330.2uS | 16.51 |




Folded cascode circuit from ADT

# PART 3: Open-Loop OTA Simulation (Behavioural CMFB)

1) Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.



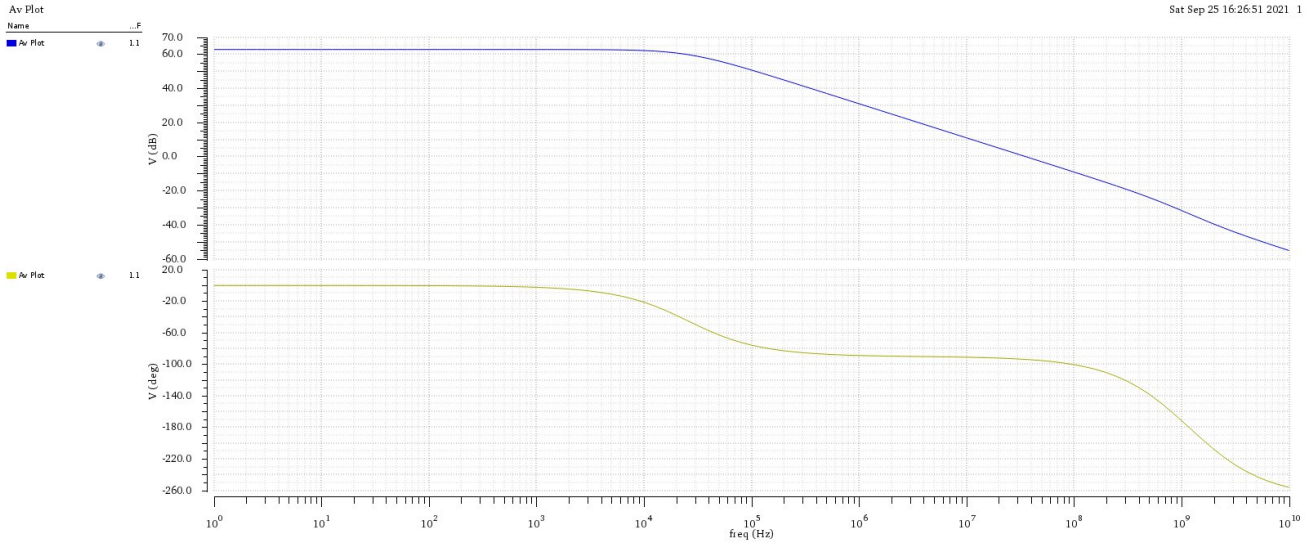

DC operating points results from DC simulation

- What is the CM level at the OTA output?
  The CM level at OTA output equals VREF value which used in comparison in CMFB circuit = 1.1V.

- What are the differential input and output voltages of the error amplifier? What is the relation between them?
  Differential input voltage is the error voltage between common mode voltage and VREF “desired CM voltage”, and differential output is the bias voltage to tail current source to set CM DC voltage, and the relation between them is the gain of error amplifier.

2) Diff small signal ccs:

- Plot diff gain (magnitude in dB and phase) vs frequency.




Bode plot for differential output results from AC analysis

- Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| TrainLAB:Lab11_TB:1 | Av Plot | | | | |
| TrainLAB:Lab11_TB:1 | Av Plot | | | | |
| TrainLAB:Lab11_TB:1 | Av Mag | 1.401k | | | |
| TrainLAB:Lab11_TB:1 | Av dB | 62.93 | | | |
| TrainLAB:Lab11_TB:1 | BW | 25.83k | | | |
| TrainLAB:Lab11_TB:1 | GBW | 36.28M | | | |
| TrainLAB:Lab11_TB:1 | UGF | 36.65M | | | |
| TrainLAB:Lab11_TB:1 | PM | 86.33 | | | |

AC analysis results from ADEXL

- Compare simulation results with hand calculations in a table (use SS parameters from OP simulation in your hand analysis).

| Circuit Parameter | Hand Analysis Results | Simulation Results |
|---|---|---|
| DC Gain MAG | 1.112k | 1.401k |
| DC Gain dB | 60.92 dB | 62.93 dB |
| Bandwidth | 34.56 kHz | 25.83 kHz |
| GBW | 38.44 MHz | 36.28 MHz |
| UGF | 38.44 MHz | 36.65 MHz |

# PART 4: Open-Loop OTA Simulation (Actual CMFB)

- **Sizing Actual CMFB Circuit:**
  1) 1st design decision is dividing current on four branches equally.
  2) And we have lengths and widths for current mirrors which are biased by VBN and VBP, also we have length and width of current mirror load which is biased by VCTRLP, so only we have to adjust width ratio of these MOSFETs to be scaled with current.
  3) The remaining MOSFETs CD PMOS, and input pair of error amplifier NMOS, assume L=1um, gm/ID=15 and ID=10uA so using ADT we can get a good estimation for width.

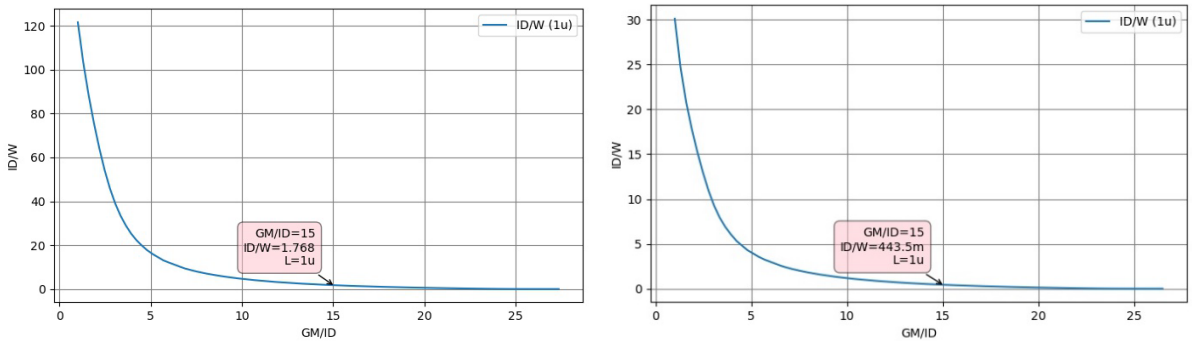
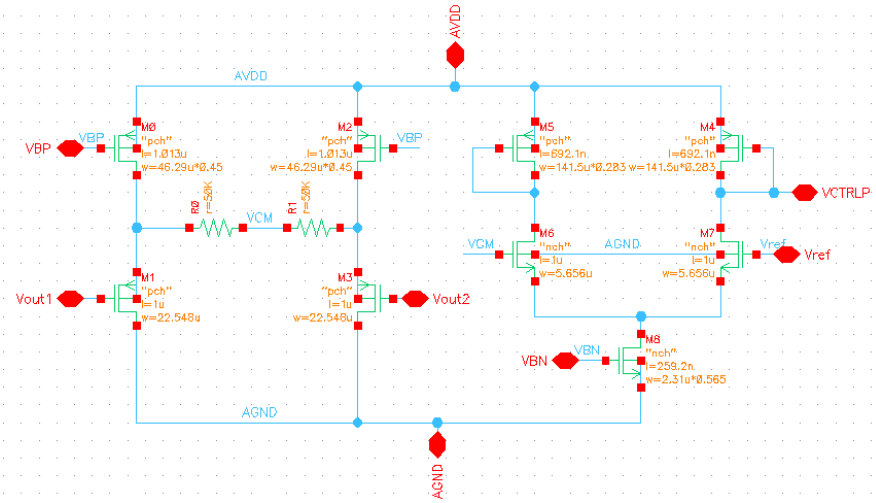



Chart used for determine width of input pair and CD MOSFETs

  4) Set VREF to be VREF+VGS=1.1+5287m=1.6, to set up output common mode level as have been in behavioural CMFB.

- **Fine Tuning for Current Budget:**

By performing previous sizing procedure, I found that circuit exceed current budget limit which is 40uA, so by tuning width of current mirrors in CD stage “sensing stage”, I have decreased current to 8uA and adjust whole current consumption of actual CMFB circuit to be 40uA instead of 42uA.
This error due to mismatch between two current mirror loads in error amplifier stage.

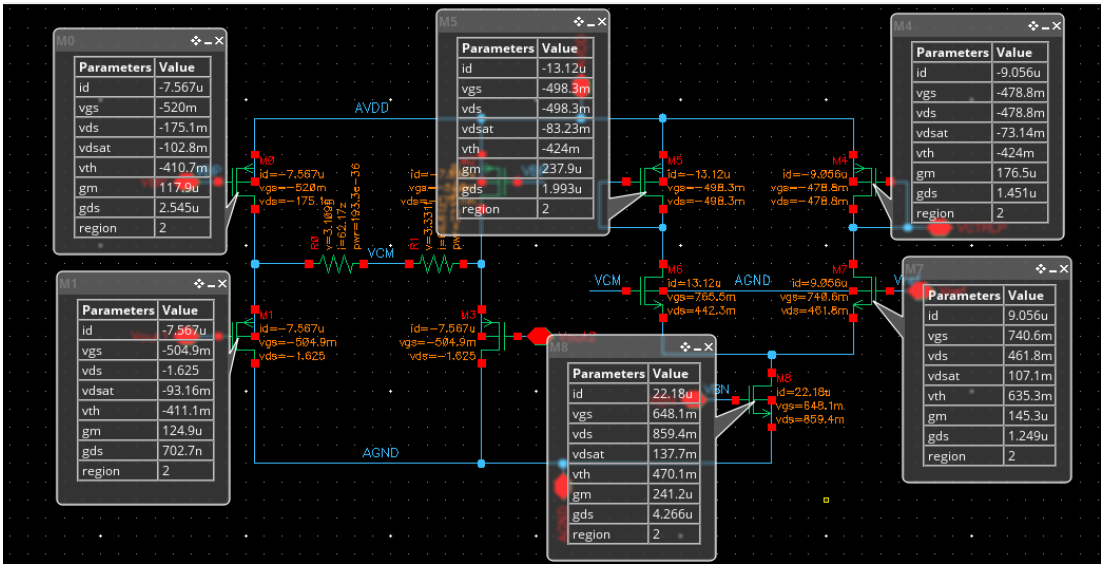



Circuit schematic from cadence with sizing annotated

- **Sizing Summary:**

| | Length | Width | Current ID | Gm | Gm/ID |
|---|---|---|---|---|---|
| Input Pair Error Amplifier | 1um | 5.656um | 10uA | 150uS | 15 |
| Current Mirror Load Error Amplifier | 692.1nm | 141.5um*0.283 | 10uA | 191.4uS | 19.14 |
| PMOS Current Mirror in CD Branch “Sensing” | 1.013um | 46.29um*0.45 | 8uA | 132.08uS | 16.51 |
| Input PMOS CD Branch | 1um | 22.548um | 8uA | 120uS | 15 |
| Tail NMOS Current Mirror for Error Amplifier | 259.2nm | 2.31um*0.565 | 20uA | 217.2uS | 10.86 |

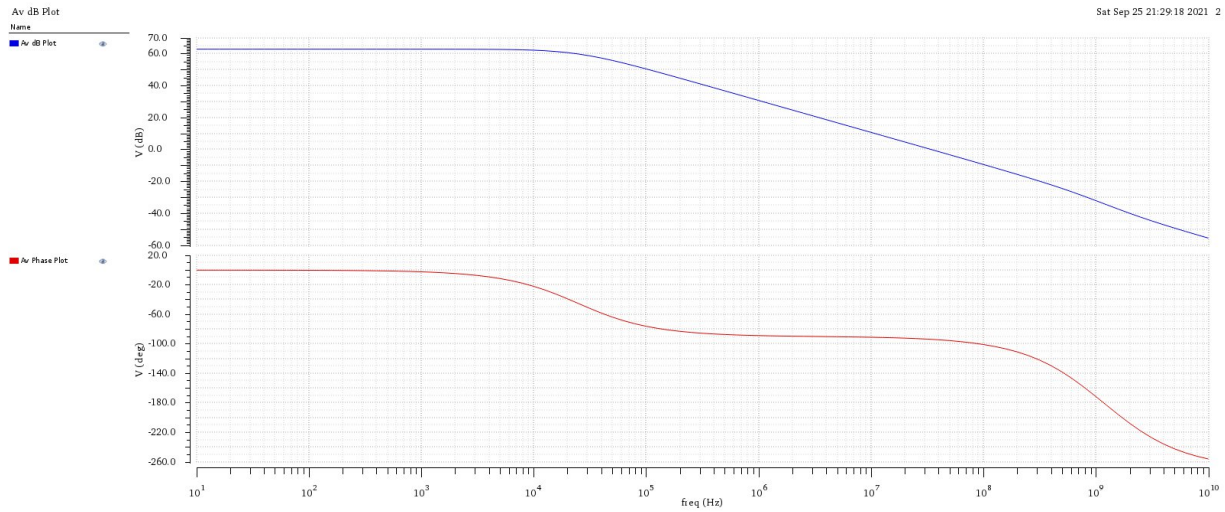
1) Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.




DC operating points results from DC simulation

- What is the CM level at the OTA output?
  The CM level at OTA output equals VREF-VGSP value which used in comparison in CMFB circuit which equals 1.6-528.7m=1.1V, as we have settled VREF to achieve this output level due to PMOS common drain stage.
- What are the differential input and output voltages of the error amplifier? What is the relation between them?
  Differential input voltage is the error voltage between common mode voltage and VREF “desired CM voltage”, and differential output is the bias voltage to tail current source to set CM DC voltage, and the relation between them is the gain of error amplifier.

2) Diff small signal ccs:
   - Plot diff gain (magnitude in dB and phase) vs frequency.




Bode plot for differential output results from AC analysis

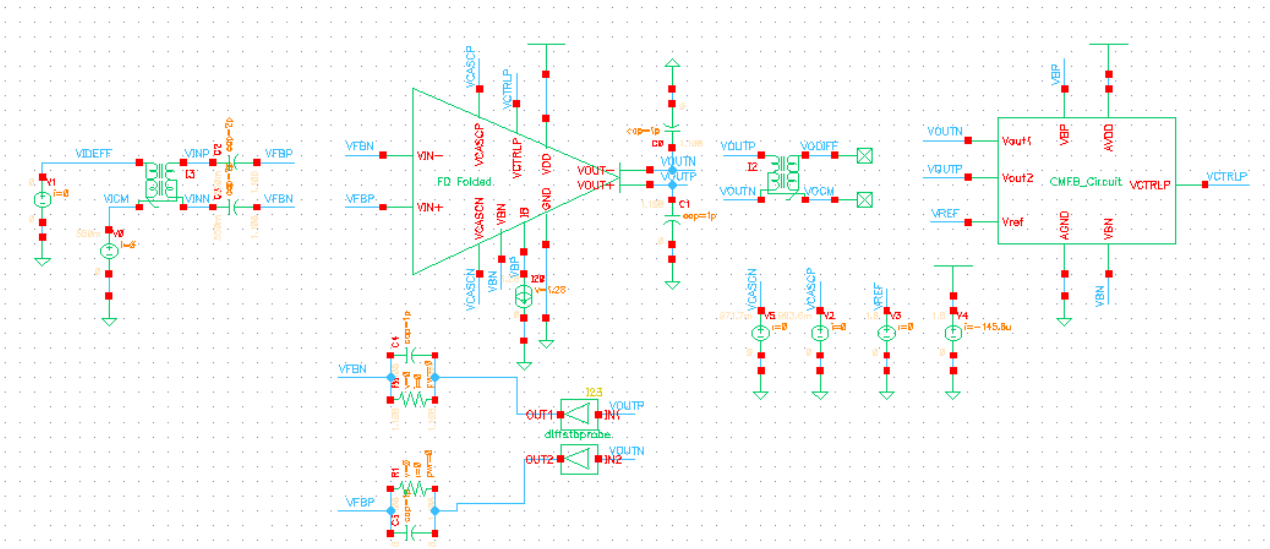
   - Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| TrainLAB:Lab11_TB:1 | Av dB Plot | | | | |
| TrainLAB:Lab11_TB:1 | Av Phase Plot | | | | |
| TrainLAB:Lab11_TB:1 | Av dB | 62.97 | | | |
| TrainLAB:Lab11_TB:1 | Av Mag | 1.407k | | | |
| TrainLAB:Lab11_TB:1 | BW | 24.75k | | | |
| TrainLAB:Lab11_TB:1 | GBW | 34.91M | | | |
| TrainLAB:Lab11_TB:1 | UGF | 35.28M | | | |
| TrainLAB:Lab11_TB:1 | PM | 86.27 | | | |

AC analysis results from ADEXL

# PART 5: Closed Loop Simulation (AC and STB Analysis)

1) Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop configuration.




Circuit schematic with feedback loop configuration

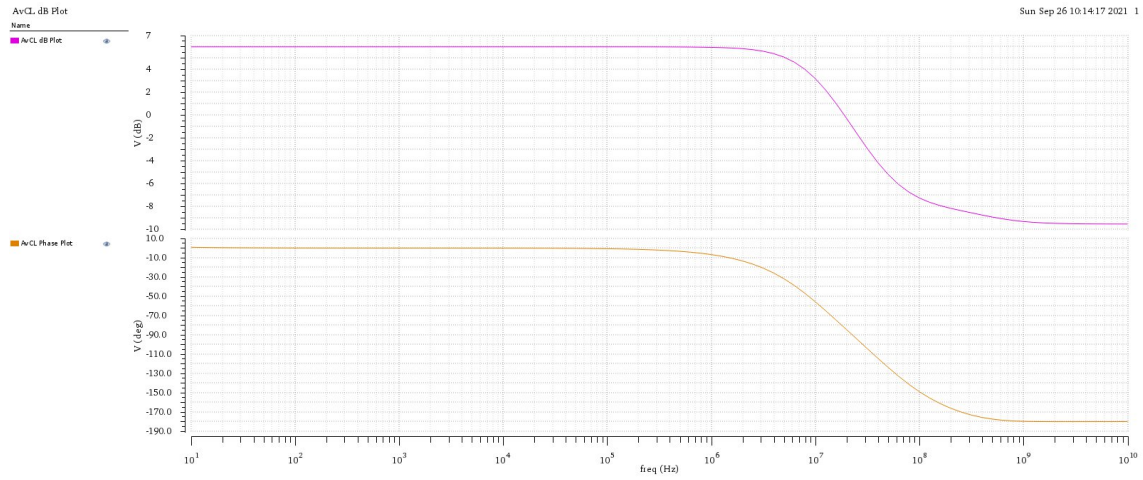
- What is the CM level at the OTA output? Why?
  CM output level is equivalent to VREF-VGSP due to CD stage in sensing branch of CMFB circuit.
- What is the CM level at the OTA input? Why?
  CM level at input of OTA is the same of CM output level due to feedback circuit on OTA, and input capacitance which block DC level from balun.

2) Differential closed-loop response:

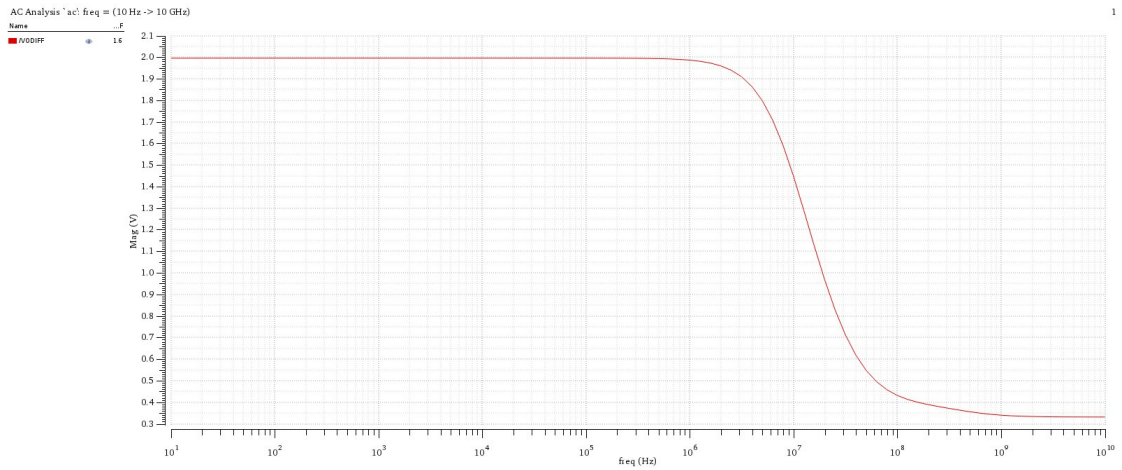
| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| | | | | | |
| TrainLAB:Lab11_TB:1 | AvCL dB | 5.999 | | | |
| TrainLAB:Lab11_TB:1 | AvCL Mag | 1.995 | | | |
| TrainLAB:Lab11_TB:1 | BW CL | 6.828M | | | |
| TrainLAB:Lab11_TB:1 | GBW CL | 13.66M | | | |
| TrainLAB:Lab11_TB:1 | UGF CL | 12.28M | | | |
| TrainLAB:Lab11_TB:1 | PM CL | 99.08 | | | |

Results from ADEXL for closed loop AC simulation

- Tuning:
  As shown from previous results that closed-loop specs not achieved, so we need to tune circuit to achieve these specs, 1st decision is to increase gm of input pair as GBW spec not achieved so increase current flow in input pair to reach that, but I found that I have exceeded current budget so 2nd decision to decrease the current flow in common gate branch to achieve current consumption spec.
- Plot VODIFF vs frequency




Bode plot result for VODIFF from AC closed-loop simulation



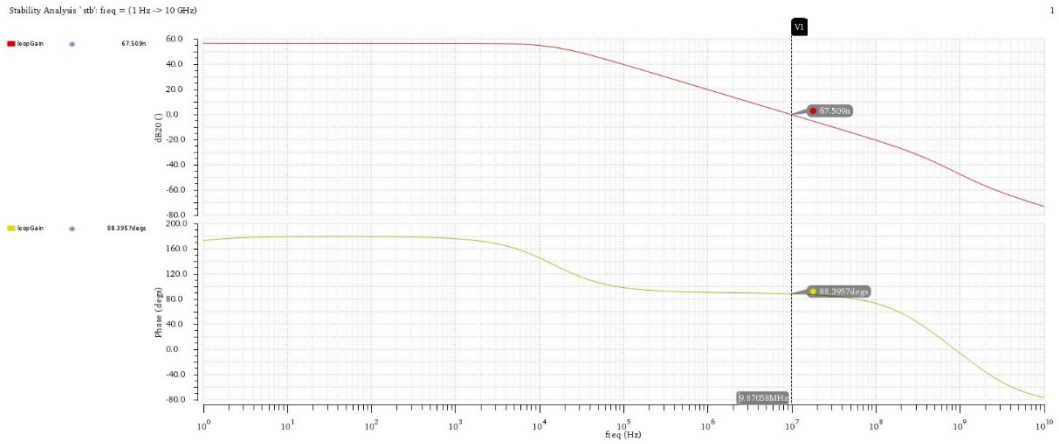

Magnitude plot for VODIFF result from AC closed-loop simulation

- Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| TrainLAB:Lab11_TB:1 | AvCL dB | 6.008 | | | |
| TrainLAB:Lab11_TB:1 | AvCL Mag | 1.997 | | | |
| TrainLAB:Lab11_TB:1 | BW CL | 10.6M | | | |
| TrainLAB:Lab11_TB:1 | GBW CL | 21.23M | | | |
| TrainLAB:Lab11_TB:1 | UGF CL | 19.21M | | | |
| TrainLAB:Lab11_TB:1 | PM CL | 97.57 | | | |

AC simulation results for closed-loop configuration after tuning

3) Differential and CMFB loops stability (STB analysis):
   - Plot loop gain in dB and phase vs frequency for the two simulations overlaid.




Loop gain bode plot from STP analysis with phase margin annotated

- Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation. Comment

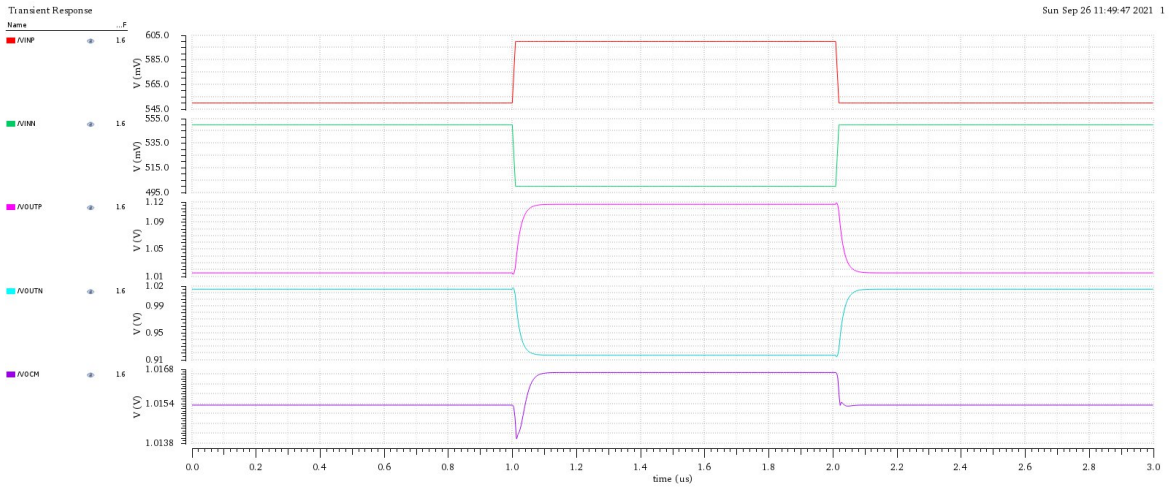
| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| TrainLAB:Lab11_TB:1 | DC LG dB | 56.69 | | | |
| TrainLAB:Lab11_TB:1 | DC LG Mag | 683.1 | | | |
| TrainLAB:Lab11_TB:1 | GBW LG | 9.77M | | | |
| TrainLAB:Lab11_TB:1 | PM LG | -91.6 | | | |

Simulation results for Loop gain parameters from ADXL

As shown from previous results that DC loop gain and GBW are half value of DC gain and GBW of open-loop simulation results, and this is due to feedback factor which equals ½ .

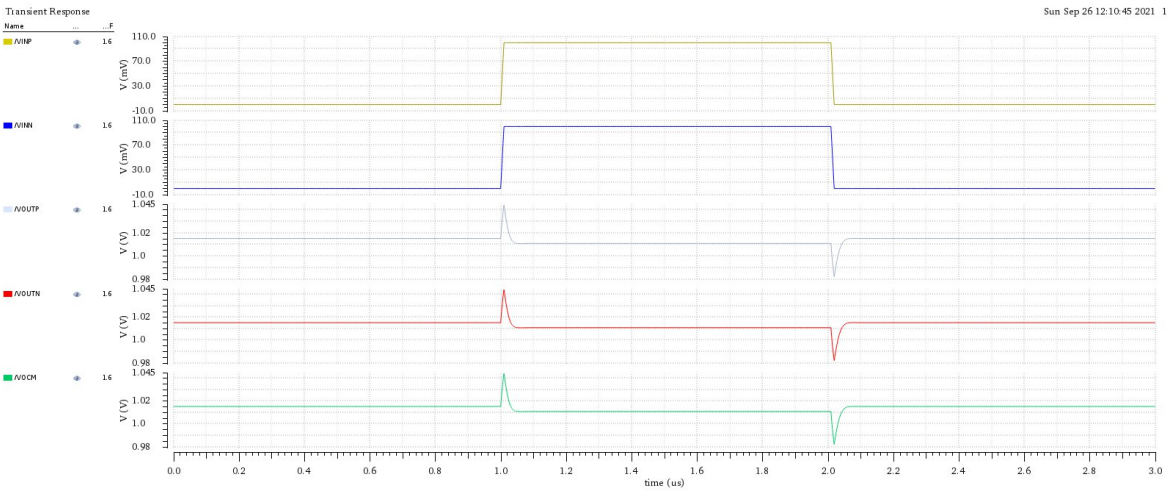
# PART 6: Closed Loop Simulation (Transient Analysis)

1) Differential and CMFB loops stability (transient analysis):
   - Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.




Transient analysis results for input and output voltages in case of VIDIFF

- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
  As shown from previous results that there is no ringing in differential signal, as we have a suitable phase margin which make system overdamped system with no ringing.
  But there is ringing in common mode signal because phase margin not sufficient to make system overdamped, so system is underdamped system.
- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

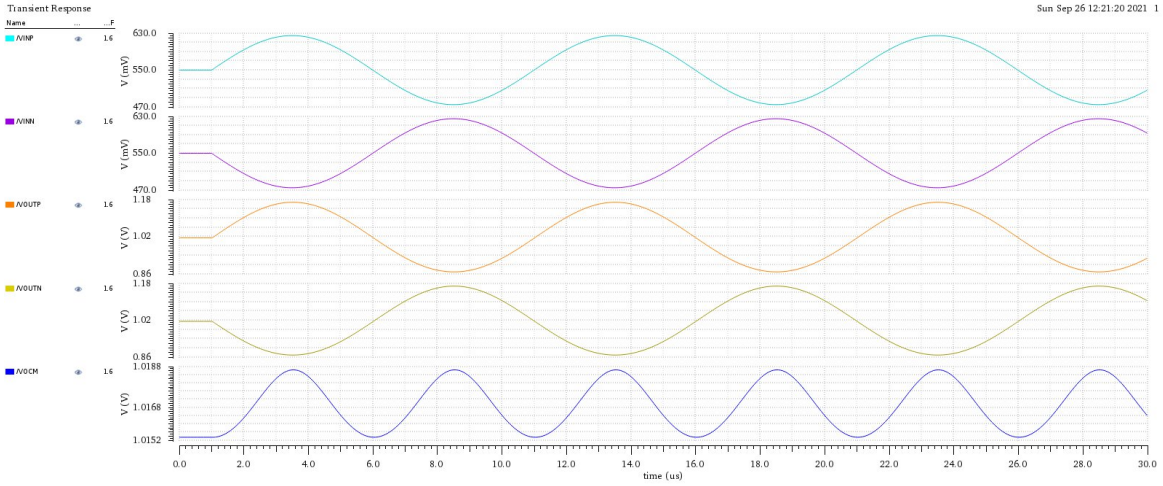



Transient analysis results for input and output voltages in case of VICM input

- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
  As shown from previous results that there is no overshoot in case of CM signal analysis, and system is considered as underdamped system because of its small phase margin.

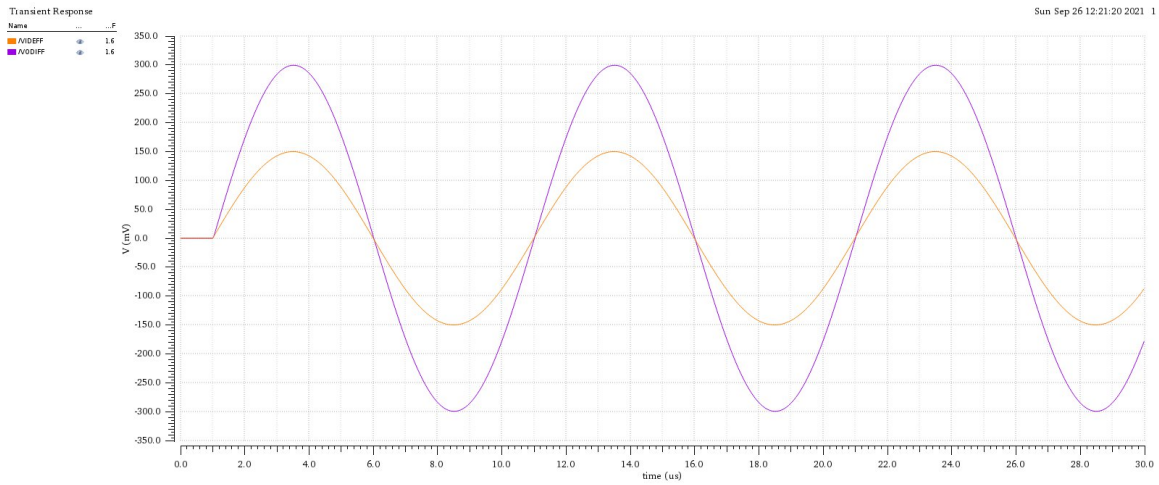
2) Output swing:

- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.




Input and output voltages on applying sine wave on diff input and transient analysis

- Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.




Voutdiff and Vidff overlaid from transient analysis simulation

- Calculate the diff input and output peak-to-peak swings and the closed loop gain.

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| TrainLAB:Lab11_TB:1 | VIDFF | | | | |
| TrainLAB:Lab11_TB:1 | VODIFF | | | | |
| TrainLAB:Lab11_TB:1 | VID P2P | 300m | | | |
| TrainLAB:Lab11_TB:1 | VOD P2P | 599.1m | | | |
| TrainLAB:Lab11_TB:1 | AvCL Trans | 1.997 | | | |
| TrainLAB:Lab11_TB:1 | VinP | | | | |
| TrainLAB:Lab11_TB:1 | VinN | | | | |
| TrainLAB:Lab11_TB:1 | VoutP | | | | |
| TrainLAB:Lab11_TB:1 | VoutN | | | | |
| TrainLAB:Lab11_TB:1 | VoCM | | | | |

Transient analysis results from ADEXL peak to peak voltages and closed-loop gain