INDRAPRASTHA INSTITUTE *of*
INFORMATION TECHNOLOGY
DELHI

Department
of
Electronics & Communication Engineering

ECE111|Digital Circuits

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END_SEM_Project:
Synchronous decade UP counter

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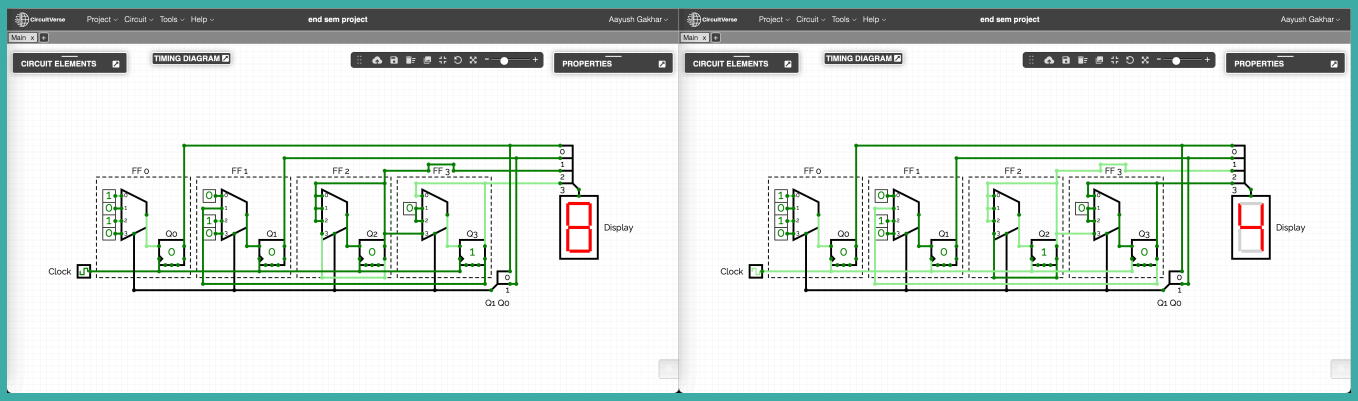
Aim:Implement a Synchronous decade UP counter in Circuit-verse and verify its operation. Realize inputs of D-flip flops with 4-input multiplexers, using Q1Q0 as the select inputs. Realize the Data inputs of the multiplexers with NOR gates.

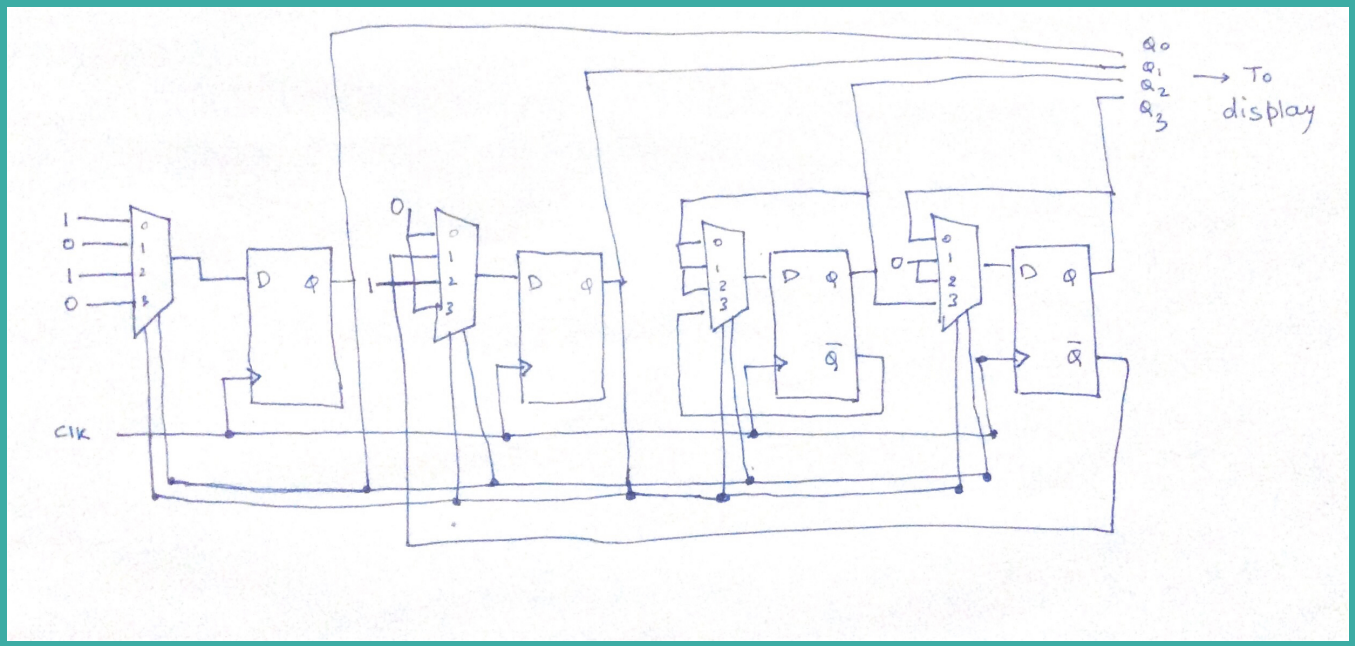
Components/ICs Used: 4:1 Mux, wire, clock, D flip flop, splitter, hex display

Youtube link: https://youtu.be/QPF-lmqr_NY

Screenshot:



Block Diagram/Circuit Diagram:



Truth Table:

Decimal	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

State Transition Table :

PS	NS	D_3	D_2	D_1	D_0
0 0 0 0	0 0 0 1	0	0	0	1
0 0 0 1	0 0 1 0	0	0	1	0
0 0 1 0	0 0 1 1	0	0	1	1
0 0 1 1	0 1 0 0	0	1	0	0
0 1 0 0	0 1 0 1	0	1	0	1
0 1 0 1	0 1 1 0	0	1	1	0
0 1 1 0	0 1 1 1	0	1	1	1
0 1 1 1	1 0 0 0	1	0	0	0
1 0 0 0	1 0 0 1	1	0	0	1
1 0 0 1	0 0 0 0	0	0	0	0

K maps (If Applicable):

D_0		$Q_1 Q_0$			
		0 0	0 1	1 1	1 0
$Q_3 Q_2$	0 0	1	0	0	1
	0 1	1	0	0	1
	1 1	X	X	X	X
	1 0	1	0	X	X

$Q_1 Q_0$	0 0	0 1	1 1	1 0
I/p OF MUX FOR D_0	1	0	0	1

D_1		$Q_1 Q_0$			
		0 0	0 1	1 1	1 0
$Q_3 Q_2$	0 0	0	1	0	1
	0 1	0	1	0	1
	1 1	X	X	X	X
	1 0	0	0	X	X

$Q_1 Q_0$	0 0	0 1	1 1	1 0
I/p OF MUX FOR D_1	0	Q_3'	0	1

D_2		$Q_1 Q_0$			
		0 0	0 1	1 1	1 0
$Q_3 Q_2$	0 0	0	0	1	0
	0 1	1	1	0	1
	1 1	X	X	X	X
	1 0	0	0	X	X

$Q_1 Q_0$	0 0	0 1	1 1	1 0
I/p OF MUX FOR D_2	Q_2	Q_2	Q_2'	Q_2

D_3		$Q_1 Q_0$			
		0 0	0 1	1 1	1 0
$Q_3 Q_2$	0 0	0	0	0	0
	0 1	0	0	1	0
	1 1	X	X	X	X
	1 0	1	0	X	X

$Q_1 Q_0$	0 0	0 1	1 1	1 0
I/p OF MUX FOR D_3	Q_3	0	Q_2	0

Logical expressions:
$D_0 = Q_0'$
$D_1 = Q_1'Q_0Q_3'+Q_1Q_0'$
$D_2 = Q_0'Q_2+Q_0'Q_2+Q_1Q_0Q_2'$
$D_3 = Q_2Q_1Q_0+Q_3Q_0'$

Observations/Results: The display shows from 0 to 9 as given in truth table.

Applications of the experiment:
Clock generation
Clock division
In frequency counting circuits