

# INDRAPRASTHA INSTITUTE of INFORMATION TECHNOLOGY DELHI

Department of Electronics & Communication Engineering

ECE111|Digital Circuits

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Lab\_6:
Combinational Circuit Design

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# Part A. Decoder Circuit for generating BCD Code from Encrypted code

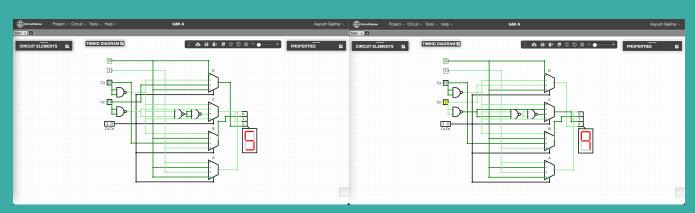
Aim: Designing and testing of a circuit for decryption/decoding of an incoming digital signal which is encrypted by some set of rules which are:

An encrypted communication system sends decimal digits encoded by a 4-bit binary code C3 C2 C1 C0 according to the following scheme, where N denotes the value of the digit:

For  $4 \ge N \ge 0$ , C3 C2 C1 C0 = 13 – N (in decimal), and for  $9 \ge N \ge 5$ , C3 C2 C1 C0 = N – 3 (in decimal).

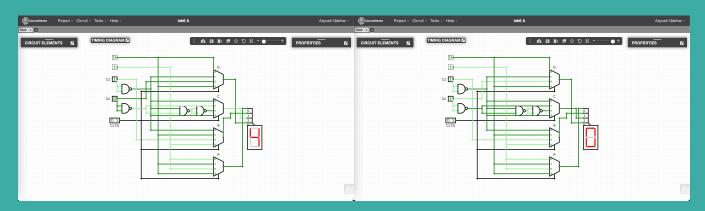
Components/ICs Used: Input, ConstantVal, Nand gate, Wire, splitter(Bitwidth=4), Hexdisplay

#### Circuit Diagram:



Input = 2(0010) Output = 5

Input = 6(0110) Output = 9



Input = 9(1001) Output = 4

Input = 13(1101) Output = 0

#### Truth Table:

| Encr. Code | <b>C</b> 3 | C2 | <b>C1</b> | CO | DE of N | D | С | В | Α |
|------------|------------|----|-----------|----|---------|---|---|---|---|
| 0          | 0          | 0  | 0         | 0  | X       | X | X | X | X |
| 1          | 0          | 0  | 0         | 1  | X       | X | X | X | X |
| 2          | 0          | 0  | 1         | 0  | 5       | 0 | 1 | 0 | 1 |
| 3          | 0          | 0  | 1         | 1  | 6       | 0 | 1 | 1 | 0 |
| 4          | 0          | 1  | 0         | 0  | 7       | 0 | 1 | 1 | 1 |
| 5          | 0          | 1  | 0         | 1  | 8       | 1 | 0 | 0 | 0 |
| 6          | 0          | 1  | 1         | 0  | 9       | 1 | 0 | 0 | 1 |
| 7          | 0          | 1  | 1         | 1  | X       | X | X | X | X |
| 8          | 1          | 0  | 0         | 0  | X       | X | X | X | X |
| 9          | 1          | 0  | 0         | 1  | 4       | 0 | 1 | 0 | 0 |
| 10         | 1          | 0  | 1         | 0  | 3       | 0 | 0 | 1 | 1 |
| 11         | 1          | 0  | 1         | 1  | 2       | 0 | 0 | 1 | 0 |
| 12         | 1          | 1  | 0         | 0  | 1       | 0 | 0 | 0 | 1 |
| 13         | 1          | 1  | 0         | 1  | 0       | 0 | 0 | 0 | 0 |
| 14         | 1          | 1  | 1         | 0  | X       | X | X | X | X |
| 15         | 1          | 1  | 1         | 1  | X       | X | X | X | X |

## K maps (If Applicable):

| D     |     | C1 C0 |     |    |     |  |  |
|-------|-----|-------|-----|----|-----|--|--|
|       |     | 0 0   | 0 1 | 11 | 1 0 |  |  |
| C3 C2 | 0 0 | X     | X   | 0  | 0   |  |  |
|       | 0 1 | 0     | 1   | X  | 1   |  |  |
|       | 11  | 0     | 0   | X  | X   |  |  |
|       | 1 0 | X     | 0   | 0  | 0   |  |  |

| C1 C0            | 0 0 | 0 1 | 11 | 10 |
|------------------|-----|-----|----|----|
| I/O OF MUX FOR D | 0   | C3' | 0  | C2 |

| С     |     | C1 C0 |     |    |     |  |  |
|-------|-----|-------|-----|----|-----|--|--|
|       |     | 0 0   | 0 1 | 11 | 1 0 |  |  |
| C3 C2 | 0 0 | X     | X   | 1  | 1   |  |  |
|       | 0 1 | 1     | 0   | Χ  | 0   |  |  |
|       | 11  | 0     | 0   | X  | X   |  |  |
|       | 1 0 | X     | 1   | 0  | 0   |  |  |

| C1 C0            | 0 0 | 0 1 | 11  | 10      |
|------------------|-----|-----|-----|---------|
| I/O OF MUX FOR C | C3' | C2' | C3' | C3' C2' |

| В     |     | C1 C0 |     |    |     |  |  |
|-------|-----|-------|-----|----|-----|--|--|
|       |     | 0 0   | 0 1 | 11 | 1 0 |  |  |
| C3 C2 | 0 0 | X     | X   | 1  | 0   |  |  |
|       | 0 1 | 1     | 0   | X  | 0   |  |  |
|       | 11  | 0     | 0   | X  | X   |  |  |
|       | 1 0 | X     | 0   | 1  | 1   |  |  |

| C1 C0            | 0 0 | 0 1 | 11 | 1 0 |
|------------------|-----|-----|----|-----|
| I/O OF MUX FOR B | C3' | 0   | 1  | C3  |

| Α     |     | C1 C0 |     |    |     |  |  |
|-------|-----|-------|-----|----|-----|--|--|
|       |     | 0 0   | 0 1 | 11 | 1 0 |  |  |
| C3 C2 | 0 0 | X     | X   | 0  | 1   |  |  |
|       | 0 1 | 1     | 0   | X  | 1   |  |  |
|       | 11  | 1     | 0   | X  | X   |  |  |
|       | 1 0 | X     | 0   | 0  | 1   |  |  |

| C1 C0            | 0 0 | 0 1 | 11 | 1 0 |
|------------------|-----|-----|----|-----|
| I/O OF MUX FOR A | 1   | 0   | 0  | 1   |

| FINAL |     |     |         |     |  |  |  |  |  |
|-------|-----|-----|---------|-----|--|--|--|--|--|
| C1 C0 | 0 0 | 0 1 | 10      | 11  |  |  |  |  |  |
| D     | 0   | C3' | C2      | 0   |  |  |  |  |  |
| С     | C3' | C2' | C3' C2' | C3' |  |  |  |  |  |
| В     | C3' | 0   | C3      | 1   |  |  |  |  |  |
| Α     | 1   | 0   | 1       | 0   |  |  |  |  |  |

Observations/Results: The hex display works according to the truth table

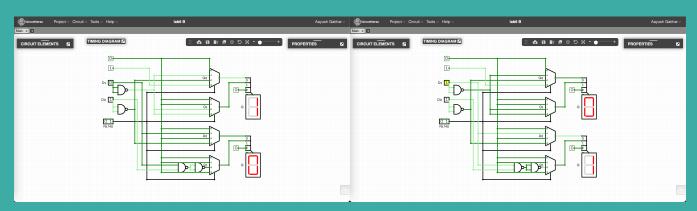
Applications:Decoders are greatly used in applications where the particular output or group of outputs to be activated only on the occurrence of a specific combination of input levels. Specific output is provided for specific input.

## Part B. Divider Circuit for 2-bit Binary Numbers

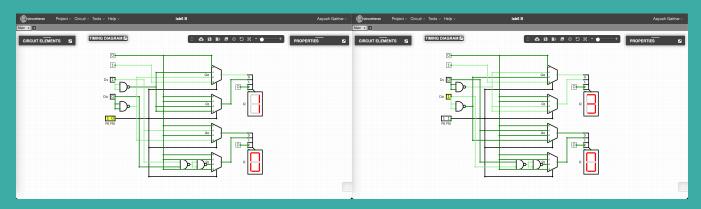
Aim: Designing and testing a circuit for dividing a 2-bit number N1 N0 by another 2-bit number D1 D0 (D1 D0  $\neq$  0) to generate a 2-bit quotient Q1 Q0 and a 2-bit remainder R1 R0.

Components/ICs Used: Input, ConstantVal, Nand gate, Wire, splitter(Bitwidth=4), Hexdisplay

#### Circuit Diagram:



Input(N1 N0 D1 D0) = 0101 Output(Q R) = 1 0 Input(N1 N0 D1 D0) = 0111 Output(Q R) = 0 1



Input(N1 N0 D1 D0) = 1010 Output(Q R) = 1 0 Input(N1 N0 D1 D0) = 1101 Output(Q R) = 30

#### Truth Table:

| N1 | N0 | D1 | D0 | Q1 | Q0 | R1 | R0 |
|----|----|----|----|----|----|----|----|
| 0  | 0  | 0  | 0  | X  | X  | X  | X  |
| 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  |
| 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  |
| 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  |
| 0  | 1  | 0  | 0  | X  | X  | X  | X  |
| 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  |
| 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  |
| 0  | 1  | 1  | 1  | 0  | 0  | 0  | 1  |
| 1  | 0  | 0  | 0  | X  | X  | X  | X  |
| 1  | 0  | 0  | 1  | 1  | 0  | 0  | 0  |
| 1  | 0  | 1  | 0  | 0  | 1  | 0  | 0  |
| 1  | 0  | 1  | 1  | 0  | 0  | 1  | 0  |
| 1  | 1  | 0  | 0  | X  | X  | X  | X  |
| 1  | 1  | 0  | 1  | 1  | 1  | 0  | 0  |
| 1  | 1  | 1  | 0  | 0  | 1  | 0  | 1  |
| 1  | 1  | 1  | 1  | 0  | 1  | 0  | 0  |

### K maps (If Applicable):

| Q1    |     | N1 N0 |     |    |     |  |  |
|-------|-----|-------|-----|----|-----|--|--|
|       |     | 0 0   | 0 1 | 11 | 1 0 |  |  |
| D1 D0 | 0 0 | X     | X   | X  | Χ   |  |  |
|       | 0 1 | 0     | 0   | 1  | 1   |  |  |
|       | 11  | 0     | 0   | 0  | 0   |  |  |
|       | 1 0 | 0     | 0   | 0  | 0   |  |  |

| N1 N0             | 0 0 | 0 1 | 11  | 1 0 |
|-------------------|-----|-----|-----|-----|
| I/O OF MUX FOR Q1 | 0   | 0   | D1' | D1' |

| Q0    |     | N1 N0 |     |    |     |
|-------|-----|-------|-----|----|-----|
|       |     | 0 0   | 0 1 | 11 | 1 0 |
| D1 D0 | 0 0 | X     | Χ   | X  | X   |
|       | 0 1 | 0     | 1   | 1  | 0   |
|       | 11  | 0     | 0   | 1  | 0   |
|       | 10  | 0     | 0   | 1  | 1   |

| N1 N0             | 0 0 | 0 1 | 11 | 10  |
|-------------------|-----|-----|----|-----|
| I/O OF MUX FOR Q0 | 0   | D1' | 1  | D0' |

| R1    |     | N1 N0 |     |    |     |
|-------|-----|-------|-----|----|-----|
|       |     | 0 0   | 0 1 | 11 | 1 0 |
| D1 D0 | 0 0 | X     | X   | X  | X   |
|       | 0 1 | 0     | 0   | 0  | 0   |
|       | 11  | 0     | 0   | 0  | 1   |
|       | 1 0 | 0     | 0   | 0  | 0   |

| N1 N0             | 0 0 | 0 1 | 11 | 1 0   |
|-------------------|-----|-----|----|-------|
| I/O OF MUX FOR R1 | 0   | 0   | 0  | D1 D0 |

| R0    |     | N1 N0 |     |    |     |
|-------|-----|-------|-----|----|-----|
|       |     | 0 0   | 0 1 | 11 | 1 0 |
| D1 D0 | 0 0 | X     | X   | X  | X   |
|       | 0 1 | 0     | 0   | 0  | 0   |
|       | 11  | 0     | 1   | 0  | 0   |
|       | 1 0 | 0     | 1   | 1  | 0   |

| N1 N0             | 0 0 | 0 1 | 11  | 10 |
|-------------------|-----|-----|-----|----|
| I/O OF MUX FOR R0 | 0   | D1  | D0' | 0  |

| FINAL |     |     |       |     |  |  |
|-------|-----|-----|-------|-----|--|--|
| N1 N0 | 0 0 | 0 1 | 10    | 11  |  |  |
| Q1    | 0   | 0   | D1'   | D1' |  |  |
| Q0    | 0   | D1' | D0'   | 1   |  |  |
| R1    | 0   | 0   | D1 D0 | 0   |  |  |
| R0    | 0   | D1  | 0     | D0' |  |  |

Observations/Results: The hex display works according to the truth table.

Applications: Dividers are used in ALU of chips to do basic division operations. This is a combinational circuit and combinational circuits have a wide variety of uses such as calculators, digital measuring techniques, computers, digital processing, automatic control of machines, industrial processing, digital communications, etc.