POKHARA UNIVERSITY

Level: Bachelor | Semester – Spring | Year : 2005
Programme: BE | Full Marks: 100
Course: Computer Organization | Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	Why are different types of addressing modes used in computer system? Describe them in brief.	8
	b)	Describe Booth's algorithm for multiplying two numbers represented in two's complement notation with an example.	7
2.	a)	Explain a general model of a control unit with a suitable diagram.	5
	b)	What are the design issues of an instruction format?	5
	c)	What is stack? Describe the memory stack organization.	5
3.	a)	Describe the different methods to generate the address of next microinstruction in microcode memory (control memory).	8
	b)	What do you mean by microprogramming language? Describe the applications of microprogramming.	7
4.	a)	Why external devices are not directly connected with bus structure of computer system? Draw an internal organization of an I/O module.	8
	b)	What is the main purpose of using DMA? Describe different types of DMA transfer modes.	7
5.	a)	What are the replacement algorithms in cache? Explain advantages and disadvantages of each with suitable examples.	5
	b)	How does the Block size affect the hit ratio in cache?	5
	c)	What are the Access methods in memory? Explain each.	5
6.	a)	What is parallel processing? Explain how pipelining hardware speed up the computation with suitable derivations.	8
	b)	What are the main functions of operating system? Describe any one function of operating system.	7
7.	Write short notes on (**Any Two**):		2x5
	a)	Vector Processing.	
	b)	I/O processor.	
	c)	Power PC addressing modes.	

POKHARA UNIVERSITY

Level: Bachelor Semester – Spring Year : 2006
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Describe assembly process for assembly language programs. How does it differ from compilation process of high level language? 8

   b) What is addressing modes? Describe different types of addressing modes. 7

2. a) Design the implementation of the simple system whose behaviour can be specified by the following RTL. 8

   j:M<-A

   o:A<-Y

   h:R<-M

   N:Y<-R, M<-R

   (Use direct connections)

   b) Explain the CPU organization of a basic computer with the help of appropriate block diagram. 7

3. a) What is the main difference between RTL and VHDL? Explain with the help of suitable example. 7

   b) What are the points the designer should consider while choosing either of micro-programmed control unit or hardwired control unit? 8

4. A kind of very simple CPU has following instructions. 15

Instructions	Instruction Code	Operation
ADD	00AAAAAA	AC←AC+M[AAAAAA]
AND	01AAAAAA	AC←AC∧M[AAAAAA]
SKIP	10XXXXXX	PC←PC+1
INC	11XXXXXX	AC←AC+1

   a) Show the RTL for the fetch cycle and execute cycle of each

instruction and state diagram.

b) Design registers section and ALU section

c) Design Hardwired control unit with necessary control signals.

5. a) Differentiate vertical and horizontal microcode with examples. 7

b) What do you understand by arithmetic pipeline? Do you think it will speed up the computation? Support your answer with derivation and suitable examples. 8

6. a) What are the different components of memory hierarchy? Explain all components in brief. 7

b) What do you mean by destination initiated data transfer without handshaking? Illustrate with timing and implementation of an example. 8

7. Write short notes on **(Any Two):** 5×2

a) Use of RISC in special purpose computer

b) Organization of multi-processor system

c) System Buses

d) Types of Interrupts

POKHARA UNIVERSITY

Level: Bachelor | Semester – Spring | Year : 2007
Programme: BE | Full Marks: 100
Course: Computer Organization | Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the factors that should be considered while designing a computer for performance? What can be done to balance the performance between processor and main memory? 7

   b) Describe the algorithm for multiplying two numbers (-9) with (-2) represented in signed magnitude. 8

2. a) What is an instruction set? What are the different design issues of instruction set? 5

   b) Draw a state diagram of instruction cycle and explain each state in brief. 5

   c) What is micro operation? Illustrate the micro operation involved in fetch and interrupt sub cycle of instruction cycle. 5

3. a) Explain the function of microprogramming control unit with suitable diagram. 8

   b) Describe different microinstruction sequencing techniques with suitable diagrams. 7

4. a) What are the reasons for not connecting peripherals directly to the system bus? Draw and explain the generic structure of the I/O module. 7

   b) How DMA overcome the drawbacks of programmed and interrupt driven I/O/ Explain DMA controller with clear diagram. 8

5. a) What are the elements of cache design? How associative mapping is different from Set-associative mapping? 8

   b) List out the key characteristic of computer memory system and explain them in brief. 7

6. a) Define scheduling. What are their types? Explain each in detail. 8

   b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six- segment pipeline with a clock cycle of 7

10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

7. Write short notes on (***Any Two***): 2×5

a) Virtual memory

b) Pentium instruction format

c) Vector processing and its use

d) Stack

POKHARA UNIVERSITY

Level: Bachelor Semester – Fall Year : 2008
Programme: BE Full Marks: 100
Course: Computer Organization Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	Discuss the Pentium and power PC evolution.	7
	b)	Describing the Booth's algorithm, find out the result of 7*(-3)	8
2.	a)	Describe the factors that influence the design of an instruction format.	5
	b)	Explain the typical Pentium processor organization.	5
	c)	What do you mean by micro-operation? Illustrate the micro-operations involved in fetch and indirect subcycles of an instruction cycle.	5
3.	a)	Discuss the sequencing techniques based on the format of address information in micro instruction.	8
	b)	Compare and contrast different I/O techniques.	7
4.	a)	What are the roles of four main register in DMA chip? Draw the sample System with DMA Controller and explain how I/O Devices and handled by DMA Controller.	8
	b)	What are the main functions of operating system? Describe any one function of operating system.	7
5.	a)	Why cache is incorporated in between the processor and main memory? In which manner data are copied into the cache from main memory and are replaced later in order to achieve higher hit ration?	8
	b)	Mention the various scheduling criteria for choosing the right scheduling algorithm.	7
6.	a)	Discuss the various levels of RAID.	8
	b)	Assume that pipeline has K = 8 segment and executes n = 120 tasks in sequence. Let the time taken to process a sub operation in each segment is 40 ns. Calculate the speed up ratio in pipe line.	7
7.	Write short notes on ***(Any Two)***		2×5
	a)	Horizontal and vertical microinstructions	
	b)	Pipelining Hazards	
	c)	Bus architecture	

POKHARA UNIVERSITY

Level: Bachelor Semester – Spring Year : 2008
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What do you mean by instruction format? What are the factors to be considered while designing the instruction set of a computer? 2+5

   b) Why do we need different types of addressing modes? Describe the general addressing modes of a computer system with some examples. 2+6

2. a) Design a 16 × 4 memory subsystem using four 8 × 2 ROM chips and low-order interleaving. 8

   b) What are the applications of VHDL? Describe the different sections of it taking an example of any logic circuit. 2+5

3. a) What are Specifications of Very Simple CPU? 5

   b) Write the micro-operations of Very Simple CPU for fetch and execute cycles. 5

   c) Design the Register and ALU section for that CPU. 5

4. a) Explain detail procedure for implementing shift-add multiplication algorithm. 3+4

   b) What is the principle concept behind the arithmetic pipeline? Draw the pipelining hardware for the following arithmetic expression and compare it with non pipelining hardware. Assume the necessary data for it. 8

      For i = 0 to 10

      $X[i] = A[i] \times (B[i] + C[i]) / D[i]$

5. a) What is the concept of hierarchical memory system? What are the elements of hierarchical memory system? 2+5

   b) What do you mean by virtual memory? Explain about the concept of paging or segmentation technique. 2+6

6. a) What are the different types of asynchronous data transfer techniques. How does asynchronous technique differ with synchronous technique? 8

   b) Differentiate between RISC and CISC computers. What is Register window? 4+3

7. Write short notes on ***(Any Two)*** 2×5

   a) Micro programmed control Vs hardwired control

   b) Mathematical Co-processor

   c) IEEE 754 floating point standard

POKHARA UNIVERSITY

Level: Bachelor Semester – Fall Year : 2009
Programme: B.E. Full Marks : 100
Course: Computer organization and architecture Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the issues to consider while designing instruction set architecture? 7

   b) How a 16 X 2 memory subsystem can be constructed from two 8 x2 ROM chips with low-order interleaving? Explain. 8

2. Design a very simple CPU that has 6-bit address register (AR), 6-bit program counter (PC), 8-bit data register (DR) and 2-bit instruction register (IR). The CPU must execute the following instructions:

Instruction	Instruction Code	Operation
COM	00XXXXXX	AC ← AC'
AND	01AAAAAA	AC ← AC ^ M[AAAAAA]
JREL	10AAAAAA	PC ← PC+AAAAAA
SKIP	11XXXXXX	PC ← PC+1

   a) Show the RTL code for the fetch and execute cycles for each instruction and draw the state diagram. 7

   b) Show the final register section and hardwired control unit for the same CPU. 8

3. a) Taking the reference of the very simple CPU of question No.2, design a very simple microsequencer using horizontal microcode. 7

   b) For the same very simple CPU design a very simple microsequencer using vertical microcode. Compare the horizontal and vertical microcode from the above scenario. 8

4. a) Write the RTL code for the booth's Algorithm. Using the same code 8

trace the multiplication of (-5) and (3).

b) Explain different design issues of cache memory. 7

5. a) What are the significance of cache memory? Write different types of mapping technique. 7

b) How DMA controller can be incorporated in a computer system? 8

6. a) Write about the instruction pipeline conflicts. Explain the remedy to overcome data conflicts. 8

b) What do you understand by the term "Cache Coherence"? Explain how can we resolve the Cache coherence problem? 7

7. Write short notes on: **(Any Two)** 5x2

a) VHDL

b) RISC VS CISC

c) Virtual Memory

POKHARA UNIVERSITY

Level: Bachelor | Semester – Spring | Year : 2009
Programme: BE | Full Marks: 100
Pass Marks : 45
Course: Computer Organization and Architecture | Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define addressing mode. Explain different types of addressing mode with example. 8

   b) Define VHDL. Write the VHDL program for full adder. 7

2. Design a very simple CPU that has 6-bit address register (AR), 6 bit program counter (PC), 8 bit data register (DR) and 2 bit instruction register (IR). The CPU must execute the following Instructions:

Instruction	Instruction Code	Operation
COM	00XXXXXX	AC ← AC'
JMP 1	01AAAAAA	PC ← AAAAAA+1
ADD 1	10AAAAAA	AC ← AC+M[AAAAAA]+1
SKIP	11XXXXXX	PC ← PC+1

   a) Write the RTL code of micro-operations for fetch and execute cycles of each instruction. 8

   b) Design the register and ALU section to implement those micro-operations. 7

3. a) A computer system with an 8 bit address bus and an 8 bit data bus uses isolated I/O. It has 64 bytes of EEPROM starting at address 00H; 64 bytes of RAM starting at address next to the last address of EEPROM and an input device at address FOH. Show the design for this system. Include all necessary logic. 8

   b) Write the differences between hardwired and micro-prorammed control unit. 7

4. a) What is the purpose of using BCD in computer system? Design 8

hardware for a BCD adder.

b) Write the RTL code for Booth's algorithm. Using same code trace the multiplication of (-5) and (3). 7

5. a) What is hierarchical memory system. Explain all the elements of memory hierarchy? 7

b) What is virtual memory? Explain about paging and segmentation techniques regarding the memory management. 8

6. a) Mention different I/O techniques. Differentiate programmed I/O and interrupt I/O. 8

b) Describe different types of topologies of multiprocessor system. 7

7. Write short notes on (**Any Two**) : 5×2

a) DMA

b) Hit ratio

c) Instruction Set Architecture

POKHARA UNIVERSITY

Level: Bachelor | Semester – Fall | Year : 2010
Programme: BE | Full Marks : 100
Pass Mark : 45
Course: Computer Organization and Architecture | Time : 3 hrs

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a. Describe the assembly process for assembly language programs. How does it differ from the compilation process? 8

   b. Design the 16x 4 memory subsystem constructed from two 16 X2 ROM chips with 7
      i. High Order Interleaving
      ii. Low Order Interleaving

2. a. Show the hardware to implement the following RTL code. 7
      i. M : X ←X +Y
      ii. N :X←X+Y'+1
      iii. O :X←X^Y

   b. What do you mean by micro sequencer ?Explain with the generic micro sequencer organization. 8

3. a. For a very simple CPU with the following instruction sets: 8

Instruction	Operation	Instruction code
ADD AAAAAA	AC ← AC+M[AAAAAA]	00AAAAAA
AND AAAAAA	AC ← AC^M[AAAAAA]	01AAAAAA
COM	AC ← AC'	10XXXXXX
OR AAAAAA	AC ← AC ∨ M[AAAAAA]	11AAAAAA

      i. Describe specifications and draw State diagram.
      ii. Design ALU and Register set

   b. For the question given in number 3,a. design a hardwired control unit. 7

4. a. Write the steps of Booth algorithm? Show the trace of the RTL code for Booths algorithm for x = 0110 and Y = 1011 8

b. What are the different topologies used to interconnect MIMD computers? Describe with suitable diagrams. 7

5. a. Define Memory hierarchy? How to convert the logical address to physical address .Explain with diagrams 8

b. Why we use asynchronous data Transfer mechanism ?Explain source initiated data transfer with examples. 7

6. a. What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Also describe what the solutions to correct these conflicts are? 8

b. Describe the microinstruction format? Explain the horizontal and vertical microcode. 7

7. Write short notes on **(Any Two):** 2×5

a. VHDL

b. DMA

c. Instruction formats

POKHARA UNIVERSITY

Level: Bachelor Semester – Fall Year : 2011
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What is system bus? Explain in details. 7

   b) Define ISA. Explain different addressing modes. 8

2. a) Define VHDL. Write the VHDL program for full adder. 7

   b) How a 16×2 memory sub system can be constructed from two 8×2 ROM chip with low order interleaving and high order interleaving. Explain with diagram. 8

OR

   a) What is RTL? Write the RTL for different arithmetic operations. Design a 4-bit decimal right shifting circuit. 7

   b) What is instruction cycle? Explain instruction cycle state diagram. 8

3. Design a CPU that meets the following specification: 15

   a) It can access 64 bytes of memory each 8 bit wide. The CPU does this by outputting a 6 bit address on its output pin A{5...0] and reading 8-bit value from memory on its inputs D[7...0].

   b) The CPU contains 6-bit AR, 6-bit PC, 8-bit Dr and 2-bit IR.

   c) The CPU realize following instruction:

Instruction	Instruction Code	Operation
SUB	00AAAAAA	AC = AC-M[AAAAAA]
AND	01AAAAAA	AC = AC^M[AAAAAA]
JMP	10AAAAAA	GOTO AAAAAA
INC	11XXXXXX	AC = AC + 1

i. Write the RTL for fetch and execute cycle and draw its register section for CPU.

ii. Design a hardwired control unit for above CPU.

4. a) Differentiate a hardwired control unit with micro-programmed control unit. 7

   b) Write the RTL code for Booth's algorithm. Using same code trace the multiplication of (-5) and (3). 8

5. a) What is hierarchical memory system? Explain any one of the cache mapping technique? 7

   b) What do you mean by destination initiated data transfer without handshaking? Illustrate with timing and implementation of an example. 8

6. a) Explain different types of conflict in instruction pipeline with example. 8

   b) Describe different types of topologies of multiprocessor system. 7

OR

   a) What is parallelism? How can it be achieved in uniprocessor systems? 7

   b) Show the layout of the cache for a CPU that can address 1M×16 of memory; the cache holds 8k×16 of data and has the following mapping strategies: give the number of bits per location and total number of locations 8

      i. Fully Associative

      ii. Direct Mapped

      iii. Two- way associative

7. Write short notes on **any two:** 2×5

   a) DMA

   b) RISC versus CISC

   c) Virtual Memory

POKHARA UNIVERSITY

Level: Bachelor Semester – Fall Year : 2012
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What do you mean by instruction format? What are the factors to be considered while designing the instruction set of a computer? 7
   b) Design the 8×2 ROM memory using Linear and two dimensional Organization. 8
2. a) What is RTL? Write the RTL for Arithmetic and Logical Instruction. 7
   b) Design a very simple CPU that has the following instruction set and Show the RTL code for execute cycle of each Instruction. Also design the Register sections with ALU. 8

Instruction	Instruction Code	Operation
ADD	00AAAAAA	AC← AC+M[AAAAAA]
OR	01AAAAAA	AC←AC V M[AAAAAA]
JMP	10AAAAAA	GOTO AAAAAA
INC	11XXXXXX	AC←AC+1

3. a) For the question given in number 2.b), design a hardwired control unit. 7
   b) Write the steps of booth algorithm? Show the trace of the RTL code for Booths Algorithm for (-8×5) 8
4. a) What is virtual memory? Describe how paging is implemented in virtual memory. 7
   b) Describe the working principle of DMA with suitable diagram. 8
5. a) What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Describe the solutions to correct data conflicts. 8
   b) Why we used Asynchronous Data Transfer mechanism ?Explain source initiated data transfer with examples 7
6. a) Why parallel processing is necessary? Expalin various types of 8

Multiprocessor organisation.

b) Describe the working principle of micro-programmed control unit of very simple CPU. How does horizontal microcode differ from vertical microcode? 7

7. Write short notes on **any two:** 2×5

a) VHDL

b) Cache memory

c) Compiling and Assembling Process

.

POKHARA UNIVERSITY

Level: Bachelor Semester – Spring Year : 2012
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain the assembling and compiling process with suitable examples. 7
   b) How a 16 X 2 memory subsystem can be constructed from two 8 x2 ROM chips with low-order interleaving? Explain. 8
2. a) What is RTL? Write the VHDL code for Full Adder 8
   b) Draw a state diagram for a Modulo6 counter and implement using the register. 7
3. a) Design a very simple CPU that has 6-bit address register (AR), 6-bit program counter (PC), 8-bit data register (DR) and 2-bit instruction register (IR). The CPU must execute the following instructions: 8

Instruction	Instruction Code	Operation
COM	00XXXXXX	AC ← AC'
AND	01AAAAAA	AC ← AC ^ M[AAAAAA]
JREL	10AAAAAA	PC ← PC+AAAAAA
SKIP	11XXXXXX	PC ← PC+1

Show the RTL code for the fetch and execute cycles for each instruction and draw the state diagram.

   b) Show the final register section and hardwired control unit for the same CPU. 7
4. a) Describe the microinstruction format? Explain the horizontal and vertical microcode. 7
   b) Write the RTL code for the shift subtraction division Algorithm. Using booth's algorithm to trace the multiplication of (4) and (2). 8

5. a) Explain different design issues of cache memory. 7

   b) Why do we use DMA? Explain DMA transfer mode with examples. 8

6. a) What are different measures to correct data conflict? Explain. 7

   b) What is parallelism? How Can it be achieved in uniprocessor system? 8

7. Write short notes on **any two:** 2×5

   a) Serial Communication

   b) Rs232-ch-8

   c) RISC VS CISC

POKHARA UNIVERSITY

Level: Bachelor Semester – Fall Year : 2013
Programme: B.E Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) What are the issues while designing an instruction set? Compare an assembling and compiling Process with an examples 7

   b) Design a 16 x 2 ROM memory using 8 x2 ROM in 8
   i) Higher order interleaving ii) Lower lever Interleaving.

2. a) Write a VHDL code for the Half Adder. 7

   b) Design a very simple CPU has the following instruction set and Show the RTL code for execute cycle of each Instruction 8

Instruction	Instruction Code	Operation
SUB	00AAAAAA	AC←AC - M[AAAAAA]
OR	01AAAAAA	AC←AC V M[AAAAAA]
AND	10AAAAAA	AC←AC ^M[AAAAAA]
DEC	11XXXXXX	AC←AC-1

3. a) From the above table also design the ALU and Hardwired control unit for the very simple CPU. 7

   b) Write do you mean by microinstruction? Describe the microinstruction format. 8

4. a) Explain the Hardware implementation of addition and subtraction algorithm 7

   b) Write the RTL code for the Shift Add Multiplication Algorithm. Use the same code to trace the multiplication of (3) and (4) 8

5. a) Describe how a 1KB cache is mapped directly with a 1MB Main Memory. Use suitable diagram to show the configuration and determine the tag and index. 8

   b) Describe the working principle of I/O Processors with suitable

diagram. 7

6. a) What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Describe the solutions to correct data conflicts 8

   b) What are the different topologies used to interconnect MIMD computers? Illustrate with suitable diagrams. 7

7. Write short notes on **any two:** 2×5

   a) UART's Internal Configuration

   b) Advance capabilities of VHDL

   c) Set Associative Mapping

POKHARA UNIVERSITY

Level: Bachelor Semester: Fall Year : 2014
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1.	a)	Explain the assembling and compiling process with suitable examples.	7
	b)	What is system bus? Explain in details.	8
2.	a)	A Computer system with an 8 bit address bus and an 8 bit data bus using isolated I/O. It has 16x8 ROM starting at the address 00H constructed using 8x8 chips; 64x8 of RAM starting at address 80 H constructed using 64x4 chips. There is an I/O device at 40 H. Show the design for the system.	8
	b)	How a 16×2 memory sub system can be constructed from two 8×2 ROM chip with low order interleaving and high order interleaving. Explain with diagram.	7
3.		Design a CPU that meets the following specification: It can access 64 bytes of memory each 8 bit wide. The CPU does this by outputting a 6 bit address on its output pin A{5…0}and reading 8 bit value from memory on its input D{7…0}.	15
4.	a)	Describe the microinstruction format? Explain the horizontal and vertical micro code.	7
	b)	Write the RTL code for Booth's algorithm. Using same code trace the multiplication of (-5) and (3).	8
5.	a)	Show the layout of the cache for a CPU that can address 1M x 16 of memory; the cache holds 8k x 16 of data and has the following mapping strategies. Given the number of bits per location and total number of locations as well. i. Fully Associative ii. Direct Mapped iii. Two – way associative	8

b) Describe the working principle of DMA with suitable diagram. 7

6. a) What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Describe the solutions to correct data conflicts. 8 7

b) Describe different types of topologies of multiprocessor system.

7. Write short notes on: (**Any two**) 2×5

a) BCD Numeric Addition

b) DMA

c) VHDL

POKHARA UNIVERSITY

Level: Bachelor Semester: Spring Year : 2014
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain the basic computer and CPU organization with the help of block diagram. 7

   b) Describe the assembly process for assembly-language programs. How does it differ from the compilation process? 8

   OR

   What do you mean by Instruction Set Architecture? What are the major issues to be considered while designing an Instruction Set Architecture?

2. a) Differentiate with suitable example(**any one**): 7

      i. Linear and multiple dimensional organizations of chips.

      ii. Higher order interleaving and lower order interleaving.

   b) What is RTL? Write the RTL for shift operations. Design a 4-bit circular right shifting circuit. 8

3. a) What are the different topologies used to interconnect MIMD computers? Describe with suitable diagrams. 5

   b) For a very simple CPU with the following instruction sets: 10

Instruction	Operation	Instruction code
ADD AAAAAA	AC←AC+M[AAAAAA]	00AAAAAA
AND AAAAAA	AC←AC^M[AAAAAA]	01AAAAAA
COM	AC←AC`	10XXXXXX
OR AAAAAA	AC←AC^{V}M[AAAAAA]	11AAAAAA

      i. Describe specifications and draw State diagram.

      ii. Design ALU and Register set.

4. a) Differentiate between Segmentation and Paging? Describe the four most common replacement algorithms related to design issues of cache memory? 8

   b) Explain the generation of micro-operation using horizontal as well as vertical microcode. Write two ways to reduce number of micro-instruction. 7

5. a) Write the RTL code for the booth's Algorithm. Using the same code to trace the multiplication of (-5) and (4). 7

   b) What are the major conflicts occurring due to instruction pipelining in RISC? Explain. Also describe what the solutions to correct those conflicts are. 8

6. a) Differentiate Serial and Parallel Communication? Describe 4 different modes of asynchronous data transfer. 7

   b) What is memory hierarchy? Explain the importance of cache memory and virtual memory in the hierarchy. 8

7. Write short notes on: (**Any two**) 2×5

   a) DMA.

   b) Cache Coherence.

   c) Instruction Formats.

POKHARA UNIVERSITY

Level: Bachelor Semester: Fall Year : 2015
Programme: BE Full Marks: 100
Course: Computer Organization and Architecture Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Describe the assembly process for assembly-language programs. How does it differ from the compilation process? 8
   b) How a 16 X 2 memory subsystem can be constructed from two 8 x2 ROM chips with low-order interleaving? Explain. 7
2. a) Design a very simple CPU that has 6-bit address register (AR), 6-bit program counter (PC), 8-bit data register (DR) and 2-bit instruction register (IR). The CPU must execute the following instructions: 8

Instruction	Instruction Code	Operation
COM	00XXXXXX	AC $\leftarrow$ AC'
AND	01AAAAAA	AC $\leftarrow$ AC $\wedge$ M[AAAAAA]
JREL	10AAAAAA	PC $\leftarrow$ PC+AAAAAA
SKIP	11XXXXXX	PC $\leftarrow$ PC+1

   b) Explain the different sections of VHDL design code. Write VHDL code for D-Flip-flop. 7
3. a) A computer system with an 8-bit address bus and an 8-bit data bus uses isolated I/O. It has 128 bytes ROM starting at address 00H constructed using 32×8 chips; 64 bytes of RAM starting at address 80H constructed using 64×4 chips. Show the design for this system. 8
   b) Multiply $(4)_{10}$ by $(-2)_{10}$ by using Booth's algorithm. 7
4. a) What are the significance of cache memory? Write different types of mapping technique. 7
   b) Differentiate between Segmentation and Paging? Describe the four 8

most common replacement algorithms related to design issues of cache memory?

5. a) How DMA controller can be incorporated in a computer system? 8
   b) Explain major set of design principles related to RISC architecture. Calculate the window size and total number of registers. Given: No. of Global registers=10, No. of Local registers=10, No. of common registers=6, No. of windows=4. 7

6. a) What is an interrupt? How is an interrupt serviced? Explain software actions in interrupt handling. 8
   b) Define Mesh Topology. Describe different memory organization of multiprocessor system. 7

7. Write short notes on: (**Any two**) 2×5
   a) MIMD Architecture.
   b) Arithmetic pipelining.
   c) Register Windows.