Computer Organization and Architecture Laboratory (CS39001)

Expt. on Integer Arithmetic

Design an 8 bit radix-4 Booth's multiplier. Carry out the following steps:

1. Day 1: Submit the RTL level ASM chart for the algorithm.

2. Datapath design – Assume that only a two's complement adder / subtractor with inputs X and Y are available; clearing, incrementation, decrementation, etc. of registers can be carried out locally around the registers themselves; a separate $M/2M$ circuit is to be designed which takes as input an operand M and produces as output either M or $2M$ depending on a control input, $selM/\overline{2M}$, say; shift-operations are to be achieved by hardwired interconnection. Suitable status detection circuits can be used locally around the registers as required by the algorithm.
   Day 1: Submit the datapath internal schematic diagram with the data and control signals with the environment and the controller depicted clearly.

3. Controller design:
   Day 1: Submit the signal level ASM chart of the controller.

4. Encoding of the controller and the datapath design:
   Day 2: Submit a Verilog structural encoding of the controller with a (behavioural encoding of a) test harness. Show its operation through simulation.
   Day 3 : Submit

   (a) Behavioural encoding of the adder / subtractor and the registers,
   (b) Structural encoding of
      i. the $M/2M$ circuit,
      ii. the status detectors and
      iii. interconnection of the datapath

   Show the operation of the complete circuit with a test harness which is to ascertain the inputs so that all the required operations are being performed under the influence of appropriate control signals; it should also be able to monitor the status line outputs of the datapath.

5. Day 3: Submit a single Verilog module comprising the encodings of the datapath, controller and the test harness after testing it fully on the FPGA kit.

Submersibles

1. ASM chart, datapath paper design, datapath diagram, signal level ASM chart of the controller in Lab report

2. Structural encoding of the controller with the test harness on the Moodle course site,

3. Encoding of the total module with the corresponding test harness on the Moodle course site,

Marking guidelines

1. ASM diagram — 5

2. Datapath diagram and datapath controller-FSM interface diagram – 10

3. controller FSM diagram – 5

4. Encoding:

   (a) Controller structural encoding with test harness and its operation demonstrated — 10
   (b) Datapath encoding – 15
   (c) Complete module with test harness and its operation demonstrated – 15

   Total Marks – 60