

COL380

Introduction to
Parallel & Distributed Programming

Agenda

- Understanding memory consistency

Memory Model

@atom

Address space

Memory Model

- Register size?
- Limit on the number of readers and writers?
- Asynchronous reads and writes
 - ➔ Global knowledge of 'time?'

 Register

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“Most recent Write”

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- Increasing power \Rightarrow reducing performance

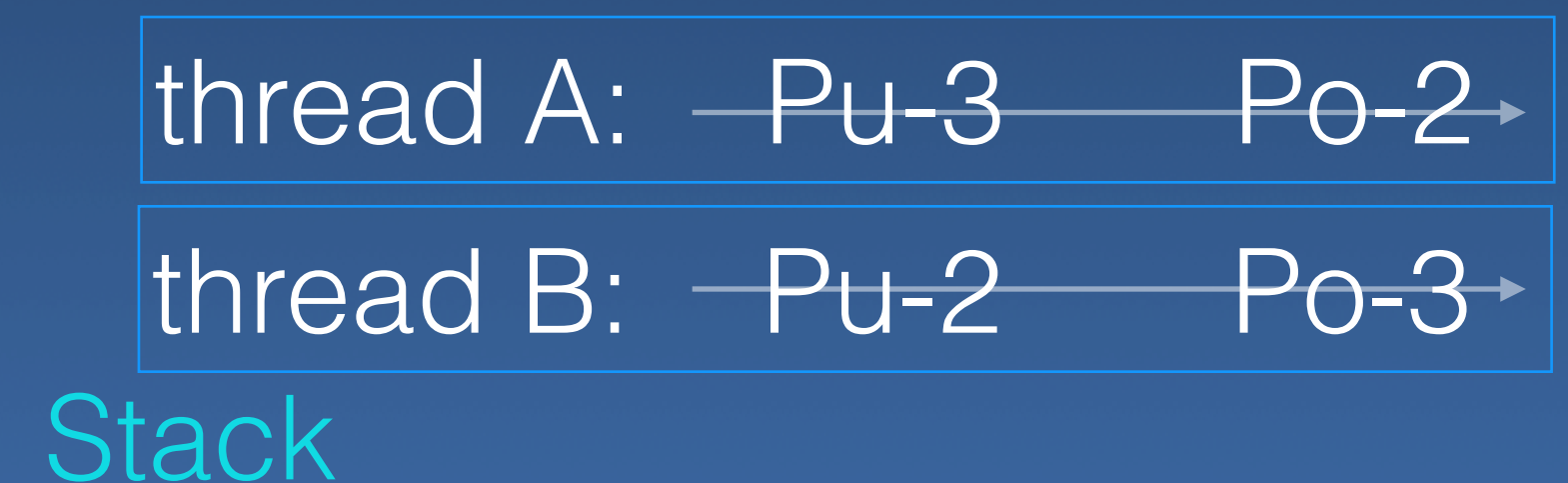
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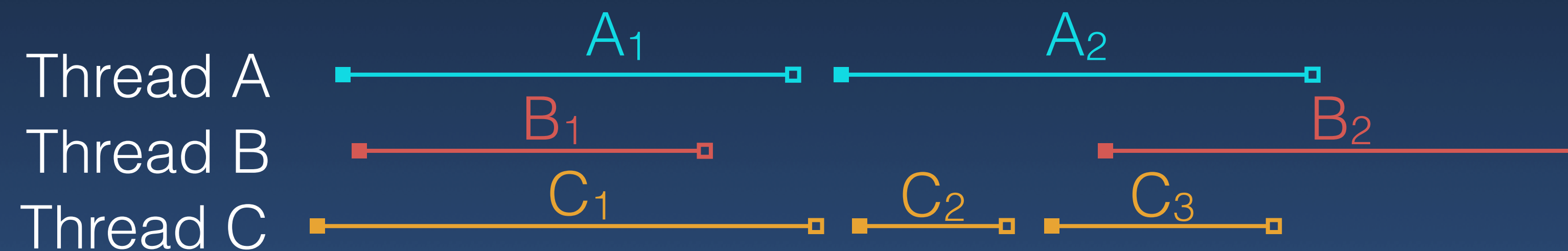
 Register

Same ideas apply to higher level data structures



Linearizable

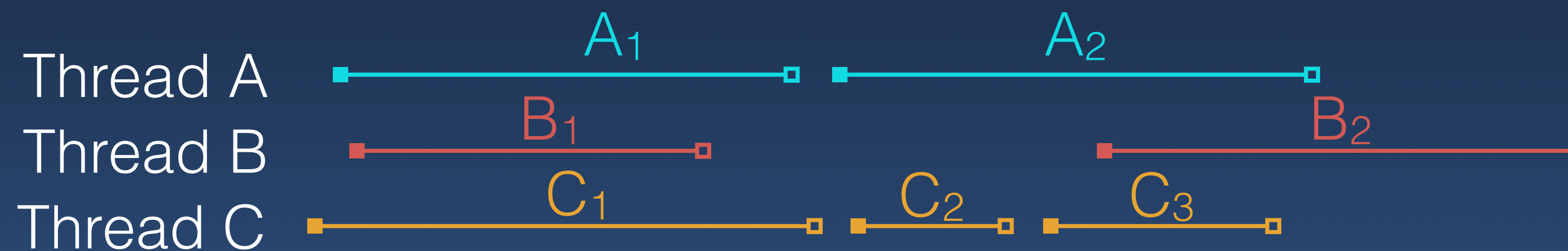
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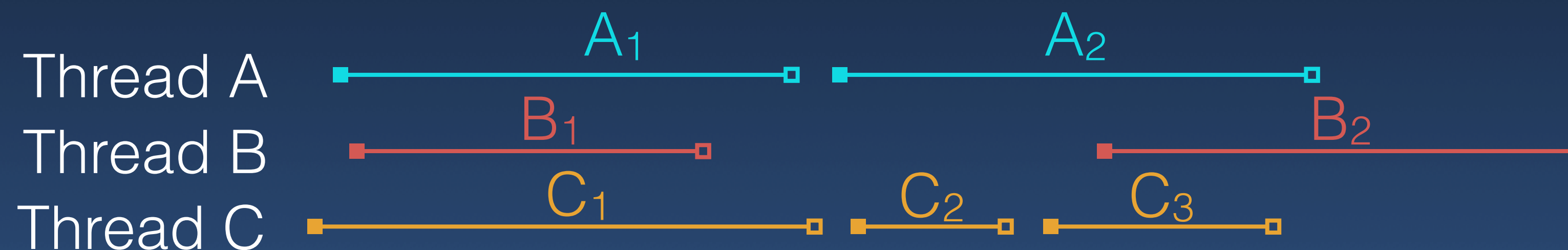


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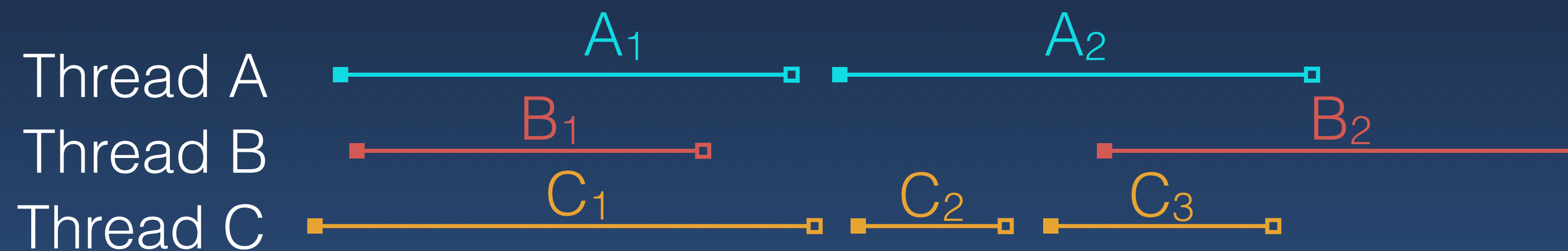


Equivalent sequential history S exists: A1, C1, B1, C2, B2, C3, A2

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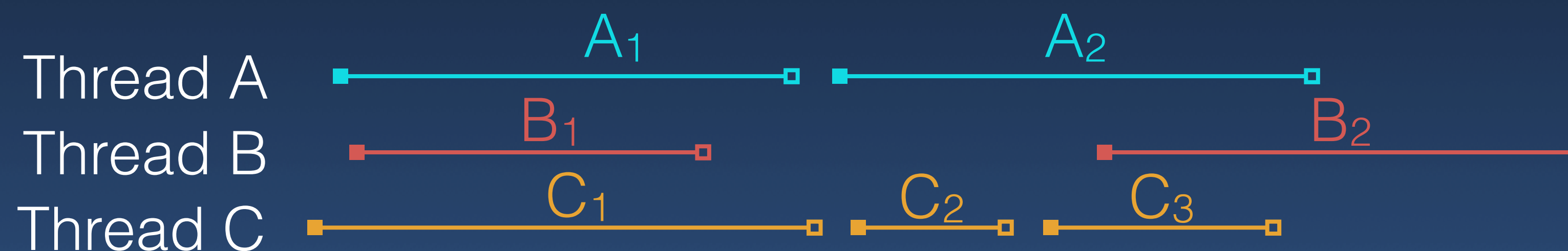
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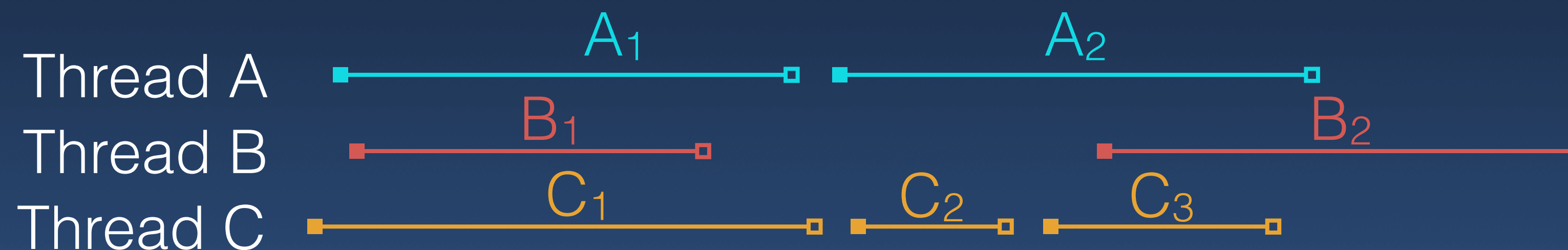
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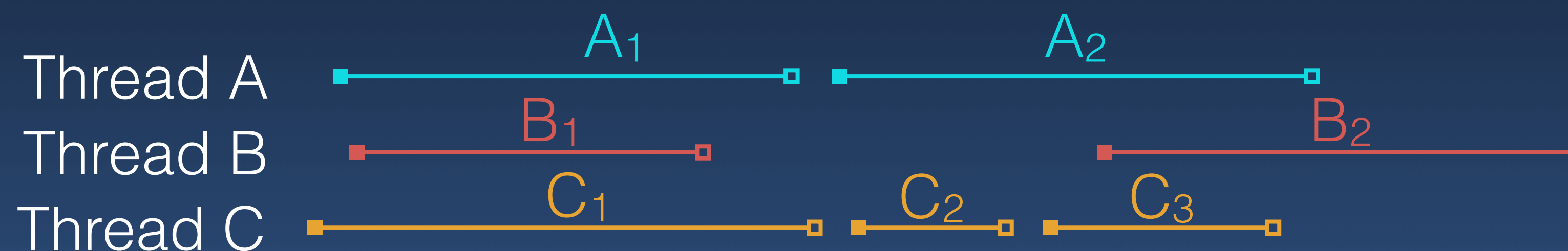
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Linearizability is Composable

Types of Registers

- Linearizable registers
 - ➔ SRSW 1-bit safe register
 - ➔ MRMW n-bit atomic linearizable register
- Sequentially consistent registers
- Causally consistent registers
- FIFO consistent registers
- Weakly consistent registers

- “A multiprocessor is sequentially consistent if the result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program.” [Lamport, 1979]

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Weaker than Linearizability

Sequentially Consistent

Thread A: 

Thread B:   

- No global notion of time
 - Only consistent Order

Sequentially Consistent

Thread A:  EnQ(5)

Thread B:

 EnQ(3)

 DeQ is 3

 DeQ is 5

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Thread A: $A_1 \longrightarrow A_2$

Thread B: $B_1 \longrightarrow B_2$

Thread C: $C_1 \longrightarrow C_2 \longrightarrow C_3$

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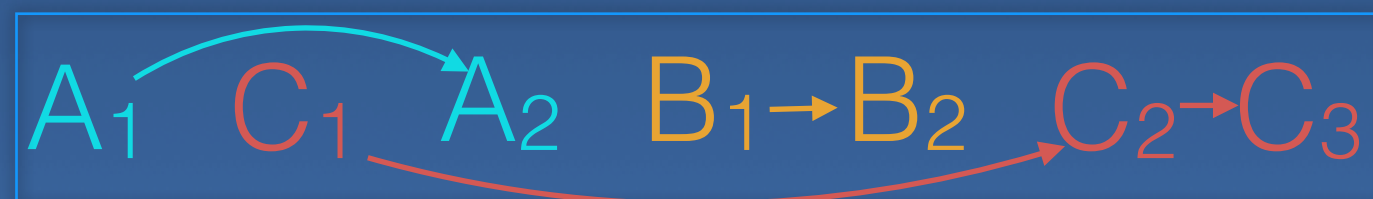
Thread B: $B_1 \longrightarrow B_2$

Thread C: $C_1 \longrightarrow C_2 \longrightarrow C_3$

Sequential History

$A_1 \rightarrow A_2$ $C_1 \rightarrow C_2 \rightarrow C_3$ $B_1 \rightarrow B_2$

A_1 C_1 A_2 $B_1 \rightarrow B_2$ $C_2 \rightarrow C_3$

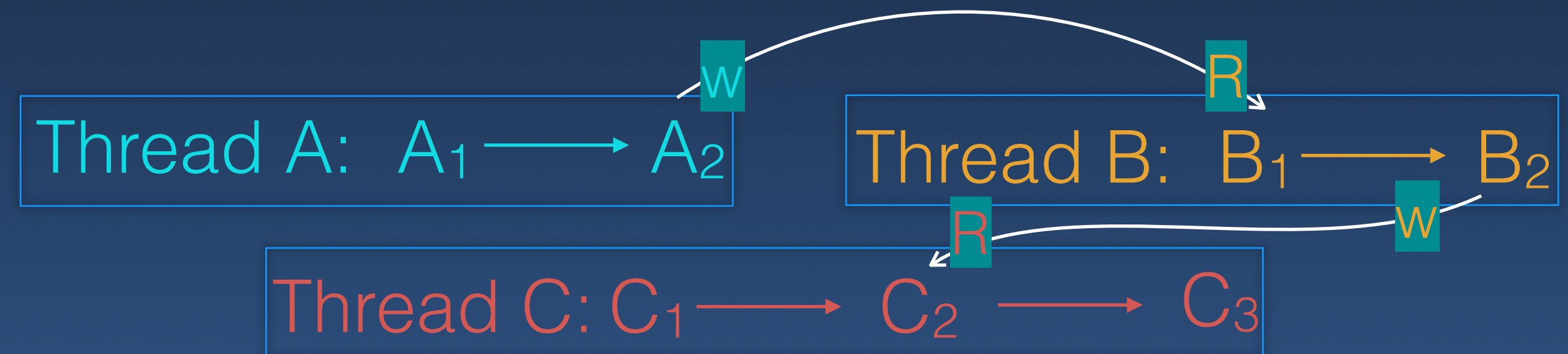


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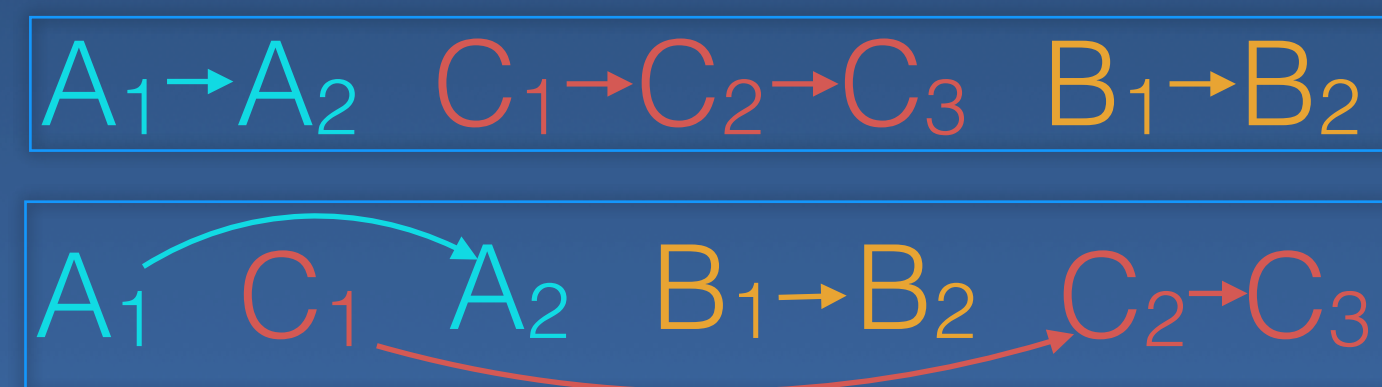
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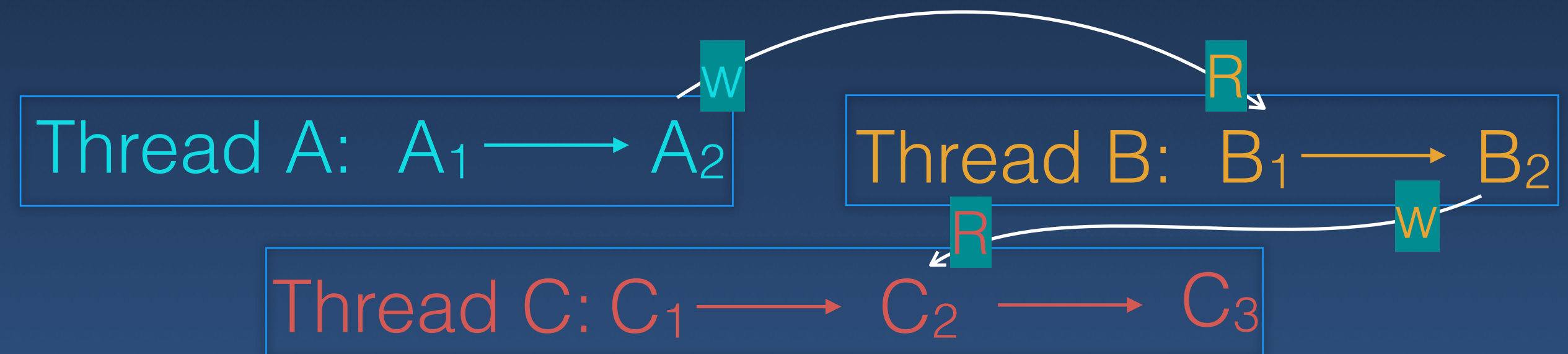
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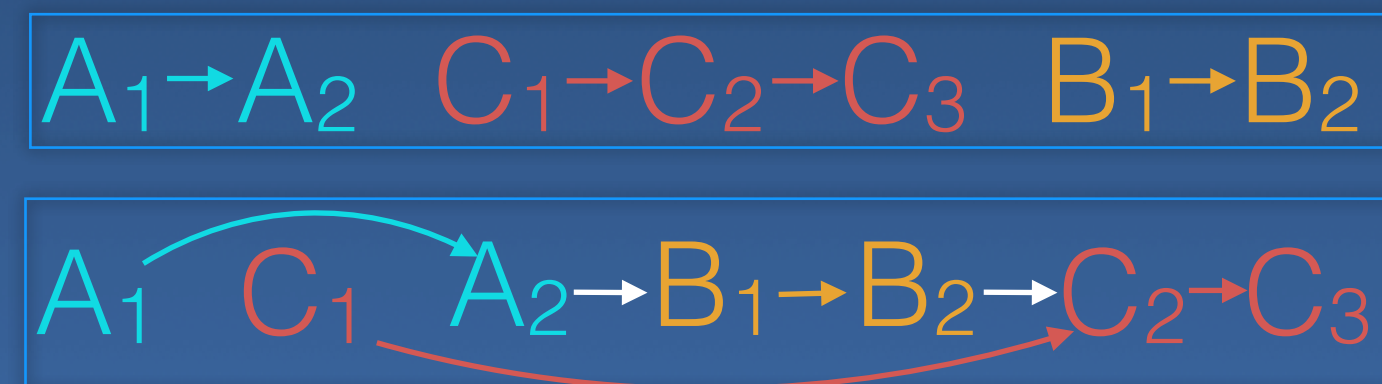
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Sequential History



Sequentially Consistent

Thread A: 

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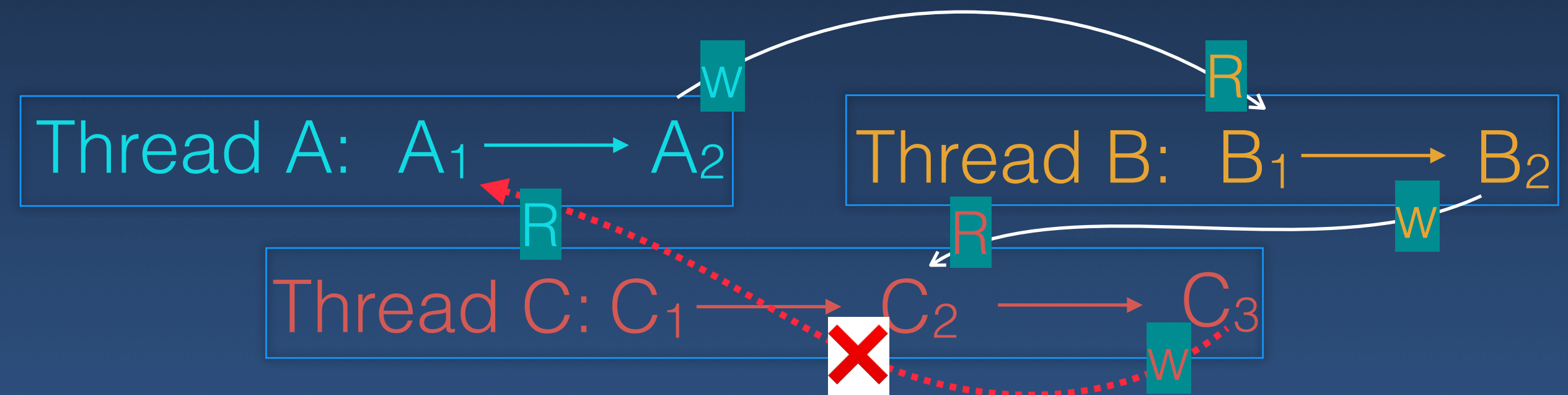
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Sequential History

$A_1 \rightarrow A_2 \quad C_1 \rightarrow C_2 \rightarrow C_3 \quad B_1 \rightarrow B_2$

$A_1 \xrightarrow{\text{blue}} A_2 \xrightarrow{\text{red}} B_1 \rightarrow B_2 \rightarrow C_2 \rightarrow C_3$

A: $(x=3) \longrightarrow (x=5)$

B: $[\text{read } x]3$

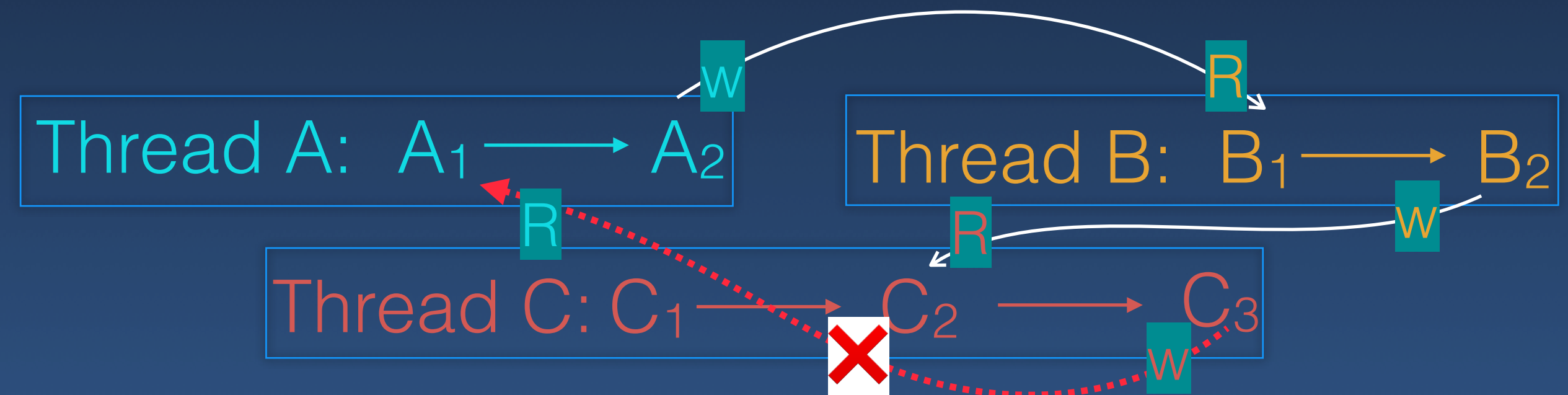
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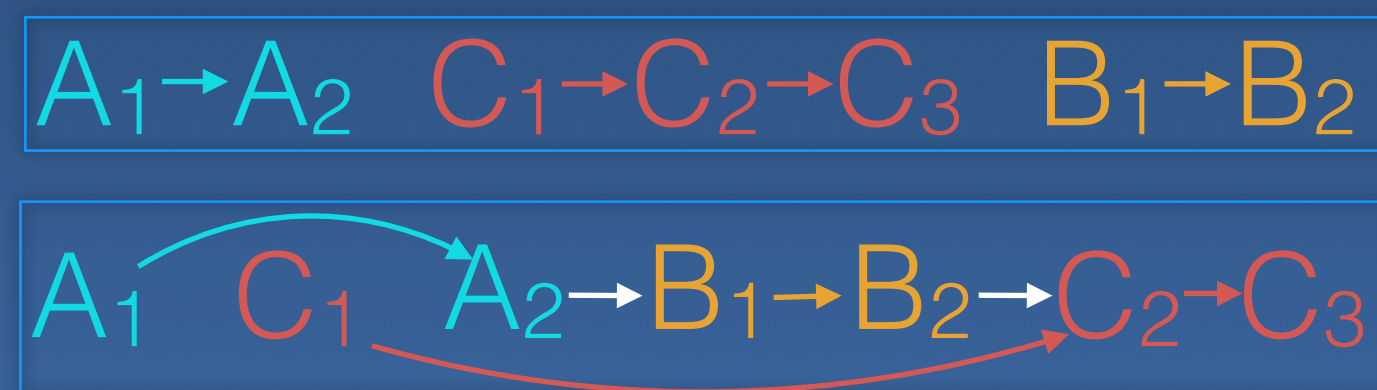
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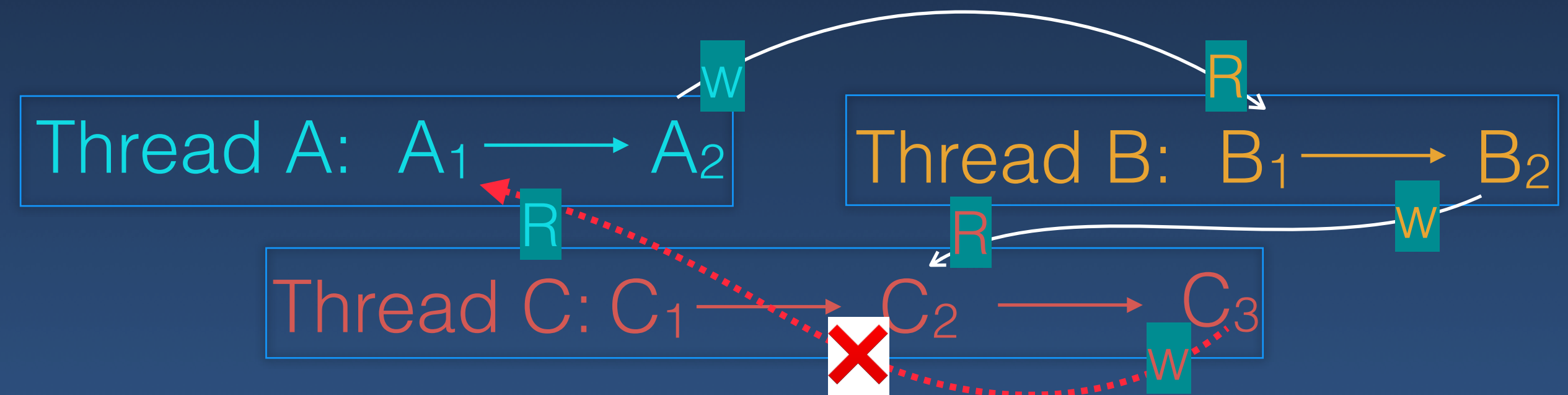
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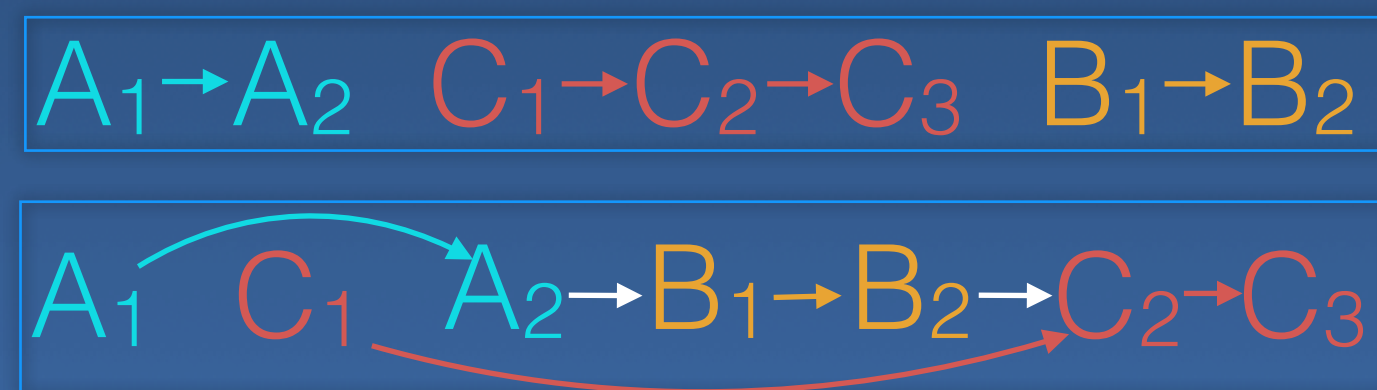
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Sequential History



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- Threads always see values written by some thread
 - ➔ No garbage Update is atomic
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initially: ready=0, data=0

thread A

thread B

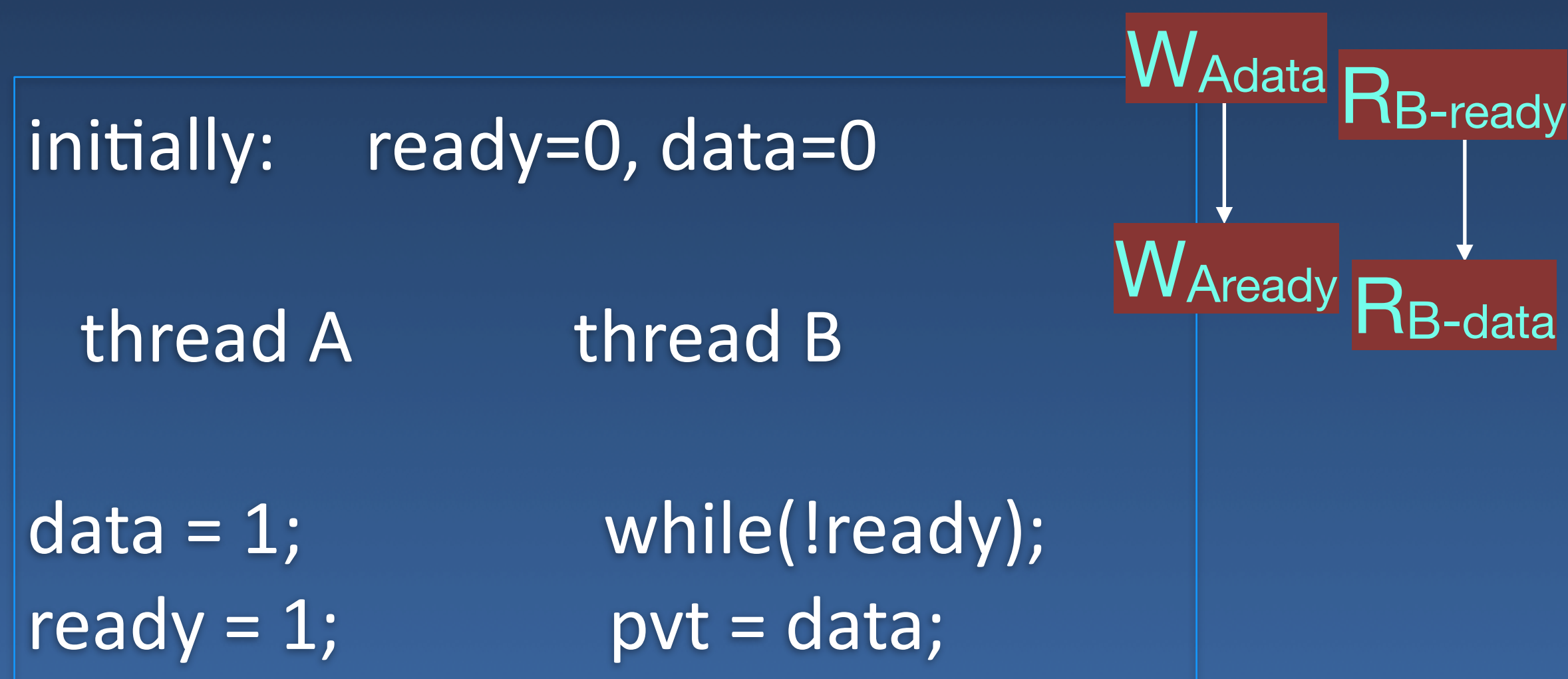
```
data = 1;  
ready = 1;
```

```
while(!ready);  
pvt = data;
```

Need: If B sees the new value of ready (1),
B must also see the new value of data (1)

Memory Consistency Semantics

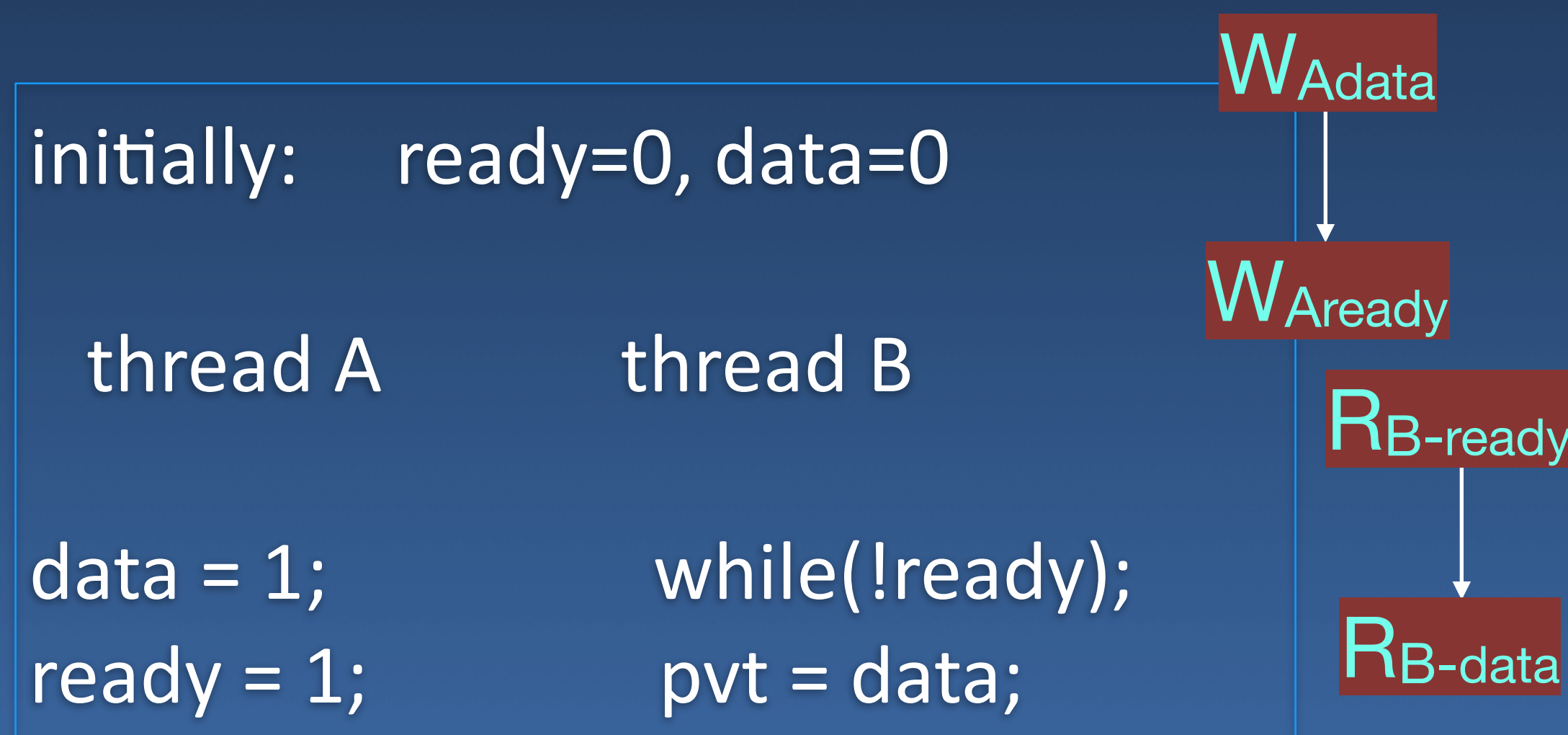
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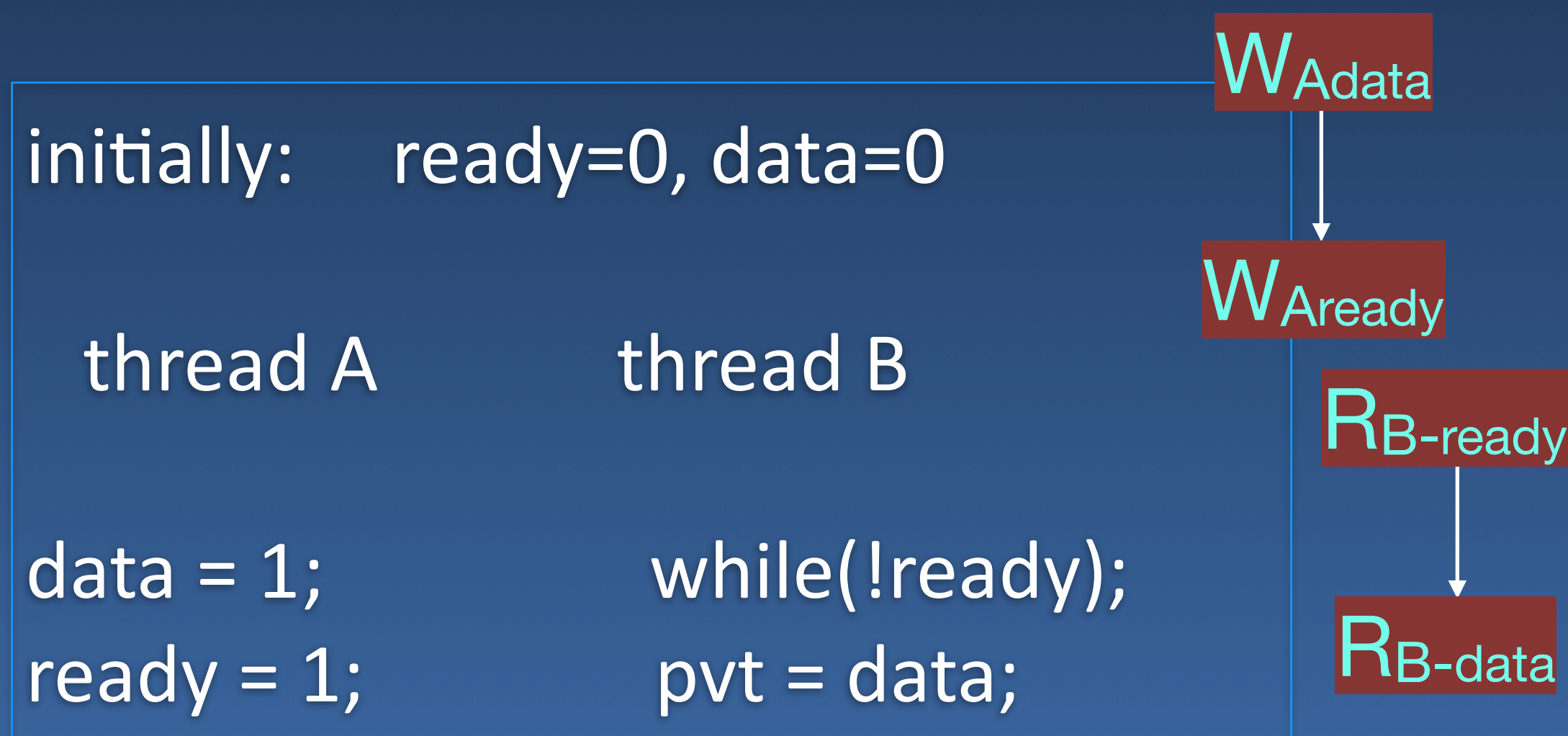
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If B sees ready =	then B may see data =
0	1
0	0
1	1

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- Linearizability
- Sequential Consistency