

Aayushi Vaish

+91-7906248323

aayushi.vaish.2016@gmail.com

<https://aayushivaish.github.io/>

Research Interests	Rich experience as electronics and communications engineer with focus on creating advanced systems for spectroscopic analysis of extra-solar planets and finding methods to understand the conditions of the planets revolving around black holes.
Education	<i>Bachelor of Technology in Electronics and Communications Engineering</i> Aug. 2016 - Sep. 2020 JSS Academy of Technical Education (Dr. A. P. J. Abdul Kalam Technical University), Noida, Uttar Pradesh CGPA: 7.92/10.0
Awards and Honors	Excellent performance in quiz competition on “Astronomy and Astrophysics” by Zenith Astronomy Club. 2020 Won a Bronze medal in Monochrome sketching to raise awareness for COVID-19 by AIIMS New Delhi. 2020 Qualified the pre-final round of International Astronomy and Astrophysics Competition. 2020 Recognized for being an active collaborator with Entrepreneurship Development Cell at JSSATEN. 2016 Recognized for excellent academic performance . 2012
Work Experiences	<i>Satellite Communications - Trainee at Ultra Tech Cements</i> June 2019 - Jan 2020 <ul style="list-style-type: none">Analyzed one-way data broadcasting and two-way interactive communications using radio waves as medium.Implemented Very Small Aperture Terminal and VSAT Services.Performed site survey to determine satellite Look Angle and the location for ODU with "look angle" clearance. <i>Transmission Management Trainee at Bharat Sanchar Nigam Limited</i> June 2018 - December 2018 <ul style="list-style-type: none">Provided insights in deployment of Optical Fiber for faster communication.Performed ground tests on various Optical Fiber Laying Methods.Researched on the role of Optical Fiber in 5G communications.
Projects Undertaken	<i>Design and Implementation of a 16-bit RISC Processor Using Verilog HDL</i> <ul style="list-style-type: none">A 16-bit RISC Processor was designed and implemented using Verilog HDL with the help of XILINX 14.2 and ISIM simulator. The purpose of this project was to learn digital designing using XILINX software and to implement what I have studied in my previous courses related to Computer Architecture and Digital Electronics. <i>Smart Attendance System for Employees using face detection and ML with Python</i> <ul style="list-style-type: none">In this project initially the details and sample pictures of employees working in a sample organization were stored. For each employee around 10 pictures were used to create training data model. Once the AI is trained with new data model, if a face is recognized by it then attendance is marked for corresponding employee and saved in a CSV file along with other necessary details.
Skills	<ul style="list-style-type: none">Programming languages: Python, C++Libraries: OpenCV, Numpy, Pandas, TensorFlowOperating systems: Mac OS, Linux, WindowsSoftware: LaTeX, Git