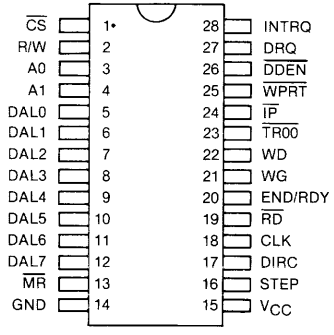
ADVANCED INFORMATION

WD1773 5¼" Floppy Disk Controller/Formatter

FEATURES

- 100% SOFTWARE COMPATIBILITY WITH WD1793
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- SINGLE (FM) AND DOUBLE (MFM) DENSITY
- 28 PIN DIP, SINGLE +5V SUPPLY
- TTL COMPATIBLE INPUTS/OUTPUTS
- 128, 256, 512 OR 1024 SECTOR LENGTHS
- 8-BIT BI-DIRECTIONAL HOST INTERFACE



PIN DESIGNATION

DESCRIPTION

The WD1773 is an MOS/LSI device which performs the functions of a 5¼" Floppy Disk Controller/Formatter. It is fully software compatible with the Western Digital WD1793-02, allowing the designer to reduce parts count and board size on an existing WD1793 based design without software modifications.

With the exception of the enable Precomp/Ready line, the WD1773 is identical to the WD1770 controller. This line serves as both a READY input from the drive during READ/STEP operations, and as a Write Precompensation enable during Write operations. A built-in digital data separator virtually eliminates all external components associated with data recovery in previous designs.

The WD1773 is implemented in NMOS silicon gate technology and is available in a 28 pin, dual-in-line package.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enable Host communication with the device.
2	READ/WRITE	R/$\overline{W}$	A logic high on this input controls the placement of data on the $\overline{D0}$-$\overline{D7}$ lines from a selected register, while a logic low causes a write operation to a selected register.
3,4	ADDRESS 0,1	A0, A1	These two inputs select a register to Read/Write data: $\overline{CS}$ A1 A0 R/$\overline{W}$ = 1 R/$\overline{W}$ = 0 0 0 0 Status Reg Command Reg 0 0 1 Track Reg Track Reg 0 1 0 Sector Reg Sector Reg 0 1 1 Data Reg Data Reg
5-12	DATA ACCESS LINES 0 THROUGH 7	DAL0-DAL7	Eight bit bidirectional bus used for transfer of data, control, or status. This bus is enabled by $\overline{CS}$ and R/$\overline{W}$. Each line will drive one TTL load.
13	MASTER RESET	$\overline{MR}$	A logic low pulse on this line resets the device and initializes the status register.
14	GROUND	GND	Ground.
15	POWER SUPPLY	V_{CC}	+5V ±5% power supply input.
16	STEP	STEP	The Step output contains a pulse for each step of the drive's R/$\overline{W}$ head. The WD1770 and WD1772 offer different step rates.
17	DIRECTION	DIRC	The Direction output is high when stepping in towards the center of the diskette, and low when stepping out.
18	CLOCK	CLK	This input requires a free-running 50% duty cycle clock (for internal timing) at 8 MHZ ± 1%.
19	READ DATA	$\overline{RD}$	This active low input is the raw data line containing both clock and data pulses from the drive.
20	ENABLE PRECOMP/ READY LINE	ENP/RDY	Serves as a READY input from the drive during READ/STEP operations and as a Write Precomp enable during write operations.
21	WRITE GATE	WG	This output is made valid prior to writing on the diskette.
22	WRITE DATA	WD	FM or MFM clock and data pulses are placed on this line to be written on the diskette.
23	TRACK 00	$\overline{TR00}$	This active low input informs the WD1770 that the drive's R/$\overline{W}$ heads are positioned over Track zero.
24	INDEX PULSE	$\overline{IP}$	This active low input informs the WD1770 when the physical index hole has been encountered on the diskette.
25	WRITE PROTECT	$\overline{WPRT}$	This input is sampled whenever a Write Command is received. A logic low on this line will prevent any Write Command from executing.
26	DOUBLE DENSITY ENABLE	$\overline{DDEN}$	This input pin selects either single (FM) or double (MFM) density. When $\overline{DDEN}$ = 0, double density is selected.

PIN DESCRIPTION (CONTINUED)

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
27	DATA REQUEST	DRQ	This active high output indicates that the Data Register is full (on a Read) or empty (on a Write operation).
28	INTERRUPT REQUEST	INTRQ	This active high output is set at the completion of any command or reset a read of the Status Register.

See page 481 for ordering information.

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WD1770/72/73 5¼" Floppy Disk Controller/Formatter Family Application Notes

INTRODUCTION

To meet the demand for a low cost compact LSI Floppy Disk Controller device, Western Digital has developed the WD1770. The WD1770 is a NMOS floppy disk controller device for 5¼" drives that incorporates the FD179X, a digital data separator and write precompensation circuitry all in a single chip. The device offers soft sector formatting, selectable stepping rates, automatic track seek with verify, and variable sector lengths. The FD1770 comes in a 28-pin dual-in-line package and operates from a single 5 volt only power supply.

APPLICATIONS

The mini-floppy controller is targeted for the low cost sector of the disk drive market, where digital data separation is preferred over analog phase lock loop. Included in this market are Personal Computers, Portable Computers and Small Business Computers.

FOLLOW ON DEVICES

WD1772

The device will be the same as the WD1770 except for increased stepping rates of 2, 3, 5 and 6ms.

WD1773

The device will be the same as the WD1770 except that it will be totally software compatible with the FD179X (No motor on feature).

HOST INTERFACING

Interfacing to a host processor is accomplished through the eight bit bidirectional Data Access Lines (DAL) and associated control lines. The DAL is used to transfer data, status and control words out of or into WD1770. The DAL having three states enabled as an output when Chip Select ($\overline{CS}$) is active low and Read/$\overline{Write}$ (R/$\overline{W}$) is high or as input receiver when $\overline{CS}$ and R/$\overline{W}$ is low. When transfer of data with the device is required by the host $\overline{CS}$ is made low. The address bits A0 and A1 combined with the R/$\overline{W}$ line select the register and direction of data.

During Direct Memory Access (DMA) data transfers between the WD1770 and Host Memory, the Data Request (DRQ) line is used in Data Transfer Control. This signal also appears as status bit 1 during Read/Write operations. On Disk Read operations the DRQ is active when an assembled byte is present in the Data Register, then reset when read by the Host. If the Host fails to read the Data register before the following byte is assembled in the data register the lost data bit is set in Status Register.

At the completion of every command INTRQ is generated. INTRQ is reset by either reading the status or by loading the command register. (After any register is written to the same register cannot be read from until 16μsec in MFM or 32μsec in FM have elasped.)

DISKETTE DRIVE INTERFACING

The WD1770 has two modes of operation depending on the state of DDEN, regardless of the state DDEN the CLK input remains at 8 MHz. Disk Reads with sector lengths of 128, 256, 512 and 1024 byte sector in both FM or MFM from 5¼" diskettes is accomplished via the internal digital data separator. Disk Write operation in MFM on inner tracks may require write precompensation. Write precompensation is enabled when bit 1 = 0, in the write command and a precompensation value of 125 ns will be produced.

The diskettes spindle motor is controlled by bit 3 of any Type I, II or III command, upon receiving a command with bit 3 = 0, the spin up sequence is enabled.

GENERAL INFORMATION

A +5 volt supply ±5% should be used as V_{CC}, and the clock input requires a free running 50% duty cycle at 8 MHz ± 1%.

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