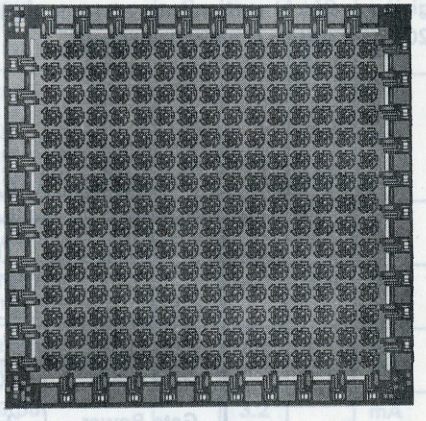
FERRANTI semiconductors

ULA 2000 Series

The 225 Cell Uncommitted Array Family

FEATURES

- Single mask custom integration
- Single supply voltage
- TTL and CMOS compatible
- Low Power Schottky TTL performance
- 2200 uncommitted components
- Digital and linear functions
- Improved system reliability
- Improved system performance
- Reduced system assembly costs
- Reduced system space and power
- Reduced system testing costs
- Rapid development time scale
- Easy layout rules for customer designing
- Suitable for battery powered equipment



Uncommitted Array

DESCRIPTION

This Uncommitted Logic Array Family provides a range of three types; Low Power, Standard and High Speed.

Each array comprises 225 uncommitted cells of three transistors and five resistors arranged in a regular matrix, and 40 peripheral interface cells all contained on a chip size of 131 mils square. The array is processed and held in stock as a standard product, complete except for the final aluminium interconnection pattern. On receipt of a customer's system requirements, a specific interconnection pattern is generated which connects the individual components within each cell to construct the circuit functions, and at the same time provides the overall system integration.

In addition to the typical logic system requirements of gates, counter and register elements, the individual components in each cell can be connected to form linear circuit functions such as operational amplifiers, oscillators, schmitt triggers, etc., thus allowing a L.S.I. combination of digital and linear functions to be achieved.

FAMILY TYPES

The Standard Array (STA) has a typical dissipation of 500 mW for a 200 gate system and is suitable for systems with operating speeds of up to 3 MHz or where precise linear circuits such as oscillators, amplifiers or comparators are required.

The Low Power Array (LPA) has a typical dissipation of 50 mW for a 200 gate system and is suitable for systems operating at speeds of up to 250 kHz. It is therefore ideal for battery powered equipment.

The High Speed Array (HSA) has been optimised for Low Power Schottky TTL compatibility giving a typical performance of 10 ns gate delay and 10 MHz clock rate. The dissipation of a 200 gate system is typically 650 mW.

TYPICAL ARRAY CHARACTERISTICS

UNITS	HSA	STA	LPA
R_L	8.0 kΩ	10 kΩ	120 kΩ
R_{IN}	2.4 kΩ	10 kΩ	120 kΩ
Gate Delay	10 ns	25 ns	200 ns
Gate Power	2.5 mW	2 mW	0.2 mW
Clock Rate	10 MHz	3 MHz	250 kHz
V_{CC}	5V	5V	5V
I_{CC}	130 mA	100 mA	10 mA

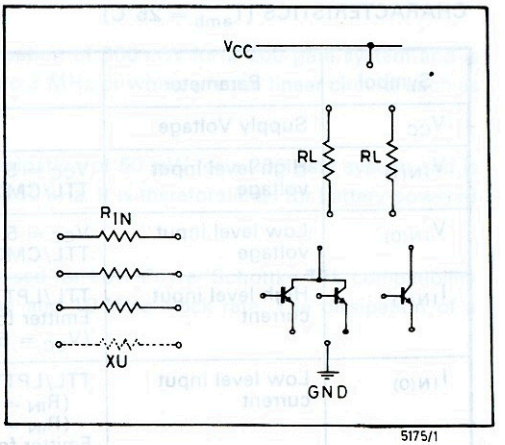
ABSOLUTE MAXIMUM RATINGS	
Supply Voltage V_{CC}	+7.0V max. −0.5V min.
Input Voltage V_{IN}	+5.5V max. −0.5V min.
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.0	5.0	5.5	V
$V_{IN(1)}$	High level input voltage	V_{CC} = 5.0V TTL/CMOS interface	2.0		5.5	V
$V_{IN(0)}$	Low level input voltage	V_{CC} = 5.0V TTL/CMOS interface	0		0.8	V
$I_{IN(1)}$	High level input current	TTL/LPTTL input. Emitter follower input (V_{CC} = 5.0V, fan out = 5)	0 0		40 40	µA µA
$I_{IN(0)}$	Low level input current	TTL/LPTTL input (R_{IN} = 20 kΩ) (R_{IN} = 4 kΩ) Emitter follower input (V_{CC} = 5.0V, fan out = 5)	0 0 0		–0.36 –1.6 40	mA mA µA
$V_{OUT(1)}$	High level output voltage	TTL/CMOS interface (I_{OUT} = –80 µA)	2.4			V
$V_{OUT(0)}$	Low level output voltage	TTL/CMOS interface (I_{OUT} = 3.2 mA)			0.5	V
$I_{OUT(1)}$	High level output current	TTL/CMOS output High current drive output		80 40		µA mA
$I_{OUT(0)}$	Low level output current	TTL/CMOS output Full fan out TTL output High current sink output		3.2 16 40		mA mA mA
tpd F_{IN} I_{CC}	*HSA* Gate delay Clock frequency Supply current	V_{CC} = 5.0V, 200 active gates 20 active gates		10 10 130 13		ns MHz mA mA
tpd F_{IN} I_{CC}	*STA*	V_{CC} = 5.0V, 200 active gates 20 active gates		25 3 100 10		ns MHz mA mA
tpd F_{IN} I_{CC}	*LPA*	V_{CC} = 5.0V, 200 active gates 20 active gates		200 250 10 1		ns kHz mA mA

ARRAY COMPONENTS

INTERNAL CELL
(225 per Array)



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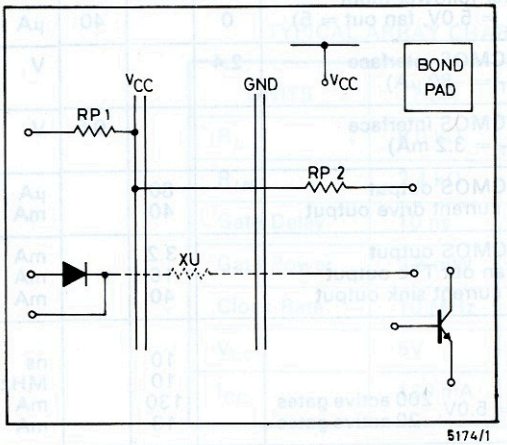

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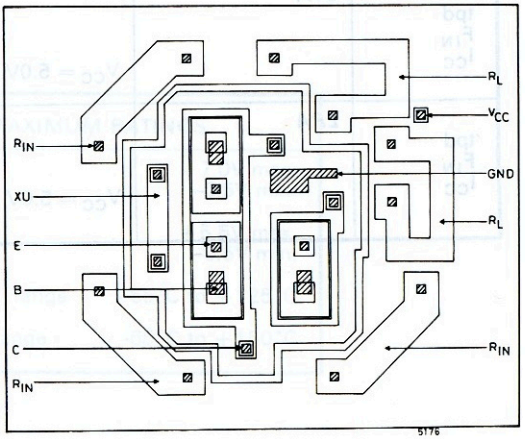
INTERFACE CELL
(40 per Array)

INTERNAL CELL LAYOUT



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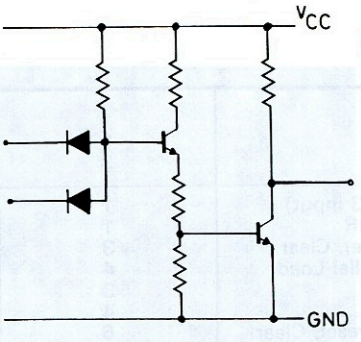
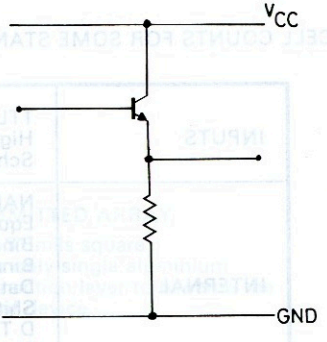
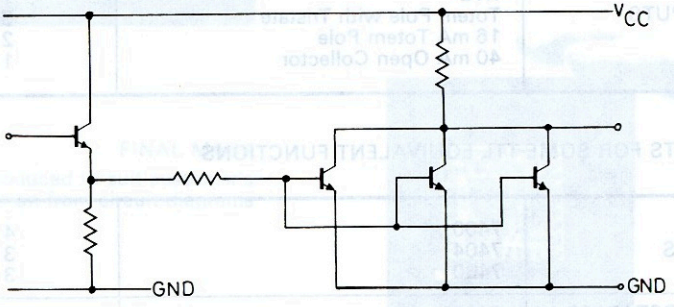
Some examples of input/output interface circuits which can be implemented with either internal or interface cell components.



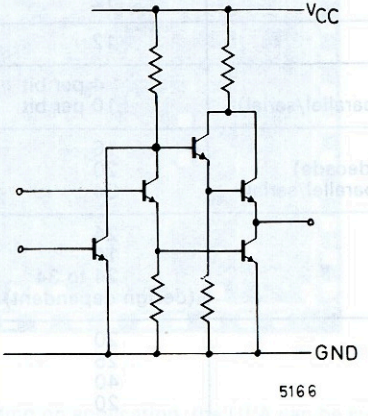
TTL/LPTTL INPUT



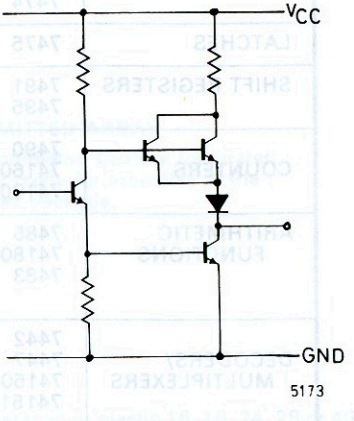
EMITTER FOLLOWER INPUT



HIGH CURRENT OUTPUT



TRISTATE OUTPUT



TOTEM POLE OUTPUT

The following list gives an indication of the number of cells which may be interconnected to produce some commonly used circuit configurations.

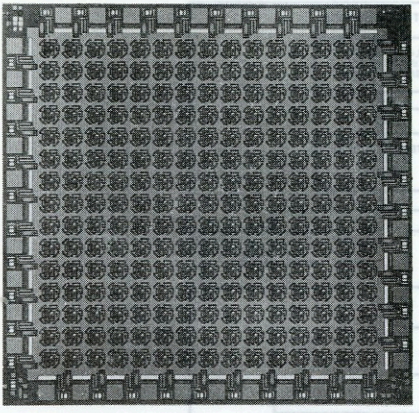
CELL COUNTS FOR SOME STANDARD FUNCTIONS

INPUTS	TTL/LPTTL Buffer	1
	High Z_{IN} Buffer	1
	Schmitt Trigger	3
INTERNAL	NAND (2 input)/NOR (3 input)	1
	Equivalence/Exclusive OR	1
	Binary Divider with Preset, Clear	3
	Binary Divider with Parallel Load	4
	Data Latch	3
	Shift Register Bit	4
	D Type Flip Flop with Preset, Clear	6
	Monostable	2
	Controlled Monostable/Oscillator	4
	Differential Amplifier	6
OUTPUTS	RTL	1
	Totem Pole with Tristate	3
	16 mA Totem Pole	2 (2 Pins)
	40 mA Open Collector	1 (2 Pins)

CELL COUNTS FOR SOME TTL EQUIVALENT FUNCTIONS

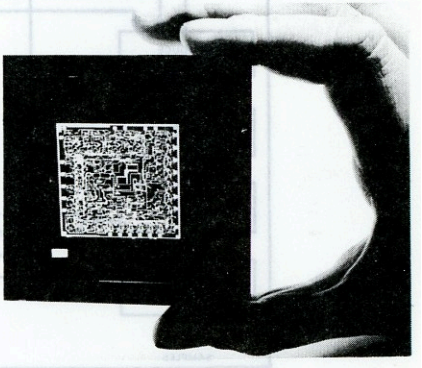
GATES	7400	4
	7404	3
	7430	3
MONOSTABLES	74121	7
	74122	8
FLIP FLOPS	7473	12
	7474	12
LATCHES	7475	12
SHIFT REGISTERS	7491 (Serial)	4 per bit
	7495 (Bidirectional parallel/serial)	10 per bit
COUNTERS	7490 (Decade)	16
	74160 (Synchronous decade)	20
	74190 (Bidirectional parallel/serial)	34
ARITHMETIC FUNCTIONS	7485	24
	74180	16
	7483	24 to 34 (design dependent)
DECODERS/ MULTIPLEXERS	7442	20
	7447	25
	74150	40
	74151	20

HOW THE ARRAY IS CUSTOMISED



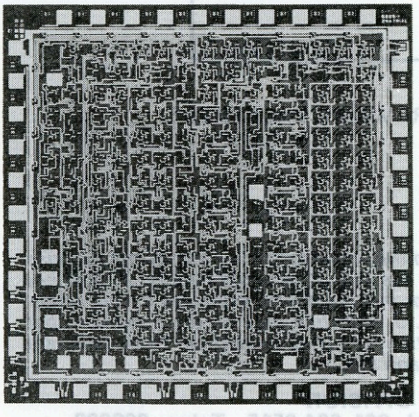
UNCOMMITTED ARRAY

Size: 131 mils square
Requires only single aluminium interconnection layer to become the functional device.



FINAL MASK

Produced to suit customer's specification from circuit diagrams



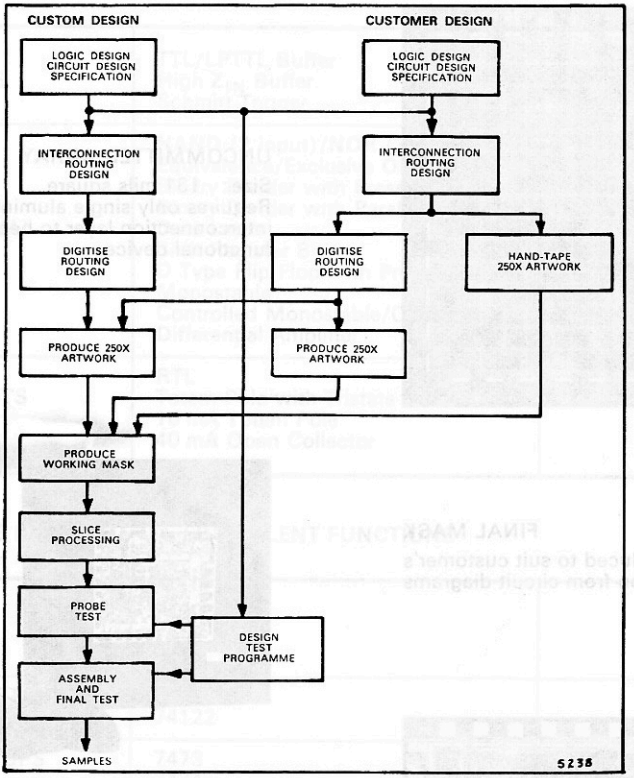
COMMITTED ARRAY

The completed Custom Integrated Circuit ready for assembly in the required package.

Depending on application, the ULA can be supplied in either ceramic or plastic 16, 18, 24, 28 or 40 lead D.I.L. packages. Flat package available on request.

DESIGN ROUTES

The diagram shows the routes by which the customer's circuit is realised on the ULA.



UNCOMMITTED LOGIC ARRAY: PROGRAMMING PROCEDURE

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