```
-- FPGA-CPU TEST PROGRAM
-- Altera Instruction Memory Initialization File
Depth = 90;
Width = 8;
Address_radix = HEX;
Data_radix = HEX;
Content
Begin
-- Use NOPS for default instruction memory values
    [40..59]: 78; -- STOP
-- Place MIPS Instructions here
-- Note: memory addresses are in words and not bytes
-- i.e. next location is +1 and not +4

-- TEST program for microcontroller
    00: 70 01;   -- START:  MOVI R0, H#01   ; constant '1'
    02: 61 50;   --     IN R1, H#50     ; command code: 0=arithmetics, 1=SWR(Ra,Rb,Rd),
    2=LWR&OUT(Ra,Rb)
    04: 09 1E;   --     JZ R1, ARITH
    06: 29 10;   --     SUBA R1, R1, R0 ; R1 := R1 - 1
    08: 09 13;   --     JZ R1, SAVE
    0A: 60 50;   -- LOADP:  IN R0, H#50     ; Ra
    0C: 61 50;   --     IN R1, H#50     ; Rb
    0E: 42 01;   --     LWR R2, R0, R1  ; R2 = RAM(R0.R1)
    10: 6A 10;   --     OUT R2, H#10    ; print R2
    12: 00;   --    JORG
    13: 60 50;   -- SAVE:   IN R0, H#50
    15: 61 50;   --     IN R1, H#50
    17: 62 50;   --     IN R2, H#50     ; RAM(R0.R1) = R2
    19: 4A 01;   --     SWR R2, R0, R1
    1B: 6A 10;   --     OUT R2, H#10    ; print R2
    1D: 00;   --    JORG

    1E: 60 50;   -- ARITH:  IN R0, H#50
    20: 61 50;   --     IN R1, H#50
    22: 22 01;   --     ADDA R2, R0, R1
    24: 6A 10;   --     OUT R2, H#10
    26: 2A 01;   --     SUBA R2, R0, R1
    28: 6A 10;   --     OUT R2, H#10
    2A: 3A 01;   --     AND R2, R0, R1
    2C: 6A 10;   --     OUT R2, H#10
    2E: 32 01;   --     OR R2, R0, R1
    30: 6A 10;   --     OUT R2, H#10
    32: 5A 00 10;   --  SWI R2, H#0010  ; RAM(0x1000) <= R2
    35: F2 01;   --     MUL R2, R0, R1
    37: 6A 10;   --     OUT R2, H#10
    39: 52 00 10;   --  LWI R2, H#0010  ; R2 <= RAM(0x1000)
    3C: 6A 10;   --     OUT R2, H#10
    3E: 10 00;   --     JMP H#00

End;
```