McMaster University

Student Number |__|__|__|__|__|__|__|__|__|__|

Surname _____

Given Name _____

FINAL EXAMINATION

April 2022 Final Exams

ELECENG 3N03

Instructor: Matiar Howlader

Examination Duration: 150 minutes

Uploading Time: 15 min

Exam Instructions:

Materials Permitted During the Exam Time Period:

The McMaster Standard Calculators (Casio FX-991MS/MS+) are the only calculators approved for this exam. No other aids are permitted. **(No electronic aids are permitted e.g. laptops, phones)**.

Instructions to Students:

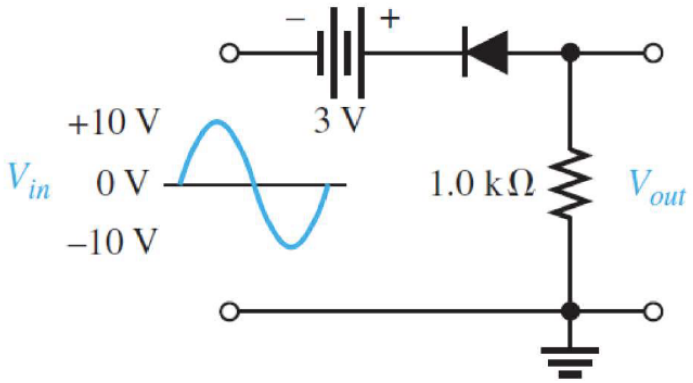
a) Write your Last Name and Student Number at the top of **EACH** page. Pages missing this information will not be marked.
b) This test paper has 4 pages and 6 questions. A formula sheet is provided on pages 6-11. Page 5 is blank. Verify you have a complete paper. You are responsible for ensuring that your copy of the paper is complete.
c) All questions are required.
d) You **MUST SHOW YOUR WORK (DETAILED SOLUTION STEPS) TO GET FULL MARKS**.
e) You are responsible for submitting your solutions in the final exam Dropbox no later than **30 MINUTES** after the exam due. Late submissions will result in recursive mark deductions. Each 1 min late for the first 5-mins results in 1 mark deduction. After the first 5-mins, every extra minute late results in 5 marks deduction.
f) You can submit your **HAND-WRITTEN** solutions in any of the following file formats (pdf, mpeg, png, jpg, and tiff). You are responsible for ensuring that your submitted file(s) are **CLEAR**, **READABLE**, and **NON-CORRUPTED**. Any corrupted (that cannot be opened), or non-clear (that cannot be easily read or with low-resolution), the file will not be marked.
g) By submitting your work, you certify that the work represents solely your independent efforts. You confirm that you are expected to exhibit honesty and use ethical behaviour in all aspects of the learning process. You confirm that it is your responsibility to understand what constitutes academic dishonesty under the Academic Integrity Policy.
Link: https://secretariat.mcmaster.ca/app/uploads/Academic-Integrity-Policy-1-1.pdf

Good luck and have a great summer break!

FINAL EXAMINATION

Question 1 (7 Marks):

Sketch the output voltage waveform for the following circuit shown in **Figure 1** assuming practical model. Note: Step by step calculation must be shown.

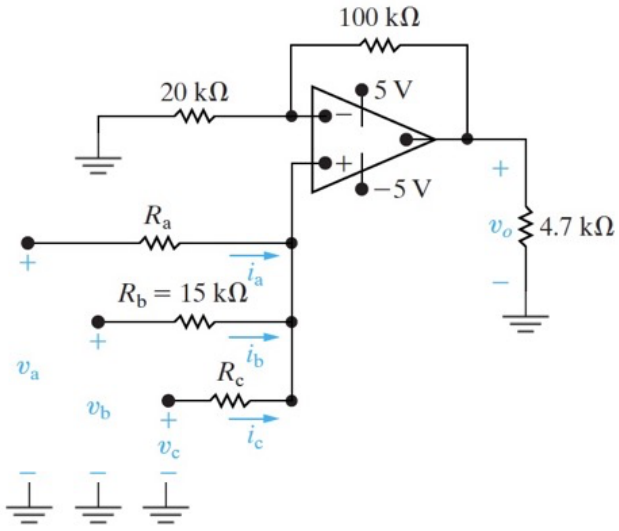


Q1. Figure 1

Question 2 (10 Marks):

A noninverting summing amplifier is given in **Figure 2**. Assume the op-amp is ideal. Design the circuit so that $v_0 = v_a + 2v_b + 3v_c$.

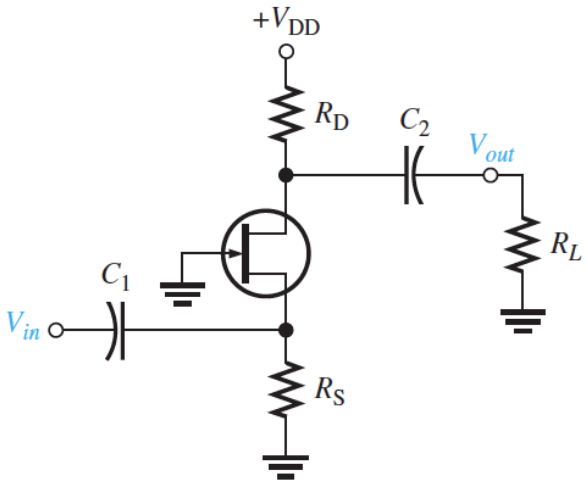
(a) Specify the numerical values of R_a and R_c.
(b) Calculate v_a, v_b, and v_c when $v_a = 0.7\ V$, $v_b = 0.4\ V$, and $v_c = 1.1\ V$.



Q2. Figure 2

Question 3 (7 Marks):

Determine the input resistance at the source terminal, the total input resistance, the voltage gain of the amplifier given below in **Figure 3**. Given values are g_m=2800 μS, V_{DD}=8 V, R_D=10 kΩ, R_S=2.2 kΩ, R_L=10 kΩ, C_1=10 μF, and C_2=10 μF.

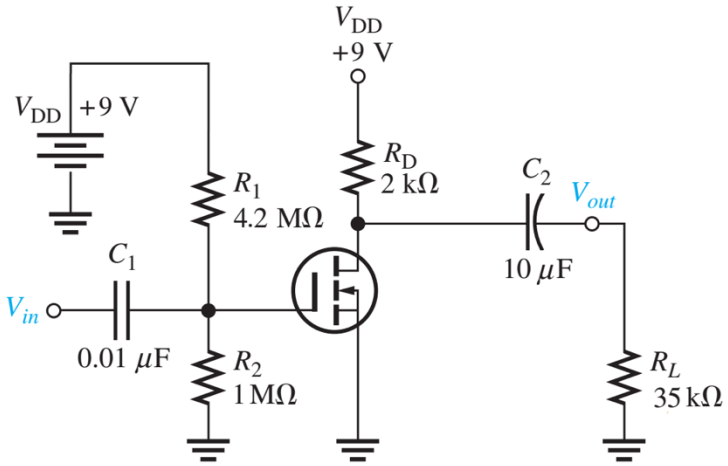


Q3. Figure 3

Question 4 (7 Marks):

For the common-source amplifier shown in **Figure 2**, $V_{GS(th)}$=1.6 V and g_m=30 mS. If $I_{D(ON)}$= 180 mA at V_{GS} = 2.5 V, and V_{in}=50 mV,

(a) Calculate the DC biasing gate-to-source voltage.
(b) Find the drain current I_D.
(c) Find the drain-to-source voltage V_{DS}.
(d) Calculate the value of V_{out}.



Q4. Figure 4

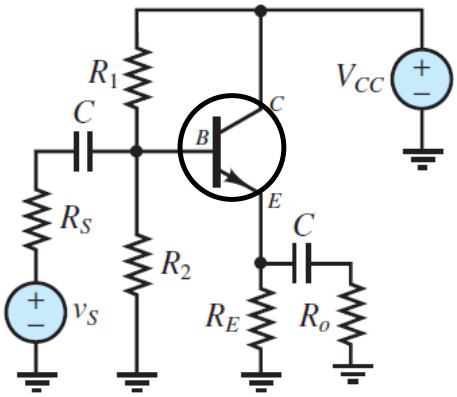
Question 5 (7 Marks):

The circuit shown in **Figure 5** is a common-collector amplifier stage implemented with a npn silicon transistor and a single DC supply V_{CC} = 12 V. Determine V_{CEQ} at the DC operating (Q) point.

R_o = 16Ω β= 130

R_1 = 82 kΩ R_2 = 22 kΩ

R_S = 0.7 kΩ R_E = 0.5 kΩ.



Q5. Figure 5

Question 6 (12 Marks):

A BJT amplifier is shown below in **Figure 6**.

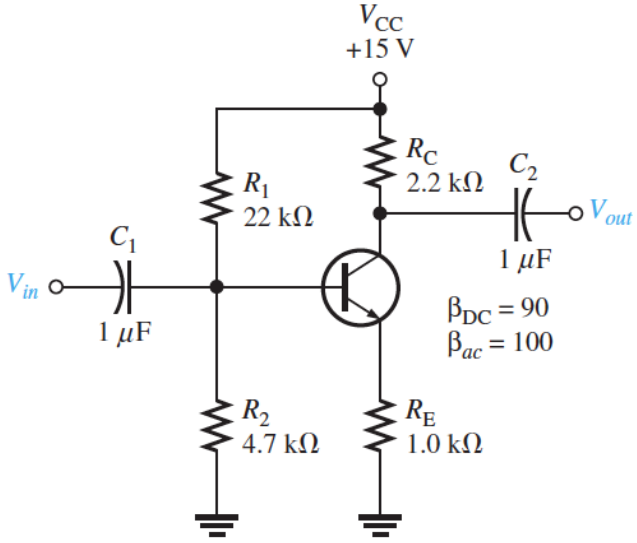
(a) Determine the DC operating point of the device.

(b) Find the voltage gain of this amplifier.

(c) What is the input resistance?

(d) What is the output resistance?

(e) When two stages of this amplifier are cascaded where the first stage is connected to a source with an input impedance of 1.0 kΩ and the second stage is connected to a load of 6.8 kΩ, what is the loaded gain of the two-stage amplifier?



Q6. Figure 6

END OF THE QUESTIONS

SIX PAGES FORMULA SHEET IS IN THE FOLLOWING PAGES

FORMULAS ARE ON THE NEXT PAGES: 6-11

Some equations you may need:

Diodes

$I_F = \frac{V_{bias}}{R_{Limit}}$	Ideal diode model
$I_F = \frac{V_{bias} - V_F}{R_{Limit}}$	Practical diode model
$I_F = \frac{V_P}{\pi}$	Half wave average value
$I_F = \frac{2V_P}{\pi}$	Full wave average value
$PIV = V_{P(in)}$	Peak inverse voltage, half wave rectifier
$PIV = 2V_{P(in)} + 0.7\ V$	Peak inverse voltage, center tapped rectifier
$PIV = V_{P(out)} + 0.7\ V$	Peak inverse voltage, bridge rectifier
$V_{p(out)} = V_{P(sec)} - 1.4\ V$	Bridge full wave output
$V_{p(out)} = V_P - 0.7\ V$	Peak half wave rectifier output (silicon)
$V_{p(out)} = \frac{V_{sec}}{2} - 0.7\ V$	Center tapped full wave output

$\text{Ripple factor(r)} = \frac{V_{r(pp)}}{V_{DC}}$

$\text{Line regulation} = (\frac{\boldsymbol{\Delta V_{out}}}{\boldsymbol{\Delta V_{in}}})\ 100\%$

$\text{Load regulation} = (\frac{V_{NL} - V_{FL}}{V_{FL}})\ 100\%$

$\text{Zener impedance } (Z_z) = \frac{\boldsymbol{\Delta V_z}}{\boldsymbol{\Delta I_z}}$

OP-AMP

$\text{CMRR} = \frac{A_{ol}}{A_{cm}}$	Common-mode rejection ratio
$\text{CMRR} = 20 \log (\frac{A_{ol}}{A_{cm}})$	Common-mode rejection ratio (dB)
$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$	Slew rate
$A_{cl(NI)} = 1 + \frac{R_f}{R_i}$	Voltage gain (non-inverting)

$A_{cl(VF)} = 1$ Voltage gain (follower)

$A_{cl(I)} = -\frac{R_f}{R_i}$ Voltage gain (inverting)

$V_{UTP} = \frac{\mathrm{R_2}}{\mathrm{R_1 + R_2}}\left(+\mathrm{V_{out(max)}}\right)$ Upper trigger point

$V_{\mathrm{LTP}} = \frac{\mathrm{R_2}}{\mathrm{R_1 + R_2}}\left(-\mathrm{V_{out}(max)}\right)$ Lower trigger point

$V_{HYS} = V_{UTP} - V_{LTP}$ Hysteresis voltage

$V_{out} = -(V_{IN1} + V_{IN2} + \ldots + V_{INn})$ *n*-input adder

$V_{out} = -\frac{R_f}{R_i}(V_{IN1} + V_{IN2} + \ldots + V_{INn})$ Adder with gain)

$V_{out} = -\left(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + \ldots + \frac{R_f}{R_n}V_{INn}\right)$ Scaling adder with gain

$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}$ Integrator output rate of change

$V_{out} = -\left(\frac{V_c}{t}\right)R_f C$ Differentiator output voltage with ramp input

JFET & MOSFET

1. $I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$
2. $g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$
3. $g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$
4. $I_D = K(V_{GS} - V_{GS(th)})^2$
5. $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$
6. $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$
7. Self Bias (n-channel J-FET):
   $V_{DS} = V_{DD} - I_D(R_D + R_S)$
8. $R_S = \left|\frac{V_{GS}}{I_D}\right|$
9. $R_{DS} \cong \frac{V_{DS}}{I_D}$
10. $V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right)V_{DD}$ E-MOSFET voltage divider bias
11. D-MOSFET:
    $V_{DS} = V_{DD} - I_{DSS}R_D$

Common source amplifier

(JFET self bias)

1. $I_D = I_{DSS}(1 - \frac{I_D R_S}{V_{GS(off)}})^2$
2. $A_V = -g_m R_d$
3. $R_{in} = R_G || (\frac{V_{GS}}{I_{GSS}})$

D-MOSFET zero bias

1. $I_D = I_{DSS}$
2. $A_V = g_m R_d$
3. $R_{in} = R_G || (\frac{V_{GS}}{I_{GSS}})$

E-MOSFET voltage divider bias

1. $I_D = K(V_{GS} - V_{GS(th)})^2$
2. $A_V = g_m R_d$
3. $R_{in} = R_1 || R_2 \, || (\frac{V_{GS}}{I_{GSS}})$

Common drain amplifier

(JFET self bias)

1. $I_D = I_{DSS}(1 - \frac{V_{GS}}{V_{GS(off)}})^2$
2. $A_V = \frac{g_m R_s}{1 + g_m R_s}$
3. $R_{in} = R_G || (\frac{V_{GS}}{I_{GSS}})$

Common gate Amplifier

(JFET self bias)

1. $I_D = I_{DSS}(1 - \frac{I_D R_S}{V_{GS(off)}})^2$
2. $A_V = g_m R_d$
3. $R_{in} = (\frac{1}{g_m}) || (R_s)$

Cascode amplifier

(Common gate amplifier)

1. $A_V \cong g_{m(CG)} X_L$

Bipolar Junction Transistors

1. $I_E = I_C + I_B$ — Transistor currents
2. $\beta_{DC} = \frac{I_C}{I_B}$ — DC current gain
3. $V_{EE} \cong 0.7\ V$ — Base-to-emitter voltage (silicon)
4. $I_B = \frac{V_{BB} - V_{BE}}{R_B}$ — Base current
5. $V_{CE} = V_{CC} - I_C R_C$ — Collector-to-emitter voltage (common-emitter)
6. $V_{CB} = V_{CE} - V_{BE}$ — Collector-to-base voltage
7. $A_V \cong \frac{R_C}{r_e'}$ — Approximate ac voltage gain
8. $V_{CE(cutoff)} = V_{CC}$ — Cutoff condition
9. $I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$ — Collector saturation current
10. $I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$ — Minimum base current for saturation

BJT Bias Circuits

Voltage-Divider Bias

1. $V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$ — For a stiff voltage divider
2. $V_E = V_B - V_{BE}$
3. $I_C \cong I_E = \frac{V_E}{R_E}$
4. $V_C = V_{CC} - I_C R_C$
5. $R_{IN(BASE)} = \frac{\beta_{DC} V_B}{I_E}$
6. $I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$
7. $I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}}$
8. $I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}}$

Emitter Bias

9. $I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}$

Base Bias

10. $V_{CE} = V_{CC} - I_C R_C$
11. $I_C = \beta_{DC}\left(\frac{V_{CC}-V_{BE}}{R_B}\right)$

Emitter-Feedback Bias

12. $I_E = \frac{V_{CC}-V_{BE}}{R_E+R_B/\beta_{DC}}$

Collector-Feedback Bias

13. $I_C = \frac{V_{CC}-V_{BE}}{R_C+R_B/\beta_{DC}}$
14. $V_{CE} = V_{CC} - I_C R_C$

BJT Amplifiers

$r'_e \cong \frac{25mV}{I_E}$	Internal ac emitter resistance

Common-Emitter

$R_{in(tot)} = R_1 \| \| R_2 \| \| R_{in(base)}$	Total amplifier input resistance, voltage-divider bias
$R_{in(base)} = \beta_{ac} r'_e$	Input resistance at base
$R_{out} \cong R_C$	Output resistance
$A_v = \frac{R_C}{r'_e}$	Voltage gain, base-to-collector, unloaded
$A_v = \frac{R_C}{r'_e+R_E}$	Voltage gain without bypass capacitor
$A_v = \frac{R_c}{r'_e}$	Voltage gain, base-to-collector, loaded, bypassed R_E
$A_v \cong \frac{R_C}{R_{E1}}$	Voltage gain, swamped amplifier
$R_{in(base)} = \beta_{ac}(r'_e + R_{E1})$	Input resistance at base, swamped amplifier
$A_i = \frac{I_c}{I_s}$	Current gain, input source to collector
$A_p = A'_v A_i$	Power gain

Common-Collector (Emitter-Follower)

$A_v \cong 1$	Voltage gain, base-to-emitter
$R_{in(base)} \cong \beta_{ac} R_e$	Input resistance at base, loaded
$R_{out} = \left(\frac{R_S}{\beta_{ac}}\right) \mid\mid R_E$	Output resistance
$A_i = \frac{I_e}{I_{in}}$	Current gain
$A_p \cong A_i$	Power gain
$R_{in} = \beta_{ac1}\beta_{ac2} R_E$	Input resistance, Darlington pair

Common-Base

$A_v \cong \frac{R_c}{r'_e}$	Voltage gain, emitter-to-collector
$R_{in(emitter)} \cong r'_e$	Input resistance at emitter
$R_{out} \cong R_C$	Output resistance
$A_i \cong 1$	Current gain
$A_p \cong A_v$	Power gain

Multistage Amplifier

$A'_v = A_{v1}A_{v2}A_{v3} \ldots A_v$	Overall voltage gain
$A_{v(dB)} = 20 \log A_v$	Voltage gain expressed in dB

END OF EXAMINATION