Assignment 1

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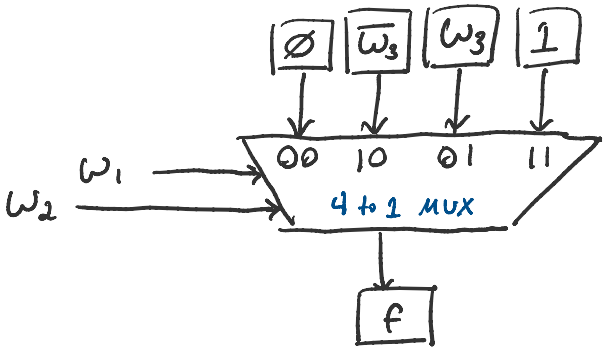
1. Implement the logic function f given in the truth table below, using only NOT gates and one 4-to-1 multiplexer.

w_1	w_2	w_3	f	
0	0	0	0	w_3
0	0	1	0	$\overline{w_3}$
0	1	0	0	w_3
0	1	1	1	w_3
1	0	0	1	$\overline{w_3}$
1	0	1	0	$\overline{w_3}$
1	1	0	1	$\overline{w_3}$
1	1	1	1	w_3



2. Give a (minimized) gate-level implementation of a circuit that converts a 3-bit binary number to the corresponding 3-bit Gray code representation. If you have not seen it before, you may need to look up what Gray codes are.

x_2	x_1	x_0	y_2	y_1	y_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

y_2:

x_0 \ x_2x_1	00	01	11	10
0	0	0	1	1
1	0	0	1	1

$y_2 = x_2$

y_1:

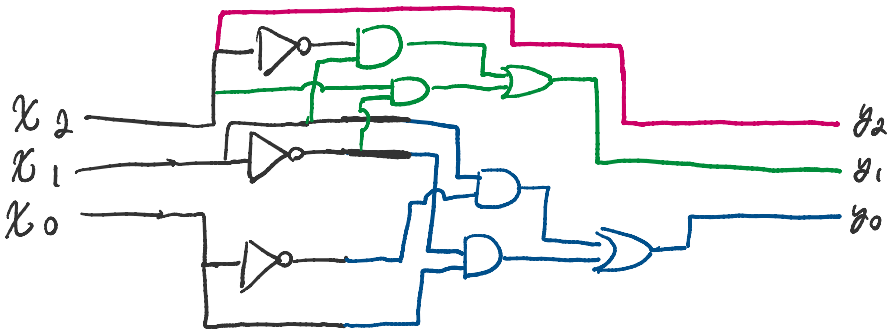
x_0 \ x_2x_1	00	01	11	10
0	0	1	0	1
1	0	1	0	1

$y_1 = \overline{x_1}x_2 + x_1\overline{x_2}$

y_0:

x_0 \ x_2x_1	00	01	11	10
0	0	1	1	0
1	1	0	0	1

$y_0 = x_0\overline{x_1} + \overline{x_0}x_1$

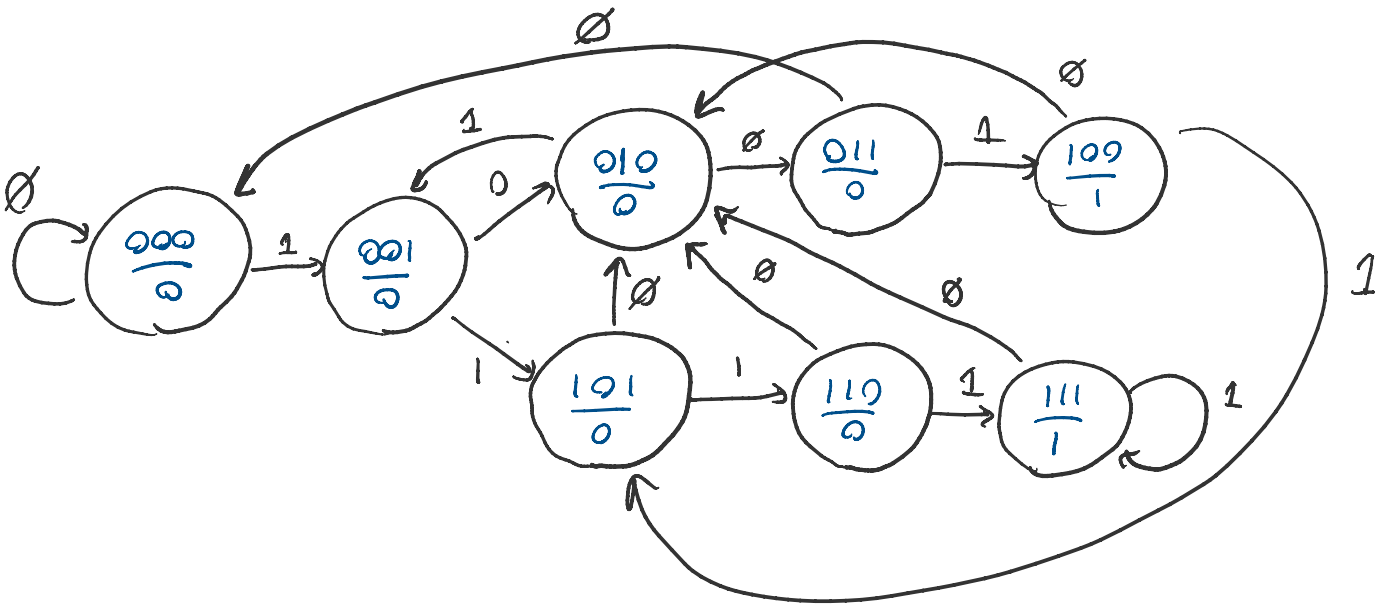


3. We wish to implement a circuit that has input w and output z. The circuit must generate $z = 1$ when the previous four values of w were 1001 or 1111; otherwise $z = 0$.

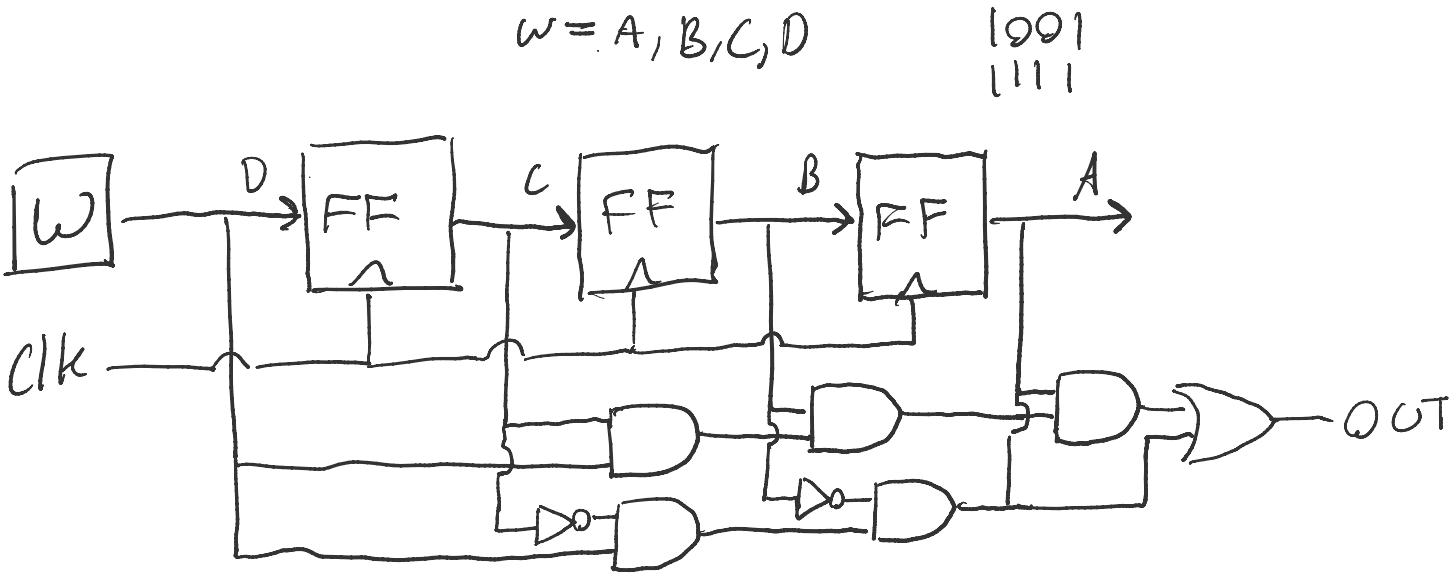
   (a) Give a Moore FSM model for the system.

   (b) Give a circuit implementation of this using D flip-flops and necessary logic gates.

   (c) Give an implementation of this system in Verilog.



(b) Give a circuit implementation of this using D flip-flops and necessary logic gates.

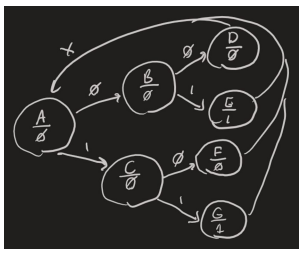


(c) Give an implementation of this system in Verilog.

```
module four_values(input w, clk, output reg z);
  reg P0, P1, P2, P3;

  always @(posedge clk) begin
    P3 <= P2;
    P2 <= P1;
    P1 <= P0;
    P0 <= w;
  end

  assign z = (P3 & P2 & P1 & P0)|(P3 & ~P2 & ~P1 &
P0);

endmodule
```

4. Consider the following Moore FSM, with input x and output z. Derive an equivalent state machine with the minimum number of states.

Present State	Next State $x=0$	Next State $x=1$	Output
A	B	C	0
B	D	E	0
C	F	G	0
D	A	A	0
E	A	A	1
F	A	A	0
G	A	A	1



X_1	X_0	Z
0	0	0
0	1	1
1	0	0
1	1	1