Assignment 3

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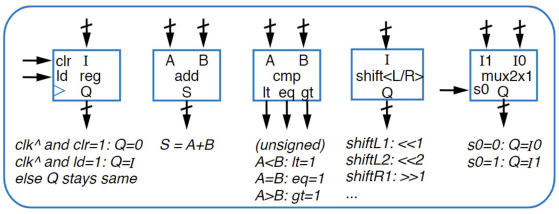
1. Design a datapath and a control FSM for an 8-bit countdown timer. It should work as follows:

   - There should be the ability to load a value into the timer.
   - When the timer reaches 0, a flag is set to indicate that the timer has finished. The timer remains at 0 until a new value is loaded.
   - When enabled, the timer decrements by one per clock cycle.

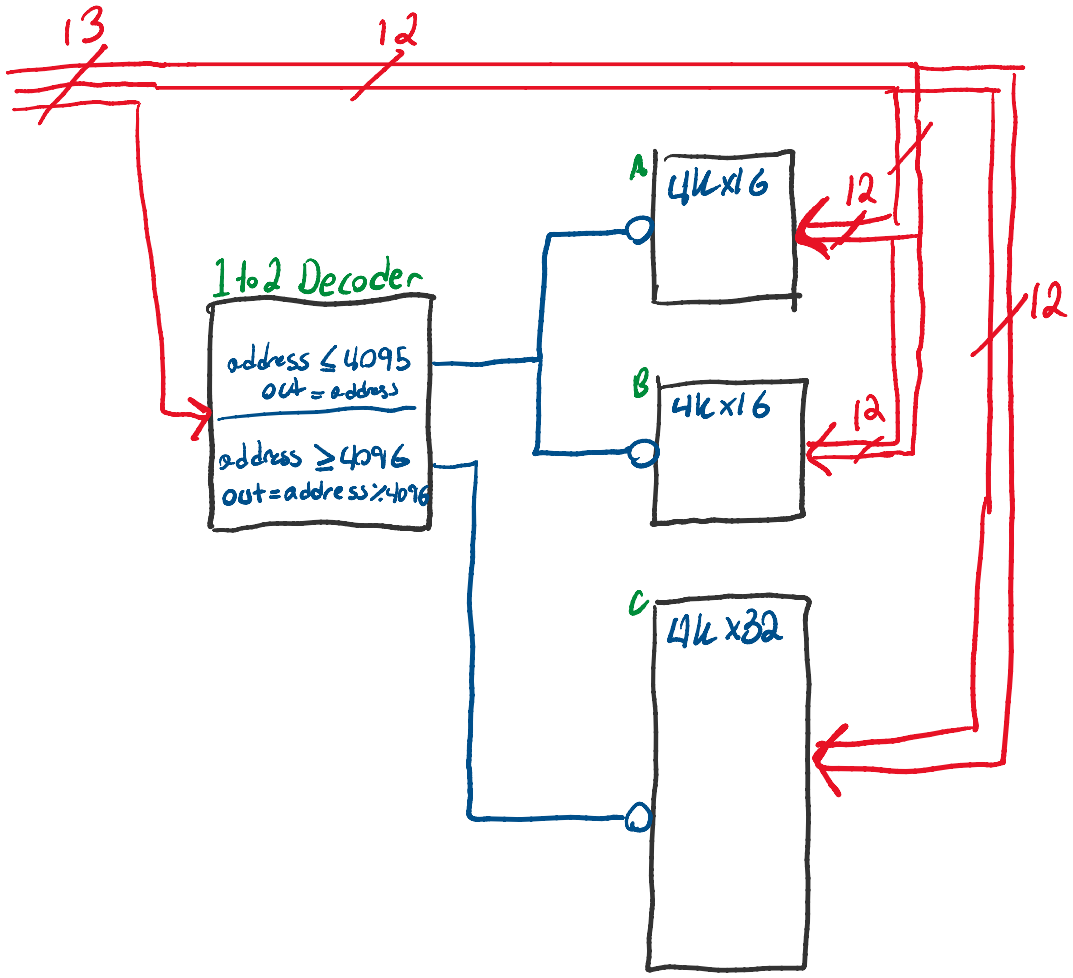
   You should include any signals (enable, reset, etc.) that you feel would be appropriate. The datapath should consist of simple elements, such as adders, comparators, multiplexers, etc.



2. Design an 8K by 32 memory using one 4K by 32 memory and two 4K by 16 memories.

$\log_2(8 \times 2^{10}) = 13$ address input signals

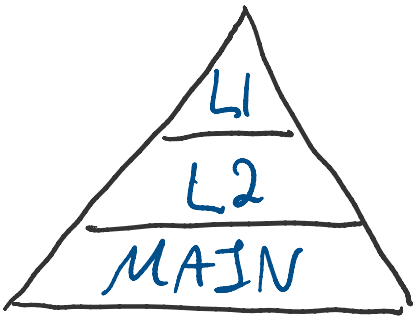
*A holds first 16 bits of word, B holds remaining 16



3. Consider the following cache structure. There are two levels of cache, $L1$ and $L2$, and main memory. $L1$ is checked first. If there is a miss in $L1$, then $L2$ is checked. If there is a miss in $L2$, then main memory is used. The cache performance parameters are:

   - $L1$ requires 1 cycle to check, with miss rate 25 percent
   - $L2$ requires 10 cycles to check, with miss rate 40 percent
   - a main memory access requires 100 cycles

   What is the average memory access time?



hit | miss→hit | miss-miss-hit

$M_{L1} = 25\%$ | $M_{L2} = 40\%$ | 100%

1 cycle | 10 cycles

avg. access time $= t_{access}$

$t_{access} = 1 + 0.25(10) + 0.25 \times 0.4(100)$

$= 13.5$ cycles