Some equations you may need:

Diodes

$I_F = \frac{V_{bias}}{R_{Limit}}$	Ideal diode model
$I_F = \frac{V_{bias} - V_F}{R_{Limit}}$	Practical diode model
$I_F = \frac{V_P}{\pi}$	Half wave average value
$I_F = \frac{2V_P}{\pi}$	Full wave average value
$PIV = V_{P(in)}$	Peak inverse voltage, half wave rectifier
$PIV = 2V_{P(in)} + 0.7\ V$	Peak inverse voltage, center tapped rectifier
$PIV = V_{P(out)} + 0.7\ V$	Peak inverse voltage, bridge rectifier
$V_{p(out)} = V_{P(sec)} - 1.4\ V$	Bridge full wave output
$V_{p(out)} = V_P - 0.7\ V$	Peak half wave rectifier output (silicon)
$V_{p(out)} = \frac{V_{sec}}{2} - 0.7\ V$	Center tapped full wave output

$$\text{Ripple factor(r)} = \frac{V_{r(pp)}}{V_{DC}}$$

$$\text{Line regulation} = \left(\frac{\boldsymbol{\Delta V_{out}}}{\boldsymbol{\Delta V_{in}}}\right) 100\%$$

$$\text{Load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right) 100\%$$

$$\text{Zener impedance } (Z_z) = \frac{\boldsymbol{\Delta V_z}}{\boldsymbol{\Delta I_z}}$$

OP-AMP

$CMRR = \frac{A_{ol}}{A_{cm}}$	Common-mode rejection ratio
$CMRR = 20 \log \left(\frac{A_{ol}}{A_{cm}}\right)$	Common-mode rejection ratio (dB)
$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$	Slew rate

$A_{cl(NI)} = 1 + \frac{R_f}{R_i}$ Voltage gain (non-inverting)

$A_{cl(VF)} = 1$ Voltage gain (follower)

$A_{cl(I)} = -\frac{R_f}{R_i}$ Voltage gain (inverting)

$V_{UTP} = \frac{R_2}{R_1 + R_2}(+V_{out(max)})$ Upper trigger point

$V_{LTP} = \frac{R_2}{R_1 + R_2}(-V_{out}(max))$ Lower trigger point

$V_{HYS} = V_{UTP} - V_{LTP}$ Hysteresis voltage

$V_{out} = -(V_{IN1} + V_{IN2} + ... + V_{INn})$ *n*-input adder

$V_{out} = -\frac{R_f}{R_i}(V_{IN1} + V_{IN2} + \ldots + V_{INn})$ Adder with gain)

$V_{out} = -(\frac{R_f}{R_1}V_{IN1} + \frac{R_f}{R_2}V_{IN2} + ... + \frac{R_f}{R_n}V_{INn})$ Scaling adder with gain

$\frac{\Delta V_{out}}{\Delta t} = -\frac{V_{in}}{R_i C}$ Integrator output rate of change

$V_{out} = -\left(\frac{V_c}{t}\right) R_f C$ Differentiator output voltage with ramp input

JFET & MOSFET

1. $I_D \cong I_{DSS}(1 - \frac{V_{GS}}{V_{GS(off)}})^2$
2. $g_m = g_{m0}(1 - \frac{V_{GS}}{V_{GS(off)}})$
3. $g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$
4. $I_D = K(V_{GS} - V_{GS(th)})^2$
5. $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$
6. $R_{IN} = |\frac{V_{GS}}{I_{GSS}}|$
7. Self Bias (n-channel J-FET):
   $V_{DS} = V_{DD} - I_D(R_D + R_S)$
8. $R_S = |\frac{V_{GS}}{I_D}|$
9. $R_{DS} \cong \frac{V_{DS}}{I_D}$
10. $V_{GS} = (\frac{R_2}{R_1 + R_2})V_{DD}$ E-MOSFET voltage divider bias

11. D-MOSFET:

$$V_{DS} = V_{DD} - I_{DSS}R_D$$

Common source amplifier

(JFET self bias)

1. $I_D = I_{DSS}(1 - \frac{I_D R_S}{V_{GS(off)}})^2$
2. $A_V = -g_m R_d$
3. $R_{in} = R_G||(\frac{V_{GS}}{I_{GSS}})$

D-MOSFET zero bias

1. $I_D = I_{DSS}$
2. $A_V = g_m R_d$
3. $R_{in} = R_G||(\frac{V_{GS}}{I_{GSS}})$

E-MOSFET voltage divider bias

1. $I_D = K(V_{GS} - V_{GS(th)})^2$
2. $A_V = g_m R_d$
3. $R_{in} = R_1||R_2\ ||(\frac{V_{GS}}{I_{GSS}})$

Common drain amplifier

(JFET self bias)

1. $I_D = I_{DSS}(1 - \frac{V_{GS}}{V_{GS(off)}})^2$
2. $A_V = \frac{g_m R_s}{1+g_m R_s}$
3. $R_{in} = R_G||(\frac{V_{GS}}{I_{GSS}})$

Common gate Amplifier

(JFET self bias)

1. $I_D = I_{DSS}(1 - \frac{I_D R_S}{V_{GS(off)}})^2$
2. $A_V = g_m R_d$
3. $R_{in} = (\frac{1}{g_m})||(R_s)$

Cascode amplifier

(Common gate amplifier)

1. $A_V \cong g_{m(CG)} X_L$

Bipolar Junction Transistors

1. $I_E = I_C + I_B$ — Transistor currents
2. $\beta_{DC} = \frac{I_C}{I_B}$ — DC current gain
3. $V_{EE} \cong 0.7\ V$ — Base-to-emitter voltage (silicon)
4. $I_B = \frac{V_{BB} - V_{BE}}{R_B}$ — Base current
5. $V_{CE} = V_{CC} - I_C R_C$ — Collector-to-emitter voltage (common-emitter)
6. $V_{CB} = V_{CE} - V_{BE}$ — Collector-to-base voltage
7. $A_V \cong \frac{R_C}{r_e'}$ — Approximate ac voltage gain
8. $V_{CE(cutoff)} = V_{CC}$ — Cutoff condition
9. $I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$ — Collector saturation current
10. $I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$ — Minimum base current for saturation

BJT Bias Circuits

Voltage-Divider Bias

1. $V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$ — For a stiff voltage divider
2. $V_E = V_B - V_{BE}$
3. $I_C \cong I_E = \frac{V_E}{R_E}$
4. $V_C = V_{CC} - I_C R_C$
5. $R_{IN(BASE)} = \frac{\beta_{DC} V_B}{I_E}$
6. $I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}$
7. $I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}}$
8. $I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}}$

Emitter Bias

9. $I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}}$

Base Bias

10. $V_{CE} = V_{CC} - I_C R_C$
11. $I_C = \beta_{DC}\left(\frac{V_{CC}-V_{BE}}{R_B}\right)$

Emitter-Feedback Bias

12. $I_E = \frac{V_{CC}-V_{BE}}{R_E+R_B/\beta_{DC}}$

Collector-Feedback Bias

13. $I_C = \frac{V_{CC}-V_{BE}}{R_C+R_B/\beta_{DC}}$
14. $V_{CE} = V_{CC} - I_C R_C$

<u>BJT Amplifiers</u>

$r_e' \cong \frac{25mV}{I_E}$	Internal ac emitter resistance

Common-Emitter

$R_{in(tot)} = R_1 \| \| R_2 \| \| R_{in(base)}$	Total amplifier input resistance, voltage-divider bias
$R_{in(base)} = \beta_{ac} r_e'$	Input resistance at base
$R_{out} \cong R_C$	Output resistance
$A_v = \frac{R_C}{r_e'}$	Voltage gain, base-to-collector, unloaded
$A_v = \frac{R_C}{r_e'+R_E}$	Voltage gain without bypass capacitor
$A_v = \frac{R_c}{r_e'}$	Voltage gain, base-to-collector, loaded, bypassed R_E
$A_v \cong \frac{R_C}{R_{E1}}$	Voltage gain, swamped amplifier
$R_{in(base)} = \beta_{ac}(r_e' + R_{E1})$	Input resistance at base, swamped amplifier
$A_i = \frac{I_c}{I_s}$	Current gain, input source to collector

$A_p = A'_v A_i$	Power gain

Common-Collector (Emitter-Follower)

$A_v \cong 1$	Voltage gain, base-to-emitter
$R_{in(base)} \cong \beta_{ac} R_e$	Input resistance at base, loaded
$R_{out} = \left(\frac{R_s}{\beta_{ac}}\right) \mid\mid R_E$	Output resistance
$A_i = \frac{I_e}{I_{in}}$	Current gain
$A_p \cong A_i$	Power gain
$R_{in} = \beta_{ac1}\beta_{ac2} R_E$	Input resistance, Darlington pair

Common-Base

$A_v \cong \frac{R_c}{r'_e}$	Voltage gain, emitter-to-collector
$R_{in(emitter)} \cong r'_e$	Input resistance at emitter
$R_{out} \cong R_C$	Output resistance
$A_i \cong 1$	Current gain
$A_p \cong A_v$	Power gain

Multistage Amplifier

$A'_v = A_{v1} A_{v2} A_{v3} \ldots A_v$	Overall voltage gain
$A_{v(dB)} = 20 \log A_v$	Voltage gain expressed in dB