Question 1 (1 point)

Match the crystal type to the tradeoff.

- [ ] High current draw
- [ ] Large physical size
- [ ] Low current draw
- [ ] Small physical size

1. Low-frequency crystal
2. High-Frequency crystal

(1)

Question 2 (1 point)

Any device connected to an I^2C bus can pull down both the data and clock lines.

- ◯ True
- ◯ False

(2)

Question 3 (1 point)

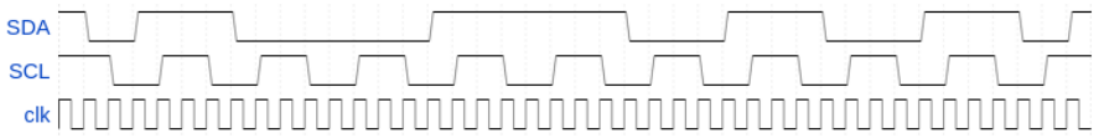
Using a 64 bit register to store Unix Epoch Time extends representable dates 1024 years into the future.

- ◯ True
- ◯ False

(3)

Question 4 (1 point)

Consider the following timing diagram, depicting the transmission of a single byte over an I^2C bus.



Was this packet acknowledged by the addressed slave device? You may assume 7 bit addressing.

- ◯ Yes.
- ◯ No.

(4)

Convert the following binary number, encoded in Binary Coded Decimal (BCD) to a number coded in standard binary. You may assume each decimal digit occupies 4 bits. Note: you must provide your answer in 16 bit binary notation.

0b1000_0111_0001_0000

(5)

Question 2 (1 point)

Which of the following are advantages of parallel communication over serial communication?

- [ ] Doesn't require a clock signal for synchronization
- [ ] Signals do not need to be debounced
- [ ] Better data transfer rate
- [ ] Less expensive infrastructure

(6)

Question 3 (1 point)

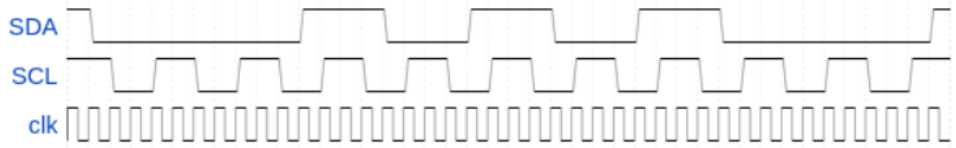
Which of the following are shift register operations?

- [ ] Read data in all at once and store for later retrieval.
- [ ] Data can be read from it one bit at a time.
- [ ] Read data in one bit at a time and store for later retrieval.
- [ ] Data can be read from it

(7)

Question 4 (1 point)

Consider the following timing diagram, depicting the transmission of a single byte over an I^2C bus.



Does this data packet indicate a read or a write request? You may assume 7 bit addressing.

- This is a write request.
- This is a read request.

(8)

Question 1 (1 point)

The **last** region of memory (numerically by address) contains the starting addresses of all interrupt service routines.

- True
- False

(9)

Question 2 (1 point)

Which of the following are advantages of interrupts versus polling?

- [ ] Faster response time
- [ ] More power efficient
- [ ] More memory efficient
- [ ] Allows for multitasking
- [ ] Allows for faster clock speeds
- [ ] Always brings chips when invited to movie night.

(10)

Question 3 (1 point)

Unix epoch time is defined as the number of _____ since 00:00:00 UTS Jan 1, 1970.

- ◯ Minutes
- ◯ Milliseconds
- ◯ Seconds
- ◯ Burgers
- ◯ Hours

(11)

Question 4 (1 point)

Match the following

[ ] Designed for use by kernel processes.	
[ ] Designed for use by user programs.	1. MSP
[ ] Stands for "Process Stack Pointer"	2. PSP
[ ] Stands for "Main Stack Pointer"	

(12)

Question 1 (1 point)

When an I^2C slave device pulls the data line low at the end of a byte transmission, this indicates:

- ◯ A stop condition
- ◯ A start condition
- ◯ A data bit transmission
- ◯ An acknowledgement transmission

(13)

Question 2 (1 point)

Real time clocks normally have an independent power source.

- True
- False

(14)

Question 3 (1 point)

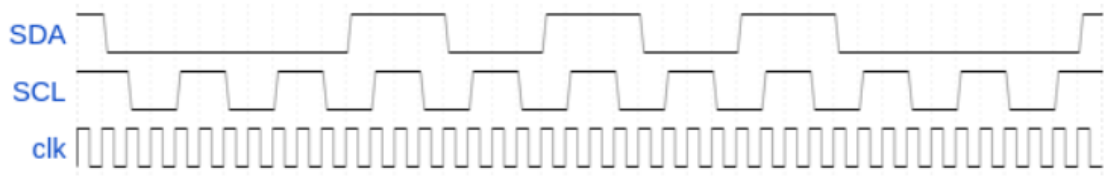
Interrupt priority is not configurable

- True
- False

(15)

Question 4 (1 point)

Consider the following timing diagram, depicting the transmission of a single byte over an I^2C bus.



Was this packet acknowledged by the addressed slave device? You may assume 7 bit addressing.

- No.
- Yes.

(16)

Question 1 (1 point)

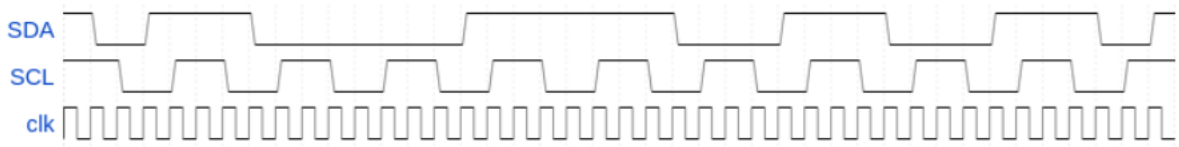
Interrupts are always serviced immediately after the current function is finished executing.

- True
- False

(17)

Question 2 (1 point)

Consider the following timing diagram, depicting the transmission of a single byte over an I^2C bus.



Assuming 7 bit addressing, what is the address of the receiving slave device? Please provide your answer in binary.

(18)

Question 3 (1 point)

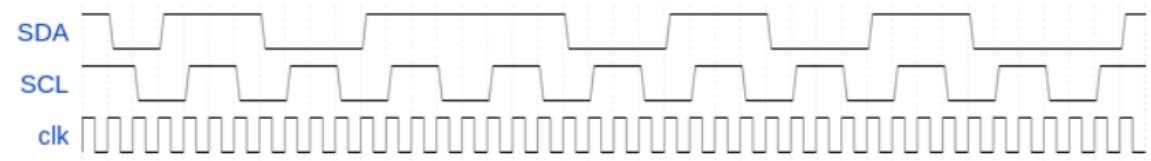
A falling edge on the I^2C data line while the clock line is high indicates

- An acknowledgement transmission
- A stop condition
- A start condition
- A data bit transmission

(19)

Question 4 (1 point)

Consider the following timing diagram, depicting the transmission of a single byte over an I^2C bus.



Does this data packet indicate a read or a write request? You may assume 7 bit addressing.

- This is a read request.
- This is a write request.

(20)

Question 1 (1 point)

An I^2C data bus allows serial communication between up to 32 devices.

- ◯ True
- ◯ False

(21)

Question 2 (1 point)

The Unix Millennium Bug iiis caused by overflow in the 32 bit register used in most RTC chips.

- ◯ True
- ◯ False

(22)

Question 3 (1 point)

An I^2C master device is responsible for timing the SCL clock signal.

- ◯ True
- ◯ False

(23)

Question 4 (1 point)

The reset interrupt handler can be configured to call main() as its ISR

- ◯ True
- ◯ False

(24)

Question 1 (1 point)

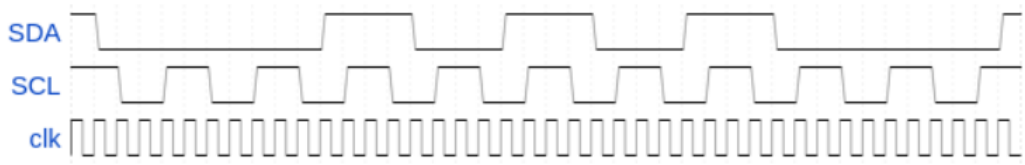
the STM32's internal crystal oscillators are not accurate enough to be used for real time clock functionality.

- ◯ True
- ◯ False

(25)

Question 2 (1 point)

Consider the following timing diagram, depicting the transmission of a single byte over an I^2C bus.



Assuming 7 bit addressing, what is the address of the receiving slave device? Please provide your answer in binary.

(26)

Question 3 (1 point)

Due to crystal inaccuracy, the average digital wristwatch loses about how much time per day?

- 20 seconds
- 0.2 seconds
- 2 minutes
- 2 seconds
- 20 milliseconds

(27)

Question 4 (1 point)

During data transmission, the data line in I^2C should only change while the clock line is high

- True
- False

(28)

Question 1 (1 point)

Order the following steps in the servicing of an interrupt.

- The ISR is executed
- Interrupt signal is detected
- The values stored in the stack are popped, and written back into register memory.
- Main execution is paused
- Main execution resumes.
- Current execution information is pushed onto the system call stack