Field Effect Transistors

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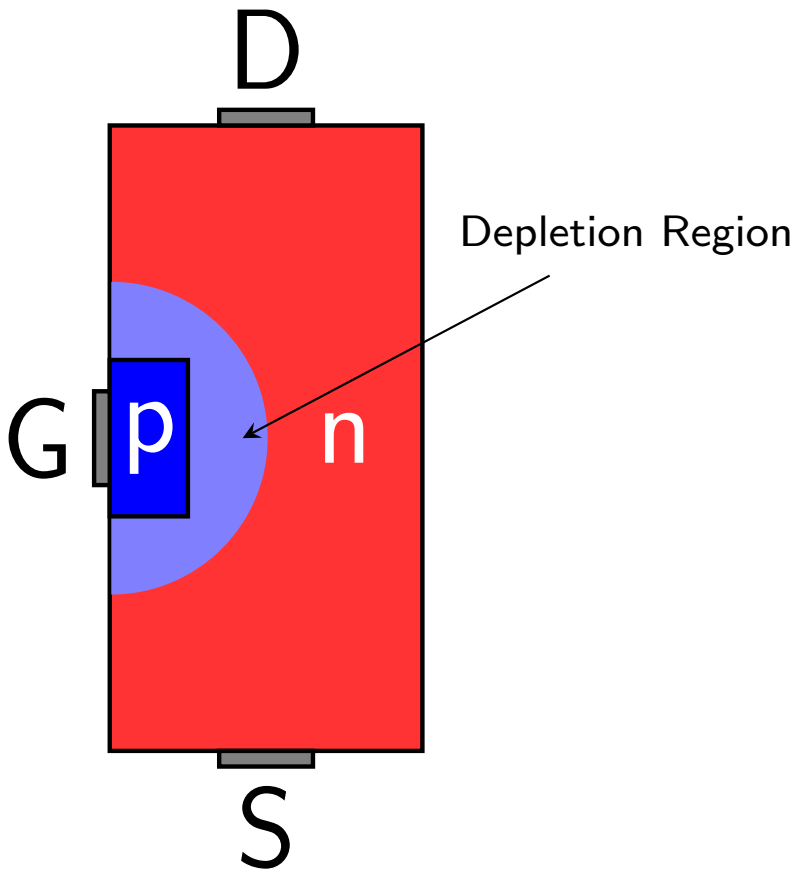
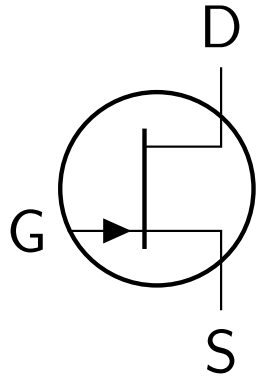
Junction Field Effect Transistors (JFET)

The JFET





A JFET is a 3 terminal voltage-controlled transistor. It consists of an *n*-type substrate connecting the Drain and Source terminals with a *p*-type region on the side. The Gate is connected to the *p* region.

The corresponding circuit symbol is shown below.

JFET Operation

The parameter controlling current is the gate-source voltage difference $V_{GS} = V_G - V_S$.

As the gate voltage becomes more negative, the *pn* junction is reverse biased which enlarges the depletion region by repelling electrons in the *n* region. Therefore, decreasing the gate voltage restricts the current flow through the *n* region.

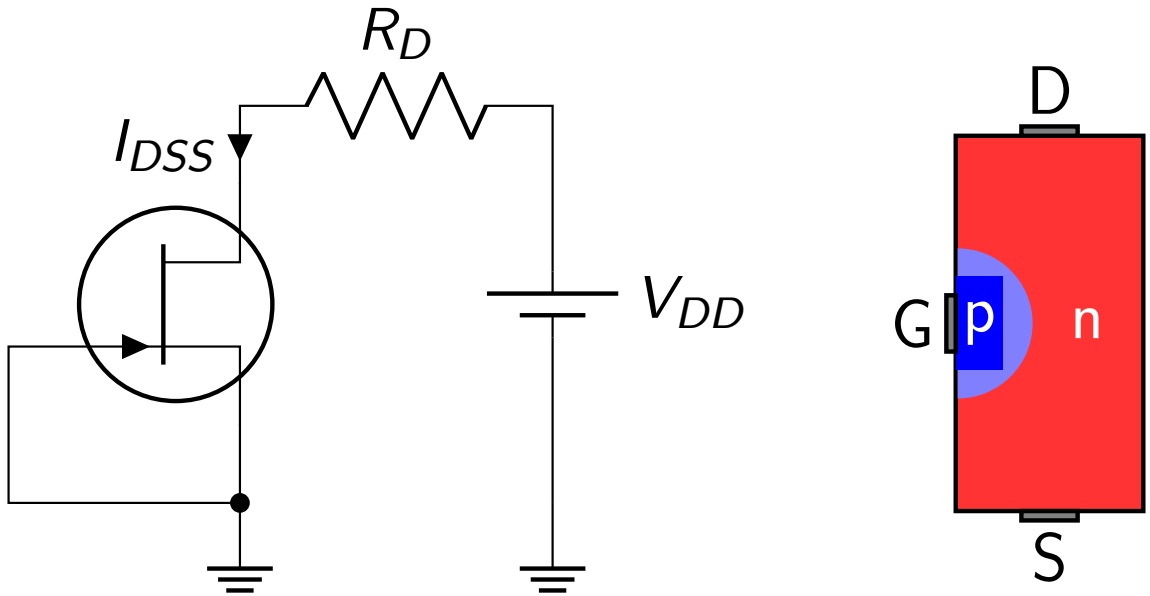
JFETs should not be operated with a positive V_{GS} since this would forward bias the *pn* junction and possibly damage the transistor.

JFET Parameters

There are a few important JFET configurations which determine the transistor's behaviour.

JFET Parameters – I_{DSS}

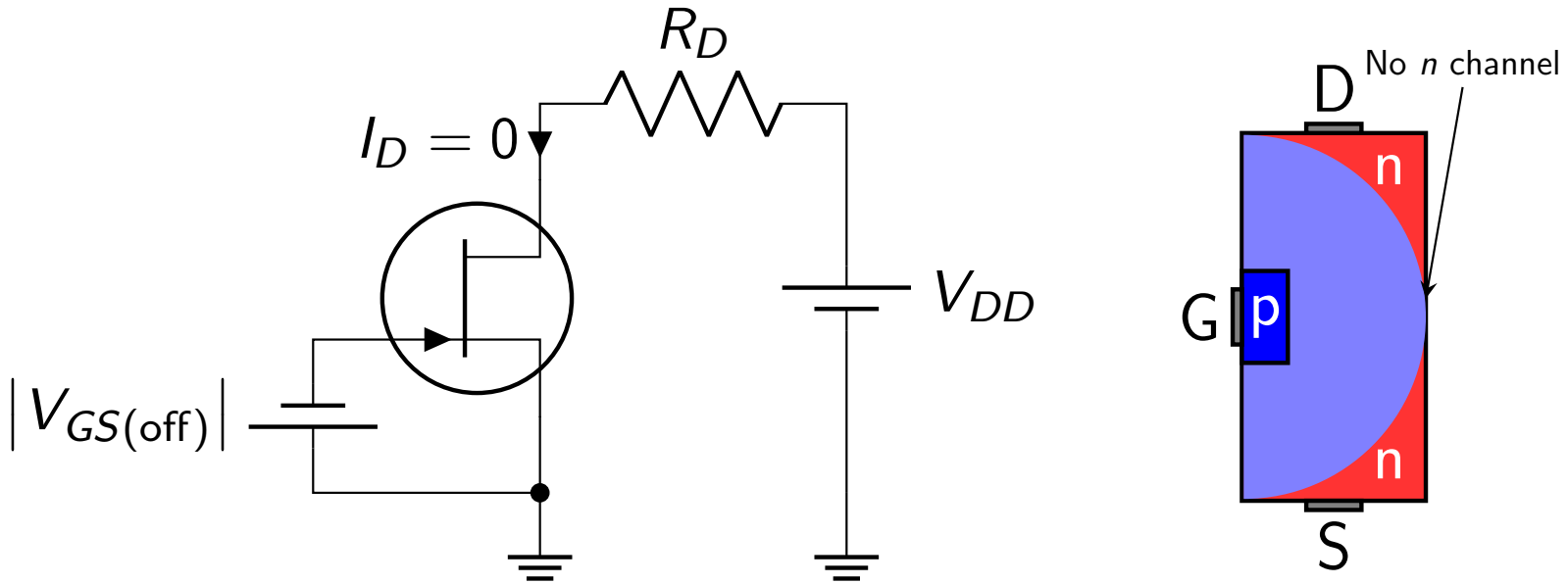
The maximum current that can flow through the transistor occurs when $V_{GS} = 0$. This current is called the "Zero-Gate-Voltage Drain Current" denoted I_{DSS}.



(In order to reach this maximum current, the drain voltage V_{DD} needs to be sufficiently large - more on this later.)

JFET Parameters – $V_{GS(\text{off})}$

As V_{GS} becomes more negative, the depletion region will expand so much that it prevents any current from flowing through the drain, so the transistor is acting like an open switch. The voltage at which this occurs is called $V_{GS(\text{off})}$.



The inverted voltage source and absolute value on $V_{GS(\text{off})}$ emphasize that the gate is at a lower potential than the source.

Operation Regions

For a fixed V_{GS}, there are 3 regions of operation for a JFET which are determined by the drain-source voltage $V_{DS} = V_D - V_S$.

1. For small V_{DS}, the transistor is in its **Ohmic region**, named because the drain current I_D is directly proportional to V_{DS}.

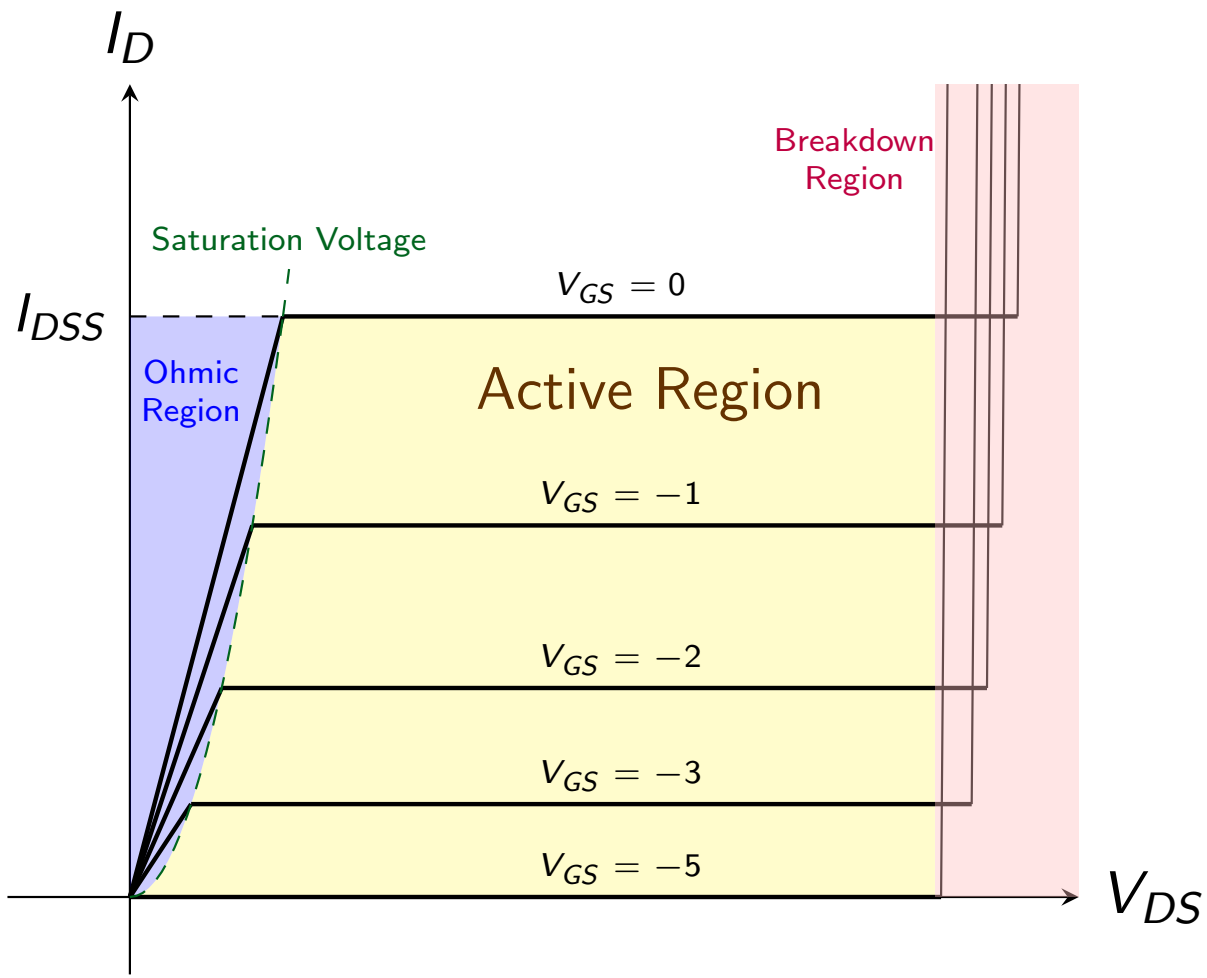
2. When V_{DS} exceeds the **saturation voltage**, the transistor enters its **active region**. In this region, the drain current is effectively constant, independent of V_{DS}.

3. For very large V_{DS}, the JFET ceases to operate effectively and enters its **breakdown region**. Current begins increasing with V_{DS} and damage may occur to the transistor.

The Ohmic and Active regions may also be called the "linear" and "saturation" regions, respectively.

Operation Regions

For fixed V_{GS}, the I_D vs V_{DS} curve described previously can be plotted. Changing the value of V_{GS} produces a family of curves, with more negative V_{GS} curves having generally lower currents.



Operation Regions

Observe that the saturation voltage is dependent on V_{GS}. More positive values of V_{GS} allow more current to flow, so it makes sense that a greater V_{DS} is required to reach the active region.

Given the gate-source voltage, the saturation voltage is $V_{DS(\text{sat})} = V_{GS} - V_{GS(\text{off})}$

The breakdown voltage is also dependent on V_{GS} but we shall not concern ourselves with its specifics.

Active Region Operation

Most JFET circuits operate in the active region, so let's note the behaviour in this region:

- Changing V_{DS} does not affect the drain current I_D
- Changing V_{GS} **does** affect the drain current as it moves "up or down" across the various V_{GS} curves.

I_D vs V_{GS}

Experiments have determined that the active region drain current is related to V_{GS} by the following equation:

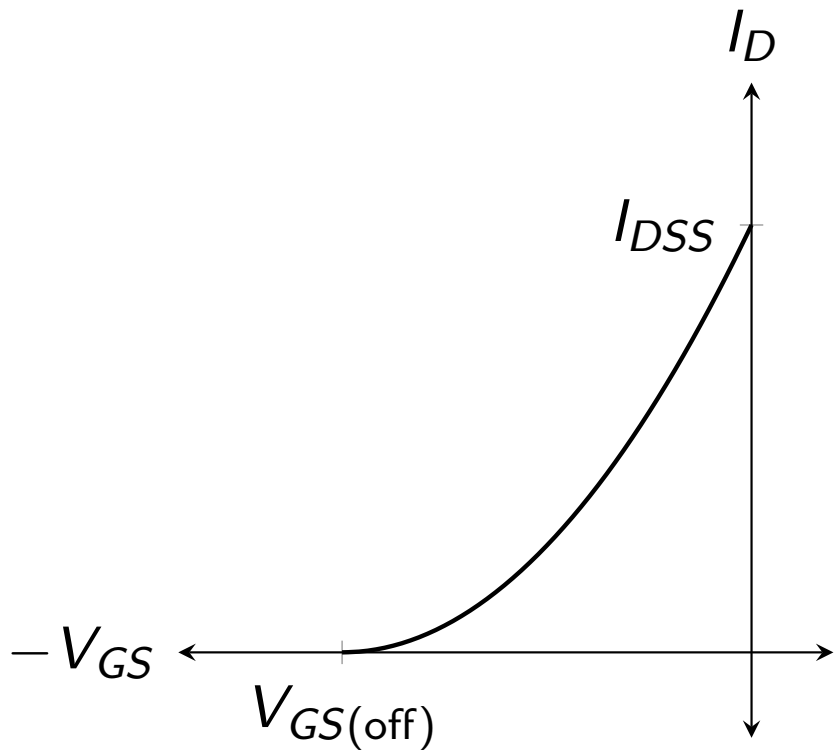
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2 \tag{1}$$

- Pluggin in $V_{GS} = 0$ shows that the drain current is equal to I_{DSS}, matching the definition of I_{DSS}.
- Plugging in $V_{GS} = V_{GS(\text{off})}$ shows that $I_D = 0$, agreeing with the definition of $V_{GS(\text{off})}$.

The equation is not valid for $V_{GS} < V_{GS(\text{off})}$. In this case, the drain current is still 0.

The Transconductance Curve

Equation 1 is call the **transconductance curve** or **transfer curve**. Graphically, it is a parabola that is tangent to the V_{GS} axis at $V_{GS(\text{off})}$ and has an I_D-intercept of I_{DSS}.



Transconductance

The slope of the transconductance curve is called the **transconductance**, denoted g_m. Since the curve is non-linear, g_m depends on V_{GS}

Take the derivative of eq. (1) to find an equation for g_m

$$\frac{\mathrm{d}}{\mathrm{d}V_{GS}}\left[I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(\text{off})}}\right)^2\right]=\frac{2I_{DSS}}{-V_{GS(\text{off})}}\left(1-\frac{V_{GS}}{V_{GS(\text{off})}}\right)$$

Define g_{m0} to be the transconductance when $V_{GS}=0$, so

$$g_{m0}:=\frac{2I_{DSS}}{-V_{GS(\text{off})}}$$

Now we can re-express g_m in terms of g_{m0} as

$$g_m=g_{m0}\left(1-\frac{V_{GS}}{V_{GS(\text{off})}}\right)$$

Solving JFET Circuits

There are two simple concepts that can be used to solve DC JFET circuits:

1. Since the gate is the end of a reverse-biased diode, there is no current flow in or out of the gate. Combining this with KCL will allow you to solve V_G.

2. The source voltage is usually dependent on I_D. Try to find an equation for V_S in terms of I_D.

By solving these two items, you have an expression for V_{GS} in terms of I_D. Combine this with the I_D vs V_{GS} relation in eq. (1) to obtain a second equation for the circuit, allowing you to solve for I_D and V_{GS}.

All other values in the circuit can be easily calculated once I_D and V_{GS} are known.

Self-Biasing a JFET

A simple way to bias a JFET is called "self-biasing" which means that the voltage difference V_{GS} is determined by the current flow through the transistor.

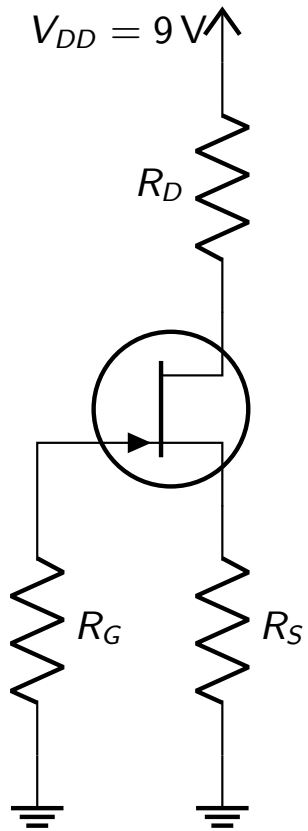
To self-bias a JFET, connect the gate to ground through a resistor. No current flows through the gate, so $V_G = 0$. Connect a resistor between the source and ground.

Current from the drain will pass through the source resistor, increasing V_S until equilibrium is reached.

Self Bias Example

Determine V_{GS} and I_D for the following circuit. Assume the transistor is in its active region.

$V_{GS(\text{off})} = -5\,\text{V} \quad I_{DSS} = 12\,\text{mA} \quad R_G = 1\,\text{M}\Omega \quad R_S = 560\,\Omega \quad R_D = 1200\,\Omega$



Since no current flows through the gate, $V_G = 0$

By KCL at the JFET, all of I_D must flow through R_S, so $V_S = I_D R_S$.

Our two equations are

$$V_{GS} = -I_D R_S \quad \text{and} \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$$

Solving gives

$$V_{GS} = -2.163\,\text{V}$$

and

$$I_D = -\frac{V_{GS}}{R_S} = 3.863\,\text{mA}$$

Self Bias Example

The details of the previous calculation are now presented in full:

$$V_{GS} = -R_S I_D = -R_S I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$$

$$-\frac{1}{R_S I_{DSS}} V_{GS} = 1 - \frac{2}{V_{GS(\text{off})}} V_{GS} + \frac{1}{{V_{GS(\text{off})}}^2} {V_{GS}}^2$$

$$0 = \frac{1}{{V_{GS(\text{off})}}^2} {V_{GS}}^2 + \left(\frac{1}{R_S I_{DSS}} - \frac{2}{V_{GS(\text{off})}}\right) V_{GS} + 1$$

Sub in known values

$$0 = \frac{1}{25} {V_{GS}}^2 + \left(\frac{1}{6.72} + \frac{2}{5}\right) V_{GS} + 1$$

Apply the quadratic formula

$$V_{GS} = -2.163\,\text{V}, -11.557\,\text{V}$$

The second solution is beyond $V_{GS(\text{off})}$ so take $V_{GS} = -2.163\,\text{V}$, then solve I_D

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-2.163\,\text{V}}{560\,\Omega} = 3.863\,\text{mA}$$

Q-Point

The difficult part of the previous example was not the JFETs or circuit analysis, rather is was isolating for V_{GS} and solving the system of equations.

The solution to the two equations represents a point of intersection on the I_D vs V_{GS} graph. The first curve is the transconductance parabola and the second is the equation for V_{GS} as a function of current through R_S. This second equation may be called the **load line**.

The intersection point is the called the **Q-Point** and it describes the DC operating voltage and current for the JFET circuit configuration.

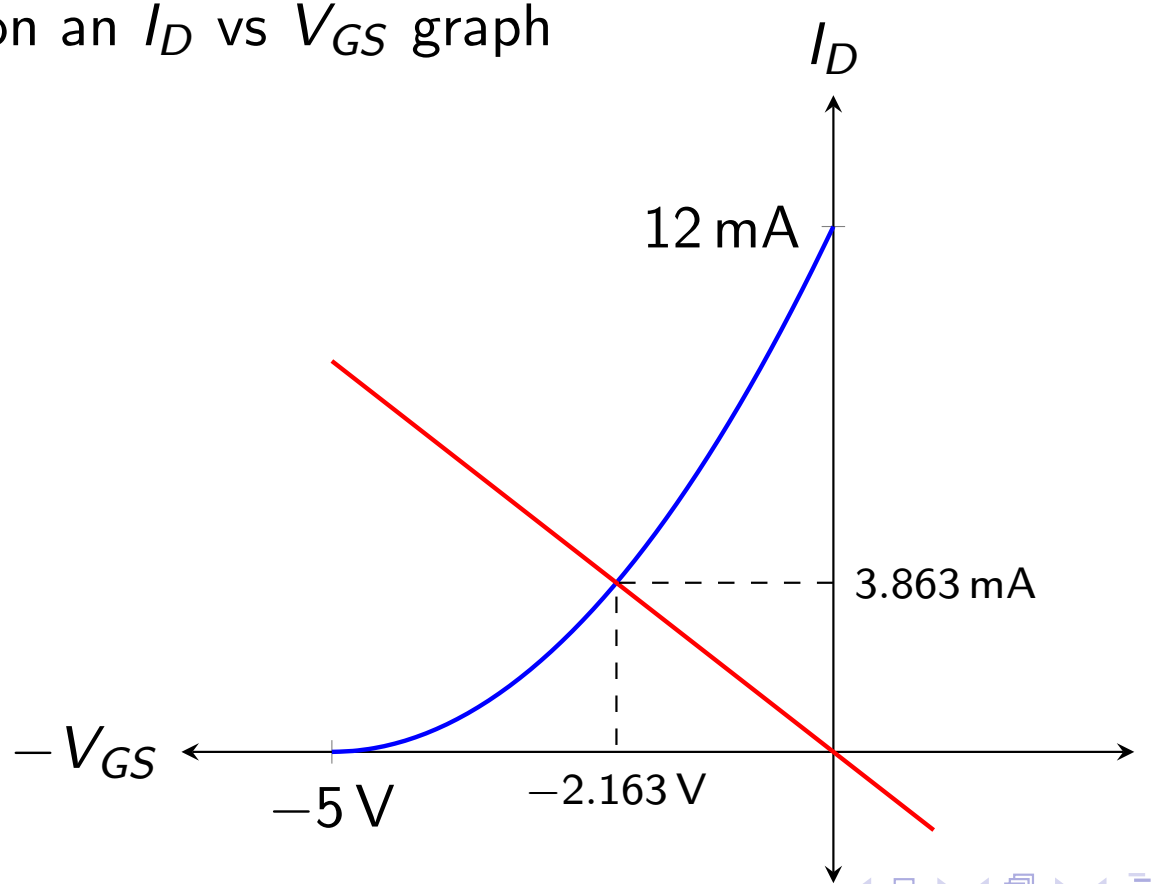
Instead of solving the equations analytically, we can plot both functions and find the point of intersection graphically.

Self Bias Example with Q-Point

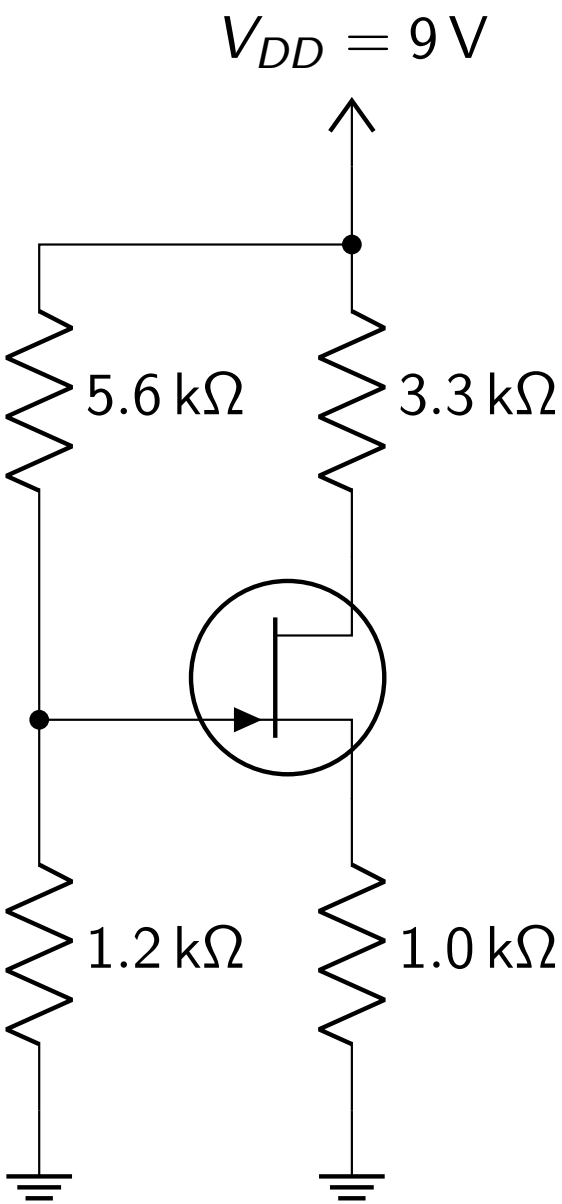
Let's repeat the previous example, starting with the two equations relating V_{GS} and I_D:

$$V_{GS} = -I_D R_S \qquad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$$

Plot both on an I_D vs V_{GS} graph



Voltage Divider Bias



Determine the Q-Point of this circuit. $I_{DSS} = 20\,\text{mA}$ and $V_{GS(\text{off})} = -3\,\text{V}$

No current flows into the gate, so KCL finds

$$V_G = \left(\frac{1.2\,\text{k}\Omega}{1.2\,\text{k}\Omega + 5.6\,\text{k}\Omega}\right) 9\,\text{V} = 1.588\,\text{V}$$

All of the drain current passes through the source resistor. V_S is the voltage across the source resistor, so

$$V_S = I_D \cdot 1.0\,\text{k}\Omega$$

The two equations relating V_{GS} and I_D are

$$V_{GS} = 1.588 - 1000 I_D$$

$$I_D = 0.020\left(1 - \frac{V_{GS}}{-3}\right)^2$$

Solving (analytically or graphically) gives $V_{GS} = -1.771\,\text{V}$ and $I_D = 3.359\,\text{mA}$

p Channel JFET

The JFET model and calculations presented in these slides were for an *n* channel JFET, meaning that the current flows through the *n* substrate. There is also a *p* channel JFET with similar operation modes and equations.

p channel JFETs were not discussed in 3N03.

Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

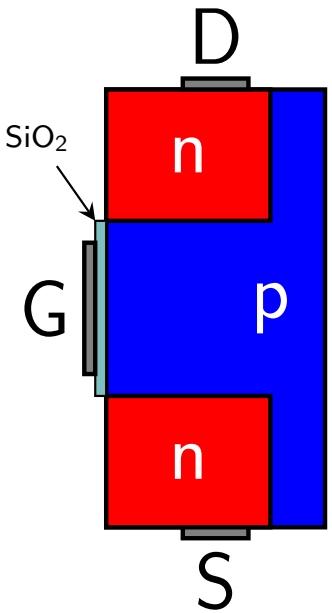
The MOSFET

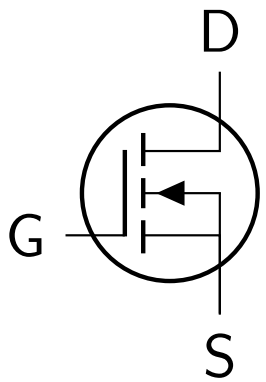
Being a field effect transistor, MOSFETs have a lot in common with JFETs. The major difference is a thin metal oxide (SiO_2) insulator on the gate, completely isolating the gate from the *pn* junction.

As with JFETs, MOSFETs can be either *n* or *p* channel, depending on how the substrates are doped. There are two subclasses of MOSFETs: Enhancement and Depletion mode, denoted E-MOSFETs and D-MOSFETs, respectively.

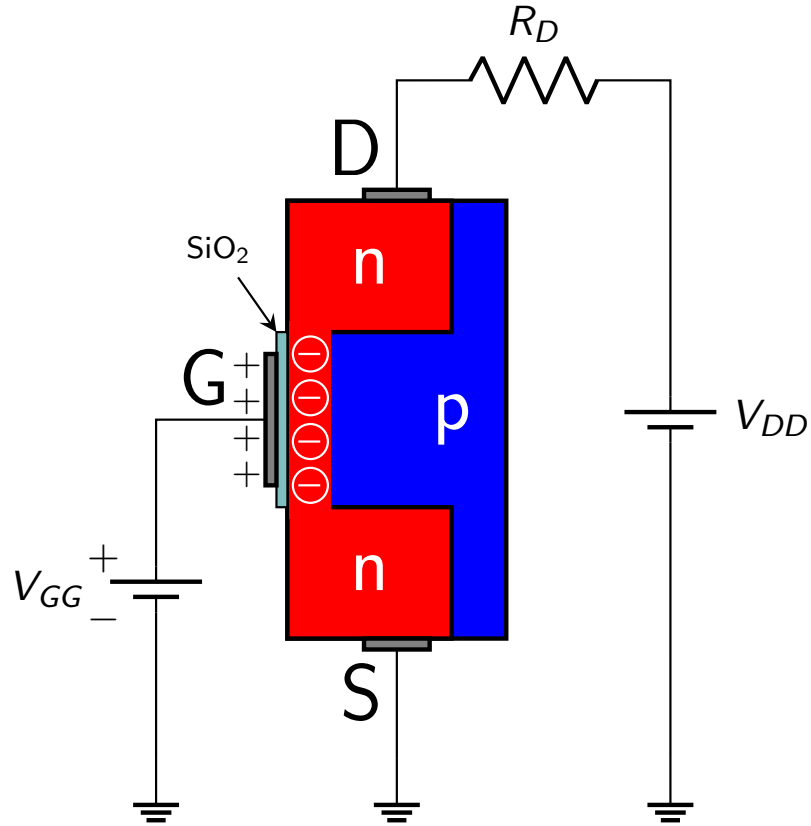
n Channel E-MOSFET

In an enhancement MOSFET, there is initially no channel for current to flow. In an *n* channel E-MOSFET, a positive gate voltage attracts minority electrons from the *p* substrate to establish an *n* channel for current to flow across.



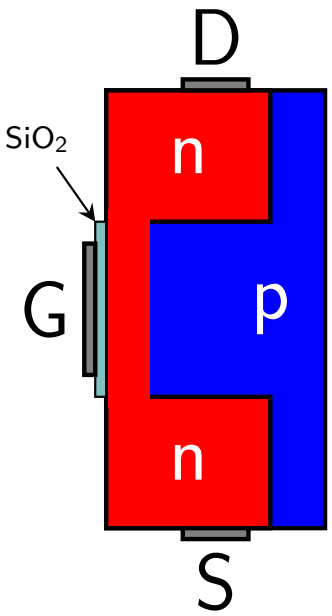


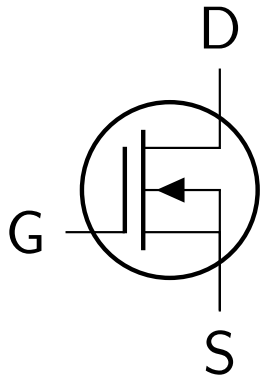
Circuit Symbol



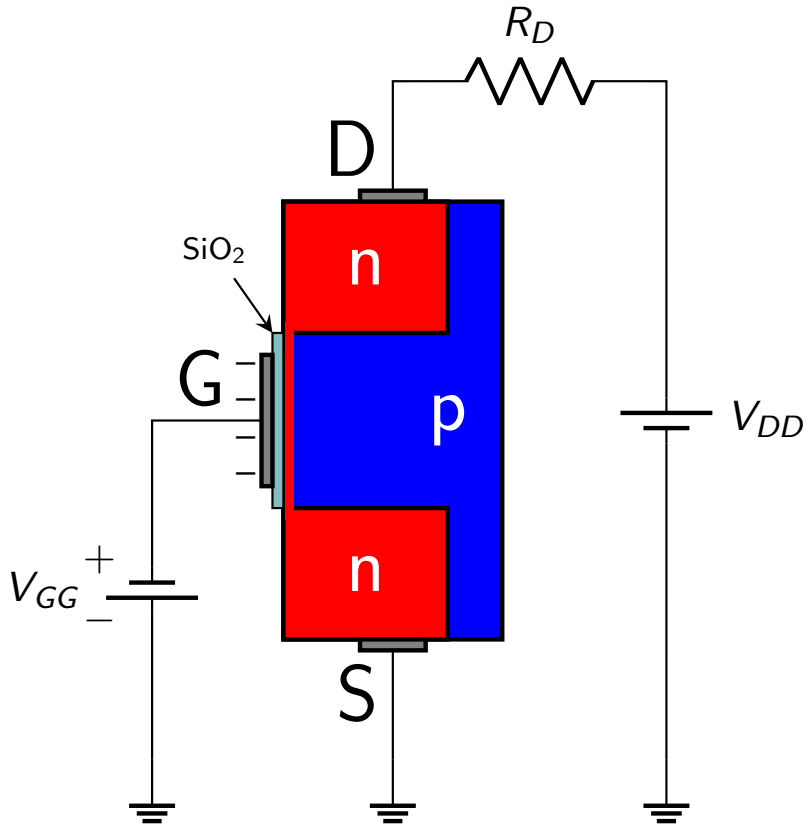
n Channel D-MOSFET

In a depletion MOSFET, there is an existing *n* channel for current to flow. A negative gate voltage will attract positive carriers, depleting the channel and reducing current flow. A positive gate voltage will further enhance the channel and let even more current through.



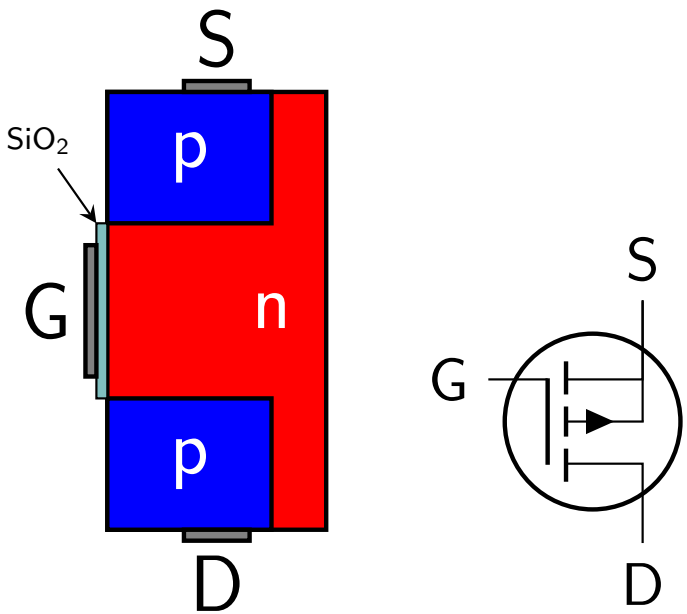


Circuit Symbol

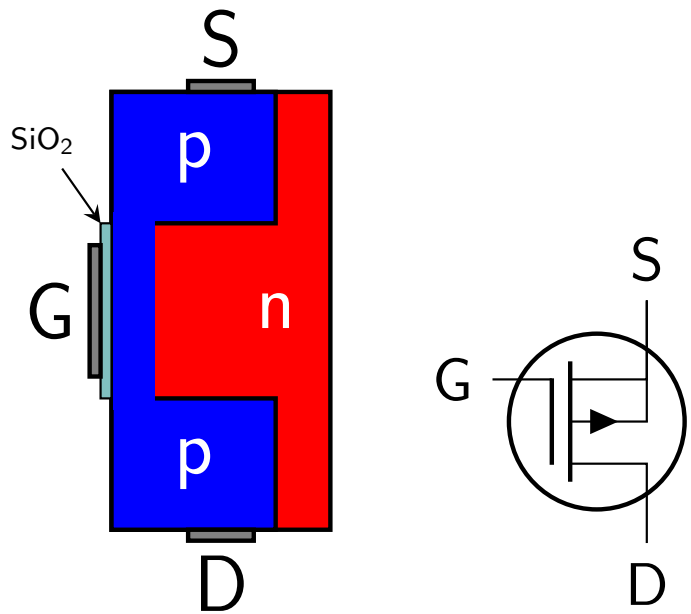


p Channel MOSFET

The *p* channel MOSFETs have the opposite substrate structure as their *n* channel counterparts. Because of this, a negative voltage is required to enhance the channel and a positive voltage will deplete it.



p Channel E-MOSFET



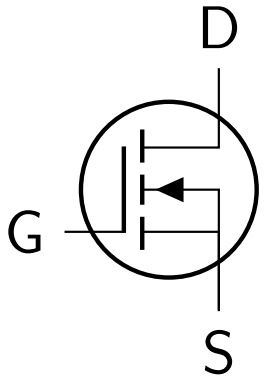
p Channel D-MOSFET

MOSFET Symbols

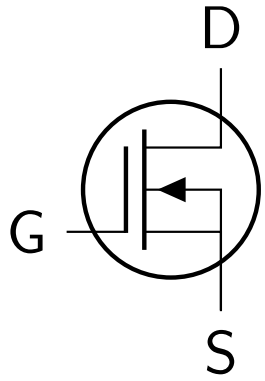
To differentiate between *n* and *p* channel, look at the direction of the arrow. An *n* channel arrow points i**n**.

Also notice that the Source and Drain terminals are swapped between *n* and *p* channel transistors.

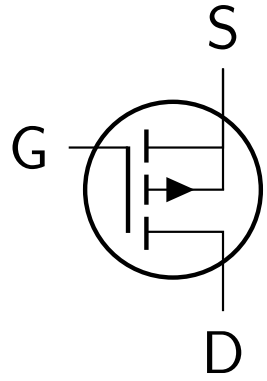
To differentiate enhancement and depletion mode, look at the vertical bar. A broken bar means there is no existing channel, so it is enhancement mode. A solid bar indicates a channel, so it is depletion mode.



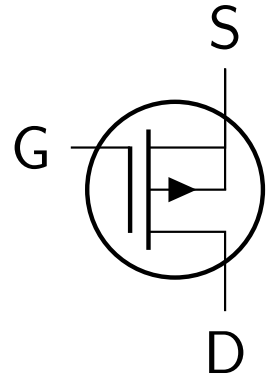
n Channel, Enhancement



n Channel, Depletion



p Channel, Enhancement



p Channel, Depletion

MOSFET Transfer Curve

MOSFETs, like JFETs, are voltage controlled current switches. For both n and p channel transistors, and for both enhancement and depletion mode, the relevant voltage is $V_{GS} = V_G - V_S$.

Remember that the source is on the low side of an n channel MOSFET but on the high side of a p channel.

As with JFETs, there is a quadratic relationship between I_D and V_{GS} in the active / saturation region of a MOSFET.

D-MOSFET Transfer Curve

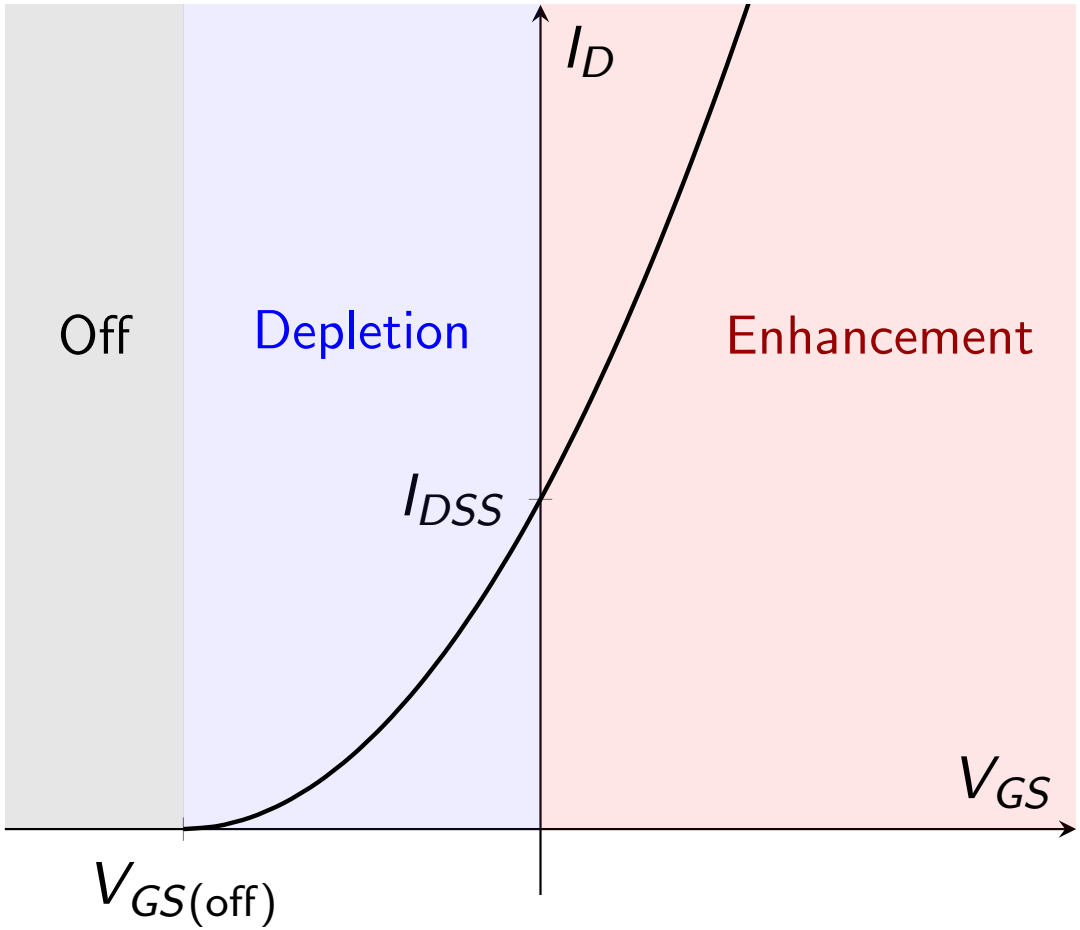
A D-MOSFET can conduct current when $V_{GS} = 0$, so it makes sense to define I_{DSS} in the same way as for JFETs. The voltage where the channel is completely depleted is called $V_{GS(\text{off})}$. The transfer curve is

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$$

Unlike JFETs, both positive and negative V_{GS} values are safe and frequently used in circuits, so this curve is valid on both sides of the I_D axis.

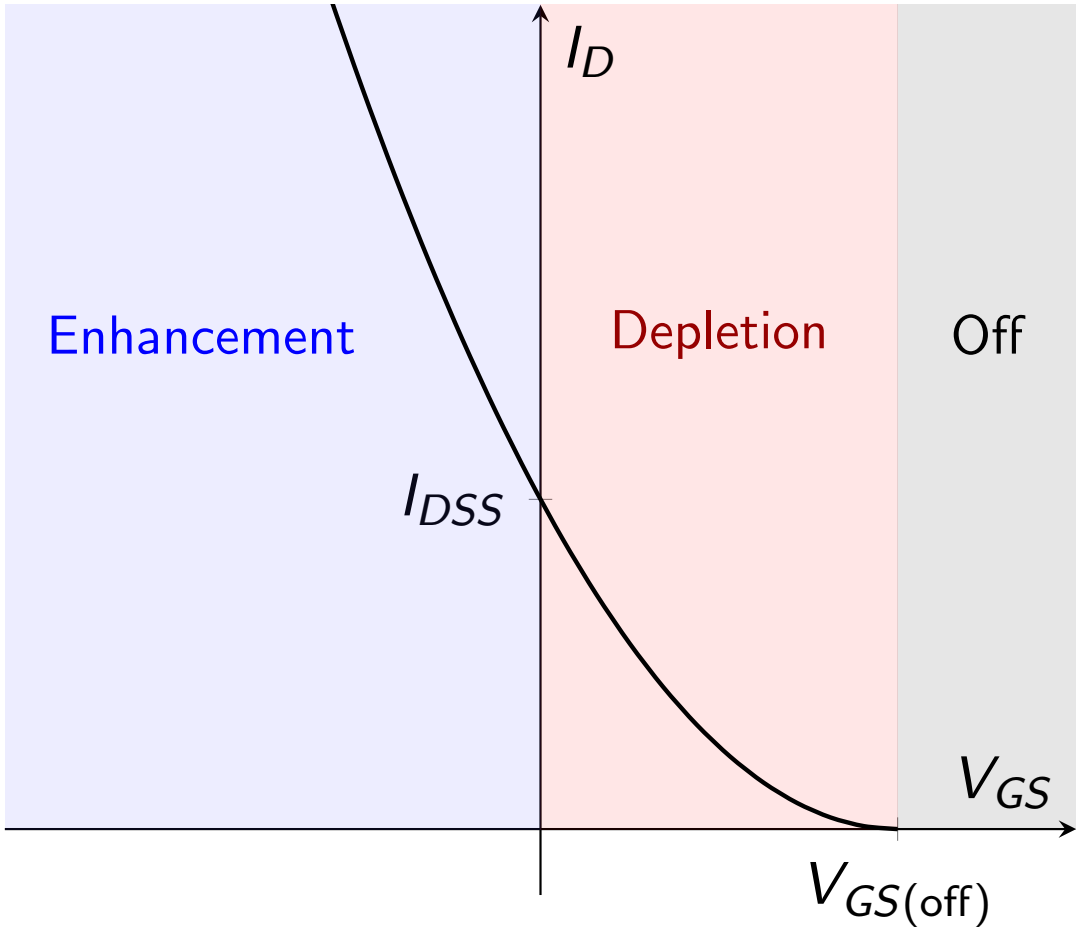
n Channel D-MOSFET Transfer Curve

The *n* channel is depleted by applying a negative gate voltage, so $V_{GS(\text{off})}$ will be negative.



p Channel D-MOSFET Transfer Curve

The p channel is depleted by applying a positive gate voltage, so $V_{GS(\text{off})}$ will be positive.



E-MOSFET Transfer Curve

Enhancement MOSFETs do not conduct current when $V_{GS} = 0$. Instead, they require the voltage to surpass some threshold to start conducting. Call this threshold voltage $V_{GS(\text{th})}$.

There is no meaning to I_{DSS} for an E-MOSFET since it does not conduct current when $V_{GS} = 0$. Therefore, the scaling factor K on the expression has no physical meaning.

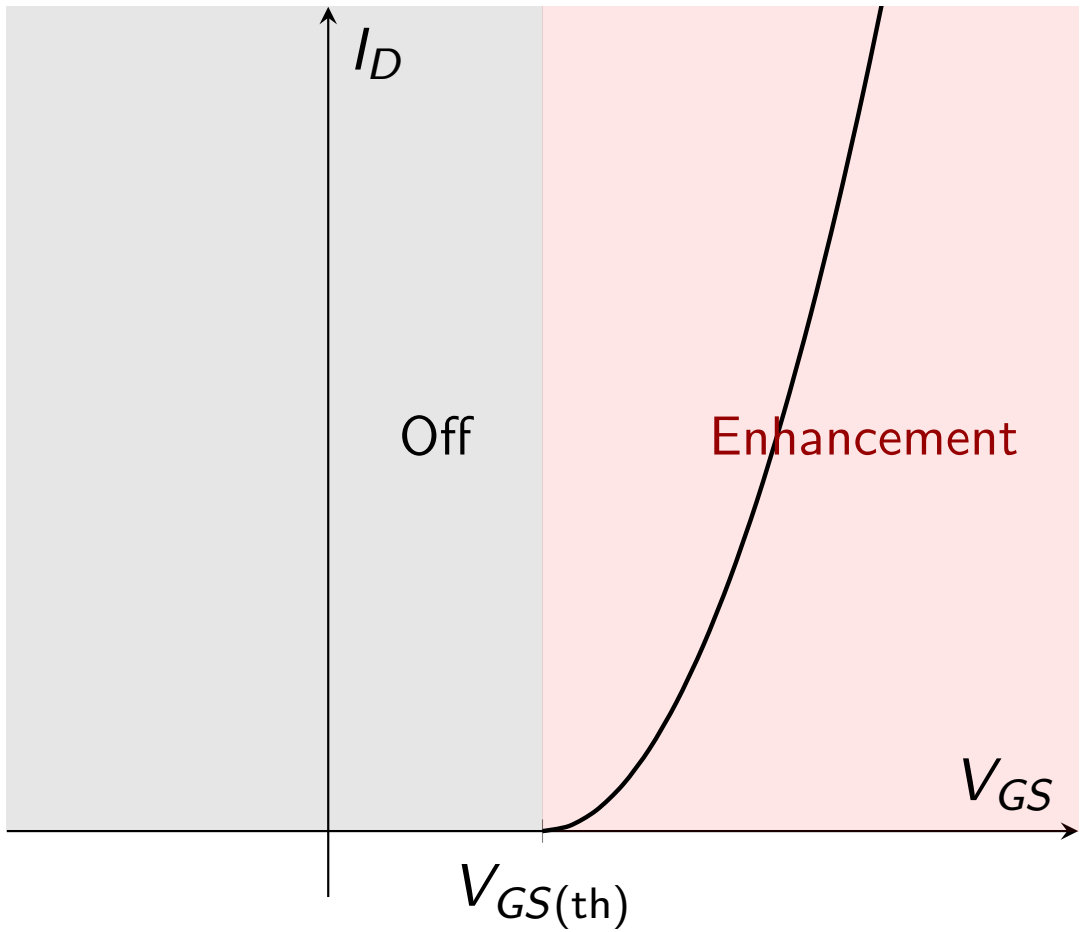
$$I_D = K\left(V_{GS} - V_{GS(\text{th})}\right)^2$$

The units of K are $\frac{\text{A}}{\text{V}^2}$ or $\frac{\text{mA}}{\text{V}^2}$

Remember to only consider the section of the parabola beyond $V_{GS(\text{th})}$, otherwise the transistor does not conduct any current.

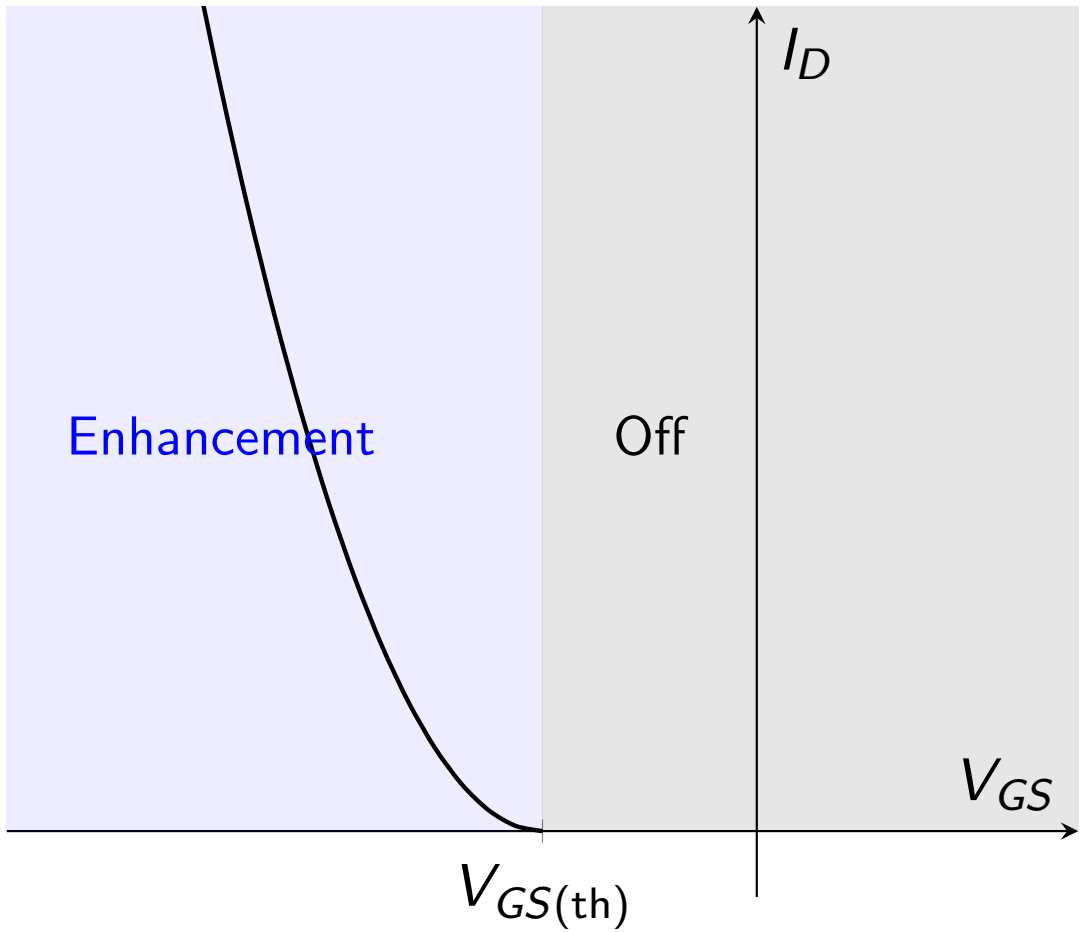
n Channel E-MOSFET Transfer Curve

The *n* channel is enhanced by applying a positive gate voltage, so $V_{GS(\text{th})}$ will be positive.



p Channel E-MOSFET Transfer Curve

The p channel is enhanced by applying a negative gate voltage, so $V_{GS(\text{th})}$ will be negative.



MOSFET Transconductance

Transconductance g_m is still defined as the derivative of the transfer curve at some V_{GS}. This means that if V_{GS} changes by a small voltage $\mathrm{d}V$, then the current I_D will change by $g_m \mathrm{d}V$.

You can easily find g_m by differentiating the appropriate transfer curve at its Q-Point.

Solving MOSFET Circuits

After identifying the channel and type of MOSFET in the circuit, follow the same steps as when analyzing a JFET circuit:

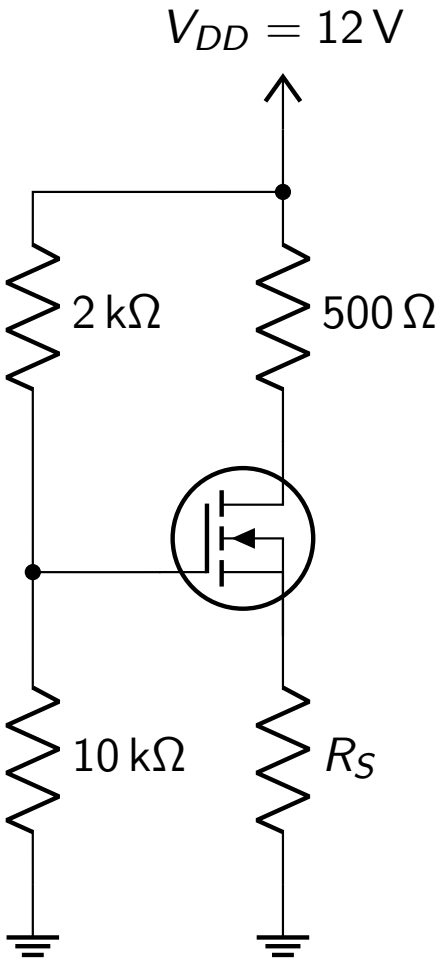
1. Solve for V_G and V_S in terms of I_D and combine to get an expression for V_{GS}.

2. Use the appropriate transfer curve equation to gain a second equation for the system.

3. Solve the system of equations (either analytically or graphically by drawing the load line).

n Channel E-MOSFET Q-Point Example

Determine the value of R_S such that $I_D = 2\,\text{mA}$. Given: $K = 6\,\text{mA/V}^2$ and $V_{GS(\text{th})} = 4\,\text{V}$.



First find V_{GS} from the transfer curve

$$2\,\text{mA} = 6\,\text{mA/V}^2\,(V_{GS} - 4\,\text{V})^2$$
$$V_{GS} = 4.577\,\text{V}$$

Solve V_G and V_S to get an expression for V_{GS}

$$V_G = \left(\frac{10\,\text{k}\Omega}{2\,\text{k}\Omega + 10\,\text{k}\Omega}\right) 12\,\text{V} = 10\,\text{V}$$
$$V_S = I_D R_S = (2\,\text{mA})\,R_S$$
$$V_{GS} = 10\,\text{V} - (2\,\text{mA})\,R_S = 4.577\,\text{V}$$

Solve for R_S

$$R_S = 2.711\,\text{k}\Omega$$

FET Amplifiers

FET Amplifiers

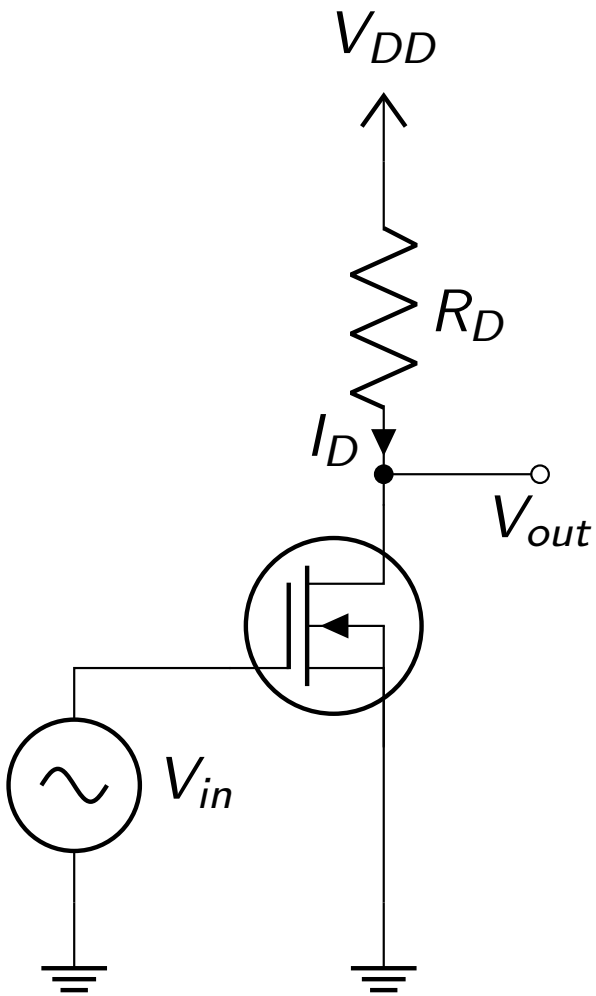
Field Effect Transistors are very useful in constructing amplifiers since they can modulate a large current based on a small voltage.

Additionally, since there is no current flow across the gate, a FET amplifier isolate and amplify a very low power signal.

Analyzing transistor amplifiers requires a good understanding of Q-Points, transconductance, and general circuit analysis techniques.

Building an Amplifier

Possibly the simplest FET amplifier uses an n channel D-MOSFET with the output voltage at the drain terminal.



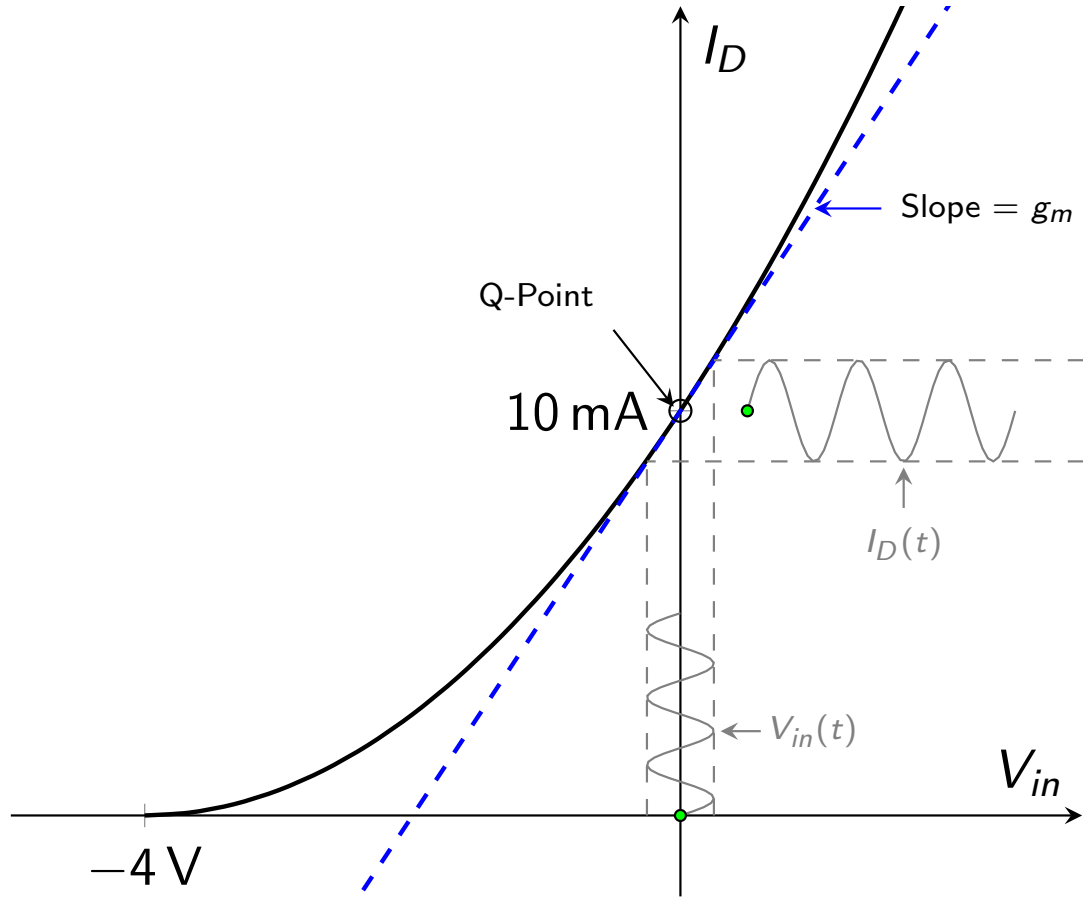
Since $V_G = V_{in}$ and $V_S = 0$, $V_{GS} = V_{in}$. As a D-MOSFET, that means the drain current is

$$I_D = I_{DSS}\left(1 - \frac{V_{in}}{V_{GS(\text{off})}}\right)^2$$

Suppose V_{in} is a small amplitude signal. Then the transfer curve can be approximated by straight line that is tangent to the curve.

The tangency point will be the DC component of V_{in}, which precisely means that the line is tangent to the Q-Point, and since transconductance is the derivative of the curve at the Q-Point, the tangent line has a slope of g_m.

For example, suppose the D-MOSFET has $I_{DSS} = 10\,\text{mA}$ and $V_{GS(\text{off})} = -4\,\text{V}$, and that the input is a $0.25\,\text{V}$ amplitude sine wave with no DC component.



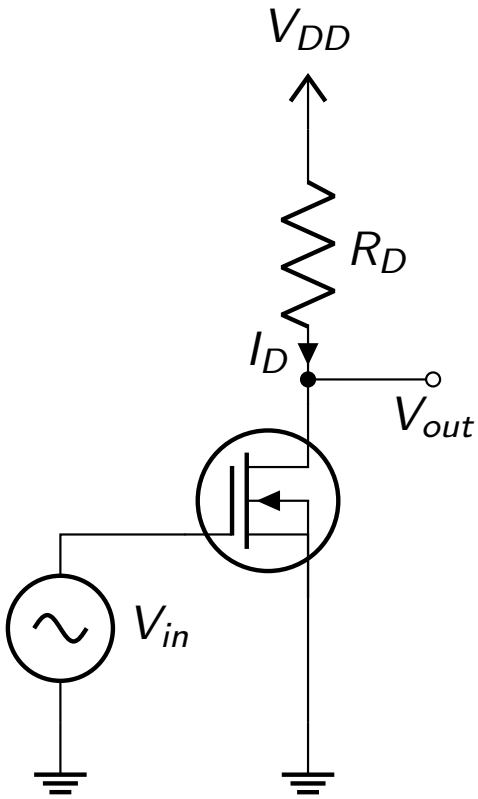
Let's analyze the previous graph

- The DC component of $V_{in} = V_{GS}$ is 0, so the Q-Point is the point on the transfer curve corresponding to $V_{GS} = 0$, which happens to have a current of $I_D = I_{DSS}$
- The derivative of the transfer curve at the Q-Point is $5\frac{\text{mA}}{\text{V}}$, so this is g_m
- For a small signal, the transfer curve can be approximated by a straight line, which is the line passing through $(0\,\text{V}, 10\,\text{mA})$ with slope g_m.
- Now the output signal $I_D(t)$ can be approximated by

$$I_D(t) = g_m V_{in}(t) + I_{D(\text{Q-Point})} = \left(5\frac{\text{mA}}{\text{V}}\right) V_{in}(t) + 10\,\text{mA}$$

- This approximation is very good for small amplitude inputs since the tangent line approximates the curve best over a small interval.

We return to the circuit to complete the amplifier analysis.



This equation calculates the current as a function of V_{in} which can be used to get an expression for V_{out}

$$\begin{aligned} V_{out} &= V_{DD} - I_D R_D \\ &= V_{DD} - R_D(g_m V_{in} + I_{D(\text{Q-Point})}) \end{aligned}$$

This equation shows that V_{out} is inversely related to V_{in}; as V_{in} rises, more current can flow, causing a larger drop across R_D, meaning that V_{out} is lower.

Improving the Amplifier – Output Coupling

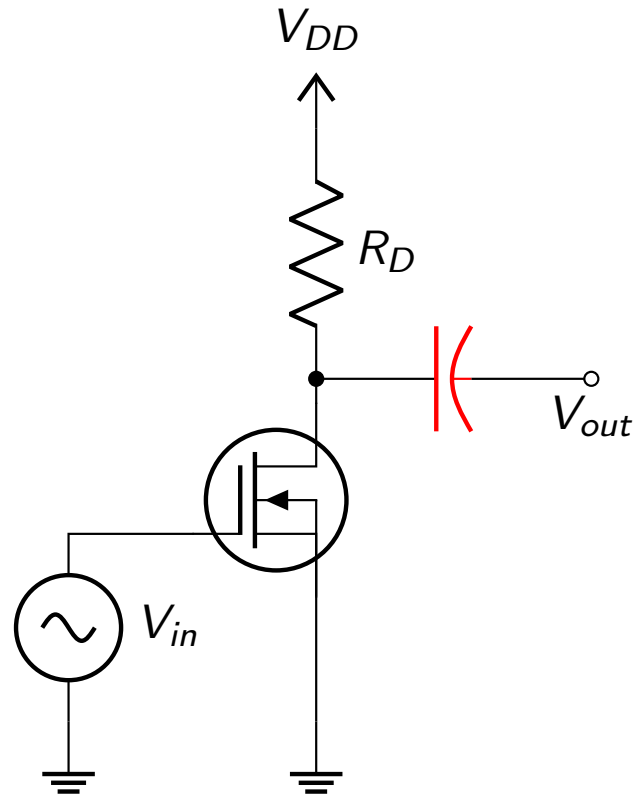
There are several issues with the previous amplifier.

One is the annoying dependence of V_{out} on V_{DD} and $I_{D(\text{Q-Point})}$. These are constant values and do nothing except shift V_{out}.

By introducing a **coupling capacitor** between the drain and V_{out}, only relative changes in the drain voltage are passed to to the output (since capacitors block constant signals).

Now the constant terms are blocked from the output, so

$$V_{out} = -R_D g_m V_{in}$$



Improving the Amplifier – Setting the Q-Point

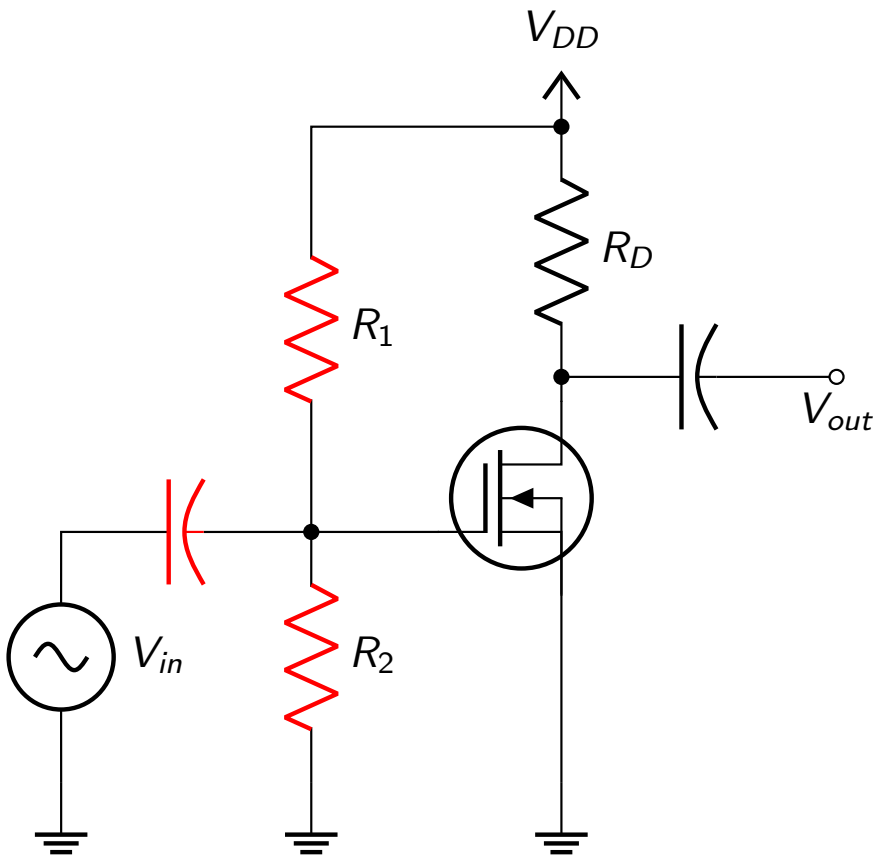
The next issue is setting the Q-Point. The current circuit's Q-Point is determined by the DC value of V_{in}. In practice, this is often 0, restricting our circuit to operating about $V_{GS} = 0$.

This is acceptable for D-MOSFETs, but will damage a JFET (by forward biasing the *pn* junction) and will not activate an E-MOSFETs since the signal will be below the threshold voltage.

A better system will allow the Q-Point bias to be configured independent of the signal.

Improving the Amplifier – Voltage Divider Bias

A voltage divider was used for biasing static circuits earlier. If the input signal is coupled to the middle of a voltage divider by another capacitor, then the AC component of the input signal will now modulate about the voltage divider bias.



Improving the Amplifier – Voltage Divider Bias

The Q-Point voltage is $V_G - V_S = \left(\frac{R_2}{R_1+R_2}\right) V_{DD}$ which then determines g_m. For small V_{in} signals, the gate voltage will vary with the same amplitude as V_{in}, so the change in current I_D is still $g_m V_{in}$. The output is now

$$V_{out} = -R_D g_m V_{in}$$

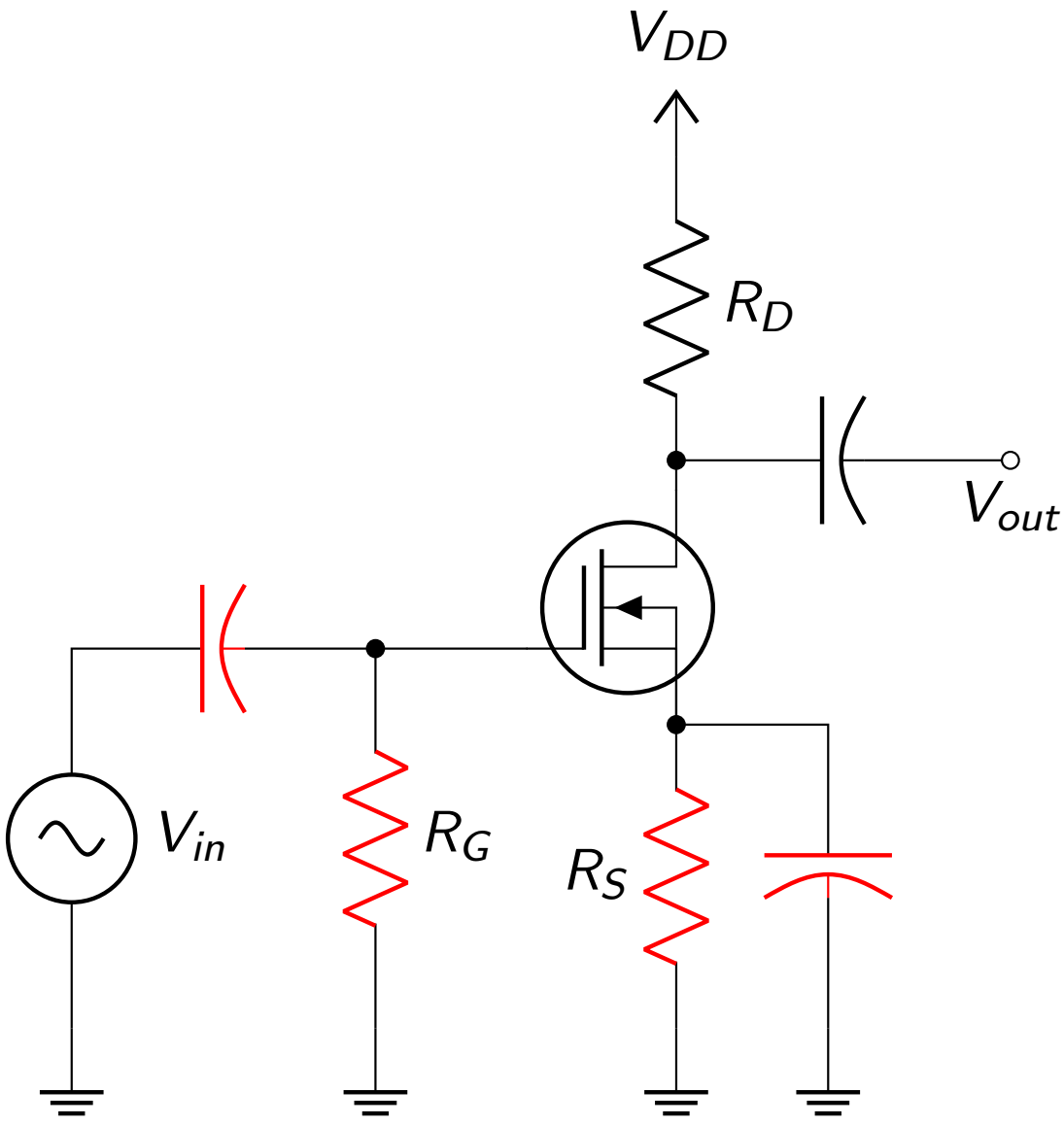
which is the same as the previous slide, but this configuration allows g_m to be set manually using R_1 and R_2, and it allows other types of FETs to be used in the circuit.

Improving the Amplifier – Self-Biasing

A different way to manually set the Q-Point is to self-bias the transistor by adding a resistor at the source. The voltage divider circuit is not used, instead a resistor pulls the gate to ground, so $V_G(\text{Q-Point}) = 0\,\text{V}$. The input is still coupled by a capacitor, causing V_G to modulate about 0 V with V_{in}.

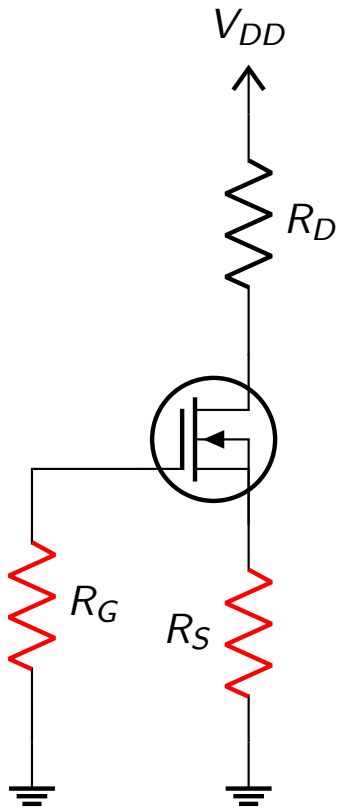
A coupling capacitor is placed in parallel to the source resistor. This allows the small changes in I_D to bypass R_S so that the source voltage remains constant.

Improving the Amplifier – Self-Biasing



Self-Biased Amplifier – DC Analysis

To find the Q-Point, analyze the system under V_{in} = constant. With no frequency modulation, all capacitors act like open switches, so they can be disconnected.



This leaves a regular self-biased transistor, for which we have already shown how to solve the Q-Point.

Closing remarks

The amplifiers had the input on the gate and output at the drain, meaning that the source is "shared" by both the input and output. For this reason, the previous amplifiers are called **common source** amplifiers.

There are also common drain (where the input is at the gate and the output is at the source) and common gate amplifiers (input at source/drain, output at drain/source).

Bipolar junction transistors (BJT) can be used to create similar amplifiers, but as current-controlled devices, their transfer curves and analysis techniques are slightly different from the method for FET amplifiers.