H7

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ENGPHYS 2E04

Introduction

In this lab the task is to create a circuit using 4 JK flip-flops and which outputs a sequence of 4-bit binary numbers to 4 LEDs. The following circuit was created to fulfill that goal. The circuit is composed of 4 JK flip flops and a single “and” gate. The circuit was solved analytically, digitally using the timing diagram plotter in multisim, and physically using the Hantek and breadboard.

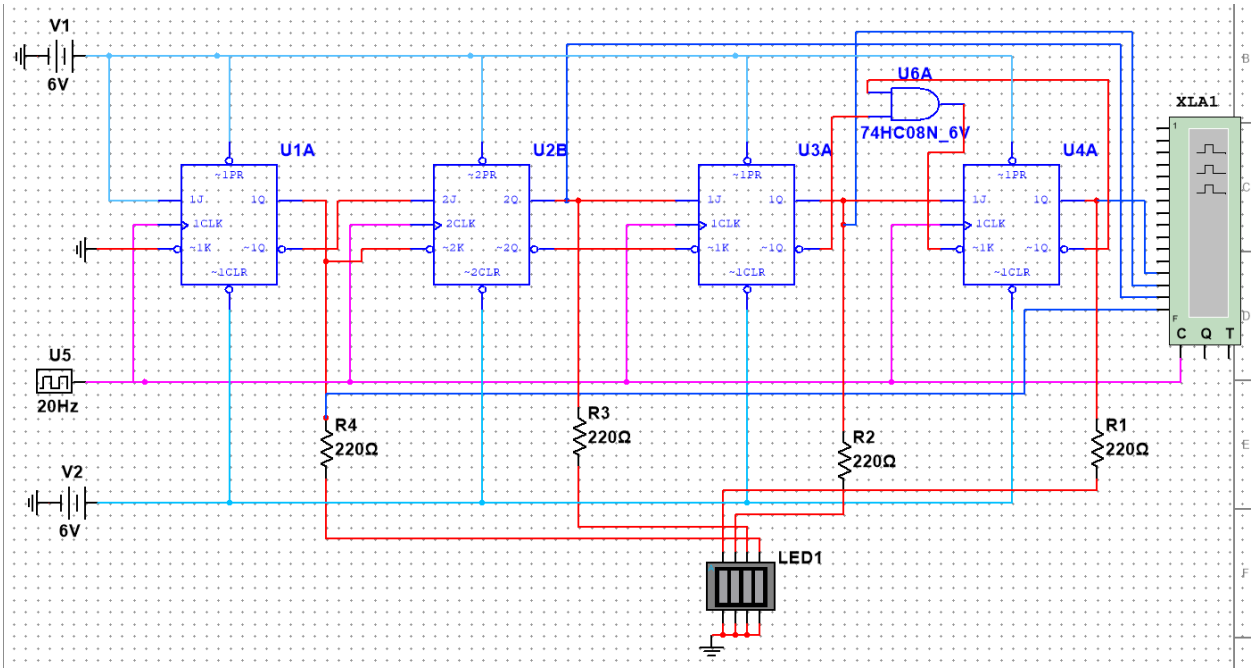


Figure 1: Circuit Diagram

Analytical Solution:

Observing the circuit, we can derive the behavior of each JK flip-flop. Note that all flip-flops are running on the same clock pulse.

J1 = 1

!K1 = 0 --> K1 = 1

Flip-flop 1 is permanently in toggle mode.

J2 = !Q1

K2 = !Q1

Flip-flop 2 is in hold (Q1 = 1) or toggle (Q1 = 0) mode since both J and K take inputs that are equal to Q1.

J3 = Q2

!K3 = !Q2 → K3 = Q2

Flip-flop 3 is in hold (Q2 = 0) or toggle (Q2 = 1) mode since both J and K take inputs that are equal to Q2.

J4 = Q3

K4 = {!Q3 & !Q4}

Flip-flop 4 has undetermined behavior at this time.

The following transition state table outlines the outputs of the flip-flops depending on various inputs, where lowercase "q" represents the previous states, and the uppercase "Q" represents the next state.

q1	q2	q3	q4	Q1	Q2	Q3	Q4
0	0	0	0	1	1	0	0
0	0	0	1	1	1	0	0
0	0	1	0	1	1	1	1
0	0	1	1	1	1	1	0
0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	1
1	0	1	1	0	0	1	0
1	1	0	0	0	1	1	0
1	1	0	1	0	1	1	0
1	1	1	0	0	1	0	1
1	1	1	1	0	1	0	0

Table 2: Transition states table

With this table, we can create a stable loop diagram which outlines the behavior of the circuit and possible starting points.

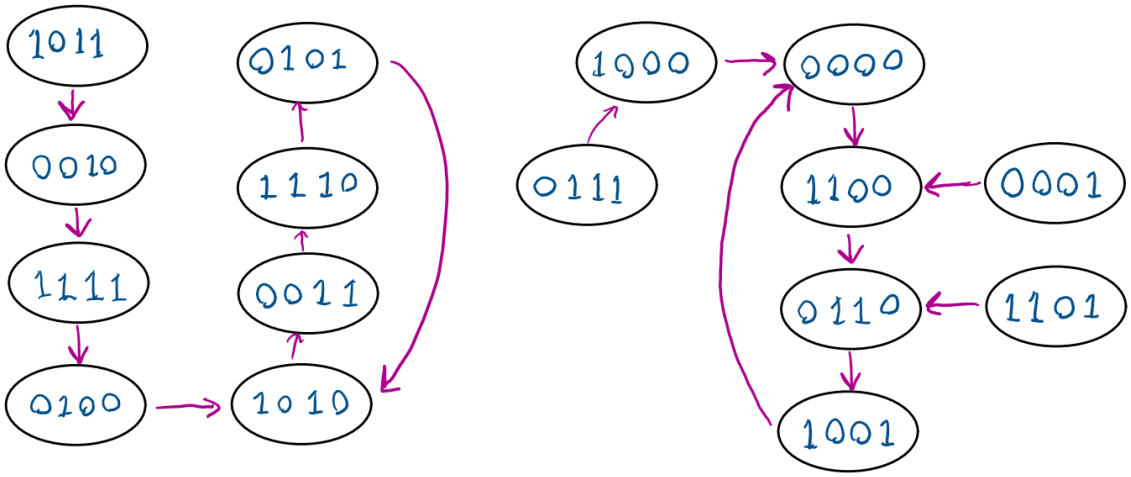


Figure 3: Stable loop diagram

In this case, the circuit has a total of 4 starting states: 1011, 0111, 0001, and 1101. The diagram shows two stable loops, the first ranging from 0000 to 1001, and the other ranging from 0101 to 1010. With the information above, we can make a timing diagram to represent each stable loop with respect to each of their starting states. Note that the stable loop is highlighted in blue.

Starting state of 1011 (loop 1010 → 0101):

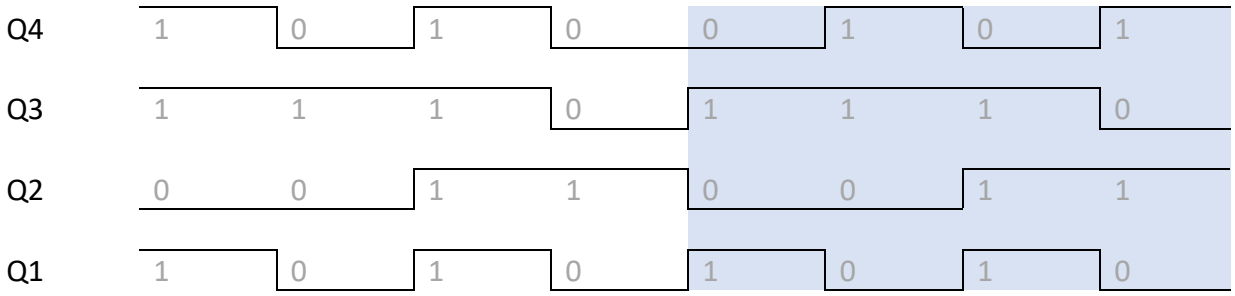


Table 2: Timing Diagram 1011

Starting State of 0111 (loop 0000 → 1001):

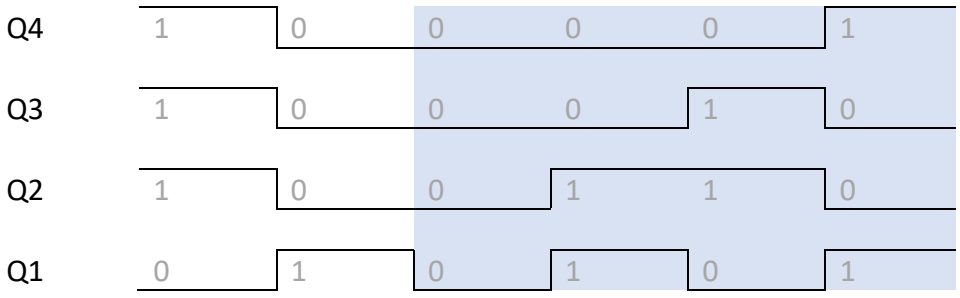


Table 3: Timing Diagram 0111

Starting State of 0001 (loop 0000 → 1001):

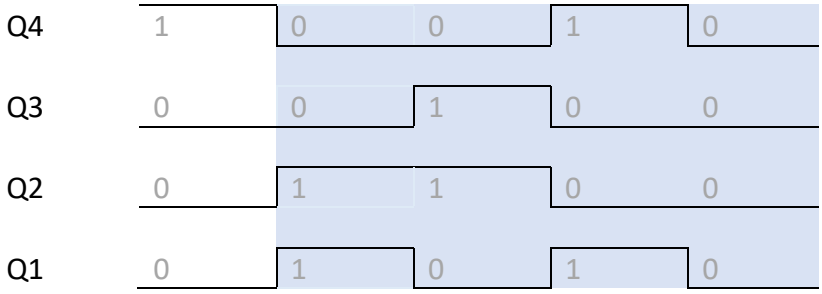


Table 4: Timing Diagram 0001

Starting State of 1101 (loop 0000 → 1001):

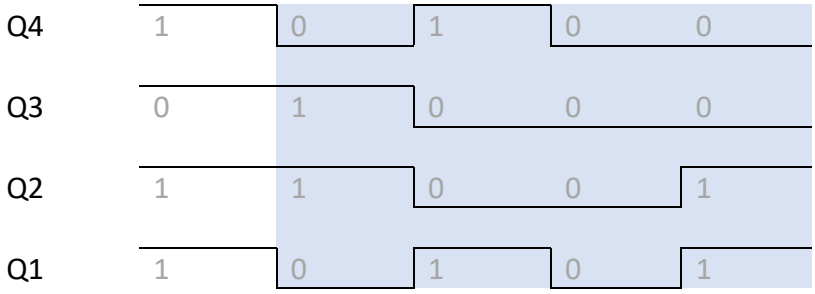


Table 5: Timing Diagram 1101

Digital Solution

The following configuration was used for all multisim solutions, with the preset and clear pins being employed to initiate starting states.

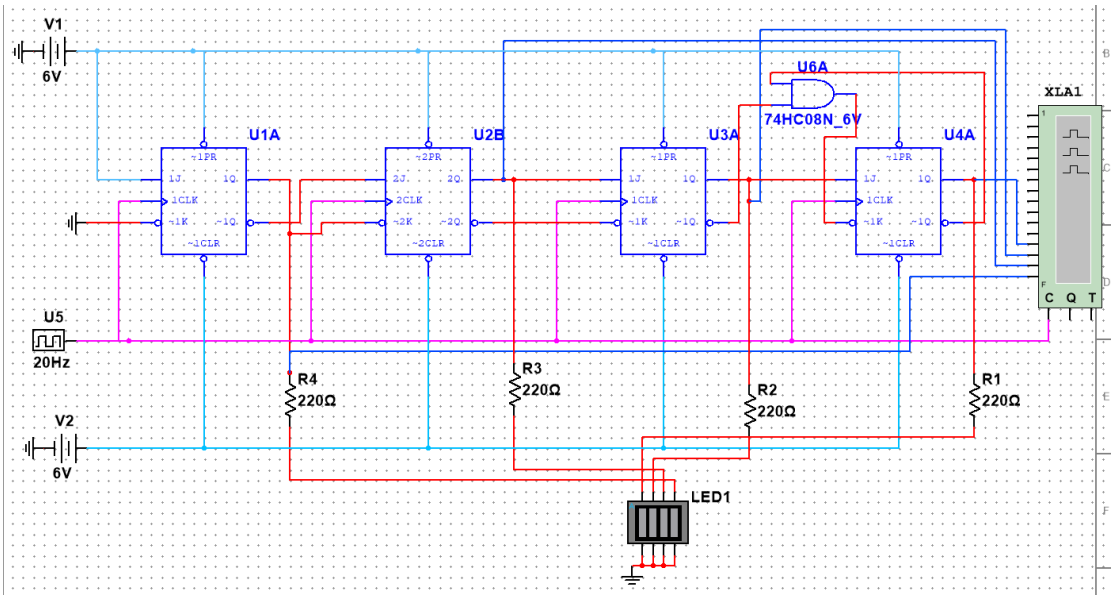
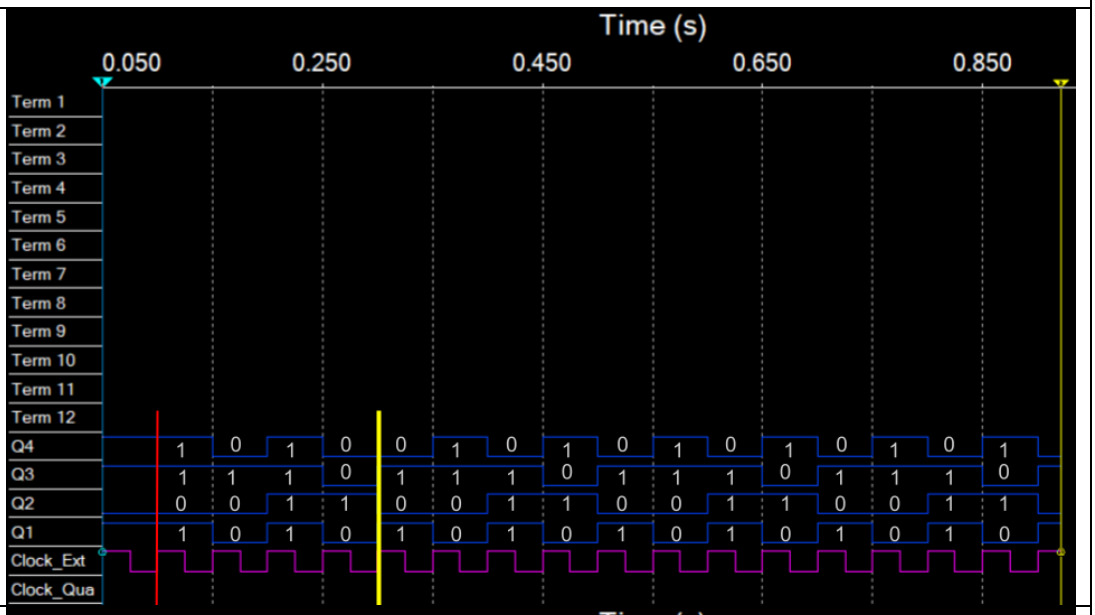
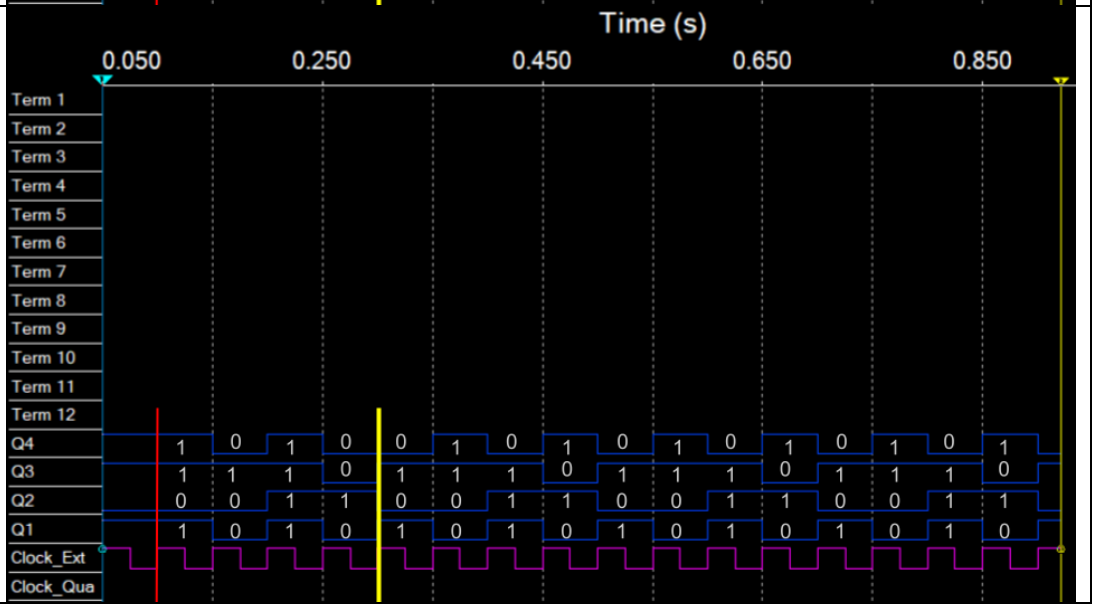


Figure 4: Multisim circuit (light blue is VCC, pink is clock, dark blue is output)

For the starting state of 1011, gates 1, 3, and 4 were preset while gate 2 was cleared using a switch. The expected behavior of this circuit is to loop through the 1010 to 0101 stable loop as described in the analytical solution. The same process was repeated for the starting states of 0111, 0001, and 1101. The following timing diagrams were derived from this process. Note that the beginning of the loop is marked by the yellow line.

Expected Behavior	Timing Diagram
1011 0010 1111 0100 1010 0011 1110 0101 Loop to 1010	
0111 1000 0000 1100 0110 1001 Loop to 0000	

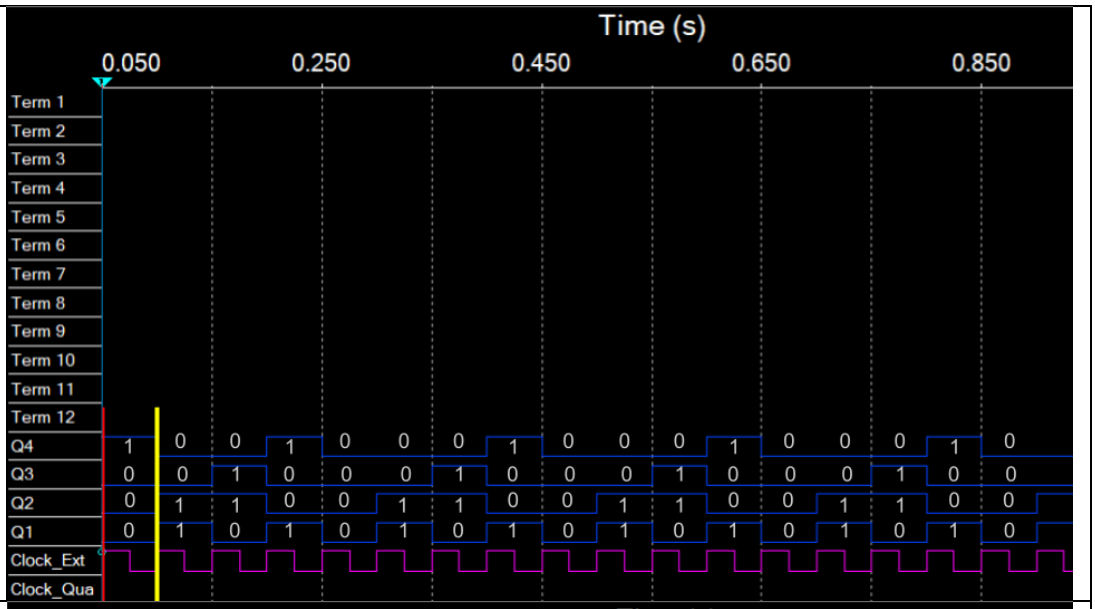
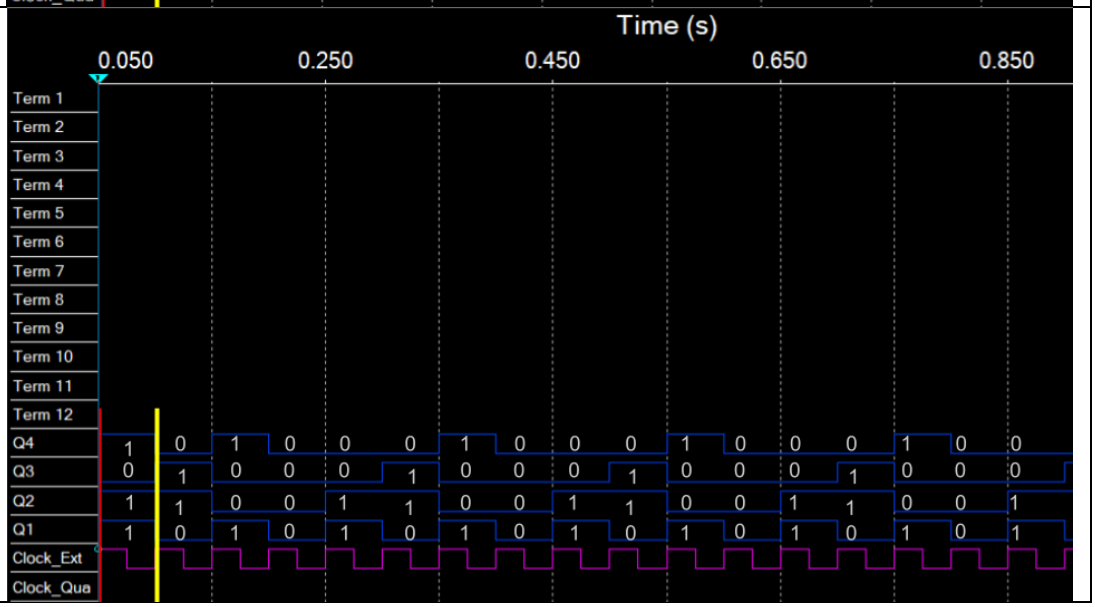
0001 1100 0110 1001 0000 Loop to 1100	
1101 0110 1001 0000 1100 Loop to 0110	

Table 6: Multisim Timing Diagram

From the results above, it can be observed that the multisim results match the analytical results, with expected behavior and actual behavior being the same.

Physical Solution

The following image shows the circuit configuration for the physical build. The build is composed of 2 JK flip-flop chips and 1 “and” chip (also one “not” chip for the clock). The clock output is connected to probe 1 of the Hantek, while the output of JK flip-flop 4 is connected to probe 2. We will be observing the output of the 4th flip-flop for comparison with the multisim

and analytical solution. To initiate the starting states I connected the necessary preset/clear pins to ground switched their connection to the positive line simultaneously.

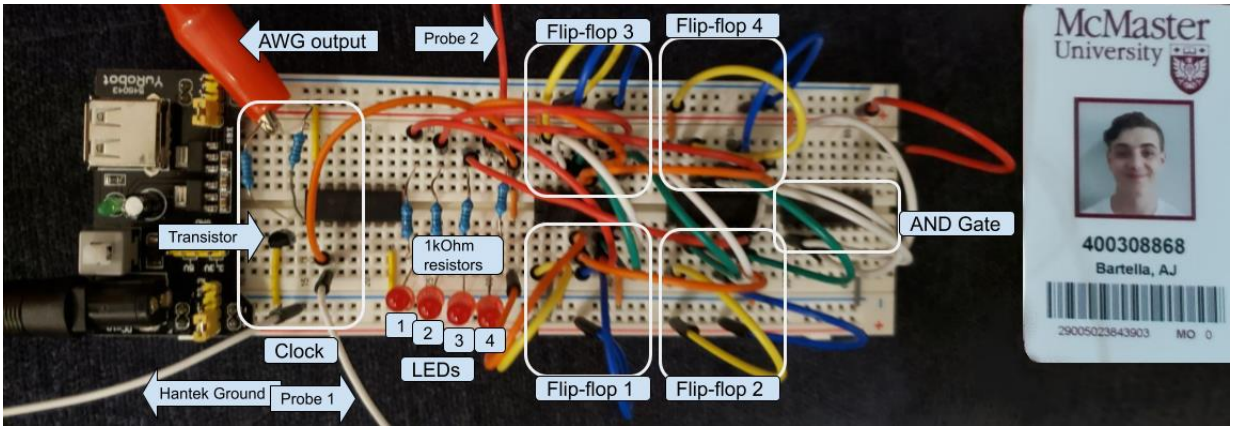
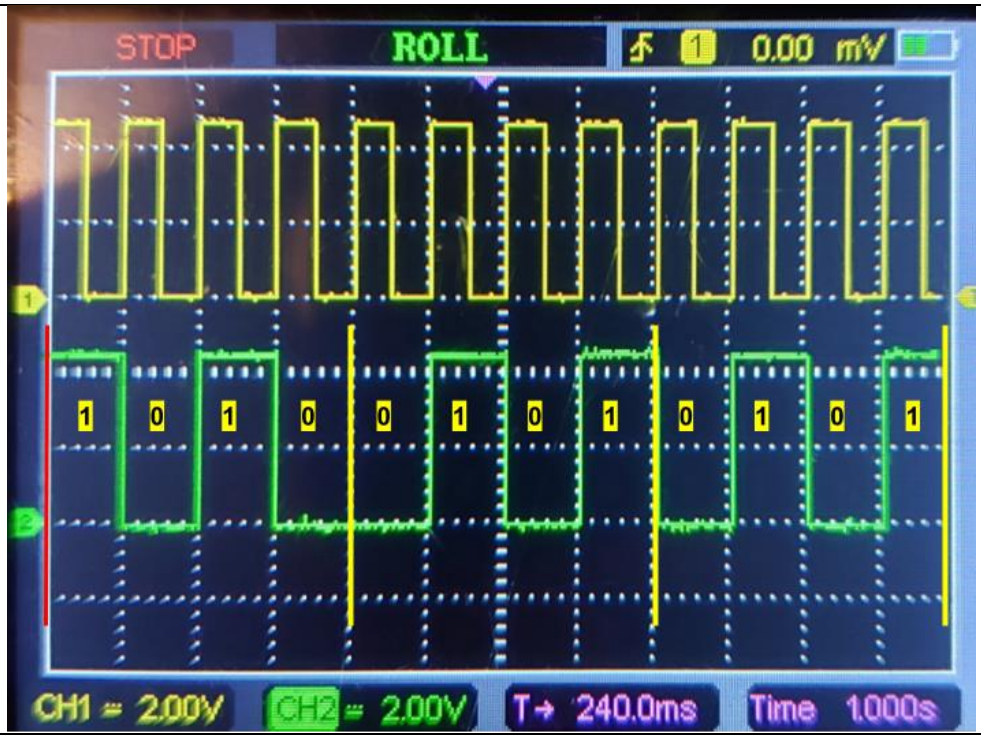
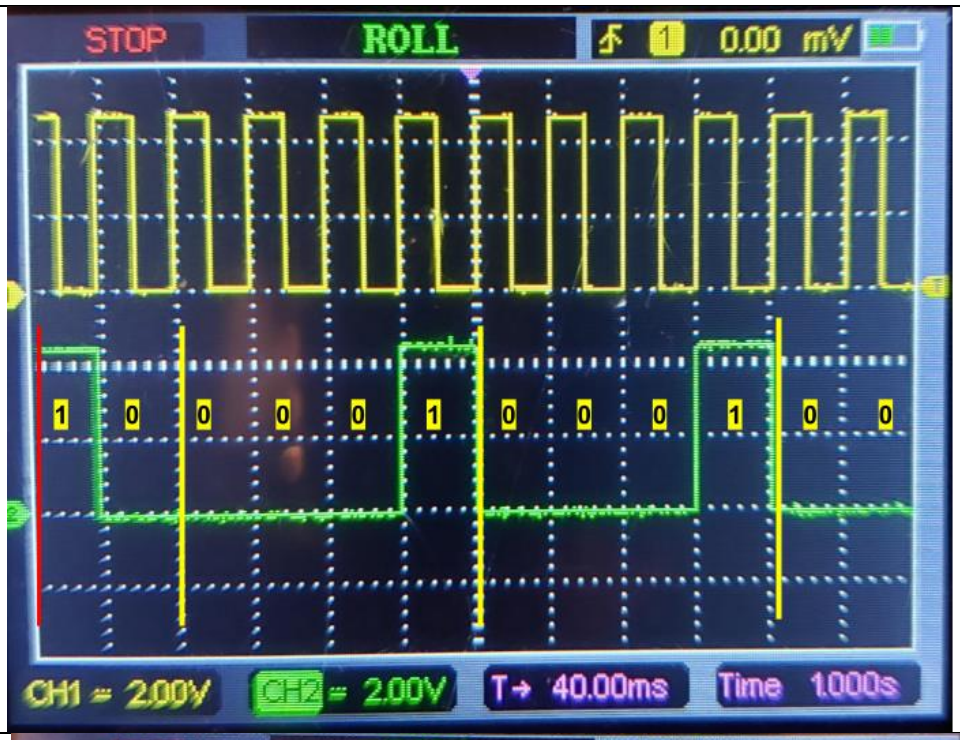
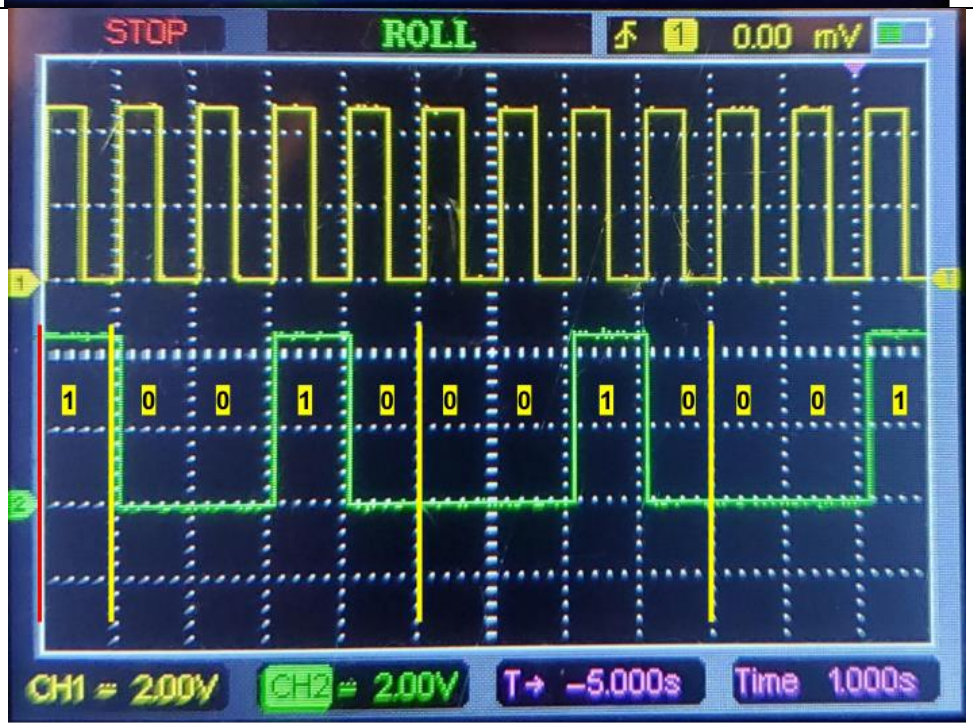


Figure 5: Physical circuit

Note that (aside from the ones connected to the clock) the white jumpers carry the $\bar{Q}$ output of each flip-flop, the green jumpers carry the Q output, the yellow wires are connected to the reset pins, the blue wires are connected to the preset pin, the orange wires carry the clock signal, and the red wires carry the Q output of each JK flip-flop for output to the LEDs.

The following table illustrates the timing diagrams for each of the four starting states. Note the yellow line marking the beginning of every stable loop.

Expected Behavior	Timing Diagram
1011 0010 1111 0100 1010 0011 1110 0101 Loop to 1010	

0111 1000 0000 1100 0110 1001 Loop to 0000	
0001 1100 0110 1001 0000 Loop to 1100	

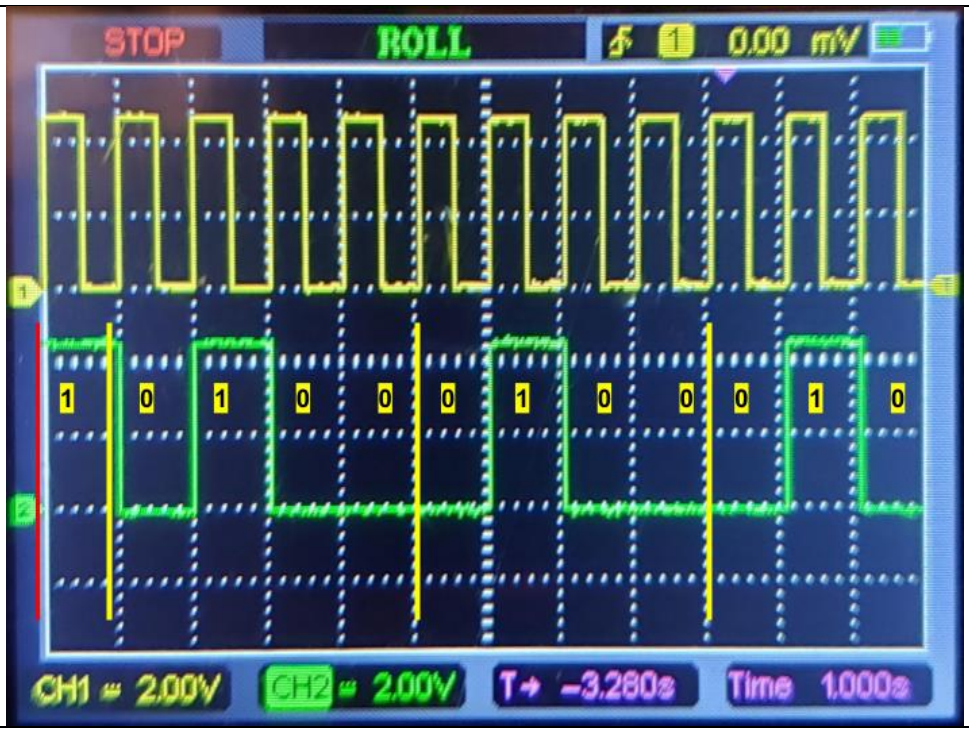
1101 0110 1001 0000 1100 Loop to 0110	

Table 7: Physical Timing Diagram – Flip-Flop 4 and Clock outputs

Observing these results, we can see another exact match with the analytical solution, meaning all expected results were produced for the fourth JK flip-flop. To verify that these positive results carry over onto the other flip-flops, the following video was made demonstrating the results using the LEDs.

https://youtu.be/5VEfO3FOGdA

As determined in the video, the physical, analytical, and digital solutions all match for each starting state and stable loop.

Conclusion

The goal of the lab was to create a circuit with 4 JK flip-flops with some combination of gates and observe the output. Analytically, this was done by observing the behavior of each flip-flop and creating timing tables. Digitally this was done using multisim by creating the circuit and using the timing diagram plotter. Physically, this was done using the Hantek and breadboard and by observing the output via LEDs and the oscilloscope. There were no errors I ran into in this lab, and all observed results from each solution method were found to be matching and correct.

I had a great time during this lab. I was really stumped by the analytical portion, but with the help of my classmates the concepts were cleared up and I was able to better understand the behavior of the JK flip-flops and how to predict their outputs properly. After getting over the

analytical solution, the multisim and physical were very easy and straightforward. Though it was confusing keeping track of all the loose wires, I had a lot of fun building the circuit and applying what I have learned.

To conclude, I am greatly enjoying the digital portion of the course so far, and I can't wait to take on the final design project.

Appendix: Enlarged images