PRÁTICA 7
TRANSISTOR BIPOLAR DE JUNÇÃO
Polarização Simples

Revisão

SEL0610 - LABORATÓRIO DE CIRCUITOS ELETRÔNICOS

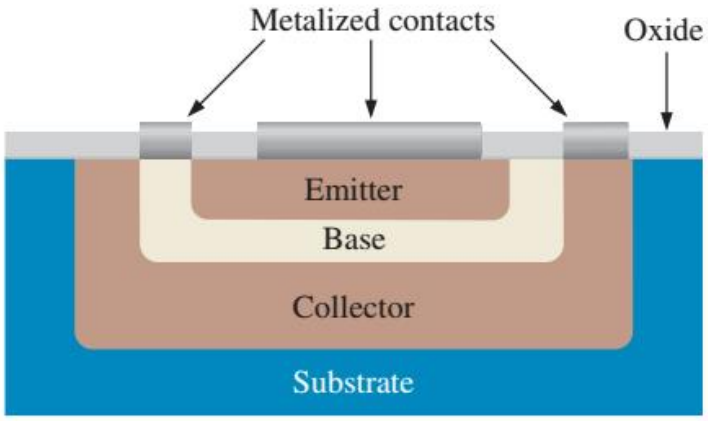
Engenharia de Computação – 6° Período Letivo

Conteúdo

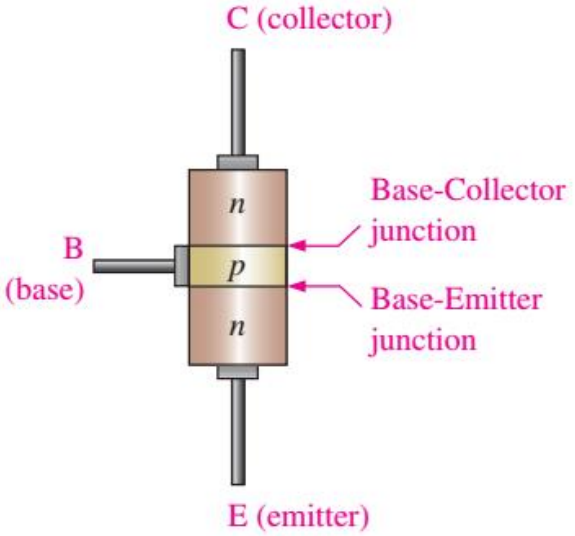
- Estrutura do TBJ
- Operação do TBJ
- Análise de Circuito
- Folha de Dados
- Teste de TBJ
- Empacotamento

Estrutura do TBJ

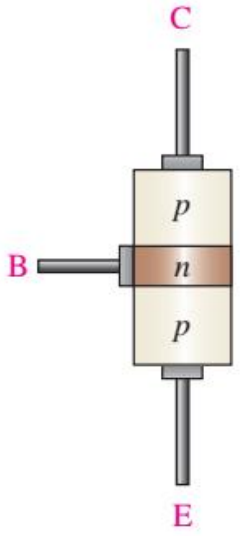
- Estrutura básica de um Transistor Bipolar de Junção



(a) Basic epitaxial planar structure

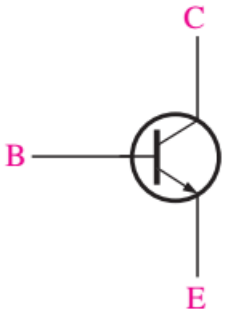


(b) *npn*

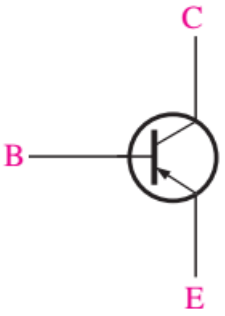


(c) *pnp*

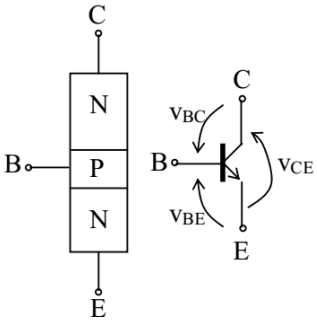
- Simbologia

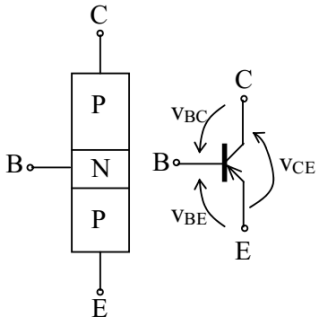


(a) *npn*

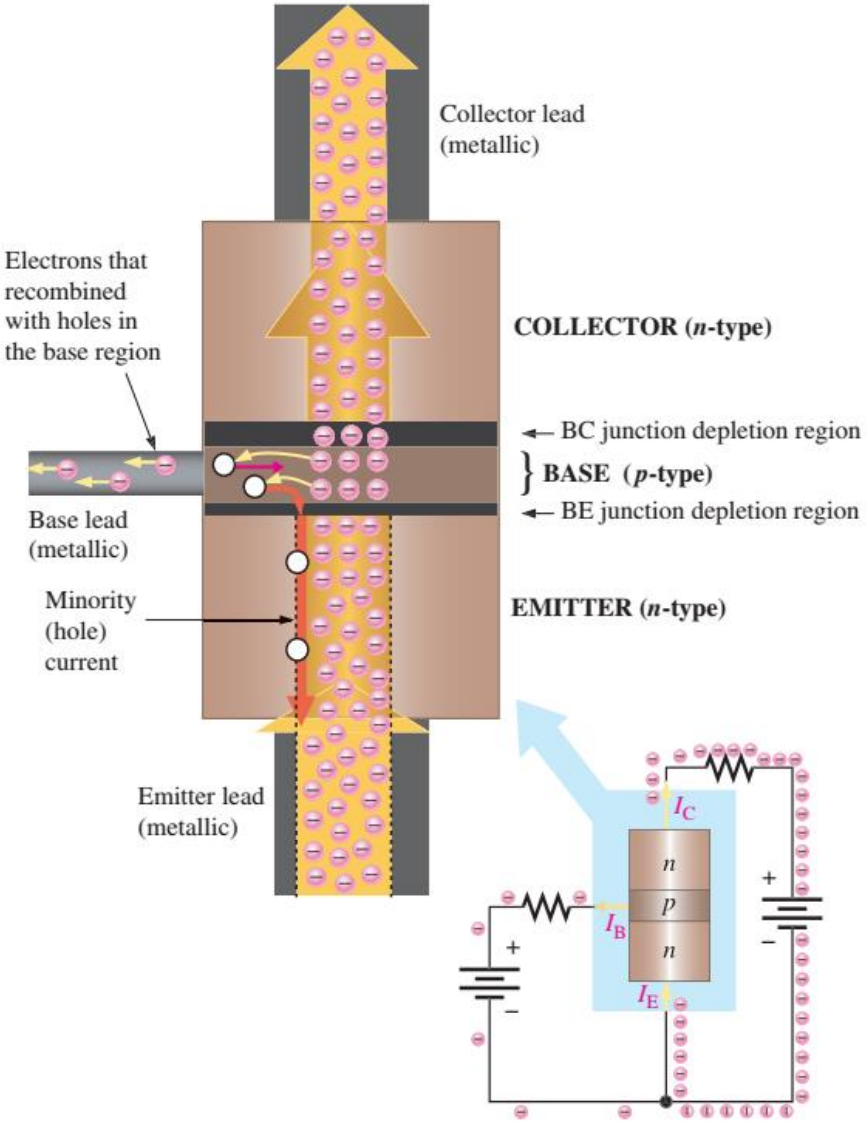


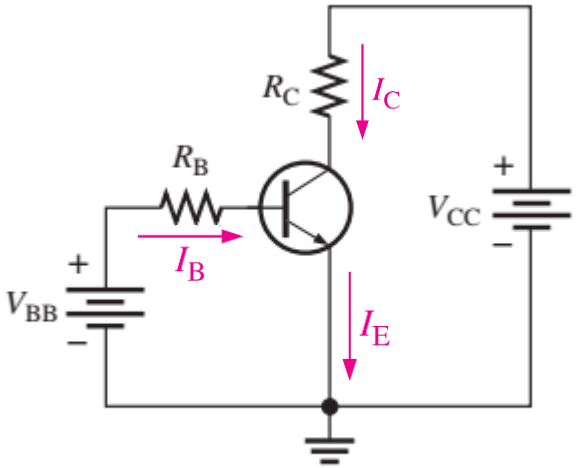
(b) *pnp*



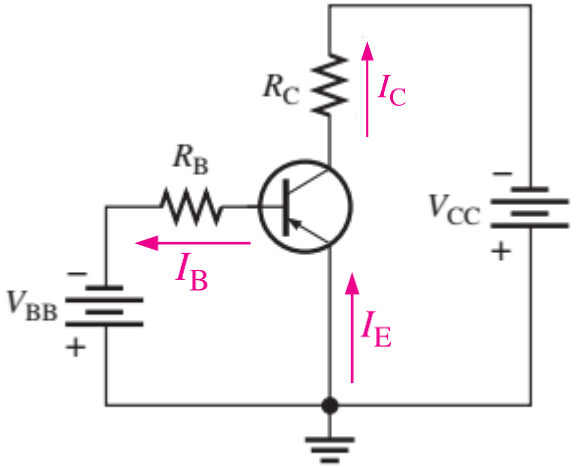


Operação do TBJ





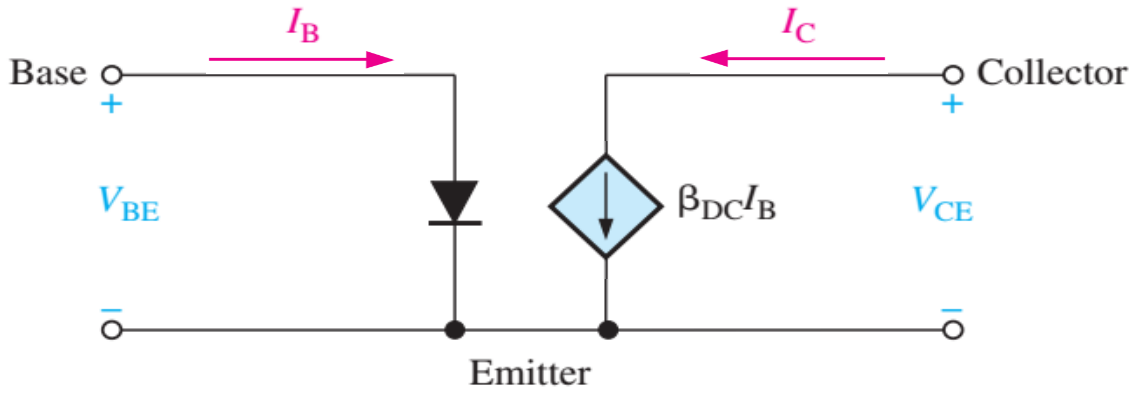
(a) *npn*



(b) *pnp*

Operação do TBJ

Modelo DC Ideal



Ganho de corrente DC

$$\beta_{DC} = \frac{I_C}{I_B}$$

$$h_{FE} = \beta_{DC}$$

$$\alpha_{DC} = \frac{I_C}{I_E}$$

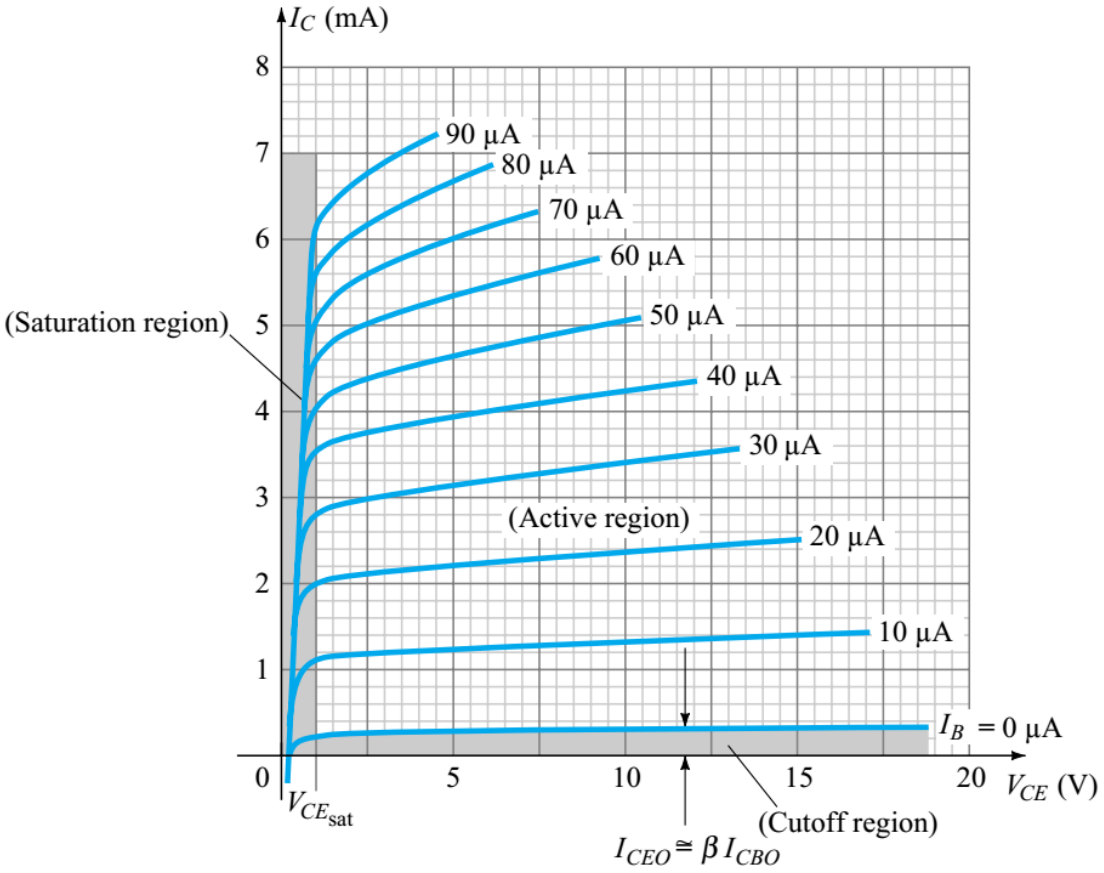
$$I_E = I_C + I_B$$

Operação do TBJ

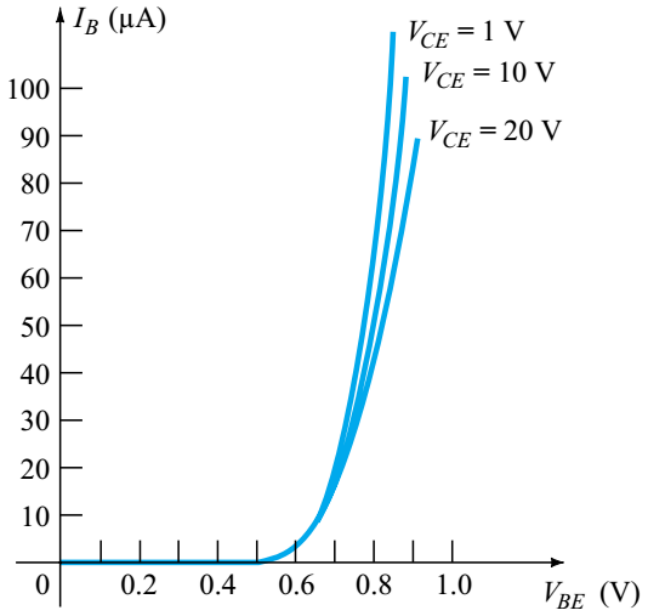
- Região de Corte
  - Junção **Base-Emissor** polarizada **reversamente**
  - Junção **Base-Coletor** polarizada **reversamente**
- Região de Saturação
  - Junção **Base-Emissor** polarizada **diretamente**
  - Junção **Base-Coletor** polarizada **diretamente**
- Região Ativa
  - Junção **Base-Emissor** polarizada **diretamente**
  - Junção **Base-Coletor** polarizada **reversamente**

Operação do TBJ

Curvas características (configuração Emissor-Comum)



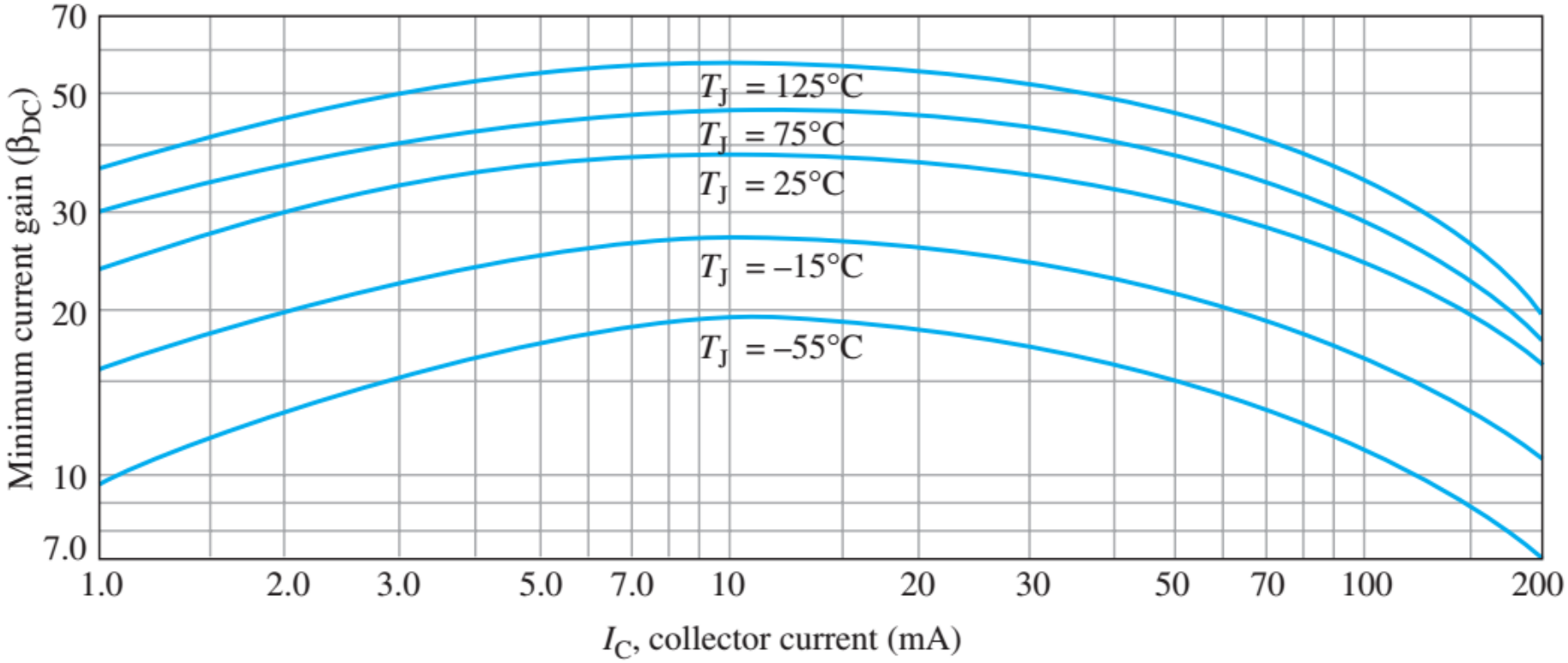
(a)



(b)

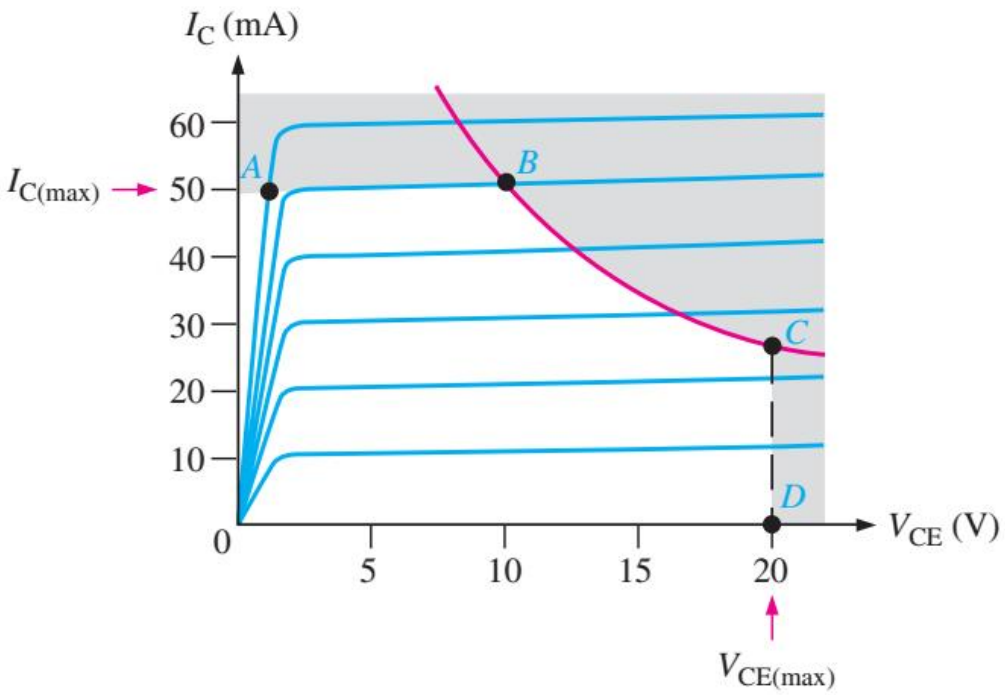
Operação do TBJ

Ganho de Corrente DC em função de corrente de coletor e temperatura



Operação do TBJ

Limites de Operação



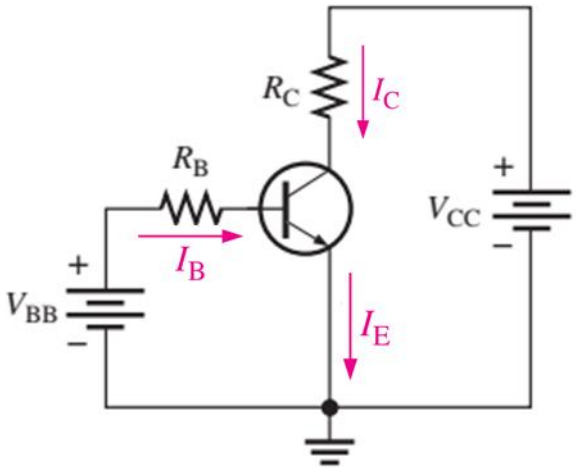
$$I_C = \frac{P_{D(max)}}{V_{CE}}$$

$$V_{CE} = \frac{P_{D(max)}}{I_C}$$

$P_{D(max)}$	V_{CE}	I_C
500 mW	5 V	100 mA
500 mW	10 V	50 mA
500 mW	15 V	33 mA
500 mW	20 V	25 mA

Análise de Circuito

Polarização Simples



(a) *npn*

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CB} = V_{CE} - V_{BE}$$

Em função do ponto de operação desejado (V_{CEQ} e I_{CQ}) os valores de R_C e R_B podem ser calculados para se obter a polarização necessária.

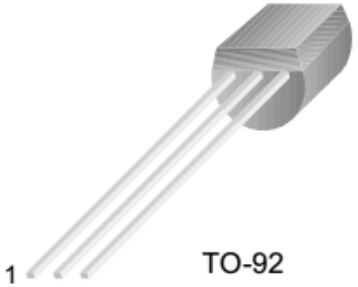
Folha de Dados

FAIRCHILD SEMICONDUCTOR™

BC237/238/239

Switching and Amplifier Applications

- Low Noise: BC239



TO-92

1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

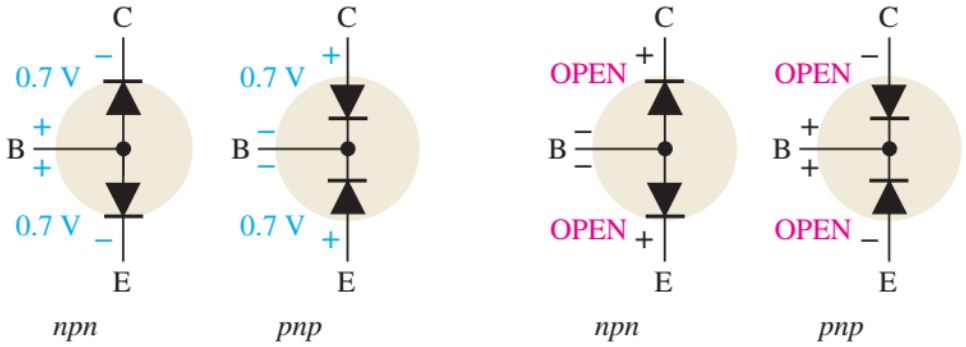
Symbol	Parameter		Value	Units
V_{CES}	Collector-Emitter Voltage	: BC237 : BC238/239	50 30	V V
V_{CEO}	Collector-Emitter Voltage	: BC237 : BC238/239	45 25	V V
V_{EBO}	Emitter-Base Voltage	: BC237 : BC238/239	6 5	V V
I_C	Collector Current (DC)		100	mA
P_C	Collector Dissipation		500	mW
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-55 ~ 150	°C

Folha de Dados

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C=2mA, I_B=0				
	: BC237		45			V
	: BC238/239		25			V
BV_{EBO}	Emitter Base Breakdown Voltage	I_E=1μA, I_C=0				
	: BC237		6			V
	: BC238/239		5			V
I_{CES}	Collector Cut-off Current					
	: BC237	V_{CE}=50V, V_{BE}=0		0.2	15	nA
	: BC238/239	V_{CE}=30V, V_{BE}=0		0.2	15	nA
h_{FE}	DC Current Gain	V_{CE}=5V, I_C=2mA	120		800	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA		0.07	0.2	V
		I_C=100mA, I_B=5mA		0.2	0.6	V
V_{BE} (sat)	Collector-Base Saturation Voltage	I_C=10mA, I_B=0.5mA		0.73	0.83	V
		I_C=100mA, I_B=5mA		0.87	1.05	V
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}=5V, I_C=2mA	0.55	0.62	0.7	V
f_T	Current Gain Bandwidth Product	V_{CE}=3V, I_C=0.5mA, f=100MHz		85		MHz
		V_{CE}=5V, I_C=10mA, f=100MHz	150	250		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		3.5	6	pF
C_{ib}	Input Base Capacitance	V_{EB}=0.5V, I_C=0, f=1MHz		8		pF
NF	Noise Figure	V_{CE}=5V, I_C=0.2mA,				
	: BC237/238	f=1KHz R_G=2KΩ		2	10	dB
	: BC239	V_{CE}=5V, I_C=0.2mA			4	dB
	: BC239	R_G=2KΩ, f=30~15KHz			4	dB

Teste de TBJ

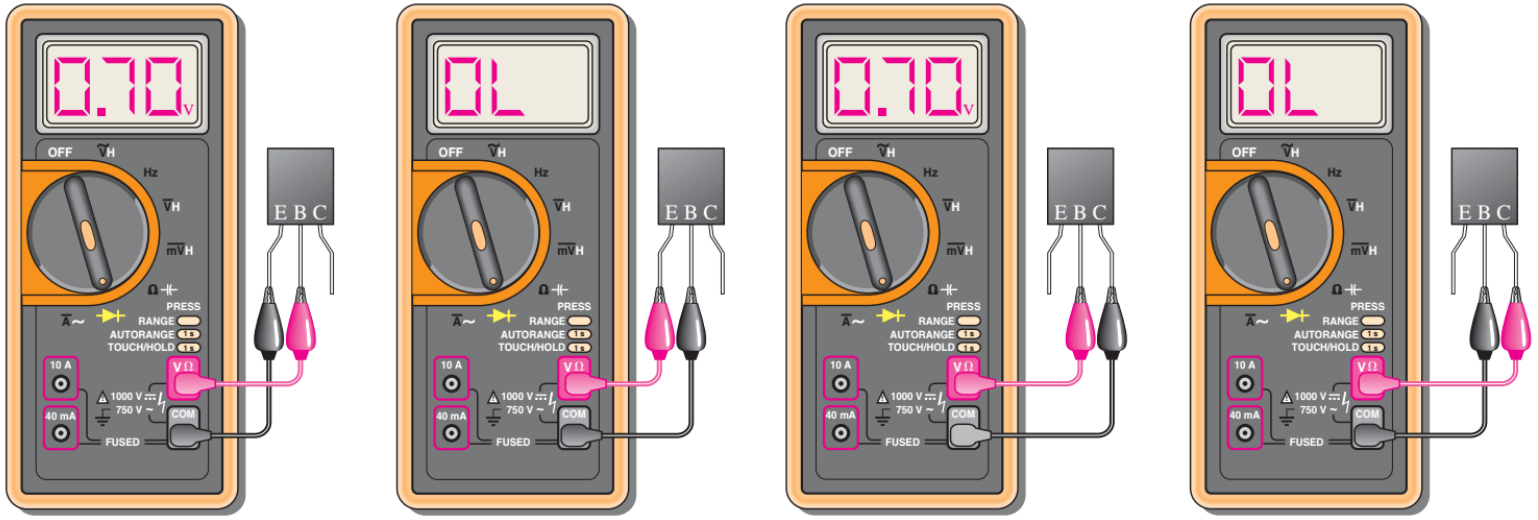


(a) Both junctions should typically read 0.7 V when forward-biased.

(b) Both junctions should ideally read OPEN when reverse-biased.

Medida de Resistência entre Base e Coletor deve ser elevada em qualquer direção, caso contrário, o transistor apresenta falha.

EXEMPLO PARA UM TBJ NPN



(a) Forward-bias test of the BE junction

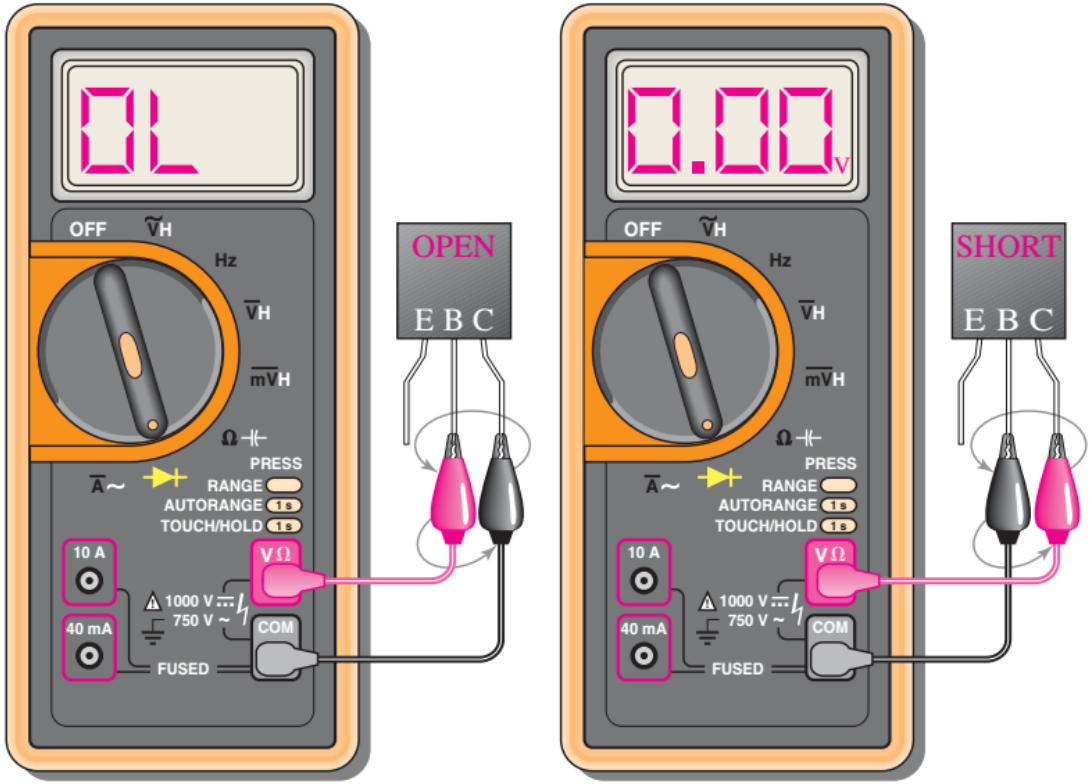
(b) Reverse-bias test of the BE junction

(c) Forward-bias test of the BC junction

(d) Reverse-bias test of the BC junction

Teste de TBJ

TRANSISTOR COM FALHA

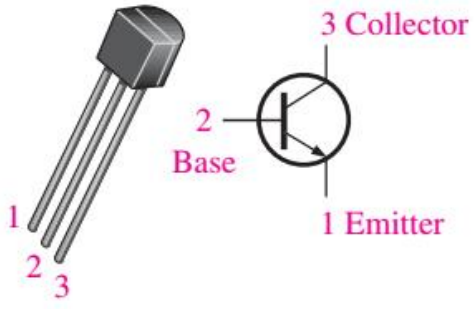


(a) Forward-bias test and reverse-bias test give the same reading (OL is typical) for an open BC junction.

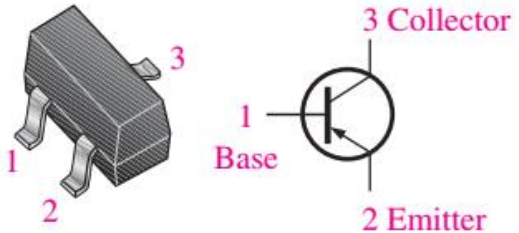
(b) Forward- and reverse-bias tests for a shorted junction give the same 0 V reading.

Empacotamento

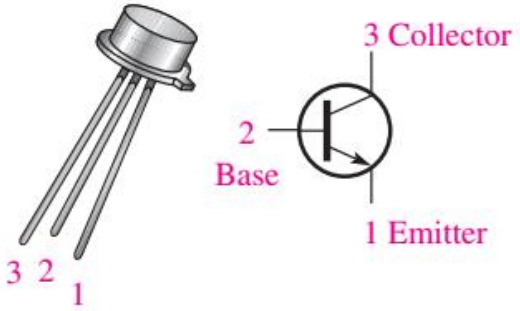
Transistores de uso geral



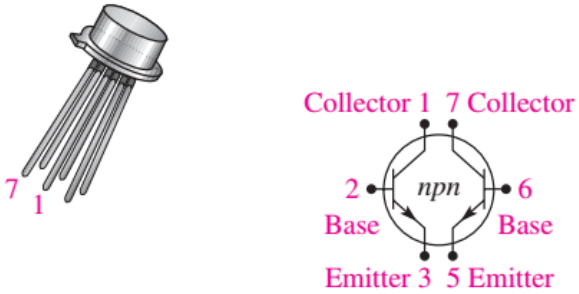
(a) TO-92



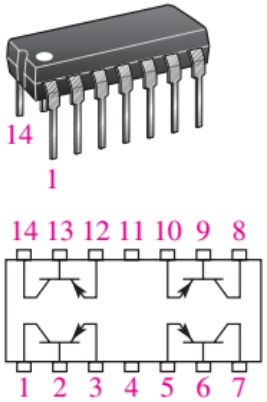
(b) SOT-23



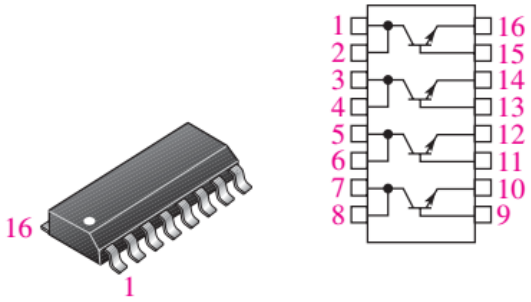
(c) TO-18. Emitter is closest to tab.



(a) Dual metal can. Emitters are closest to tab.



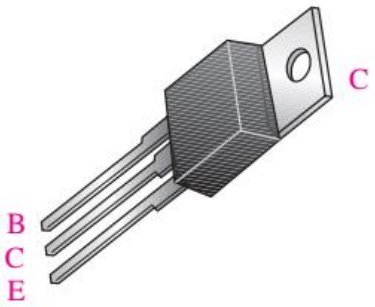
(b) Quad dual in-line (DIP) and quad flat-pack. Dot indicates pin 1.



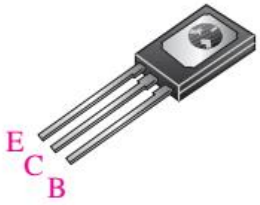
(c) Quad small outline (SO) package for surface-mount technology

Empacotamento

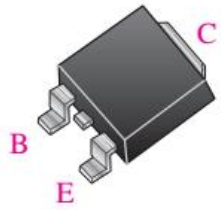
Transistores de potência



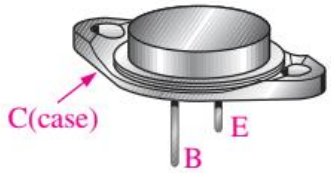
(a) TO-220



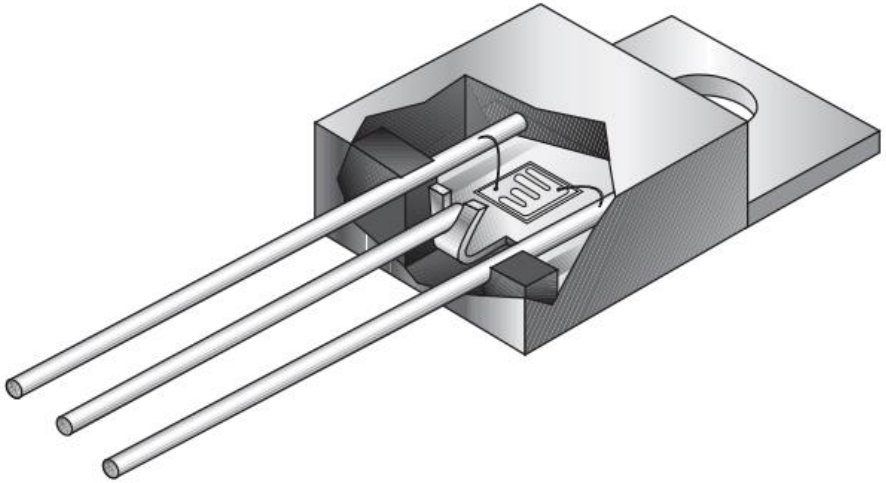
(b) TO-225



(c) D-Pack



(d) TO-3



(e) Greatly enlarged cutaway view of tiny transistor chip mounted in the encapsulated package

Referência

Boylestad, R. L., Nashelsky, L. Dispositivos Eletrônicos e teoria de circuitos, 8ª. Edição, Pearson.

Fairchild Semiconductors, BD237/238/239, *Data Sheet*, Rev. B, Jan. 2001.