PRÁTICA 4 – CIRCUITOS REGULADORES CC

Revisão

SEL0610 - LABORATÓRIO DE CIRCUITOS ELETRÔNICOS

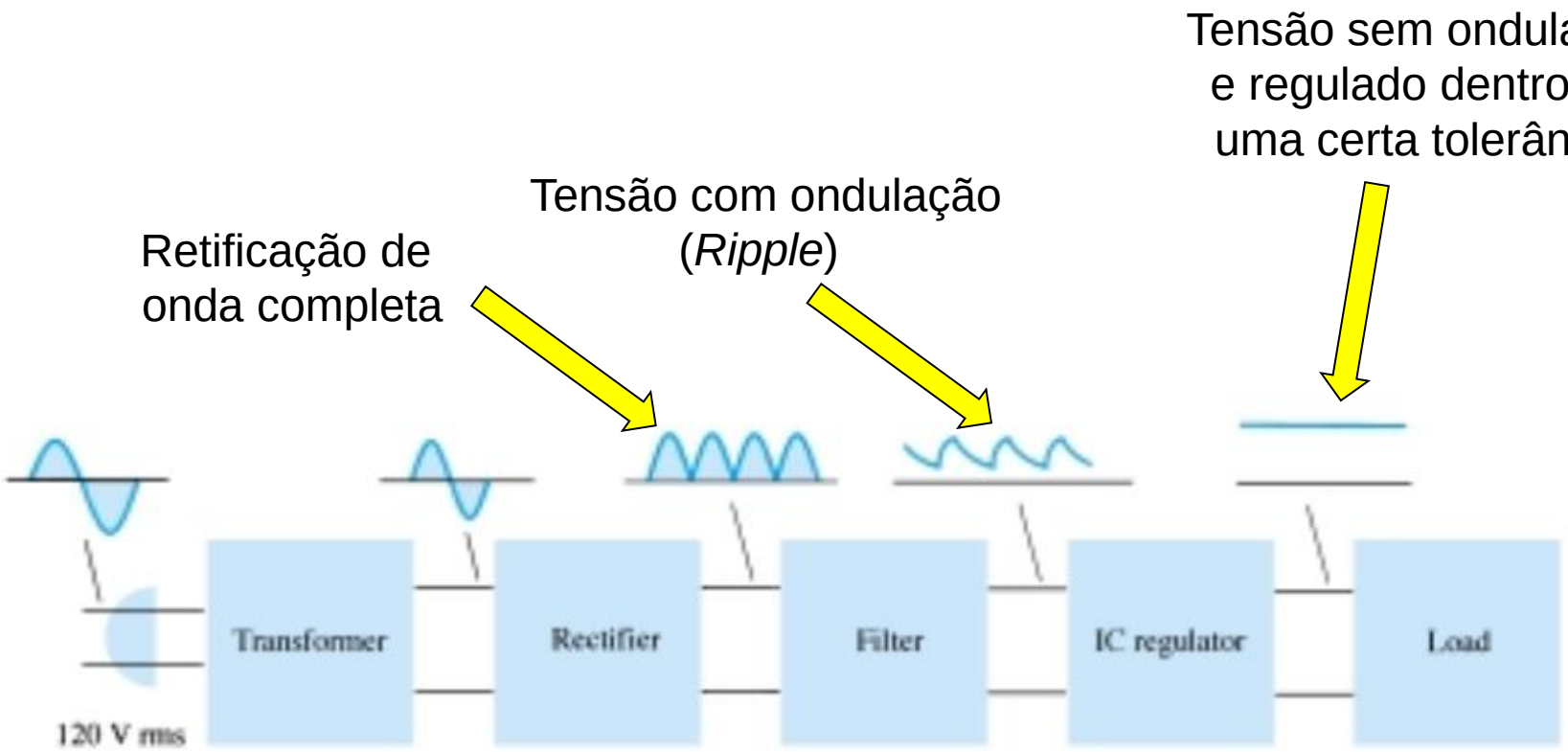
Engenharia de Computação – 6° Período Letivo

Conteúdo

- Fonte de Tensão
- Regulador com Zener
- Circuito Integrado Regulador de Tensão

Fonte de Tensão

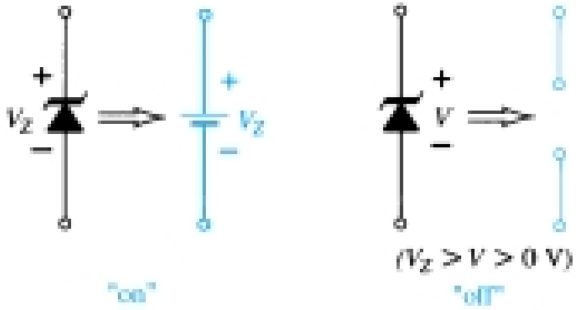
Diagrama em blocos de uma fonte de tensão

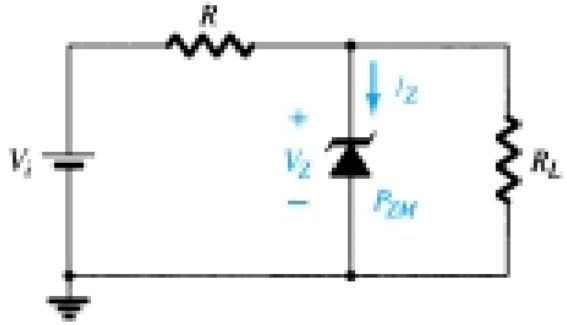


Retificação de Meia Onda

- Regulador com Zener

Polarização do diodo Zener





$$V = V_L = \frac{R_L V_i}{R + R_L}$$

Deve-se garantir que o Zener opere no estado “on”

$$V_L = V_Z$$

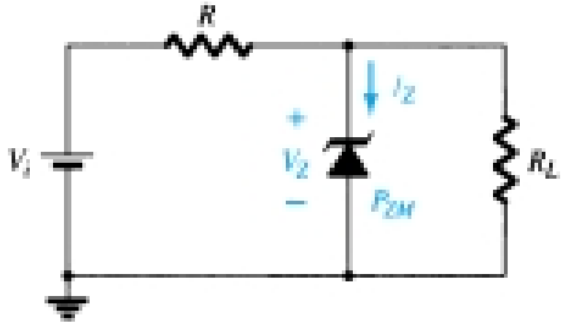
$$I_Z = I_R - I_L$$

$$P_Z = V_Z I_Z$$

Retificação de Meia Onda

- Regulador com Zener (Limites de Operação)

Considerando V_i Fixo e R_L Variável



$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Valor Mínimo da Resistência da Carga

$$R_{L_{\min}} = \frac{R V_Z}{V_i - V_Z}$$

Valor Máximo da Resistência da Carga

$$I_R = \frac{V_R}{R}$$

$$I_Z = I_R - I_L$$

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}}$$

$$I_{L_{\min}} = I_R - I_{ZM}$$

$$V_R = V_i - V_Z$$

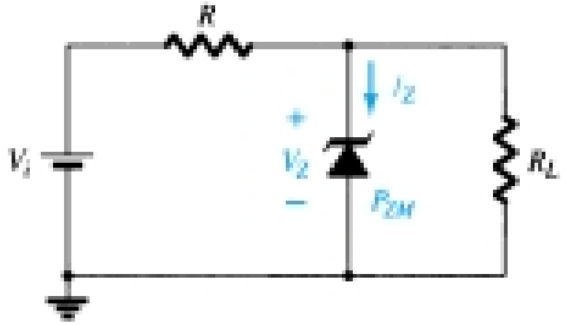
$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}}$$

I_{ZM} máxima corrente no diodo (Folha de Dados)

Retificação de Meia Onda

- Regulador com Zener (Limites de Operação)

Considerando V_i Variável e R_L Fixo



$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Valor Mínimo de V_i
(limitado pela V_Z)

$$V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L}$$

Valor Máximo de V_i
(limitado pela I_{ZM})

$$I_{R_{max}} = I_{ZM} + I_L$$

$I_L = V_Z / R_L$ (const.)

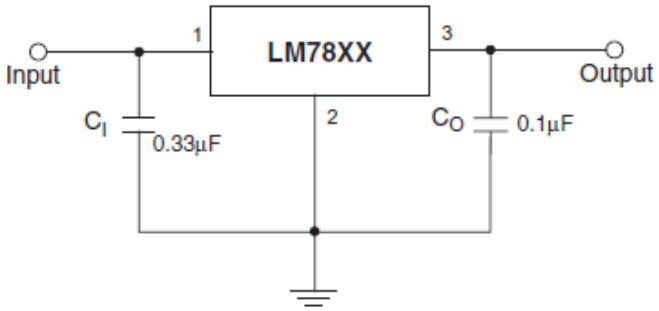
$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$V_{i_{max}} = I_{R_{max}} R + V_Z$$

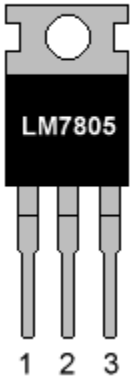
Retificação de Onda Completa

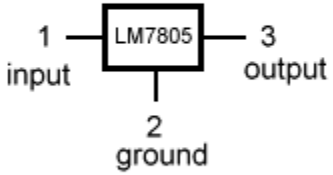
- Circuito Integrado Regulador de Tensão

7805



LM7805 PINOUT DIAGRAM



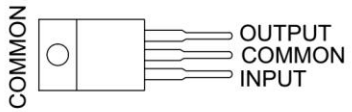


Retificação de Onda Completa

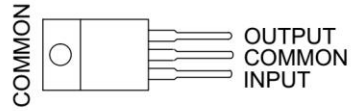
Circuito Integrado Regulador de Tensão

- **3-Terminal Regulators**
- **Output Current up to 1.5 A**
- **Internal Thermal-Overload Protection**
- **High Power-Dissipation Capability**
- **Internal Short-Circuit Current Limiting**
- **Output Transistor Safe-Area Compensation**

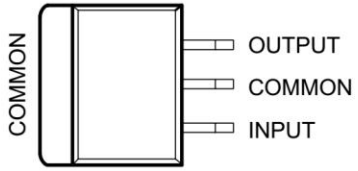
KC (TO-220) PACKAGE
(TOP VIEW)



KCS (TO-220) PACKAGE
(TOP VIEW)



KTE PACKAGE
(TOP VIEW)



recommended operating conditions

			MIN	MAX	UNIT
V_I	Input voltage	µA7805C	7	25	V
		µA7808C	10.5	25	
		µA7810C	12.5	28	
		µA7812C	14.5	30	
		µA7815C	17.5	30	
		µA7824C	27	38	
I_O	Output current			1.5	A
T_J	Operating virtual junction temperature	µA7800C series	0	125	°C

Retificação de Onda Completa

- Circuito Integrado Regulador de Tensão

electrical characteristics at specified virtual junction temperature, V_I = 10 V, I_O = 500 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J†	μA7805C			UNIT
			MIN	TYP	MAX	
Output voltage	I_O = 5 mA to 1 A, V_I = 7 V to 20 V, $P_D \leq$ 15 W	25°C	4.8	5	5.2	V
		0°C to 125°C	4.75		5.25	
Input voltage regulation	V_I = 7 V to 25 V	25°C		3	100	mV
	V_I = 8 V to 12 V			1	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	0°C to 125°C	62	78		dB
Output voltage regulation	I_O = 5 mA to 1.5 A	25°C		15	100	mV
	I_O = 250 mA to 750 mA			5	50	
Output resistance	f = 1 kHz	0°C to 125°C		0.017		Ω
Temperature coefficient of output voltage	I_O = 5 mA	0°C to 125°C		–1.1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz	25°C		40		μV
Dropout voltage	I_O = 1 A	25°C		2		V
Bias current		25°C		4.2	8	mA
Bias current change	V_I = 7 V to 25 V	0°C to 125°C			1.3	mA
	I_O = 5 mA to 1 A				0.5	
Short-circuit output current		25°C		750		mA
Peak output current		25°C		2.2		A

† Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.33-μF capacitor across the input and a 0.1-μF capacitor across the output.

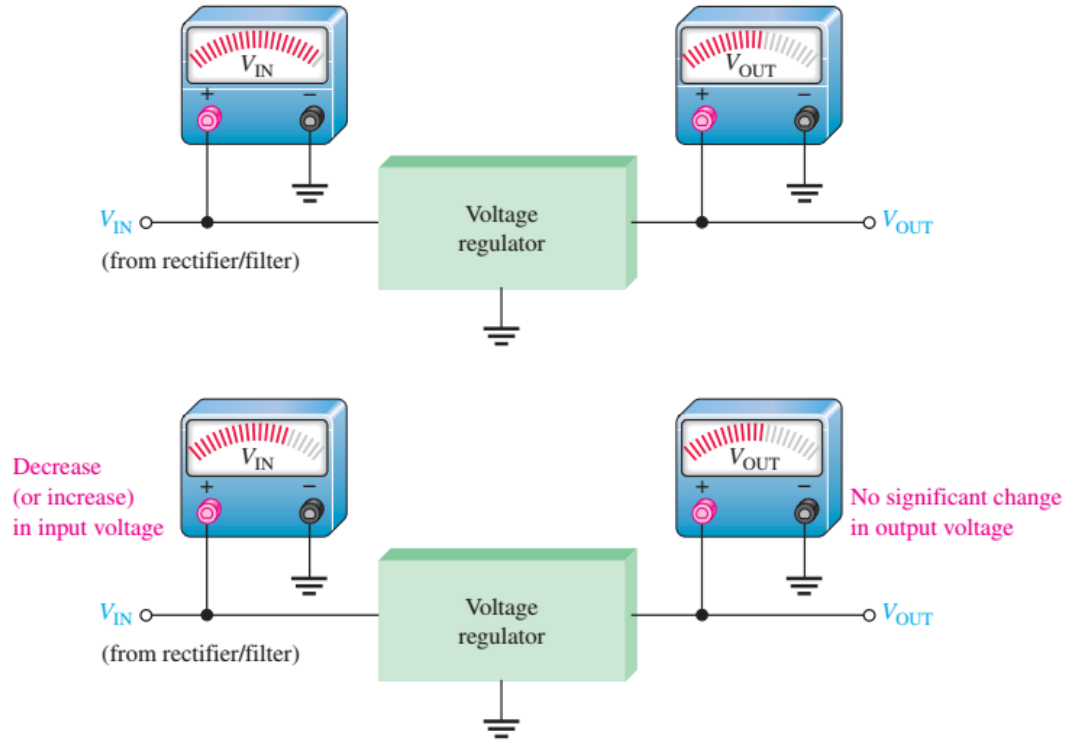
Retificação de Onda Completa

- Circuito Integrado Regulador de Tensão

Regulagem de Linha

$$\text{Line regulation} = \left(\frac{\Delta V_{OUT}}{\Delta V_{IN}}\right)100\%$$

$$\text{Line regulation} = \frac{(\Delta V_{OUT}/V_{OUT})100\%}{\Delta V_{IN}}$$

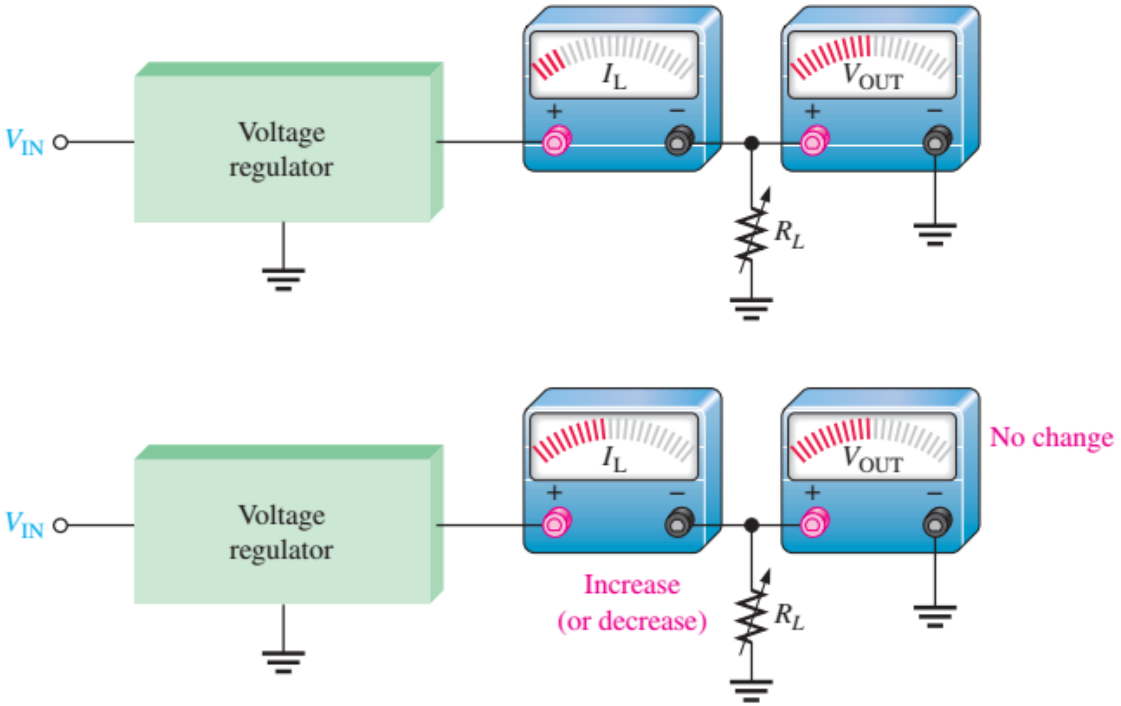


Retificação de Onda Completa

- Circuito Integrado Regulador de Tensão

Regulagem de Carga

$$\text{Load regulation} = \left(\frac{V_{NL} - V_{FL}}{V_{FL}}\right)100\%$$



V_{NL} – Tensão de saída na condição sem carga

V_{FL} – Tensão de saída na condição de carga total

Referência

Boylestad, R. L., Nashelsky, L. Dispositivos Eletrônicos e teoria de circuitos, 8ª. Edição, Pearson.