

# Scenario X

## Real Time Audio Descrambler using FPGA

### Outline

- Introduction
- Analogue Solution
- Digital Solution
- Conclusion

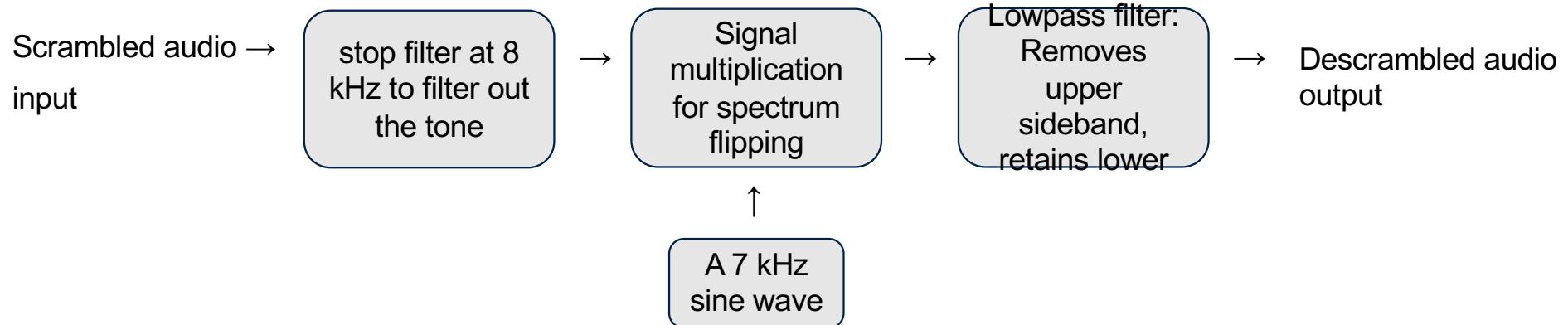
Group 35



# Introduction

Scrambled → DC biasing → ADC → 8kHz bandstop filter → multiply by sinewave → DAC → Low pass filter → power amplifier → Speaker audio input

## How to Descramble



# Block diagram for the descrambling

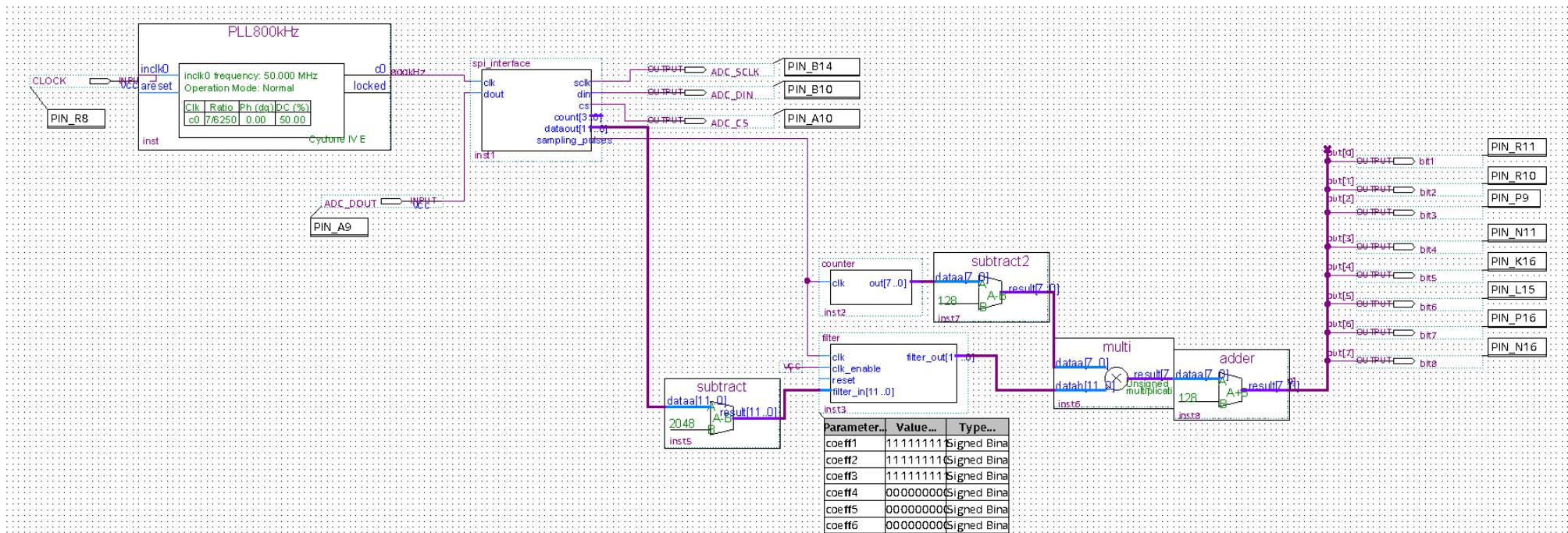
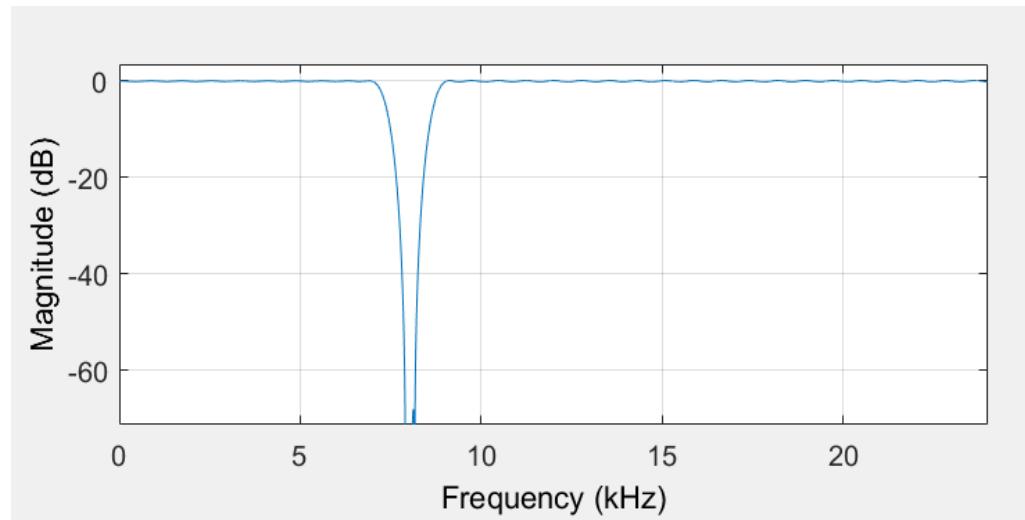


Fig1. A schematic for the audio unscrambling method

# Bandstop filter



*Fig2.* Bandstop filter with active double T-trapping filter

# 7kHz sinewave generation



Fig. 7kHz sinewave

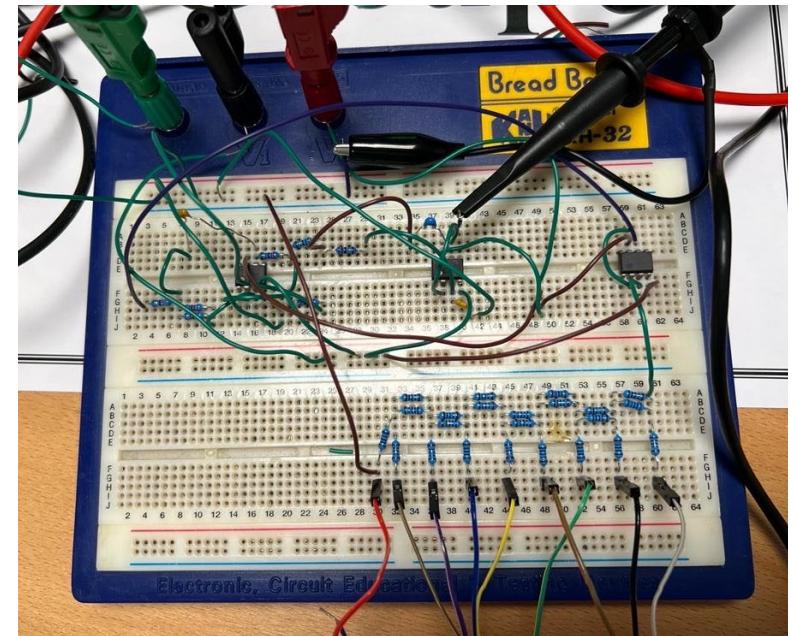


Fig. Bread Board Circuit Diagram

# Using the linear ramp

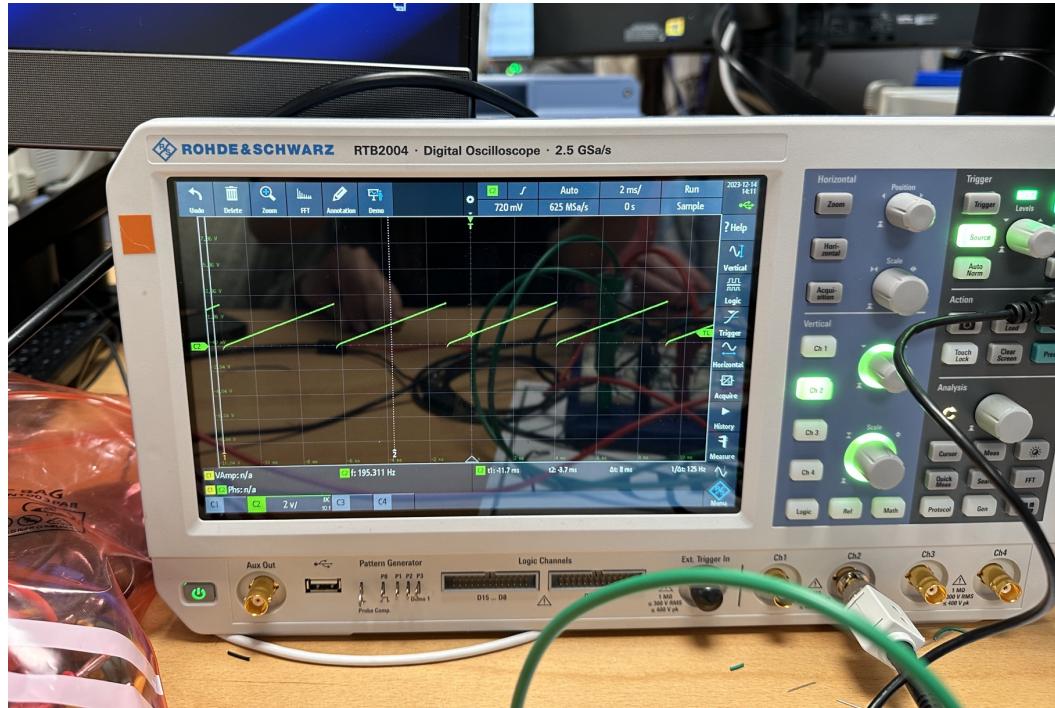


Fig. Test the external DAC using the linear ramp

# R-2R DAC

The R-2R DAC design utilizes operational amplifiers for safety, connecting the ladder only to the passive non-inverting inputs.

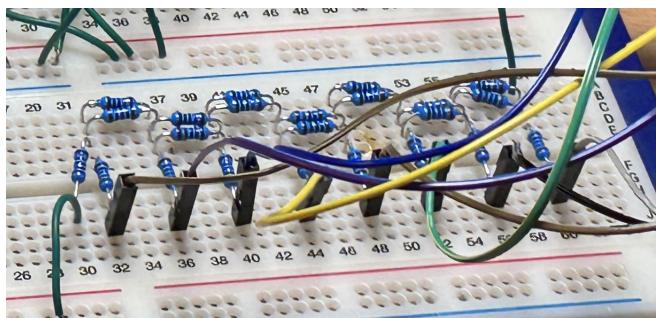
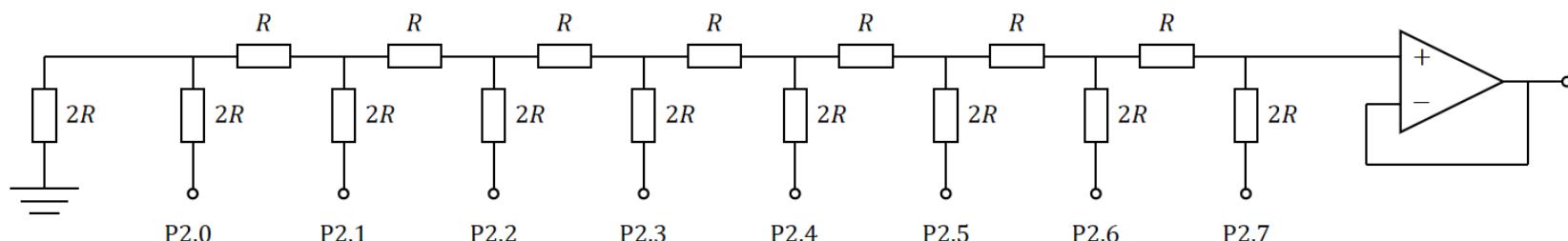


Fig. R-2R DAC design



( $2R$  is  $1\text{k}\Omega$  and so  $R$  is  $500\Omega$ )

# Potentiometer biasing

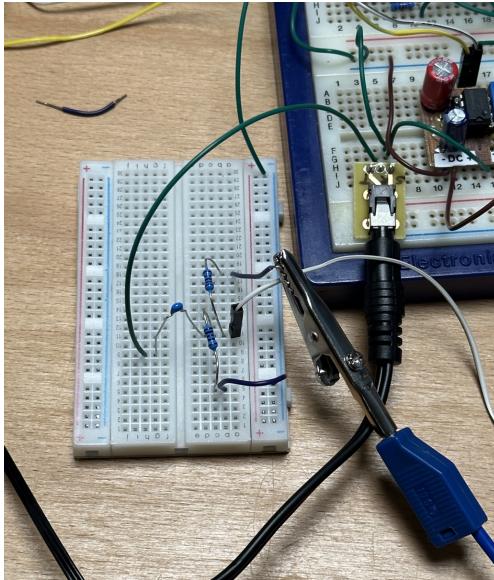


Fig. Real circuit

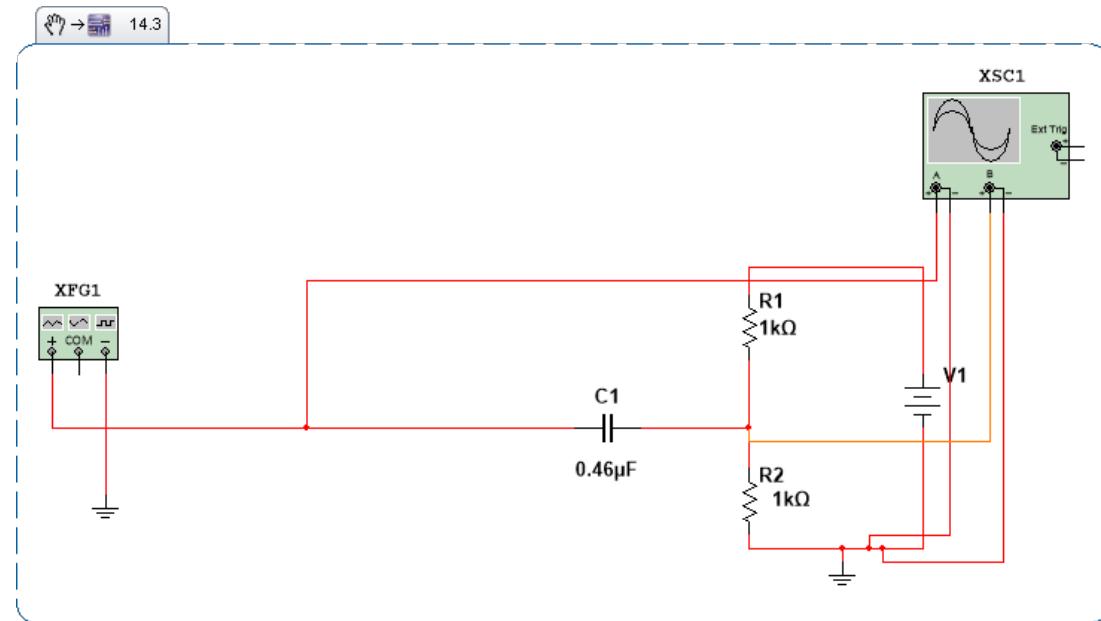


Fig. Potentiometer biasing circuit to shift the output to 1.65V

# Contribution

- Abby: Test DAC, build/test dc bias component, build/test bandstop filter and ADC.
- Anthony: Was responsible of the full programming of FPGA
- Zain: Design/build/test the low pass filter, test the bandstop filter, test/ troubleshoot the DAC.
- Evelyn: Build the DAC, build the low pass filter, made the presentation slides