Engineering Assignment Coversheet

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Assignment Title:	Voltage Controlled Oscillator and Cascode Amplifier
Subject Number:	ELEN90062
Subject Name:	High Speed Electronics
Student Name:	Rui Yuan, Huawang Liu, Haotian Xia
Lecturer/Tutor:	
Due Date:	28/08/2018

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Has an extension been granted? Yes / No (circle)

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Student signature Rui Yuan Huawang Liu Haotian Xia Date 28/08/2018

University of Melbourne
ELEN90062 High Speed Electronics
WORKSHOP

WORKSHOP 2 REPORT

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I Colpitts Oscillator Simulation

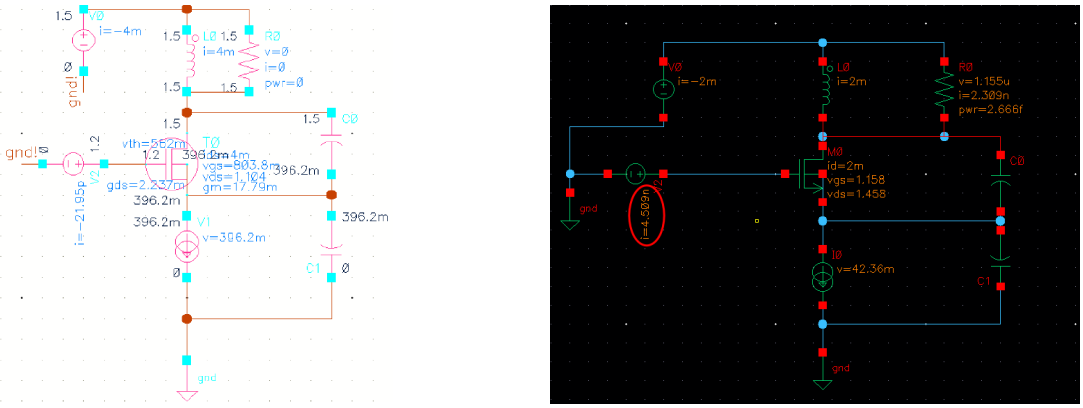

Figure 1: Given and built Colpitts Oscillator Circuit

I.1 Exclusive Summary

In the first circuit, we considers important design issues of the oscillator (frequency, amplitude, and condition of start up). We then complement the Colpitts Oscillator circuit as above, and compare its simulation performance with theoretical values. We find the exist difference may caused by parasitic capacitors.

I.2 Calculate the minimum gain (gm), required to start the oscillations.

As we are given $L = 1nH$, $C1 = C2 = 24pF$, and $R = 500\Omega$ respectively, at resonance when transconductance is minimum to guarantee startup:

$$\frac{ng_mR}{n^2g_mR + 1} = 1 \tag{1}$$

Yields, we need

$$g_m > \frac{1}{R(n - n^2)} \tag{2}$$

Where the capacitor ratio n is:

$$\begin{aligned} n &= \frac{C1}{C1 + C2} \\ &= \frac{1}{2} \end{aligned} \tag{3}$$

Hence:

$$g_m > \frac{1}{500 \times (\frac{1}{4})} \\ > 8mS \tag{4}$$

Which means the minimum necessary g_m to start oscillation is $8mS$.

I.3 Calculate the frequency of oscillations, f.

$$f = \frac{1}{2\pi\sqrt{L(\frac{C_1C_2}{C_1+C_2})}} \\ = \frac{1}{2\pi\sqrt{1 \times 10^{-9}\frac{(24\times10^{-12})^2}{48\times10^{-12}}}} \\ \approx 1.453 \times 10^9 = 1.453Ghz \tag{5}$$

I.4 Implement the circuit

From figure 1, we choose nmos24 NMOS transistor model. To get a unit loop transmission magnitude, **we need to balance the source current and drain current** as the figures below. When comparing the different widths of NMOS, we can obtain the balanced point between MOS and current. After several trials, the width of NMOS is obtained.

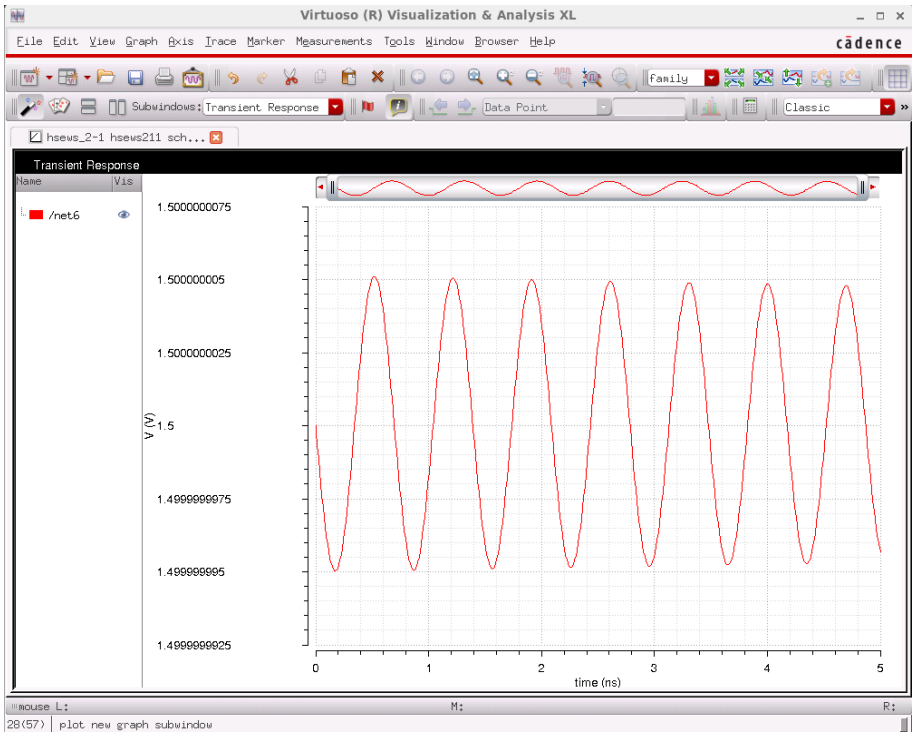

Figure 2: 400um width of NMOS

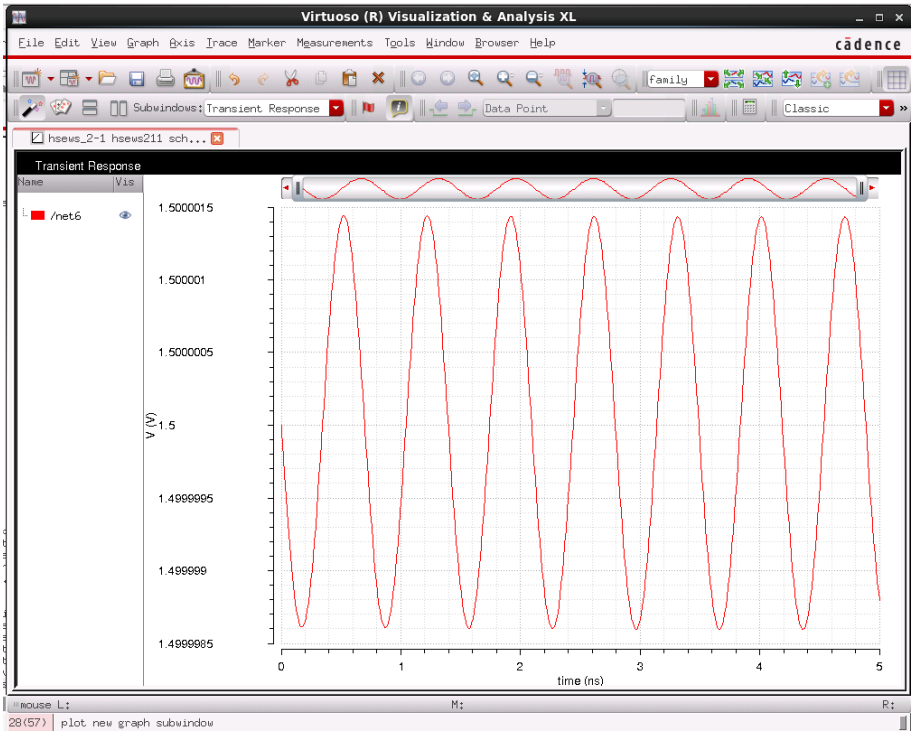

Figure 3: 570um width of NMOS

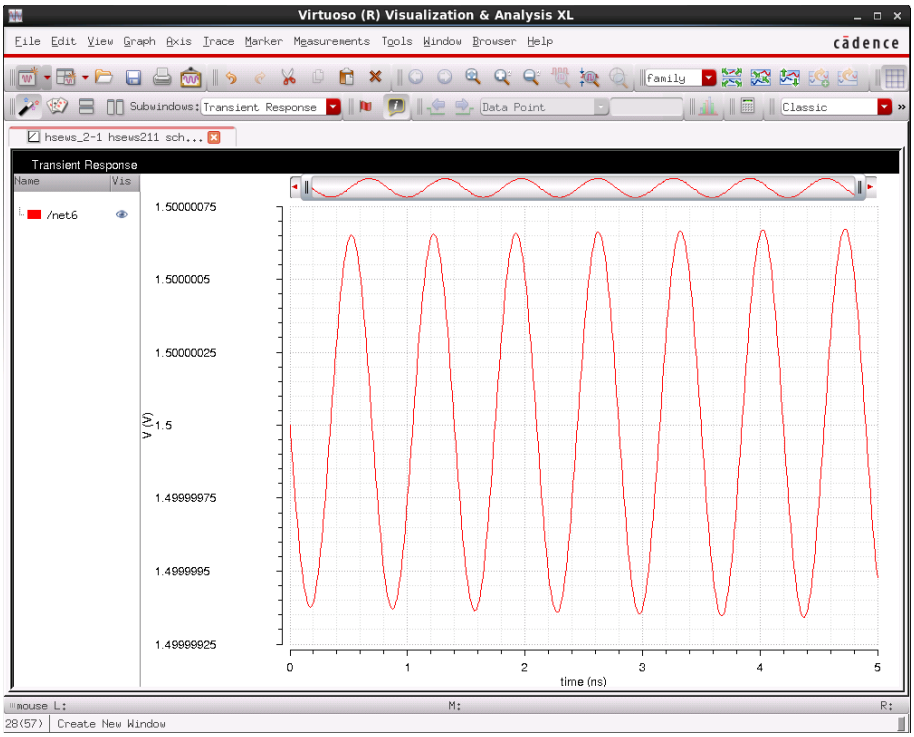

Figure 4: 700um width of NMOS

Hence, we set the $570um$ width NMOS transistor and the the $2mA$ current source.

I.5 set maxstep and observe the output signal

To get more than 10 simples period period of the signal, we need:

$$\begin{aligned} maxstep &< \frac{0.1}{f} \\ &< 66.7ps \end{aligned} \tag{6}$$

Yielding, we set maximum step to $10ps$. it is also shown in figure 5:

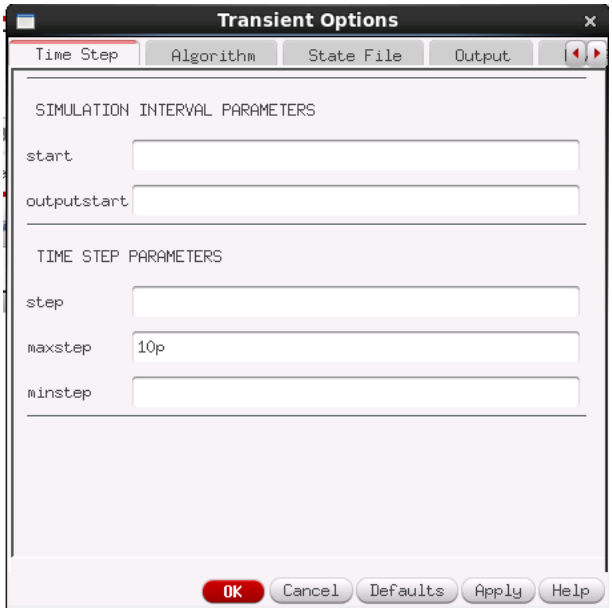

Figure 5: parameter set for maximum step

I.6 Simulation and calculation compare

From figure below, we find a significant difference between simulated and calculated values of frequency. which is $f = \frac{1}{697.911} \times 10^{12} = 1.43GHz$, the real frequency is $20MHz$ less than the calculation result. **The main reason is because the parasitic capacitors in the transistor which do not be considered in our calculations.** From the perspective of amplitude, since the bias current is 4.5nA in figure 1, $V_{tank} = 2I_{bias}R(1-n) = 2.25uV$

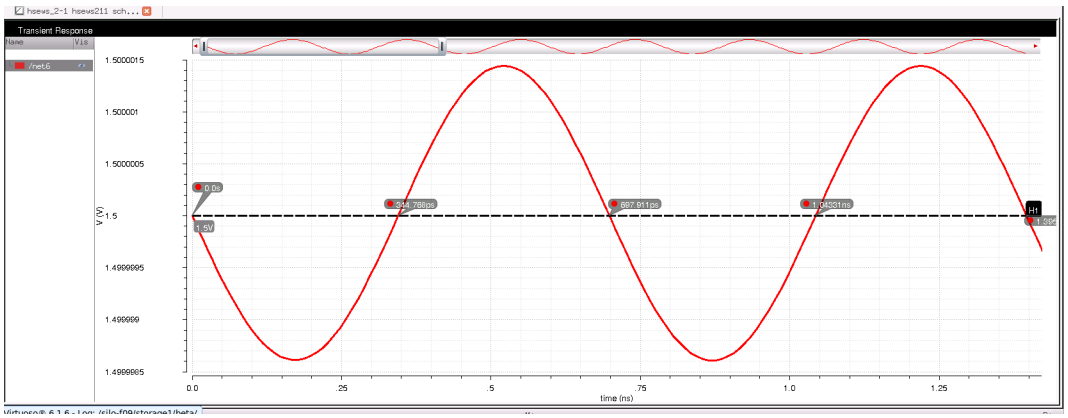

Figure 6: Real frequency plot

II Input Matching of Cascode Amplifier at 1.5 GHz

II.1 Executive Summary

In this part, the circuit is a cascode amplifier, the resistant is not match at the input of the signal by measuring the load resistance. the matching based on L-matching circuit is designed in this part, by doing the simulation and calculation, the final result is obtained and the value of serial inductor is 7.8312nH and the parallel capacitor is 7.294pF

II.2 Build the circuit and bias the transistor

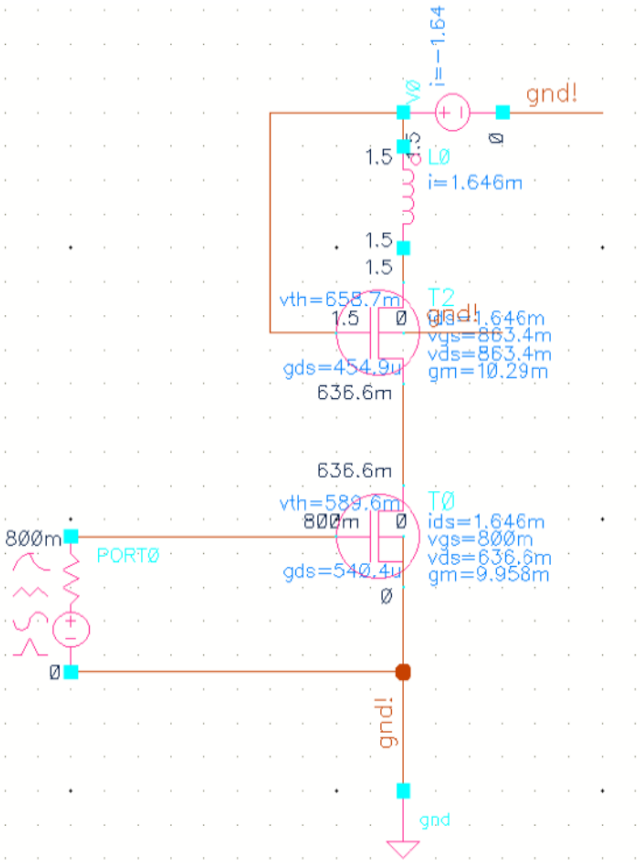

Figure 7: Cascode Amplifier Circuit

II.3 Simulate S-Parameter of the input port

The plotted S-Parameter is as below:

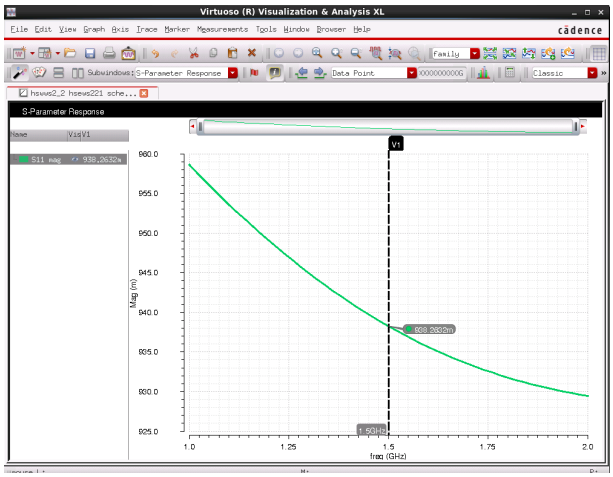

Figure 8: non-matching S parameter

From the figure 8, we can state almost all power is reflected. Under this condition, we need to match our source impedance and load impedance.

II.4 Design an input L-matching circuit

Firstly, we plotted Z_l to find the load impedance at $1.5Ghz$ is as below, we have $R_l = 3.902\omega$ and $X_l = 60.1428\Omega$:

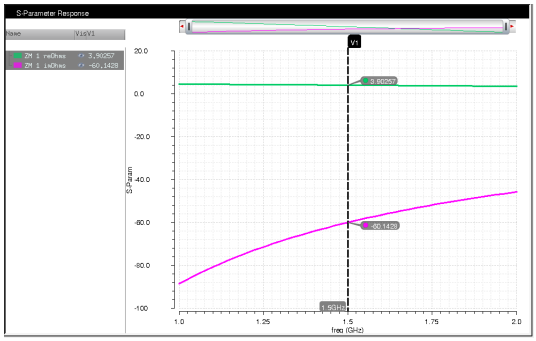

Figure 9: The measured load impedance at Port Zero

By comparing the resistance of R_S and R_L, we should boosts our input impedance. Yields, we connect the load in series with the inductance and build the L-match circuit as below:

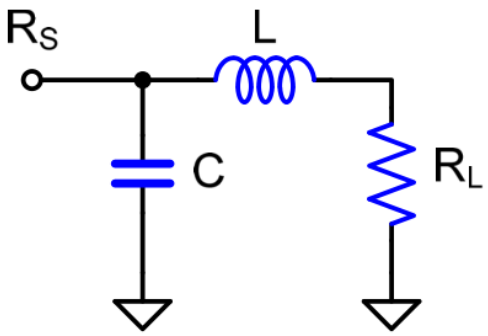

Figure 10: Implemented L-match circuit

From the L-matching circuit we build, and follow the L-matching procedure in lecture four:

$$R_{hi} = max(R_S, R_L) = 50\Omega \tag{7}$$
$$R_{lo} = min(R_S, R_L) = 3.902\Omega \tag{8}$$
$$m = \frac{R_hi}{R_lo} = 12.812 \tag{9}$$
$$Q = \sqrt{m-1} = 3.437 \tag{10}$$
$$X_s = Q \cdot R_L = 13.412 \tag{11}$$
$$X_p = -X_s \cdot (1 + Q^{-2}) = -14.548 \tag{12}$$
$$C = -1/(X_p \times 2\pi \times f) = 7.294pf \tag{13}$$
$$H = (X_s - X_l)/(2pi \times f) = 7.8312nH \tag{14}$$

the designed L matching circuit in the cadence is shown in Figure 11

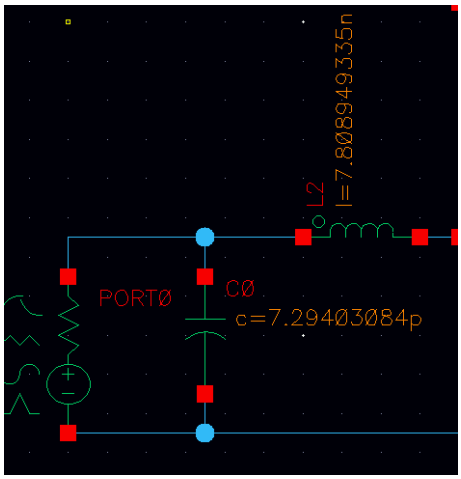

Figure 11: matching circuit

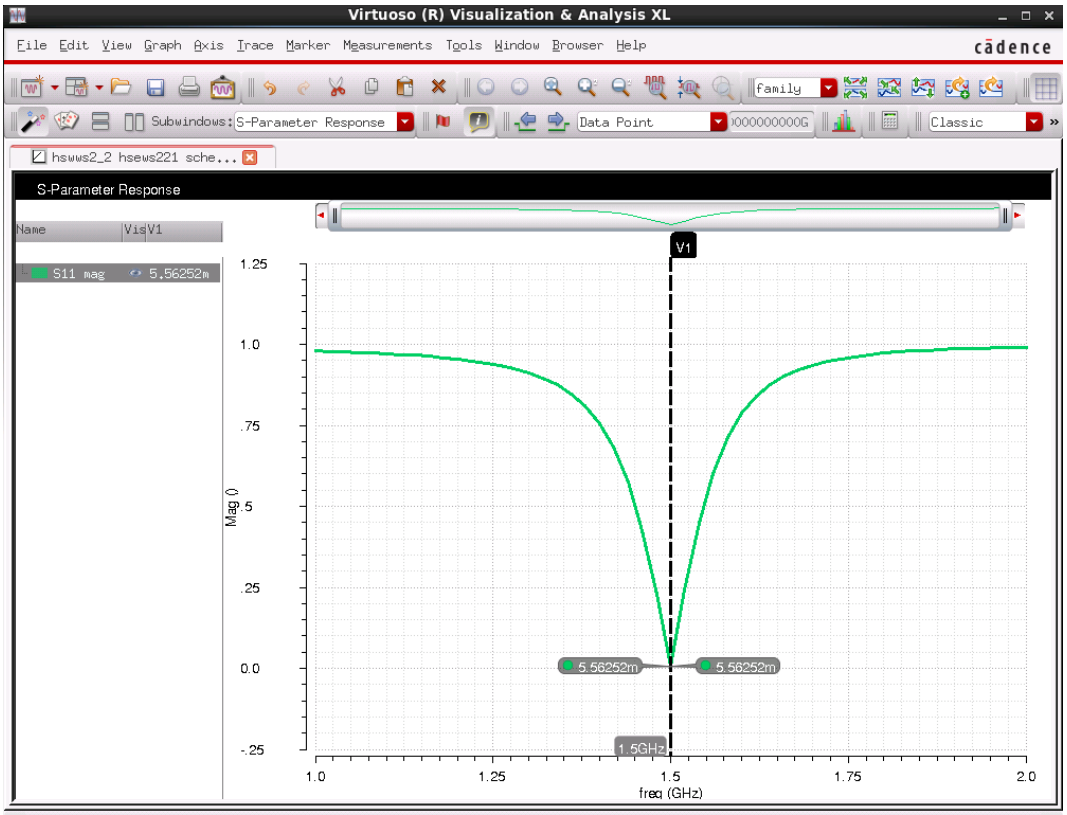

Figure 12: S parameter after matching circuit

After implementing our L-matching circuit, we regenerate S-Parameter in figure 12. **The new S-Parameter we get at** $1.5Ghz$ **is 0.005**. We can state the reflection coefficient is almost zero at required frequency which means our circuit is nearly perfect match at the selected frequency. **The reason why the S-Parameter is not exact zero at 1.5Ghz is because our accuracy limit on those components parameters**. If we want to increase the selectivity of our circuit, a possible solution is use a π match circuit which can provide flexibility on Q value. We can also state the same conclusion by the smith chart as below:

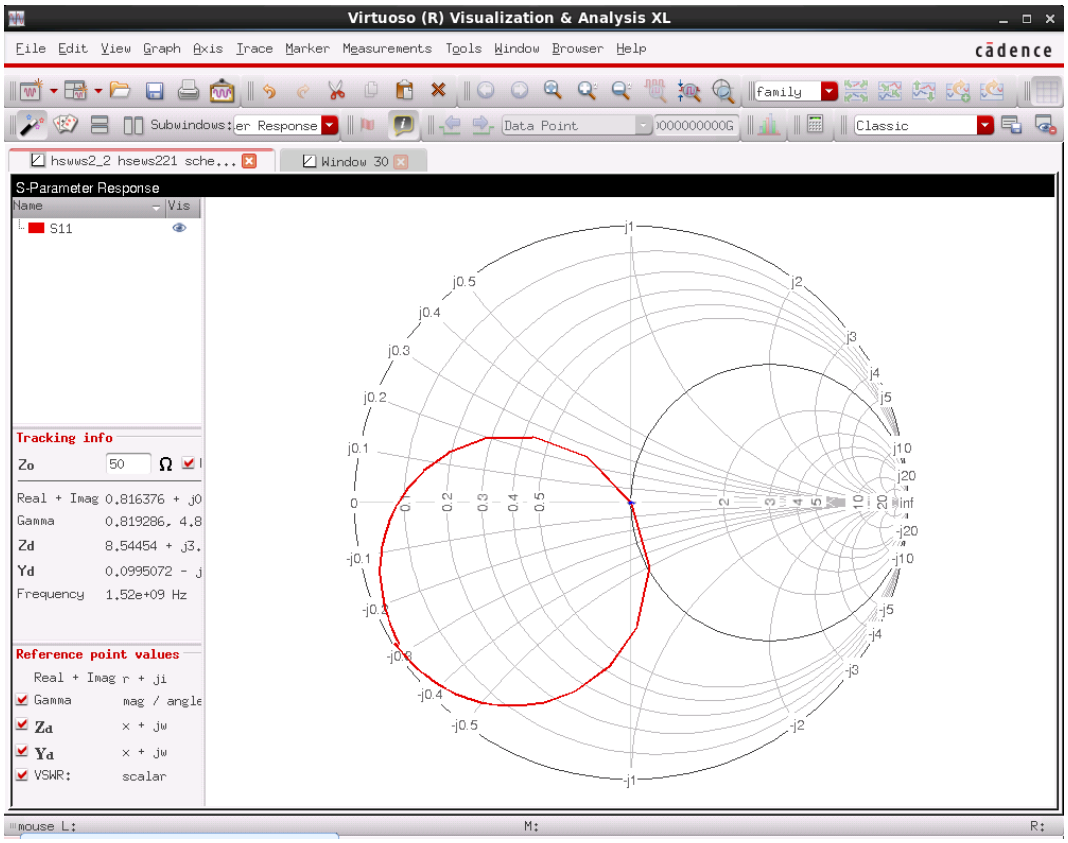

Figure 13: smith plot after matching