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Assignment Title:	Logic Gates
Subject Number:	ELEN90062
Subject Name:	High Speed Electronics
Student Name:	Rui Yuan, Huawang Liu, Haotian Xia
Lecturer/Tutor:	
Due Date:	04/11/2018

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Student signature Rui Yuan Huawang Liu Haotian Xia Date 04/11/2018

University of Melbourne

ELEN90062 High Speed Electronics WORKSHOP

WORKSHOP 5 REPORT

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Contents

1 The Schottky Clamp

1.1 Question 1.4

The schematics of RTL logic gate is shown in figure 1.

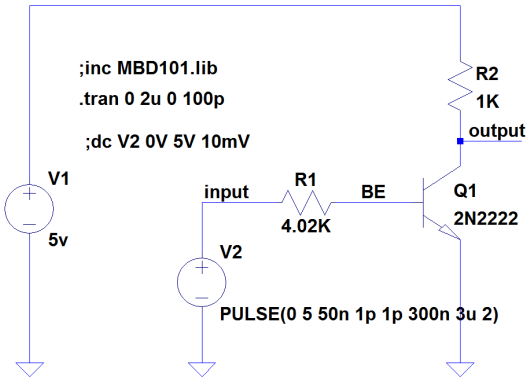
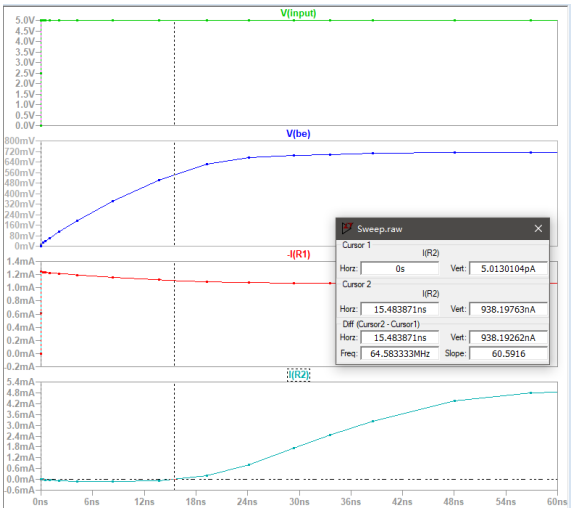
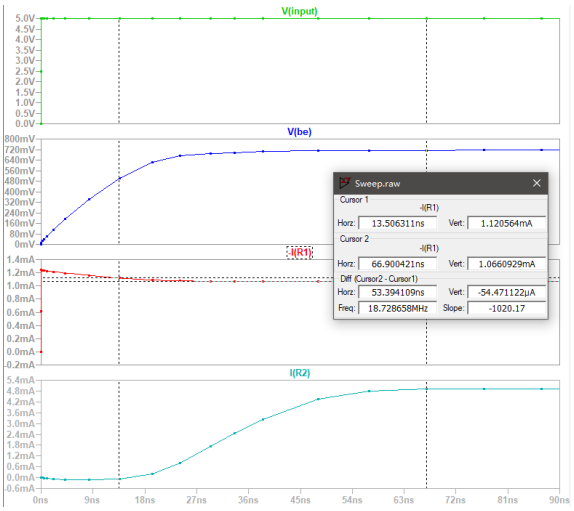


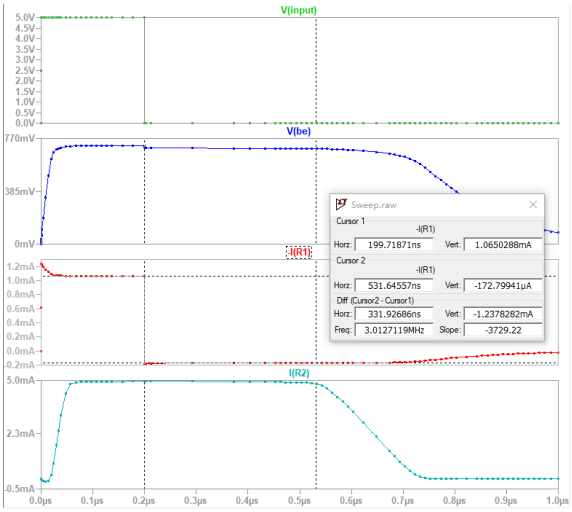
Figure 1: schematics of RTL logic gate



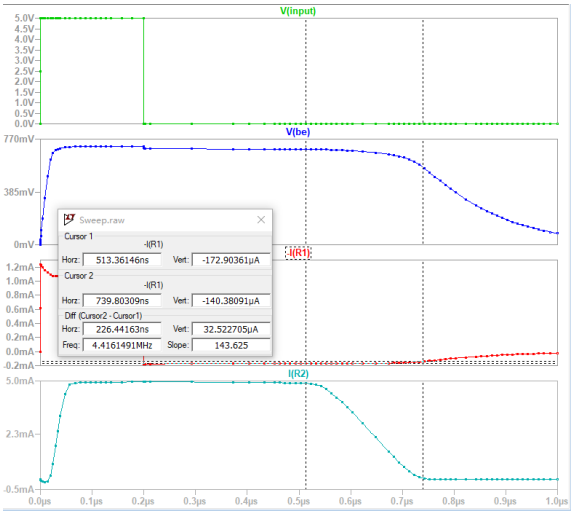
(a) measured turn on delay



(b) measured fall time delay



(c) measured charge storage delay



(d) measured rise time delay

Figure 2: Measured delays

From figure 2, we find that the **turn on delay** in the circuit is $15.48nS$, the fall time is $53.39nS$, the charge storage delay is $331.92nS$ the rise time is $226.44nS$.

1.2 Question 1.5

When the input pulse duration is 300ns, the charge storage delay is shown in figure 3, In this figure, we can find that the **charge storage delay is 403.54nS**.

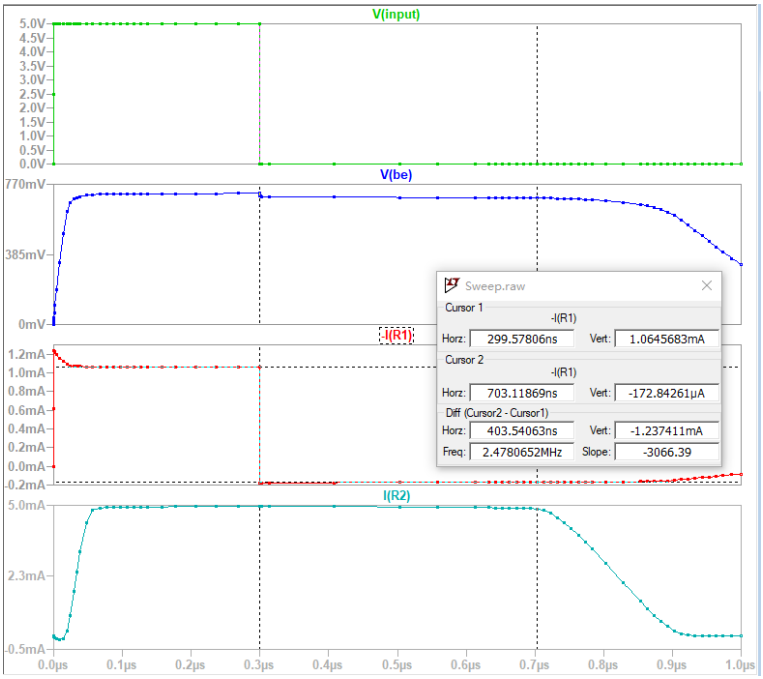


Figure 3: Charge storage delay when pulse duration is 300ns

When the input pulse duration is 400ns, the charge storage delay is shown in figure 4. In this figure, we can find that the **charge storage delay is 425.91ns**.

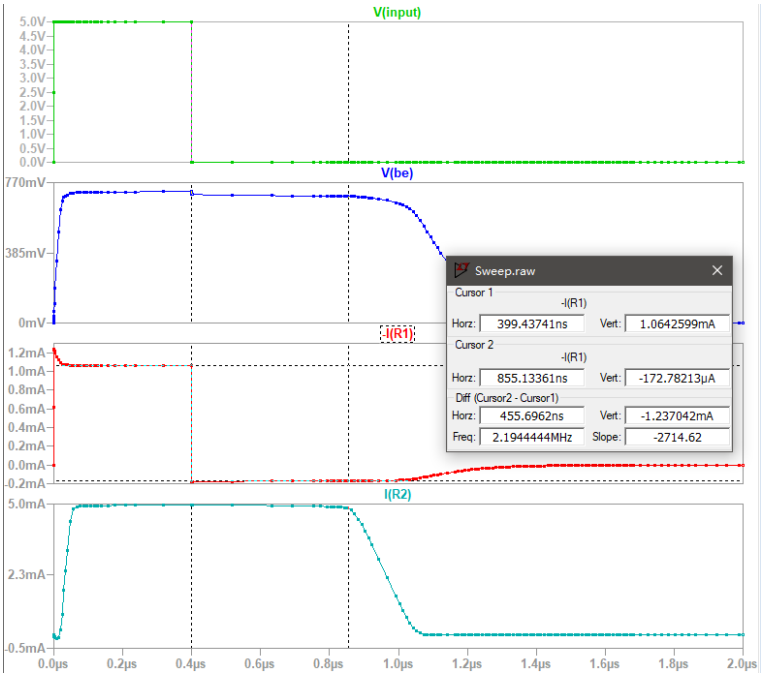


Figure 4: Charge storage delay when pulse duration is 400ns

When the input pulse duration is 500ns, the charge storage delay is shown in figure 5. In this figure, we can find that the **charge storage delay is 455.69ns**

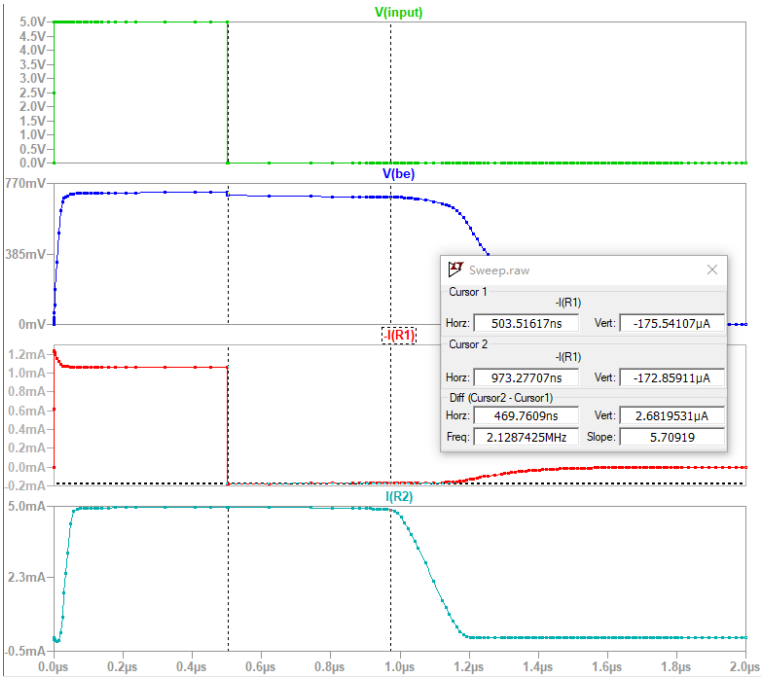


Figure 5: Charge storage delay when pulse duration is 500ns

From the measurements, we find that **smaller input pulse duration leads to shorter charge storage delay. The reason is that before the BJT leaves the saturation region, the excess charge stored in BJT due to the input pulse must be removed. Because input pulse with shorter duration will generate less excess charges, the charge storage delay is smaller.**

1.3 Question 1.6

We use the measurements in the scenario that the input pulse duration is 200ns to calculate τ_x From the lecture note we have

$$t_{CSD} = \tau_x \times ln(\frac{I_{B-ON} - I_{B-SAT-OFF}}{I_{B-SAT} - I_{B-SAT-OFF}}) \tag{1}$$

Our measurements for I_{B-ON}, I_{B-SAT}, $I_{B-SAT-OFF}$ are shown in figure 6 and 7. Our measured $V_{CE-SAT} = 290mV$, charge storage delay is 332nS as measured in 1.1 From the measured currents above, while we are give $\beta_F = 160$. We have equations:

$$I_{B-ON} = \frac{V_2 - V_{BE-ON}}{R_B} = 1.07mA \tag{2}$$

$$I_{B-SAT} = \frac{V_{CC} - V_{CE-SAT}}{\beta_F R_C} = 0.03mA \tag{3}$$

$$I_{B-SAT-OFF} = -173.85uA \tag{4}$$

$$\tau_x = \frac{t_{CSD}}{ln(\frac{I_{B-ON} - I_{B-SAT-OFF}}{I_{B-SAT} - I_{B-SAT-OFF}})}$$

$$= 173nS \tag{5}$$

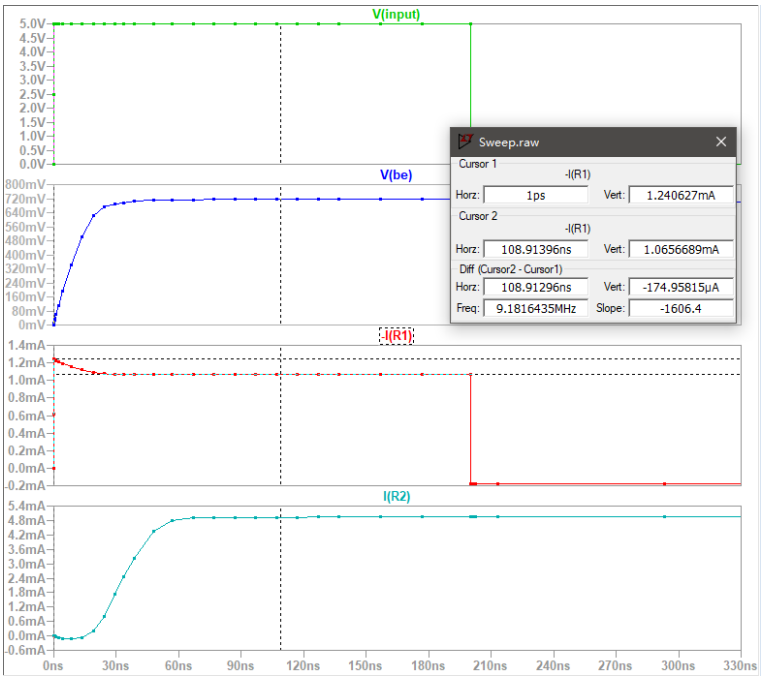


Figure 6: The values of I_{B-ON}, when input pulse duration is 200ns

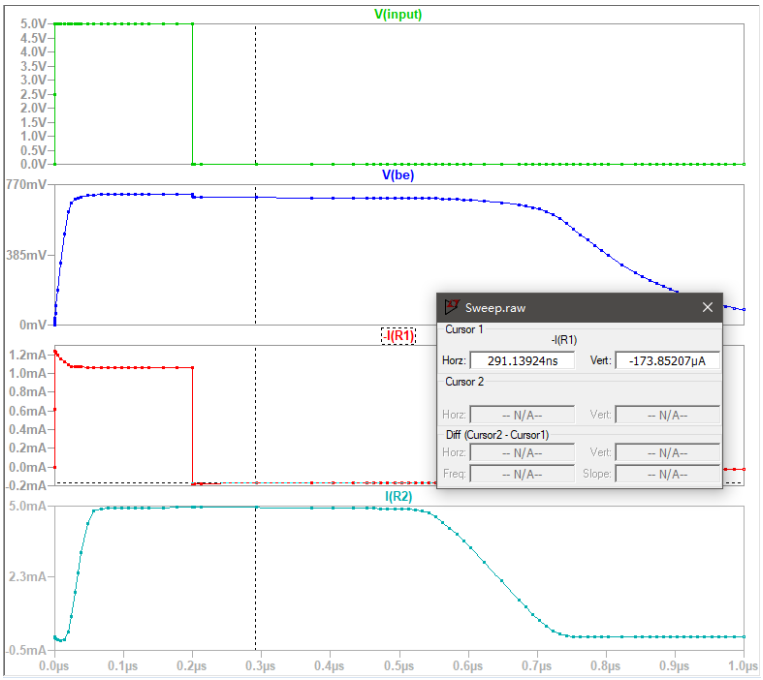


Figure 7: The values of $I_{B-SAT-OFF}$ when input pulse duration is 200ns

1.4 Question 1.7

After replacing the series base resistor with double resistance, we obtain the measurements for new t_{CSD} which is shown in figure 8.

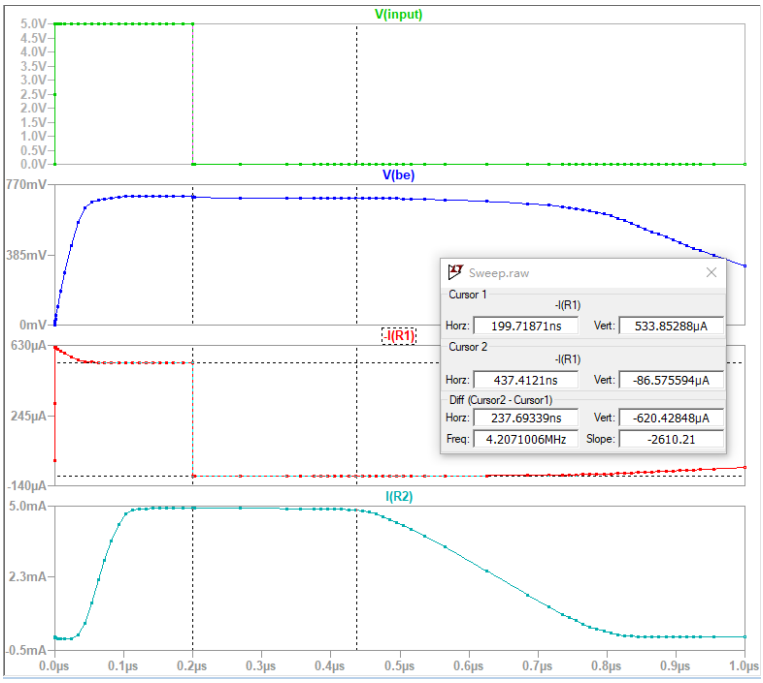


Figure 8: charge storage delay when input pulse duration is 200ns

From those measurement above, the charge storage delay is 237.69nS

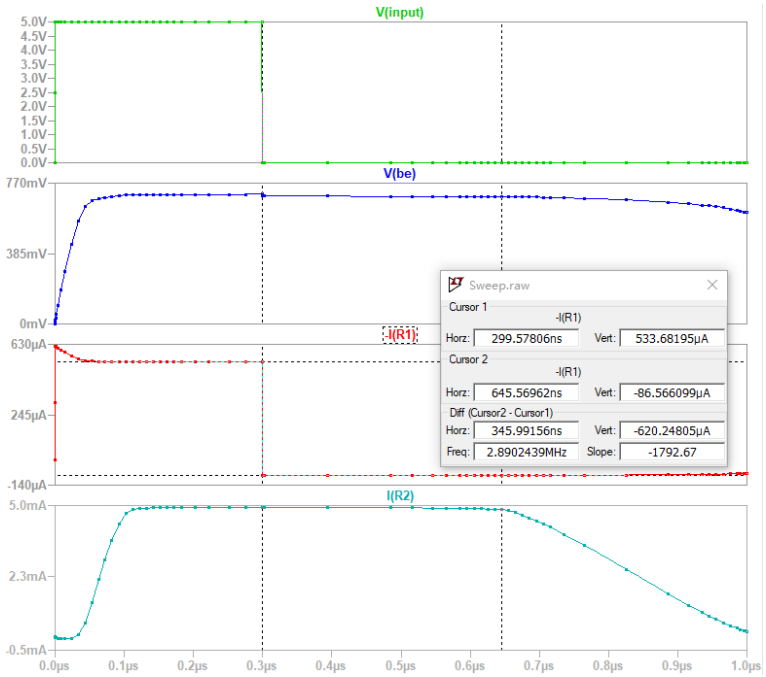


Figure 9: charge storage delay when input pulse duration is 300ns

From figure 9, we can find that the charge storage delay is 345.99nS

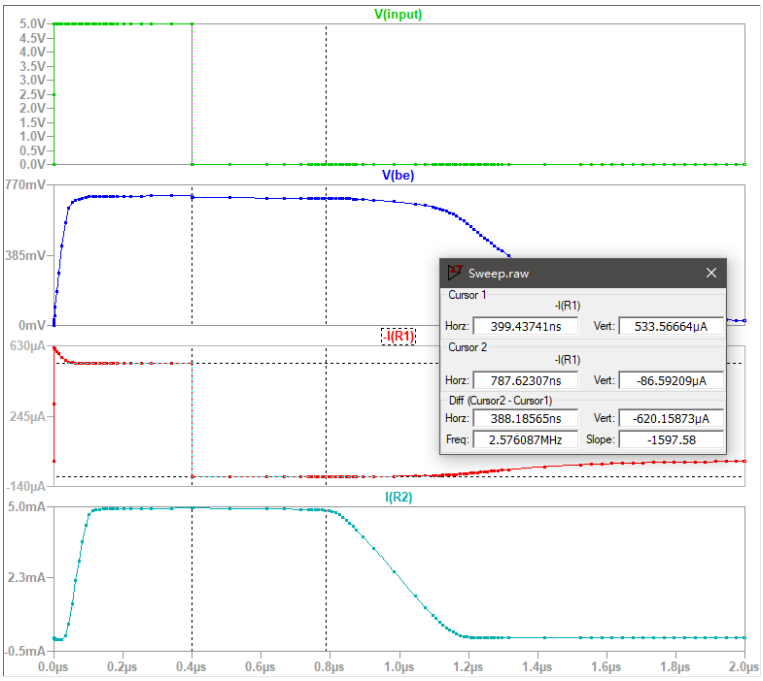


Figure 10: charge storage delay when input pulse duration is 400ns

From figure 10, we can find that the charge storage delay is $388.18nS$

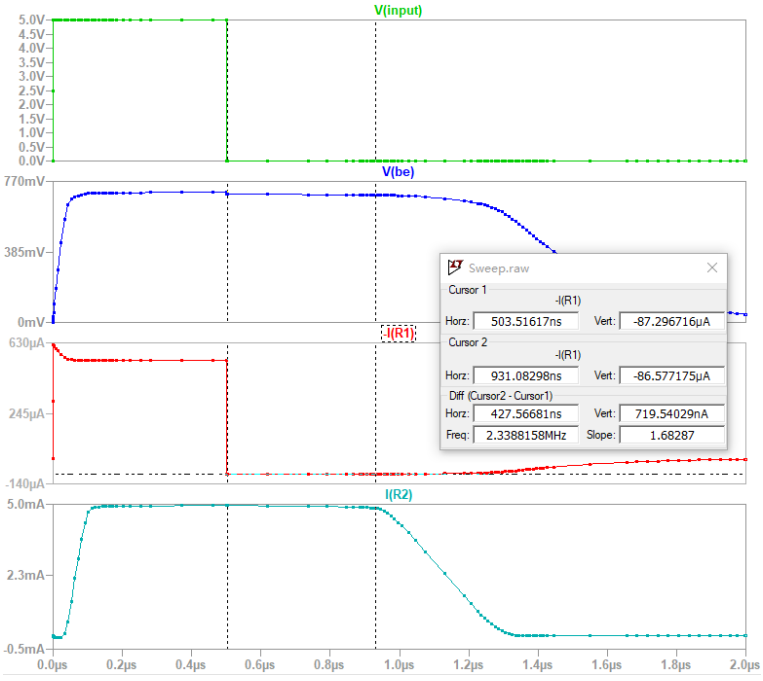


Figure 11: charge storage delay when input pulse duration is 500ns

From figure 11, we can find that the charge storage delay is $427.57nS$

The measurement of I_{B-ON}, $I_{B-SAT-OFF}$ when input pulse duration is 200ns are shown in figure 12 and 13. We also measured $V_{CE-SAT} = 320mV$

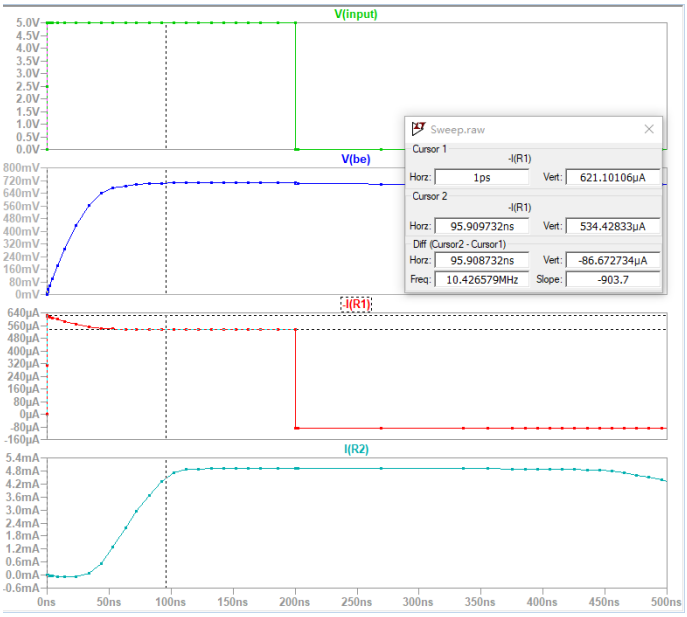


Figure 12: The values of I_{B-ON}, when double the serial resistance

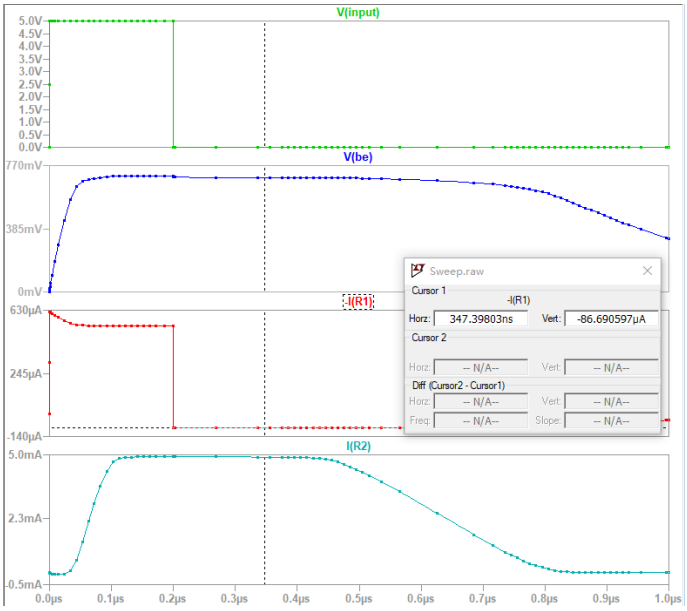


Figure 13: The values of $I_{B-SAT-OFF}$ when double the serial resistance

$$I_{B-ON} = \frac{V_2 - V_{BE-ON}}{R_B} = 534uA \tag{6}$$

$$I_{B-SAT} = \frac{V_{CC} - V_{CE-SAT}}{\beta_F R_C} = 29uA \tag{7}$$

$$I_{B-SAT-OFF} = -(\frac{V_1 + V_{BE-ON}}{R_B}) = -86.7uA \tag{8}$$

$$\tau_x = \frac{t_{CSD}}{ln(\frac{I_{B-ON} - I_{B-SAT-OFF}}{I_{B-SAT} - I_{B-SAT-OFF}})}$$

$$= 141.8nS \tag{9}$$

τ_x changed slightly and becomes $141.8nS$ compared with $173nS$ in 1.6. When base resistor doubled,

our base current I_{B-ON}, I_{B-SAT}, $I_{B-SAT-OFF}$ decreased to a half, this can be verified by comparing with equation 2-4. However, since our charge storage delay changed from 331.92nS to 237.69nS. Henceforth, our τ_x changed a little (as ln function decrease the difference).

1.5 Question 1.8

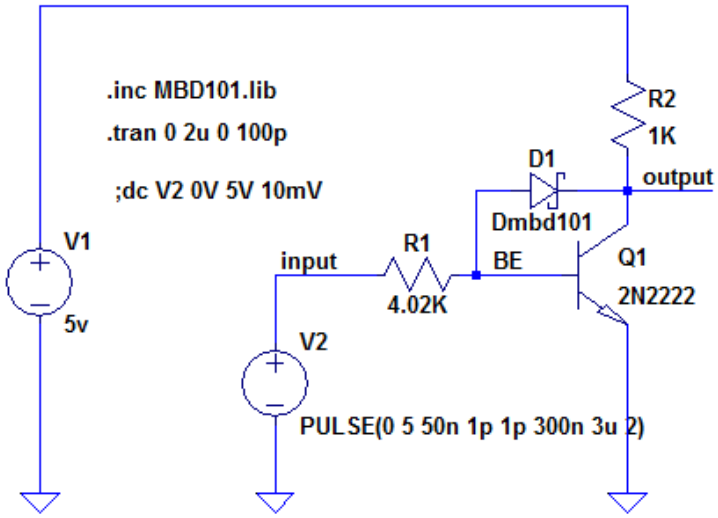
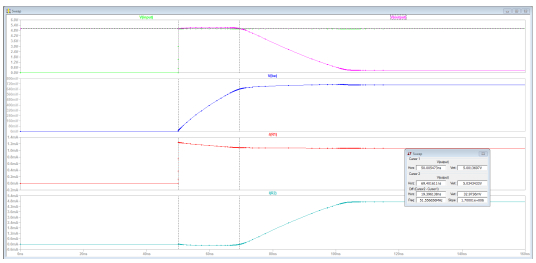
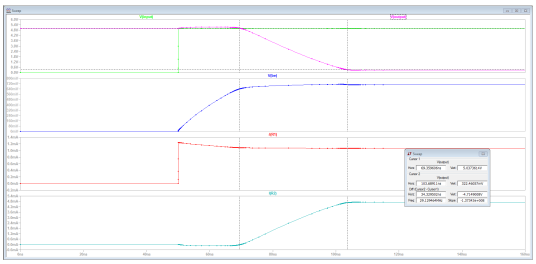


Figure 14: the RTL logic circuit with clamp

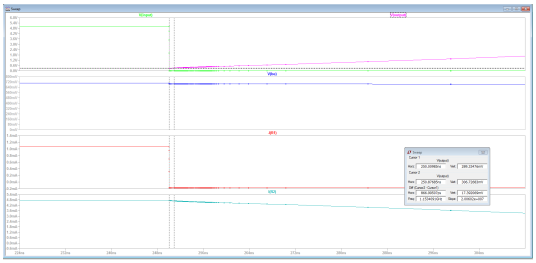
The measured delays for input pulse duration of $200nS$ is given in figure 15, where turn on delay is $19.40nS$, the fall time is $34.33nS$, the charge storage delay is $867.0ps$, and the rise time is $207.77nS$:



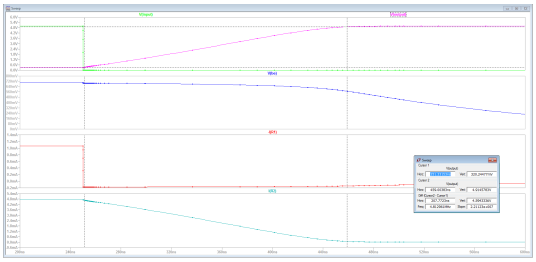
(a) measured turn on delay



(b) measured fall time delay



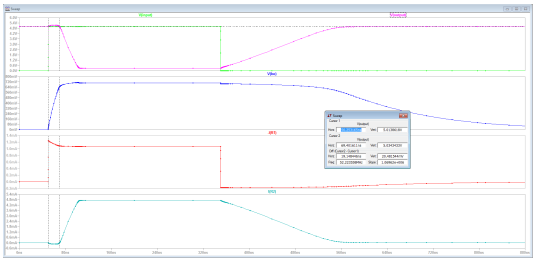
(c) measured charge storage delay



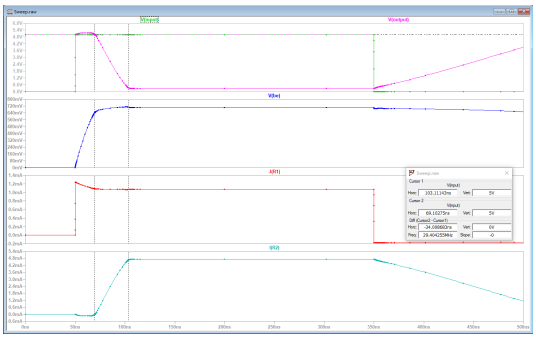
(d) measured rise time delay

Figure 15: Measured delays when input impulse duration is $200nS$

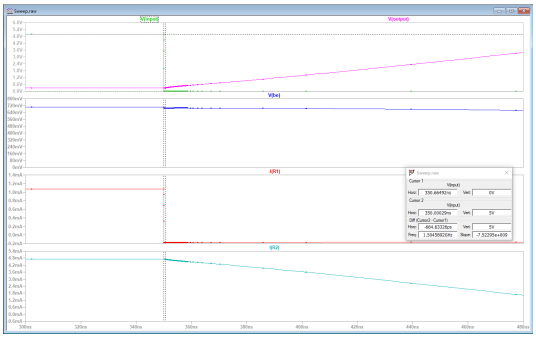
The measured delays for input pulse duration of $300nS$ is given in figure 16, where turn on delay is $69nS$, the fall time is $34nS$, the charge storage delay is $665pS$, and the rise time is $213nS$.



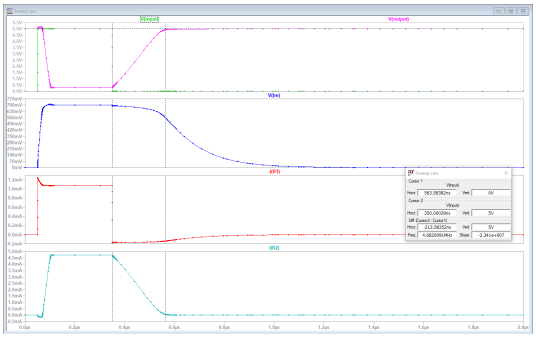
(a) measured turn on delay



(b) measured fall time delay



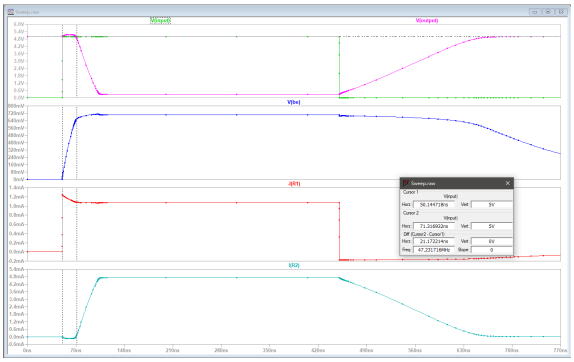
(c) measured charge storage delay



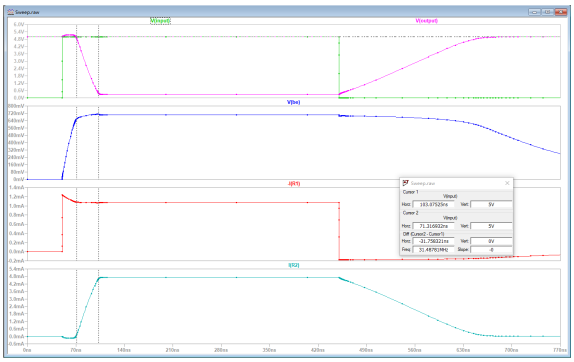
(d) measured rise time delay

Figure 16: Measured delays when input impulse duration is $300nS$

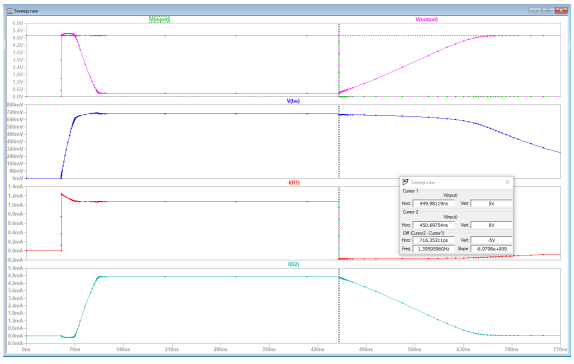
The measured delays for input pulse duration of 400ns is shown in figure 17, where turn on delay is 21.2nS, the fall time is 31.8nS, the charge storage delay is 716ps, and the rise time is 203nS:



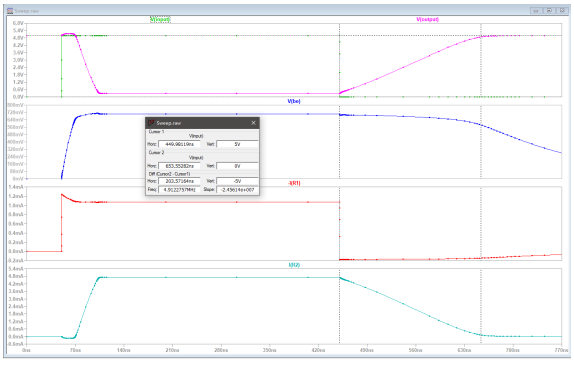
(a) measured turn on delay



(b) measured fall time delay



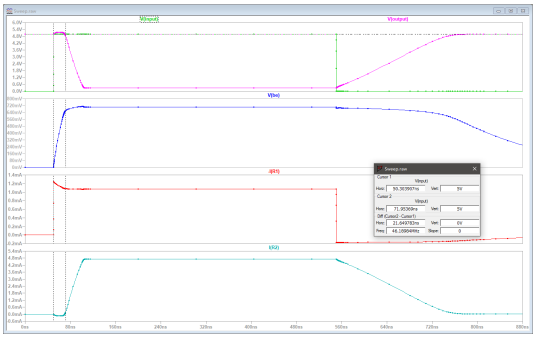
(c) measured charge storage delay



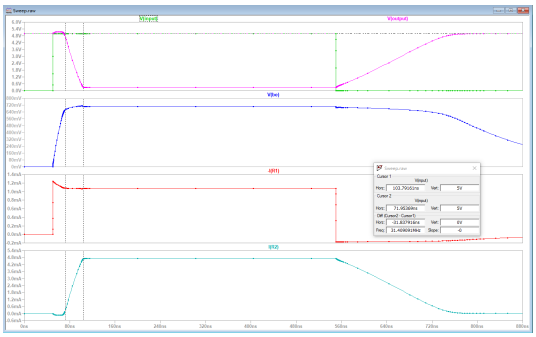
(d) measured rise time delay

Figure 17: Measured delays when input impulse duration is $400nS$

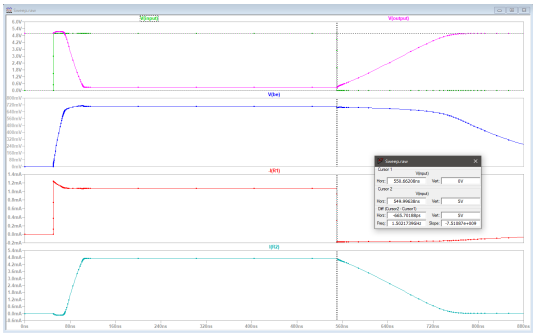
The measured delays for input pulse duration of 500ns is obtained in figure 18, , where turn on delay is 21.6nS, the fall time is 31.4nS, the charge storage delay is 665ps, and the rise time is 209.6nS:



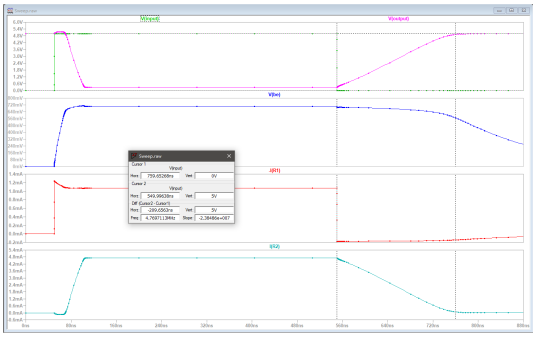
(a) measured turn on delay



(b) measured fall time delay



(c) measured charge storage delay



(d) measured rise time delay

Figure 18: Measured delays when input impulse duration is $500nS$

Comparing these value with their unclamped counterparts, the charge storage delay has been improved significantly. The overall delays are also improved.

1.6 Question 1.9

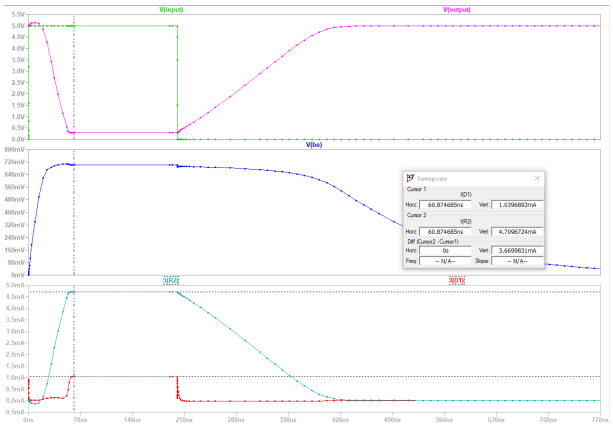


Figure 19: The current of clamp diode and BJT collector when near saturation region

From the figure 19, we can obtain that the current in the clamp diode is $1.04mA$ and the collector current is $4.71mA$. Due to the introduced clamp diode, the voltage of BE can be clamped to only $0.412V$, but not $-0.688V$ without this diode (the results are obtained from simulation of LT spice). Therefore, the charge in the base region is reduced when the BJT is in saturation region, the charge storage delay can be reduced sharply according to this clamping method.

2 TTL and LSTTL

2.1 Question 2.2

From leture notes, we have:

$$t_{PHL} \approx t_{ON} + t_{FALL} \tag{10}$$

$$t_{PLH} \approx t_{CSD} + t_{RISE} \tag{11}$$

The schematics is shown in figure 20

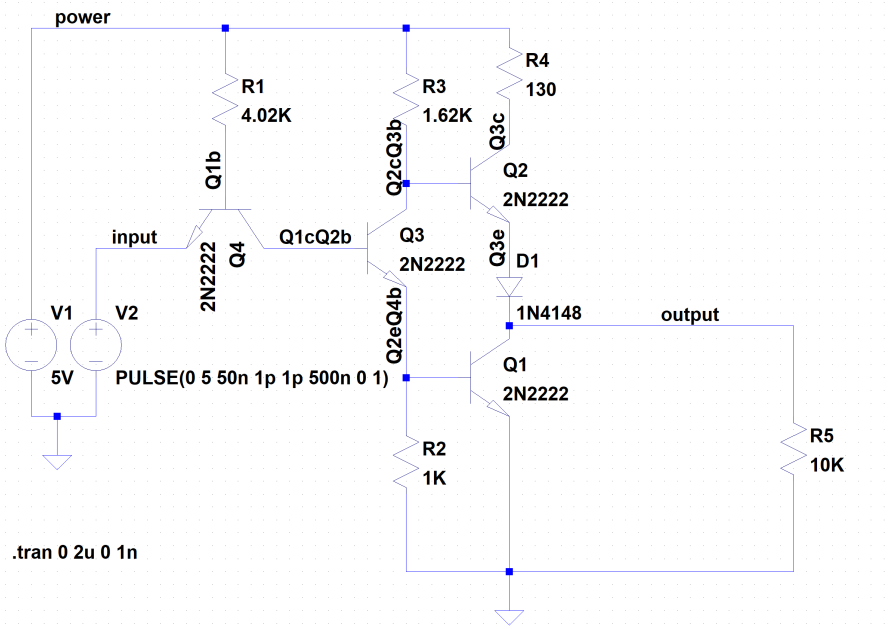
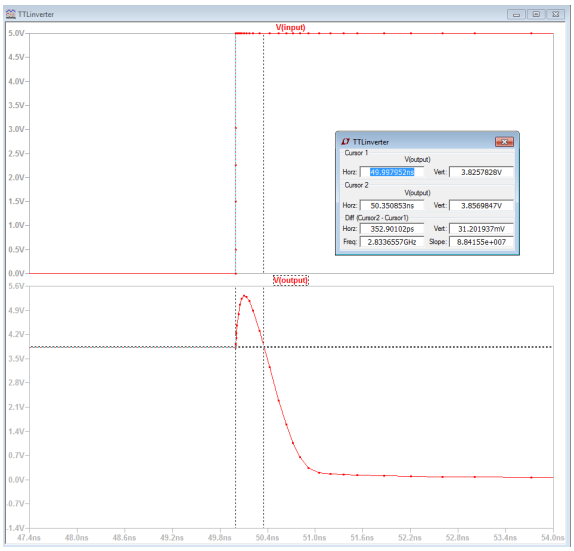
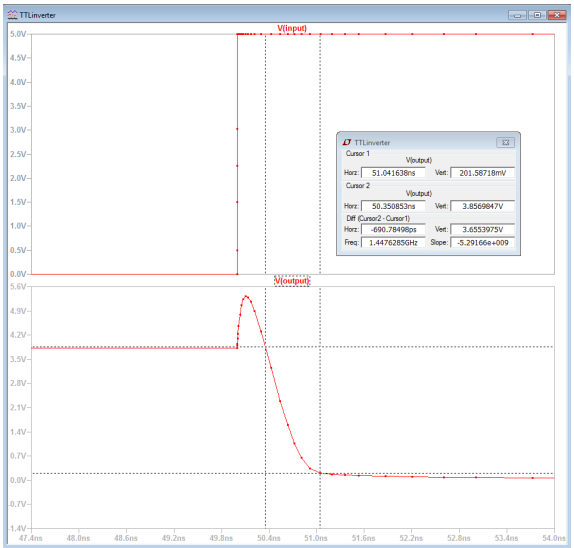


Figure 20: Built Schematic

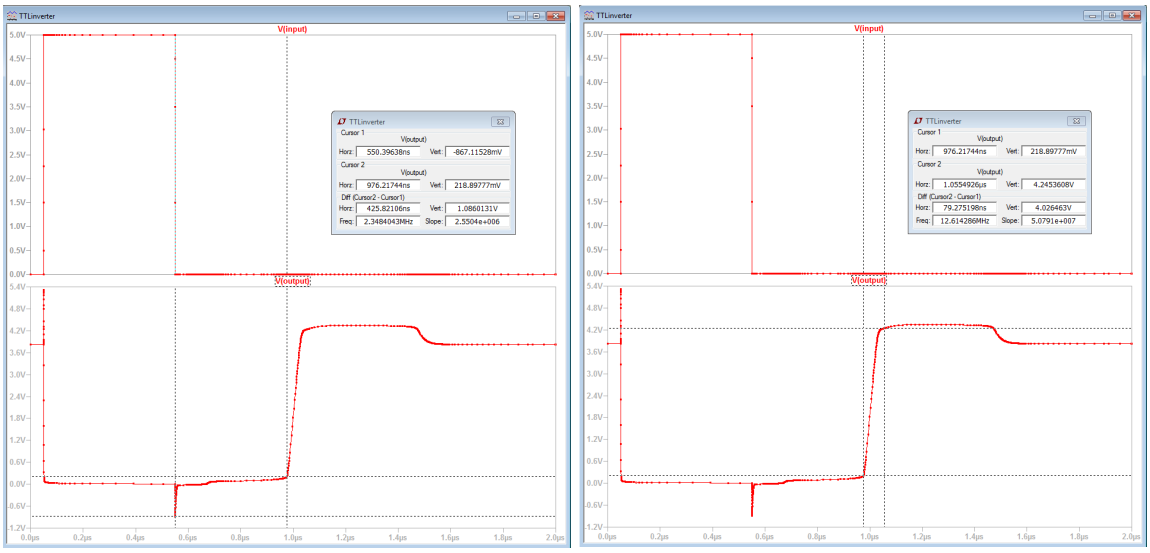
After implementing the simulation circuit, we measure $t_{ON} = 353ps$, $t_{FALL} = 691ps$, $t_{CSD} = 426ns$, $t_{RISE} = 79ns$ as figure 22:



(a) measured turn on delay



(b) measured fall time delay



(a) measured charge storage delay (b) measured rise time delay

Figure 22: Measured delays

Hence, our $t_{PHL} \approx 1ns$, $t_{PLH} \approx 505ns$. The low-to-high propagation time is far larger than the other. **The reason is that charge storage delay contained is significant when transistors working in deep saturation region.** This can be further verified by the working state of each transistor as below (Two transistors working in saturation region).

2.2 Question 2.3

By measuring the voltage at base, emitter and collector, we get the working state of each transistors. The work states of three NPN transistors from output to input are as below:

Figure 23: Work state of Q1

From the figure above, when input voltage is 5V, Q1 is working at saturation region as $V_{BE} = 5V > 0, V_{BC} = 4.8V > 0$.

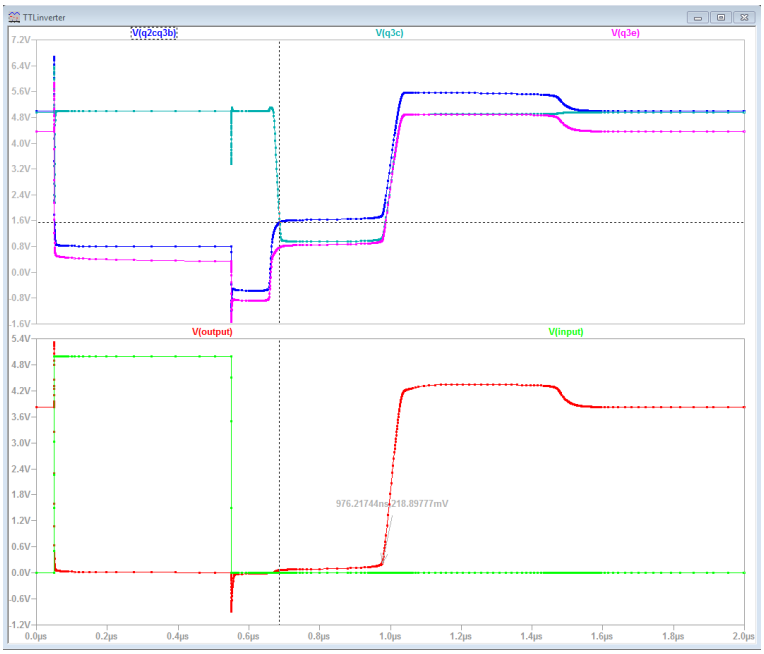


Figure 24: Work state of Q2

From the figure above, when input voltage is 5V, Q2 is working at active region since $V_{BE} = 0.8 - 0.4 = 0.4V > 0, V_{BC} = 0.8 - 5.0 = -4.2V < 0$.

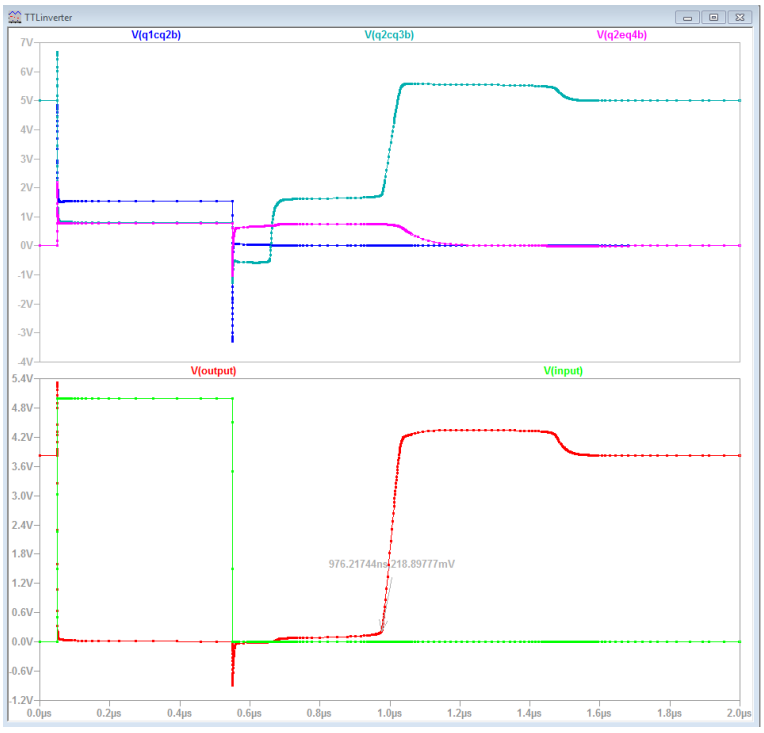


Figure 25: Work state of Q3

From the figure above, when input voltage is 5V, Q3 is working at saturation region since $V_{BE} = V_{BC} = 0.8V > 0$.

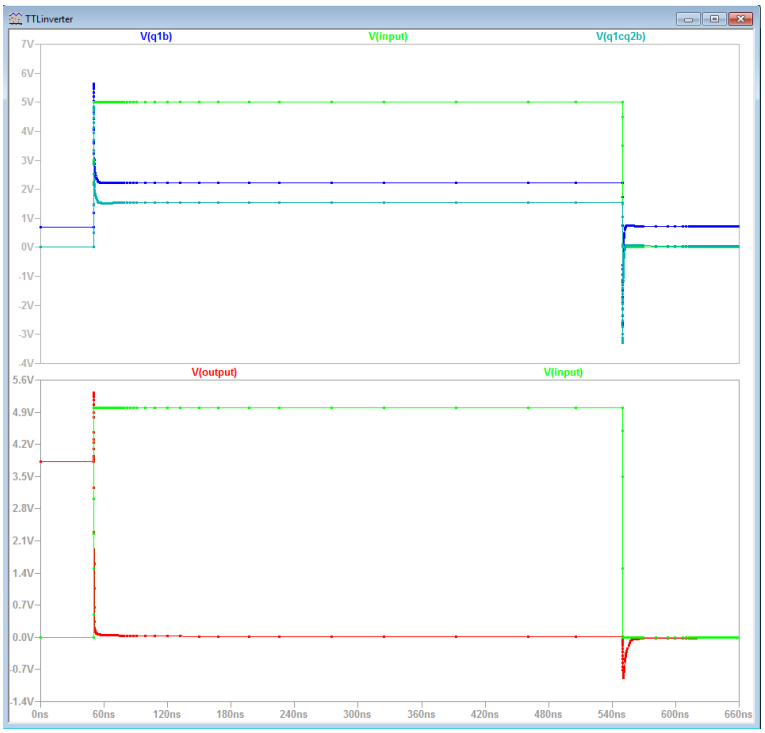


Figure 26: Work state of Q4

From the figure above, when input voltage varies from 0 to 5V, Q4 is working from saturation region to reverse active as $V_{BE} = 2.2 - 5 = -2.8V < 0$, $V_{BC} = 2.2 - 1.6 = 0.6V > 0$. From figures above, the output voltage has a huge increase at $1us$. **The diode D1 in the schematic is preventing the output voltage re-pulls to Q2 when output voltage increasing.**

2.3 Question 2.4

The measured plotted instantaneous power is as below:

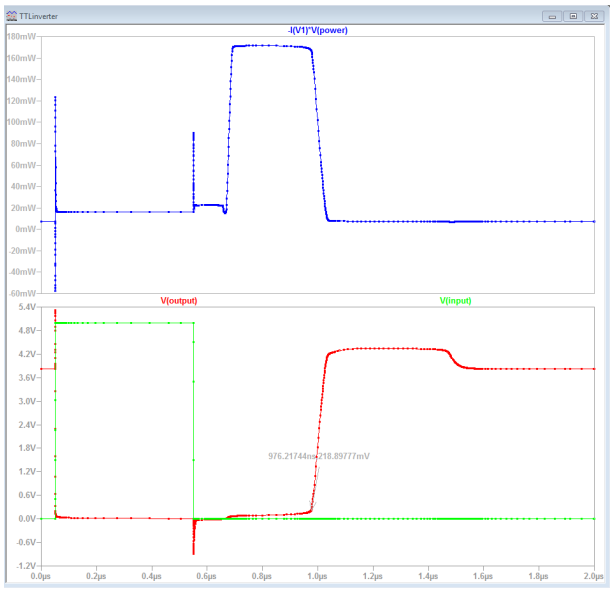


Figure 27: Instantaneous power at Vpower

Our measured peak power between 0 2 us is $122.88mW$ at $50.91ns$. The average power measured in the

$2uS$ interval is $37.128mW$ as below:

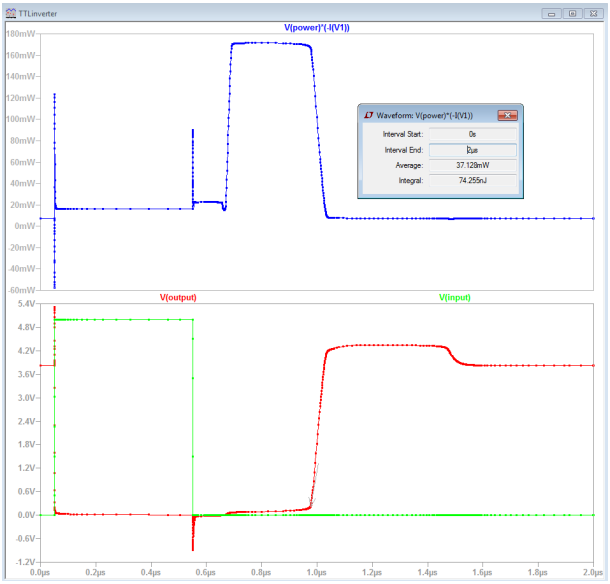


Figure 28: Average power in the 2us at V1

2.4 Question 2.5

The built schematic is as below:

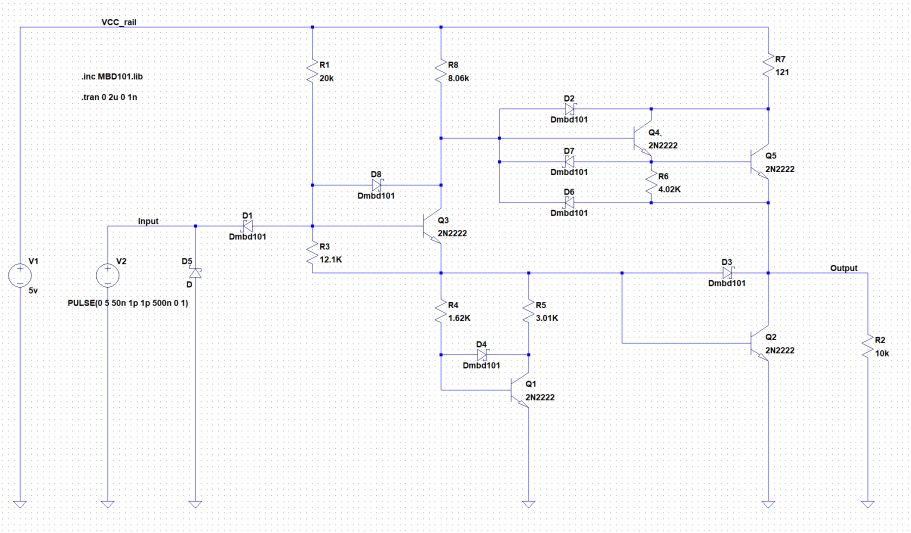
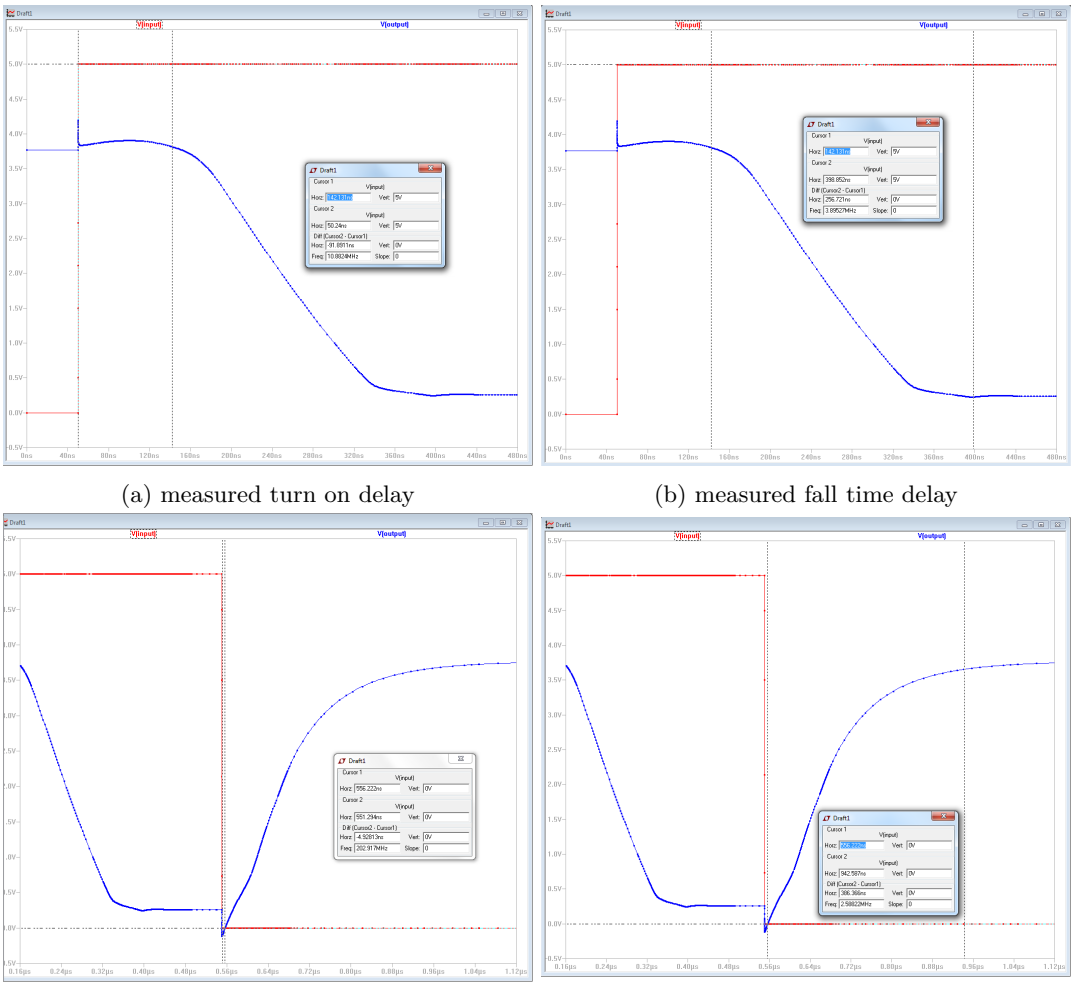


Figure 29: Built STTL circuit

Similarly, we can get $t_{PLH} = 392ns$ and $t_{PHL} = 294ns$ from the measured delays as below:



(a) measured turn on delay

(b) measured fall time delay

(c) measured charge storage delay

(d) measured rise time delay

Figure 30: Measured delays

By comparing the gathered t_{PLH} and t_{PHL} with their counterparts in the TTL circuit. The low-to-high propagation time is decreased a lot. **The reason is that charge storage delays in the circuit are significantly decreased by implementing Schottky clamps.**

2.5 Question 2.6

The instantaneous power is as below:

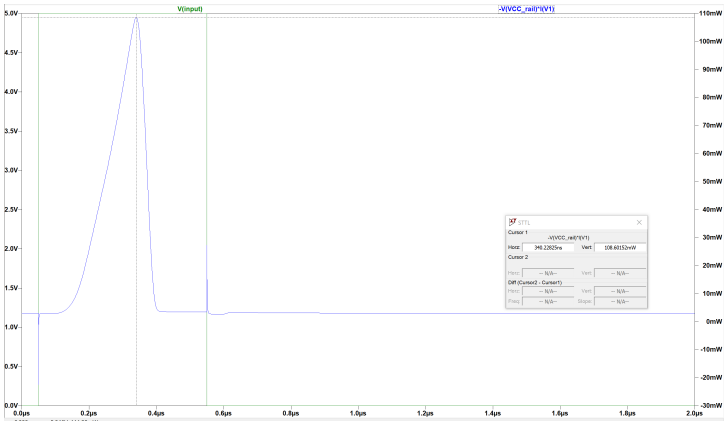


Figure 31: Measured peak power

The peak power is $108.6mW$ and the average power is $9.48mW$. **Comparing these value with TTL circuit above, the power efficiency in LSTTL circuit has been much improved as most transistors are prevented from deep saturation.** When it comes to the overall performance, the LSTTL circuit is a better choice compared with TTL circuit. The general propagation delay is similar, where LSTTL has a much shorter charge storage delay and rise delay, a larger turn on delay and fall time delay. This is because that Schottky clamps prevent the circuit from deep saturation which would affect much on charge storage delay and fall delay. The power efficiency is much higher as current is limited by active pull-down.

2.6 Question 2.7

The plotted base, emitter, and collector voltage for q5 is as below:

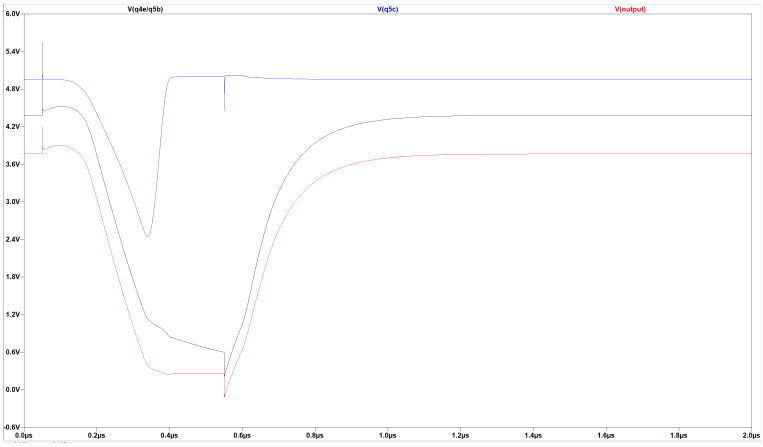


Figure 32: Measured transistor q5

From the figure above, **there is not a time when base voltage can be clamped to 0.4 beyond collect voltage like all other transistors.** Hence, our q5 is not a anti-saturation clamp. Anti-saturation clamps can prevent the deep saturation state by a Schottky diode between base and collector which can guarantee the voltage drop $V_{be} \leq 0.4V$. From this prospective, **Q5 is not a Schottky transistor as the voltage drop between base and collector can be 0.8V** ($2V_{D,ON}$). This is consistent with the simulation result we get.

2.7 Question 2.8

Build the circuit and implement DC sweep as below:

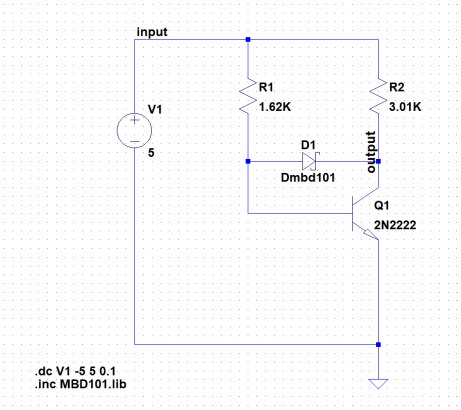


Figure 33: Test schematic of q2

To show this can be seen as an active pull-down, we measured current pulling in as below:

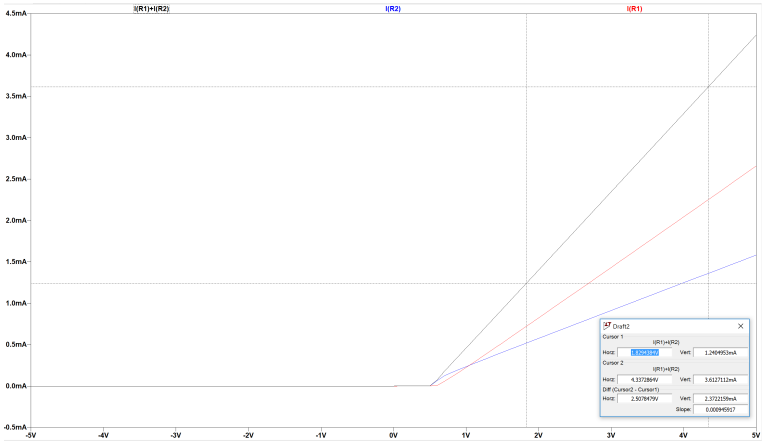


Figure 34: corresponding current as input sweeping

This circuit can be seen as a 1000Ω resistor after the base voltage is larger than 0.7V. Hence, it acts like an active pull-down which will limit the input voltage for Q2.**On the other hand, this circuit can improve the switching speed as it would not decrease the current while pulling down the voltage. Hence, larger current will increase the charge speed of Q2.**

3 Emitted coupled logic (ECL)

3.1 Question 3.1

The built 10K Emitter coupled logic circuit is below:

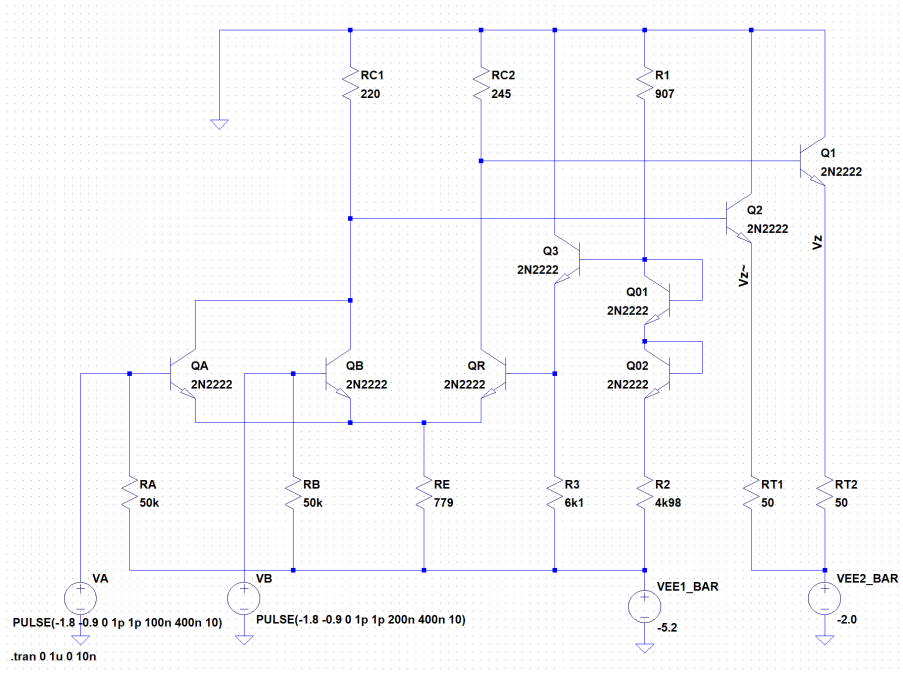


Figure 35: Built ECL

i according to the definition of ECL, all the voltage is negative and the highest voltage is GND (zero) in this circuit. Hence, the circuit is a **NECL**.

ii The resistors **RT1** and **RT2** share a different voltage which independent to the basic logic part. Yields the two resistors should be external to logic gate. More concretely, **as the ECL signals are extremely fast, we need terminate the signal into a characteristic impedance Z_o, those two resistors illustrate this Z_o** .

iii The reason for driving terminated transmission lines is that there are two emitter followers at the output ports. the emitter follower does not have on-chip load and therefore ECL can be used for driving the terminated transmission line. The third part of the ECL gate circuit is composed of the two emitter followers, Q2 and Q3. The emitter followers do not have on-chip loads, since in many applications of high-speed logic circuits the gate output drives a transmission line terminated at the other end, as indicated in Fig. 15.27. (More on this later in Section 15.4.6.)

iv The sub-circuit QD1, QD2 and R2 is used as the bias network for one side of different pair which is determining the input voltage swing center(in other words, it supply the bias voltage).

3.2 Question 3.2

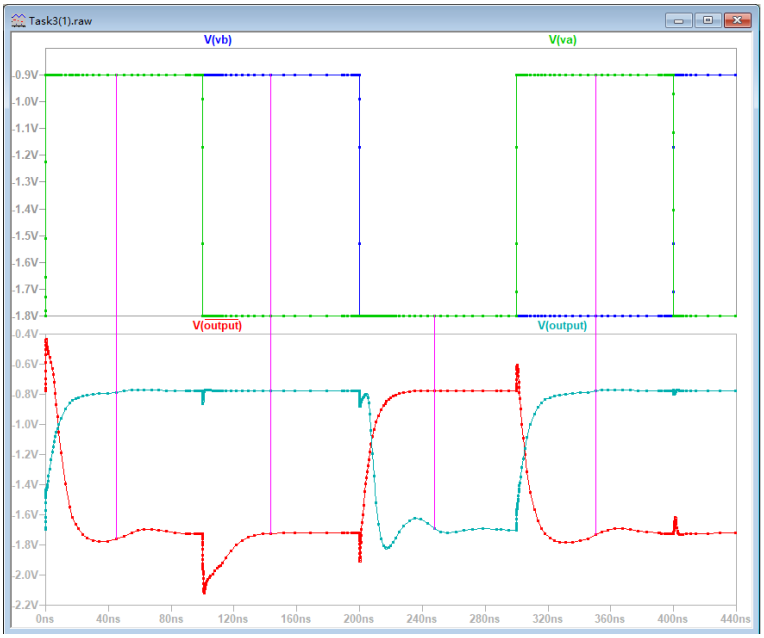


Figure 36: logic function of ECL

1. From the datasheet shown in figure 40,we can obtain the input figure for NPEL, V_{IL} is from $-1.95V$ to $-1.48V$ and V_{IH} is from $-1.17V$ to $-0.94V$. in our simulation, we adjust the high input value as $-0.9V$, and low input value is $-1.8V$.

2. Based on the various input value, the output value can be obtained, based on the figure 36, the output figure is shown in table 1

output port	logic high	logic low
$\overline{output}$	$-0.79V$	$-1.72V$
$output$	$-0.79V$	$-1.72V$

Table 1: the output level at $Q1$ and $Q2$

3. From figure 36, we can obtain the truth table shown in table 2. After analyzing the truth table, yielding the logic functions: *output* port behaves **OR gate** and the $\overline{output}$ port behaves the **NOR gate**.

V_A	V_B	$\overline{output}$	$output$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Table 2: the truth table of ECL

3.3 Question 3.3

1. The input voltage is equal to V_A for the two output voltages which is shown in figure 38, in this circuit, we know that the two input are connected, hence, the input should be the same one. the low voltage (-1.8V) represents the logic '0' and high voltage (-0.9V) acts as the logic '1'. Also, the logic input and output simulated result is shown in figure 37.

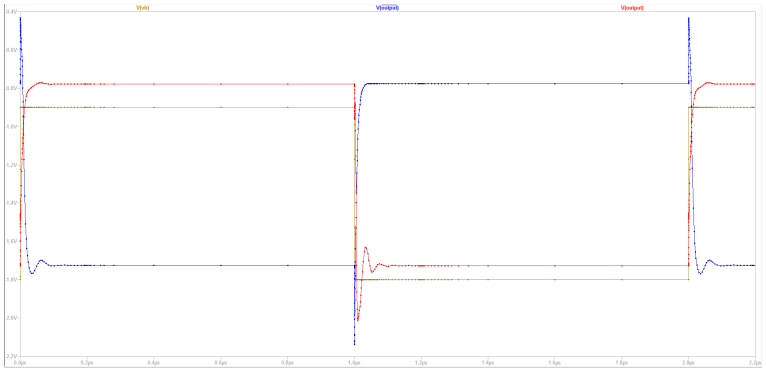


Figure 37: logic function of ECL

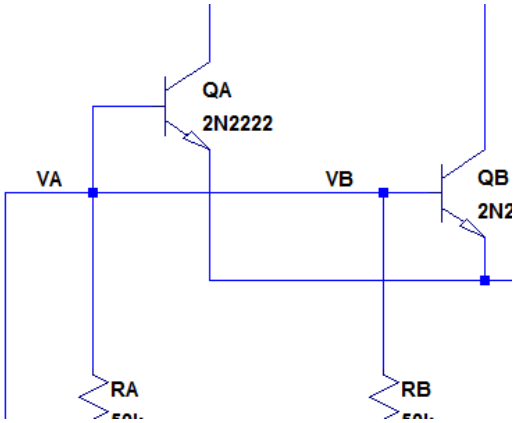


Figure 38: the same input for ECL

2. The transfer voltage can be obtained from LT-spice plot which is shown in figure 39. The results are listed in the table 3. by comparing the measured figures with given in datasheet, wen can obtain that

Category	actual voltage	datasheet reference(at room temperature)
V_{IL-MAX}	$-1.33V$	$-1.48V$
V_{IH-MIN}	$-1.159V$	$-1.13V$
V_{OL-MAX}	$-1.68V$	$-1.63V$
V_{OH-MIN}	$-0.809V$	$-0.98V$

Table 3: the value of input and output voltage in ECL

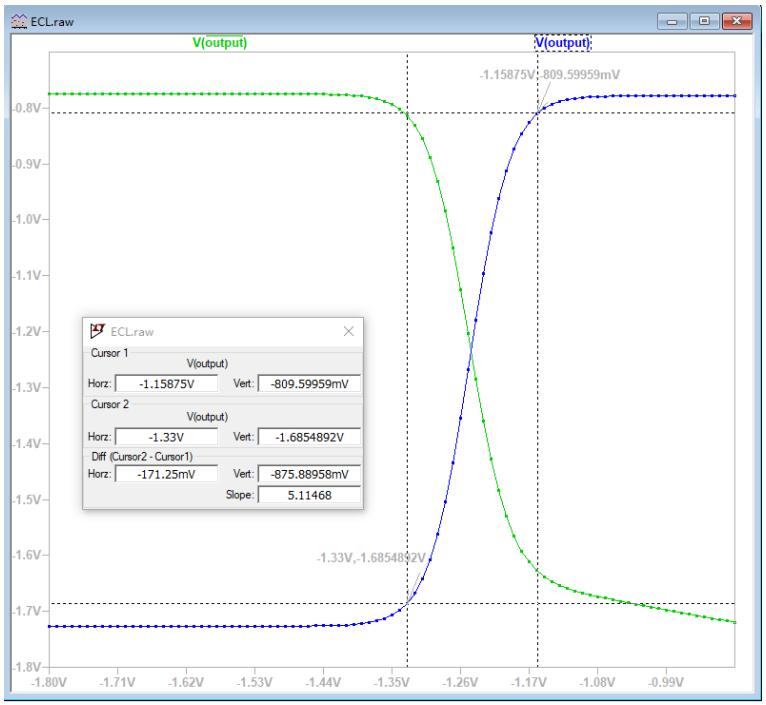


Figure 39: transfer characteristics of logic gate

3. The NM_H and NM_L can be obtained by using the result of last section.

$$\begin{aligned} NM_L &= V_{IL-MAX} - V_{OL-MAX} \\ &= -1.33V + 1.68V = 330mV \\ NM_H &= V_{OH-MIN} - V_{IH-MIN} \\ &= -0.809V + 1.159V = 330mV \end{aligned} \tag{12}$$

While comparing the high/low input/output obtained in this ECL circuit which is shown in table 3, the values are almost same or better than the figure in the datasheet (given in figure 40).
In this case, some measurement error may occurs when reading the figure from simulation results, hence the result obtained from simulation may have tiny difference with datasheet. In addition, the 10K ECL circuit can be built by different modes of BJT, hence, different modes or manufacturer may have different specifications. therefore, some small difference on the high or low level can be neglected in application.

Table 4. DC CHARACTERISTICS V_{CC} = +5.0 V ±5%; V_{EE} = −5.2 V ±5%, V_{CC} = 0 V (Note 1)

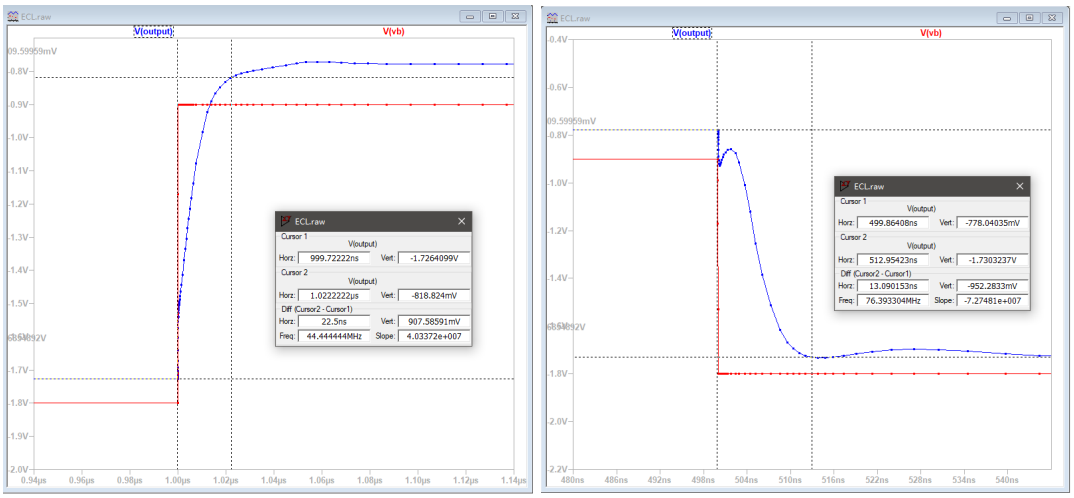
		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 2)	−1020		−840	−980		−810	−920		−735	mV
V_{OL}	Output Low Voltage (Note 2)	−1950		−1630	−1950		−1630	−1950		−1600	mV
V_{IL}	Input LOW Voltage ($\overline{LEN}$)	−1.95		−1.48	−1.95		−1.48	−1.95		−1.45	mV
V_{IH}	Input HIGH Voltage ($\overline{LEN}$)	−1.17		−0.84	−1.13		−0.81	−1.07		−0.735	mV

Figure 40: specific figure in the datasheet

3.4 Question 3.4

The high-to-low and low-to-high output propagation times $t_{PHL} = 13.09nS$ and $t_{PLH} = 22.5nS$ can be obtained from the plot in the LT-spice (shown in figure 41) and the transient simulation is given in 37.
When comparing the propagation delay to TTL, we find that the T_{PHL} almost same, but the T_{PLH} in ECL is much shorter than TTL, the reason is that the **charge storage delay** decrease a lot in ECL circuit.
Another comparison on the ECL and LSTTL shows that the T_{PHL} of ECL is longer than LSTTL due

to the fall time of ECL, but the T_{PLH} is much shorter than LSTTL due to the limited **charge storage delay**.



(a) ECL low-to-high propagation delay (b) ECL high-to-low propagation delay

Figure 41: ECL propagation delay

3.5 Question 3.5

The instantaneous and average power are given in figure 42 and the average power consumption is $29.928mW$. Comparison with TTL (37.1mW) and LSTTL (9.48mW), ECL has a relevant high power consumption.As a result, The circuit of TTL and LSTTL are both need higher power than LSTTL.

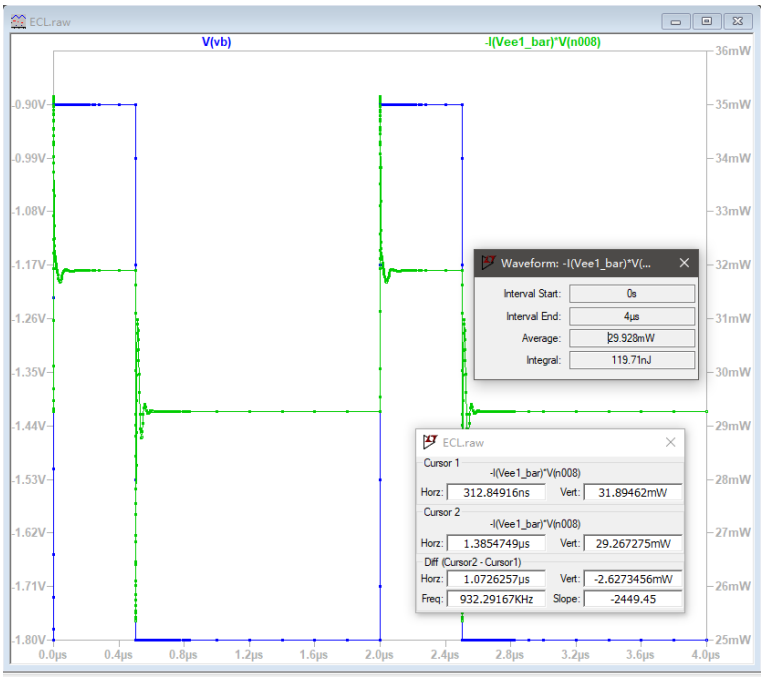


Figure 42: Instantaneous power and average power consumption plot

3.6 Question 3.6

for ideal case, what we expect is that the average power dissipation should no change when the frequency changes. However, when the output status is changing, the quite large instance power consumption will occur. Therefore, the average consumption will increase as the frequency rises.

4 CMOS

4.1 Question 4.1

The built circuit in LTspice is as below:

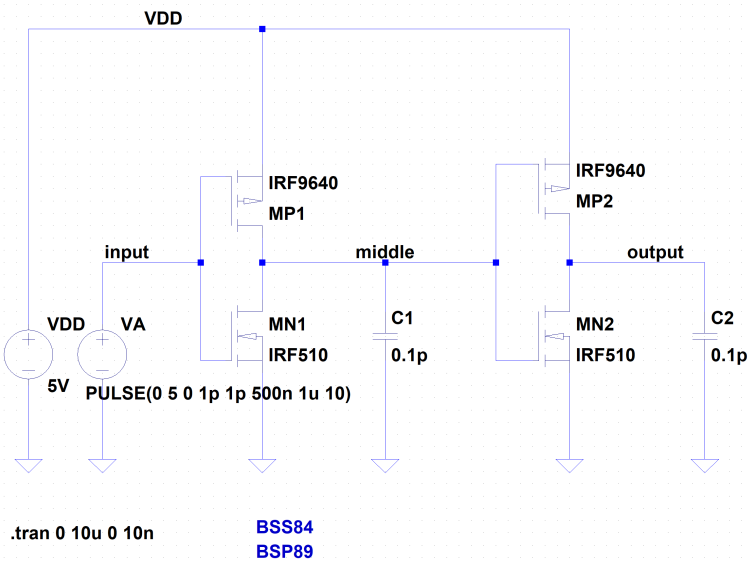


Figure 43: Schematic for task 4

4.2 Question 4.2

The transisent plots for the whole circuit are as below:

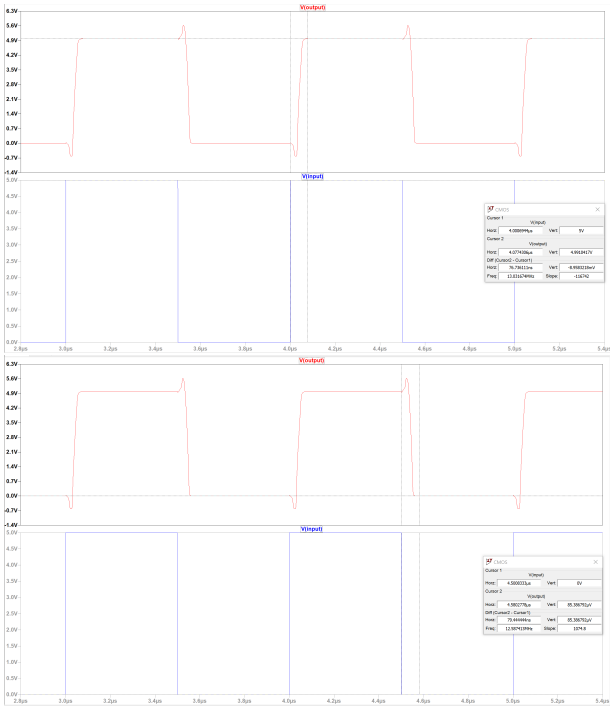


Figure 44: simulation result

Frome the figure above, the measured $t_{PLH} = 76.7nS$ and $t_{PHL} = 79.4nS$ **Compare this values with their counterparts in TTL, LSTTL and ECL circuit, the over-whole propagation time**

is much approved. Since it's two CMOS inverters in series, the propagation speed for a single converter should be even faster.

4.3 Question 4.3

Simulated current flow shown as below:

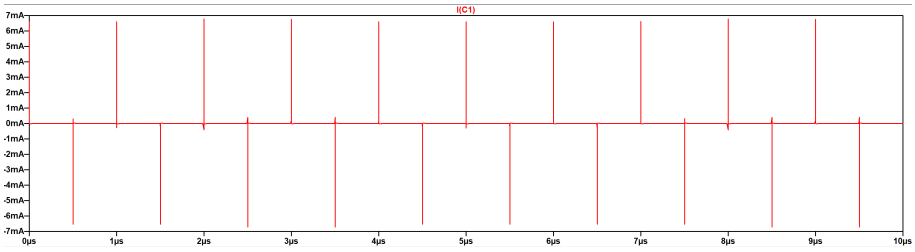


Figure 45: Current flow from the first gate

The steady state value of this current is 0. Since only during the transition band it has current change between two transistors.

4.4 Question 4.4

The figure below shows the instantaneous power and C1 voltage, **then we can state the fluctuation is caused by charging or releasing power of the capacitor.** Measured dissipated power at transient is 32mW. The overall power consumption is extremely low compared with the previous designs as power only dissipated during the state transient (the measured average is 1.128uW).
Comparing power consumption of each design during 0-2us: TTL and ECL consume most power (37.128mW and 29.9mW), LTTL design reduces the power consumption to 9.48mW. CMOS design has the most power efficiency, only consume 1.128uW.

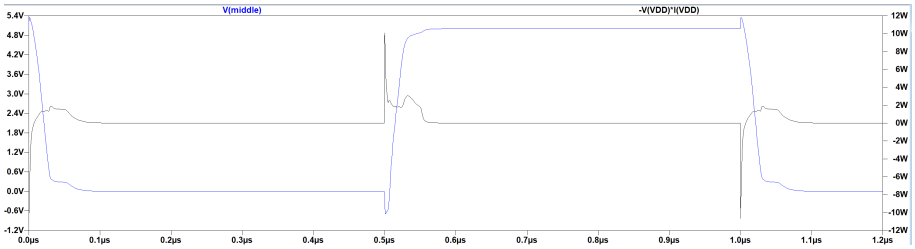


Figure 46: Power dissipated by the circuit

4.5 Question 4.5

Compared the power MOSFETS we plugged in this experiments with the normal signal MOSFETS, the former ones consume less power when switch is ON and OFF. Henceforth, out power dissipation will increase. The reason behind is that the on-resistance is minimized in the power MOSFETS which can also reduce the propagation delay. Besides these, gate oxide of the power MOSFETS is thick which can handle the high voltage input.

5 BiCMOS

5.1 Question 5.1.1

The built schematic is as below:

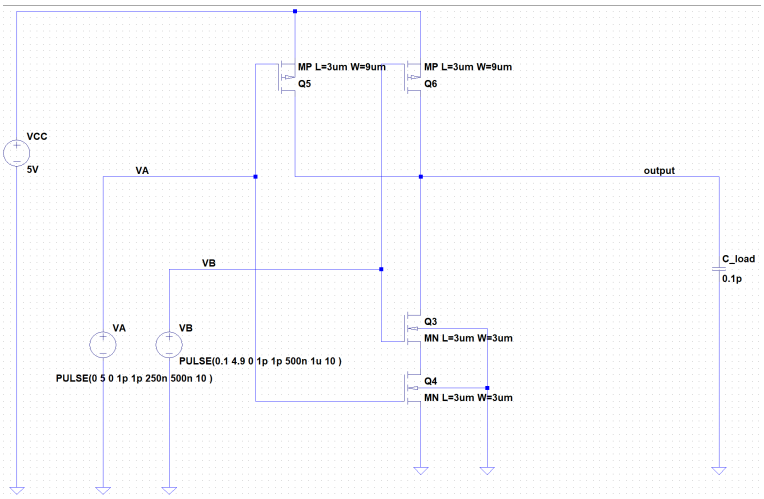


Figure 47: Schematic of the BiCMOS inverter

5.2 Question 5.1.2

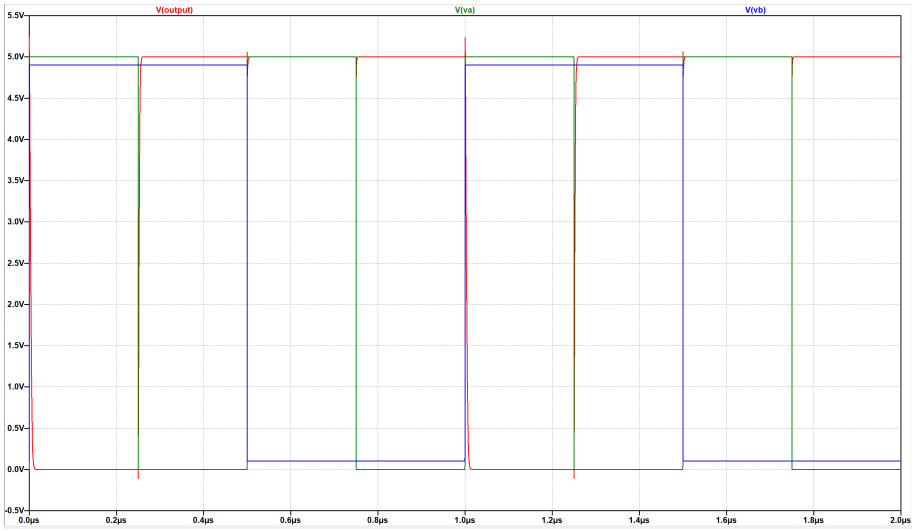


Figure 48: Plotted logical relation

Based on the plotted output voltage and input voltage, since only if two inputs are high, the output would become low, **this logical circuit is a 'NAND' gate circuit.**

5.3 Question 5.1.3

When $C_{LOD} = 0.1pf$, the measured high-to-low and low-to-high output propagation delays are $t_{PHL} = 19.4nS$ and $t_{PLH} = 17nS$.

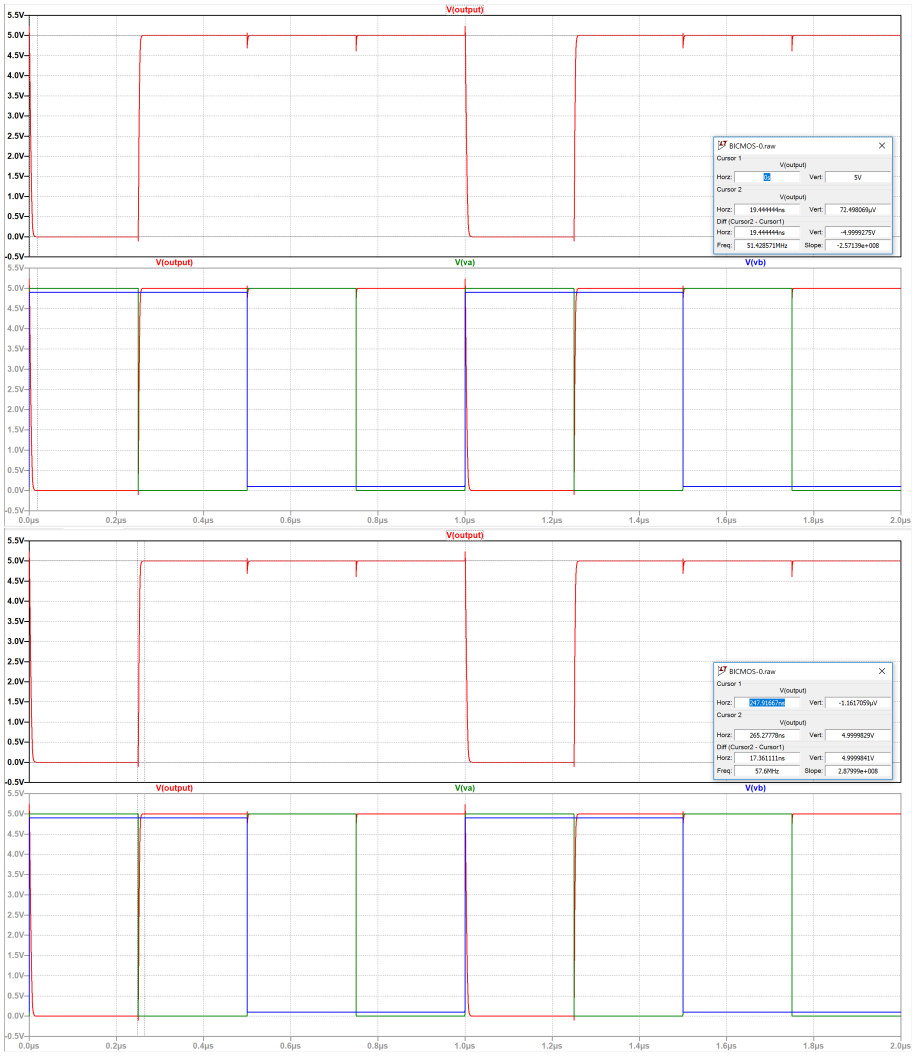


Figure 49: Plotted delay when $C_{LOD} = 0.1pf$

When $C_{LOD} = 1pf$, the measured high-to-low and low-to-high output propagation delays are $t_{PHL} = 127.7nS$ and $t_{PLH} = 70.17nS$.

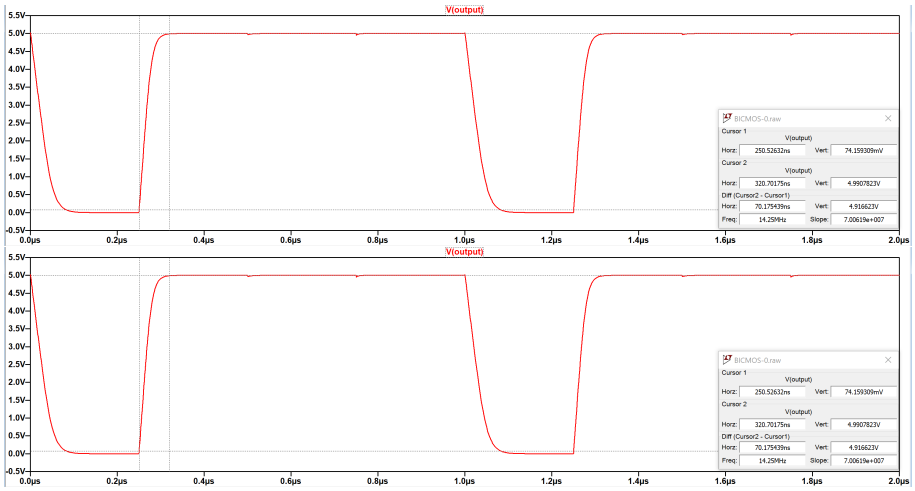


Figure 50: Plotted delay when $C_{LOD} = 1pf$

When $C_{LOD} = 10pf$, the high-to-low propagation delays cannot be fully measured as it is larger

than 0.25uS pulse width. Under this circumstance, $t_{PHL} = 250nS$ and $t_{PLH} = 749nS$. To obtain the accurate delay, we then increase the pulse width of A to 1u ,B to 2u, and measured $t_{PHL} = 995nS$ and $t_{PLH} = 696nS$ as below.

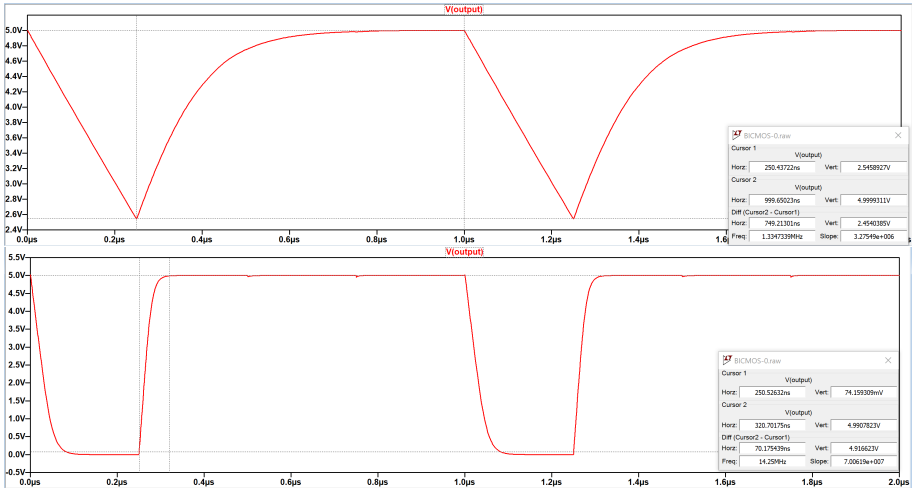


Figure 51: Plotted delay before and after increasing pulse width

In conclusion, the circuit is mainly limited by high-to-low delay which increase as the load capacitor increasing. Hence, the circuit can drive 0.1pF and 1pF capacitor while the 10pF capacitor is beyond the capability of this circuit.

5.4 Question 5.2.1

After implementing a BJT push-pull output stage, the built schematic states below:

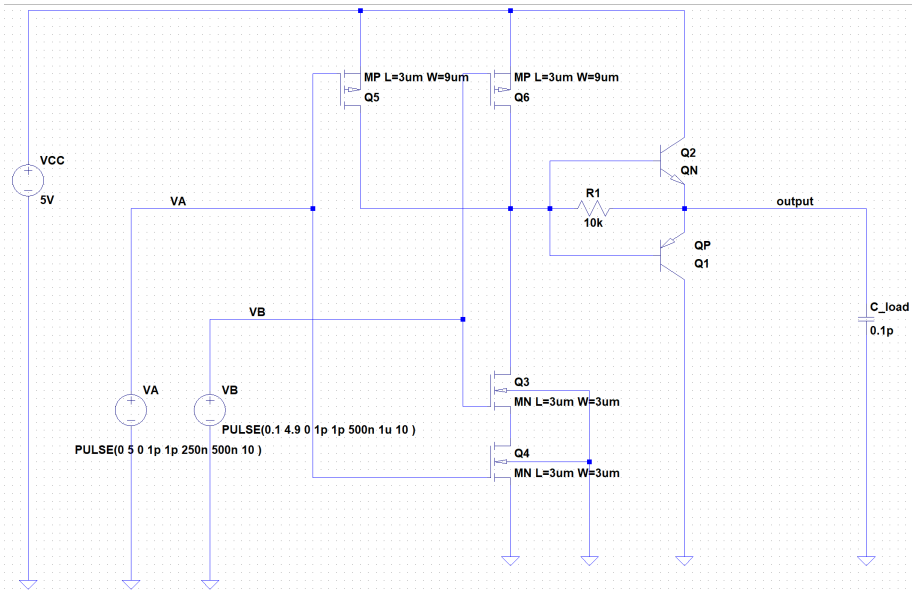


Figure 52: BiCMOS inverter with push pull circuit

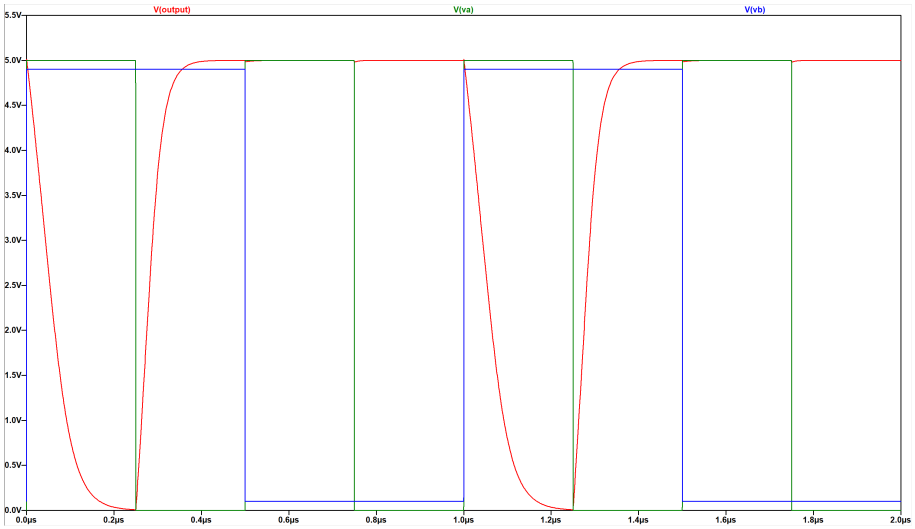


Figure 53: Plotted logical relation

From output and input plot above, the logical function is consistent with the circuit in 5.1 and it is a **'NAND'** logical circuit.

5.5 Question 5.2.2

When $C_{LOD} = 0.1pf$, the measured high-to-low and low-to-high output propagation delays are $t_{PHL} = 247.6nS$ and $t_{PLH} = 407.8nS$.

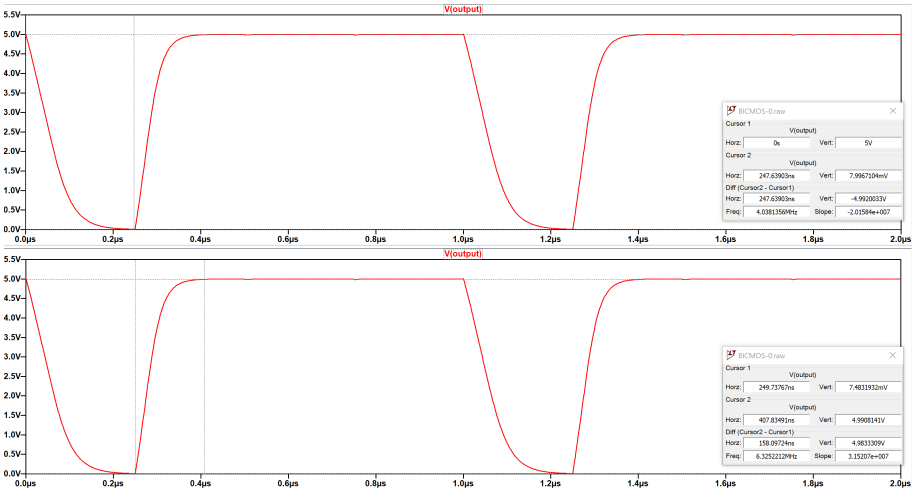


Figure 54: Plotted delay when $C_{LOD} = 0.1pf$

When $C_{LOD} = 1pf$, the measured high-to-low delay already beyond 0.25us pulse width. Under this circumstance, $t_{PHL} = 250nS$ and $t_{PLH} = 591nS$.

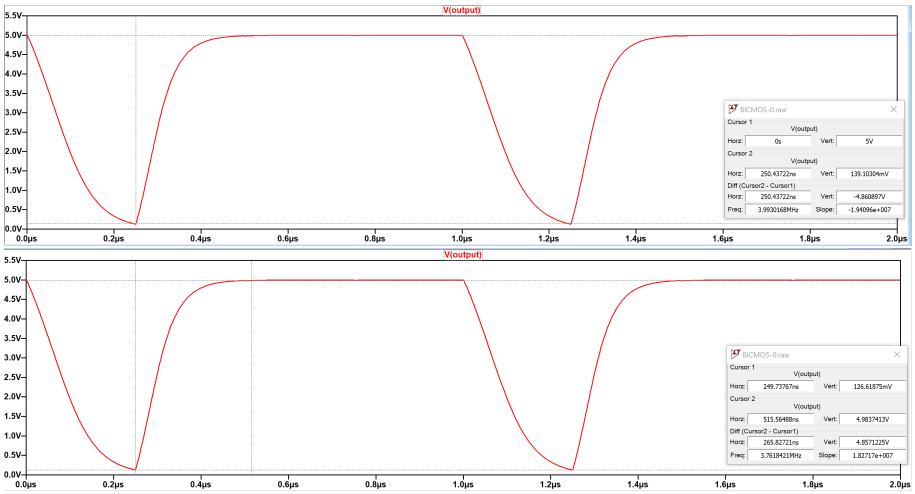


Figure 55: Plotted delay when $C_{LOD} = 1pf$

Similarly, when $C_{LOD} = 10pf$, both t_{PHL} and t_{PLH} reach the input pulse width. Under this circumstance, $t_{PHL} = 250nS$ and $t_{PLH} = 750nS$.

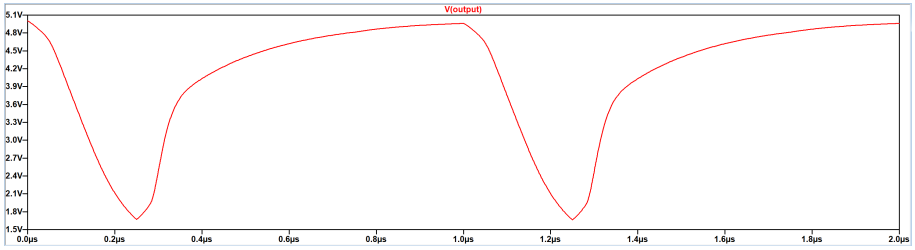


Figure 56: Plotted delay when $C_{LOD} = 10pf$

By comparing 5.2.2 and question 5.1.3, after we plugging a BJT push-pull circuit, this structure increases the delays of the circuit and degenerate the capability of the circuit (as it cannot handle the capacitor with above 1pf capacitance from the perspective of noise magin). On the other hand, it improved the output performance by eliminating output ripple and current gain. **Henceforth, the general trade-offs made are between output impedance, current gain and noise margin.**

5.6 Question 5.2.3

By observing the output with resistor disconnected as below, **we can state the resistor we used is to compensate the voltage lost on BJT.** Without this resistor, our output voltage won't reach 5V and 0V as shown below, the effect discussed can be verified by comparing this with figure 48 or 49:

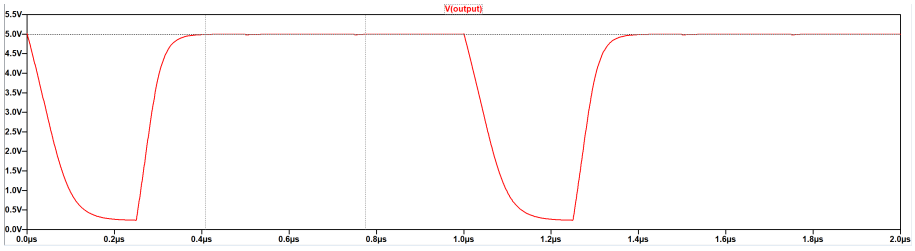


Figure 57: Plotted output when resistor disconnected

5.7 Question 5.3.1

By modifying the schematics from BICMOS-2, the BiCMOS logic gate with auxiliary inverters is obtained, the schematics and simulated plots are shown in figure 58.

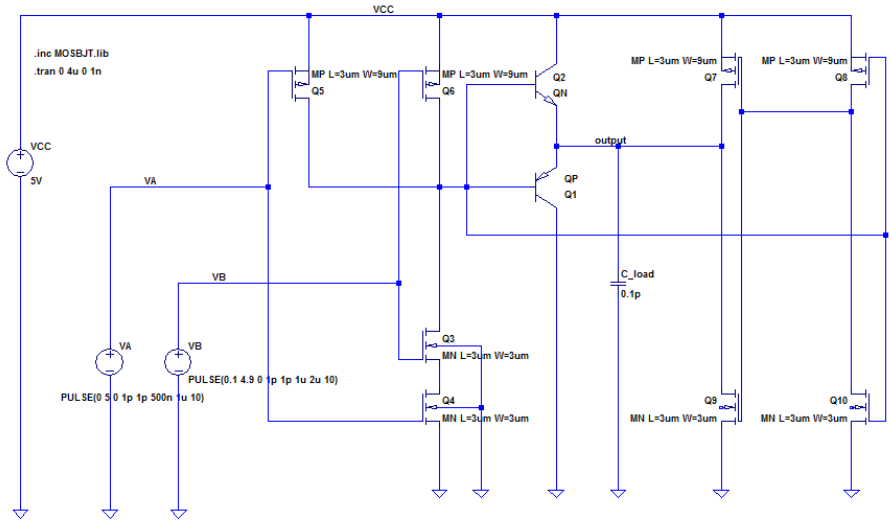


Figure 58: The schematics of BICMOS gate with auxiliary inverters

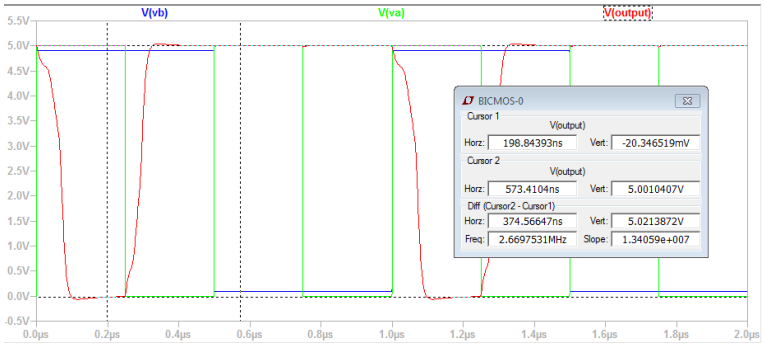


Figure 59: output voltage display

Similarly, this circuit is a **'NAND'** gate.

5.8 Question 5.3.2

The high and Low output voltage in this section is shown in figure 59. From this output, we know that the high voltage is $5.0V$ and the low voltage is $-20mV$. After comparing with 5.1 and 5.2, the purpose of auxiliary CMOS inverters are to improve the noise margin. by using the auxiliary CMOS inverters, the high is higher than former output and the low output voltage is lower than former output.

5.9 Question 5.3.3

The instantaneous power in this circuit is shown in figure 60. the instant power is measured and the value is $228.906mW$. While comparing with basic CMOS logic circuit, the instant power is $210.299mW$. therefore, CMOS logic gate with auxiliary inverters has larger instant power than simple CMOS logic gate.

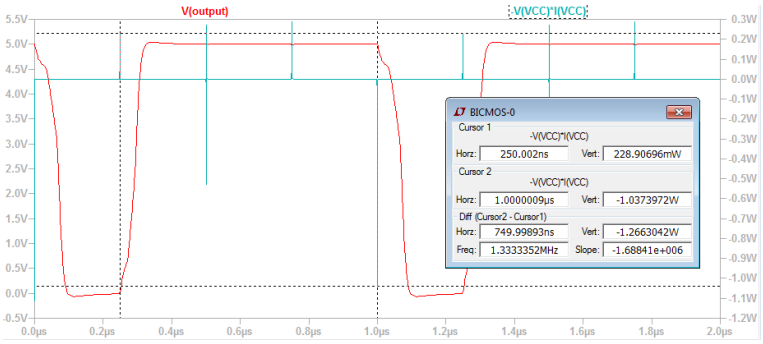


Figure 60: instantaneous power of BICMOS logic circuit

5.10 Question 5.3.4

By varying the frequency of input signal, the frequency of output signal will change. we change the output frequency to half and twice on original signal. the average power dissipations are shown in figure 61 to 63. the average power for comparison are $48.254uW$, $95.713uW$ and $182.49uW$ respectively. For ideal purpose, the power dissipation should be dependent on the frequency. However, the power dissipation will increase while the frequency changing faster.

The reason is that higher frequency means the increase frequency of changing the voltage level which will result in the increase the dynamic dissipation (shoot through and capacitive shunting result from changing of input and output voltage level). Therefore, the average power dissipation is higher while the logic gate working at higher frequency.

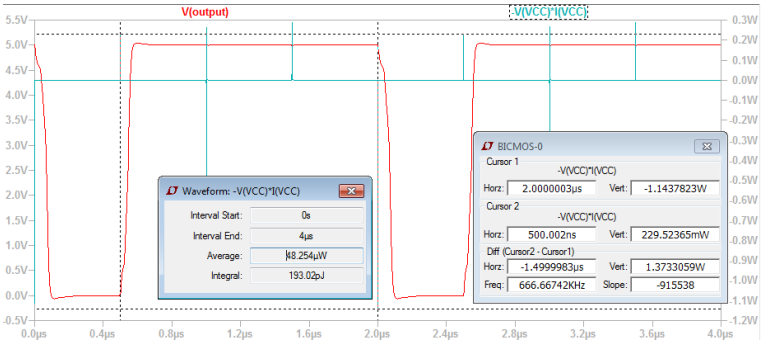


Figure 61: lower output frequency

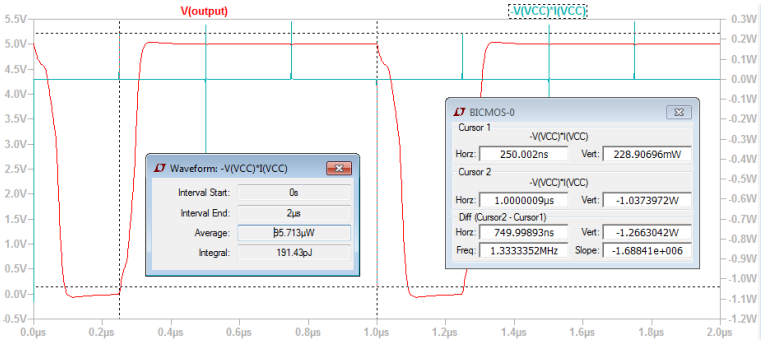


Figure 62: normal output frequency

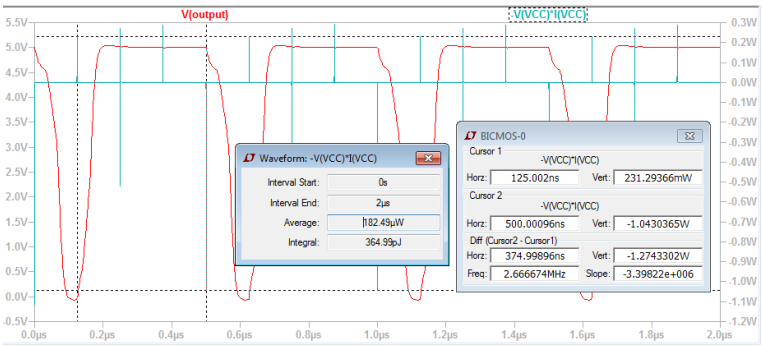


Figure 63: higher output frequency

6 SUMMARY

6.1

CMOS logic family is best suited to low power applications.
The feature of CMOS logic circuit is that the drain current is controlled by the gate voltage and the drive circuit is very simple. From question 4.3, CMOS logic circuit consume power only during the transition band. This can can be verified by comparing power consumption of different circuit design in question 4.4.

6.2

ECL, CMOS and BiCMOS logic families are suited to high switching speeds.
For ECL logic family, it is a kind of unsaturated logic circuit which means the BJTs in ECL logic circuit do not work in the saturation region. Hence, the switching speed of the ECL logic family can be very fast.
For CMOS and BiCMOS logic families, compared with ECL logic family, they use MOSFET instead of BJT to increase the switching speed in high speed applications.

6.3

ECL and BiCMOS logic families are suited to driving low impedance loads.
For ECL logic family, it uses emitter-follower output stage. Emitter-follower has low output impedance and can provide high current gain.
For BiCMOS logic circuit, it contains bipolar output stage which can provide high current gain.
Hence, they can provide high drive current in order to drive low impedance loads.

6.4

Question 1, explain the trade off between the switching speed and current drive:
On one hand, because of the minority carriers and charge storage delay, BJT's switching speed is slow and it is not commonly used in high speed electronics applications. And we need to use MOSFET to increase the switching speed. On the other hand, for the same size, because of the high trans-conductance, BJT's output current is higher than the CMOS which means BJT has a better performance for current drive. But use BJT will decrease the switching speed.
Hence, the trade off between current drive and switching speed is that, sometimes, we needs to sacrifice the switching speed in order to obtain better current drive capability, or degrade the current drive capability in order to increase the switching speed.
Question 2, Which families are designed for high switching speed and good performance for current drive?
ELC and BiCMOS logic family are designed for both. For ELC logic family, on one hand, emitter follower has low output impedance and can provide high current gain. On the other hand, the unsaturated circuit can increase the switching speed. For BiCMOS, on one hand, it contains bipolar output stage to increase

the capability of current drive. On the other hand, MOSFET is used to increase the switching speed for high speed applications.