GATE VOLTAGE PROPAGATION DELAY IN POWER MOSFETS

by

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CHAPTER I

INTRODUCTION

Since the first transistor was successfully made operational in early 1950's, different types of semiconductor devices have appeared on the market to perform various tasks. When these devices are used according to their specifications, they are reliable. Because of their recognized reliability, lifetime, and reproducibility, the number of semiconductor devices for switching high currents has increased in recent years. Among different power devices which have been designed to switch high currents, power MOSFETs have been found to have many attractive features, some of which are given below:

1. MOSFETS have negative temperature coefficients, and unlike bipolar transistors, do not suffer from thermal runaway.
2. They are majority carrier devices, and as such, they do not suffer from minority storage time effects, so that they have high switching speed and cut off frequencies;
3. They require fewer processing steps and can be more densely packed than bipolar transistors.

Basically, a power MOSFET consists of a large number of small individual MOSFETs, known as cells, all connected in parallel. The electrical contacts through which current flows into and out of each cell are paralleled via highly conductive metals; the cell gates or controlling elements, are interconnected with polysilicon films which are four orders of magnitude less conductive than the metal. This multitransistor structure can switch high currents.

Although the power MOSFET has many attractive features, recent studies {1} have shown that its performance still needs improvement. For example, the overall device behaves like a transmission line and suffers from gate voltage propagation delay. Preliminary studies {1} have indicated that, because of gate propagation delay, cells near the input gate electrode experience a much higher than normal current density during a turn-on drive, whereas remote cells are over driven during a turn-off.

The need to ensure that the power MOSFET is a reliable switch and is compatible with the present technology has motivated this work. Chapter II outlines the basic structure and operation of the device, and describes how the input signal propagates down the gate interconnects. Chapter III presents the design modifications and their justifications. Finally, simulation measurements and their

comparisons of the experimental results with the predictions are described in chapter IV.

CHAPTER II

THEORY

2.1 Basic structure of a vertical power MOSFET

A brief discussion of the vertical power MOSFET is included here by way of introduction and for completeness; detailed information on this and other types of power MOSFET can be found elsewhere (see for example Ref.{2}).

At present, the high density power MOSFET contains between one and two million paralleled cells per square inch; this multitransistor, shown in figure 2.1, is capable of switching very high currents. Structurally, each cell is made up of a source and body, and all the cells have a common drain. The drain consists of a heavily-doped n+, and lightly-doped n, layers. The n+ layer is highly conductive and assures an ohmic contact on the back of the wafer. As shown in the figure, the lightly-doped n layer is implanted between the n+ and the body regions. This enables the device withstand high voltages, because most of the drain voltage falls across the high resistivity region. Also, the body is heavily p-type doped away from, and lightly p-type doped near, the oxide layer, to ensure that, when population

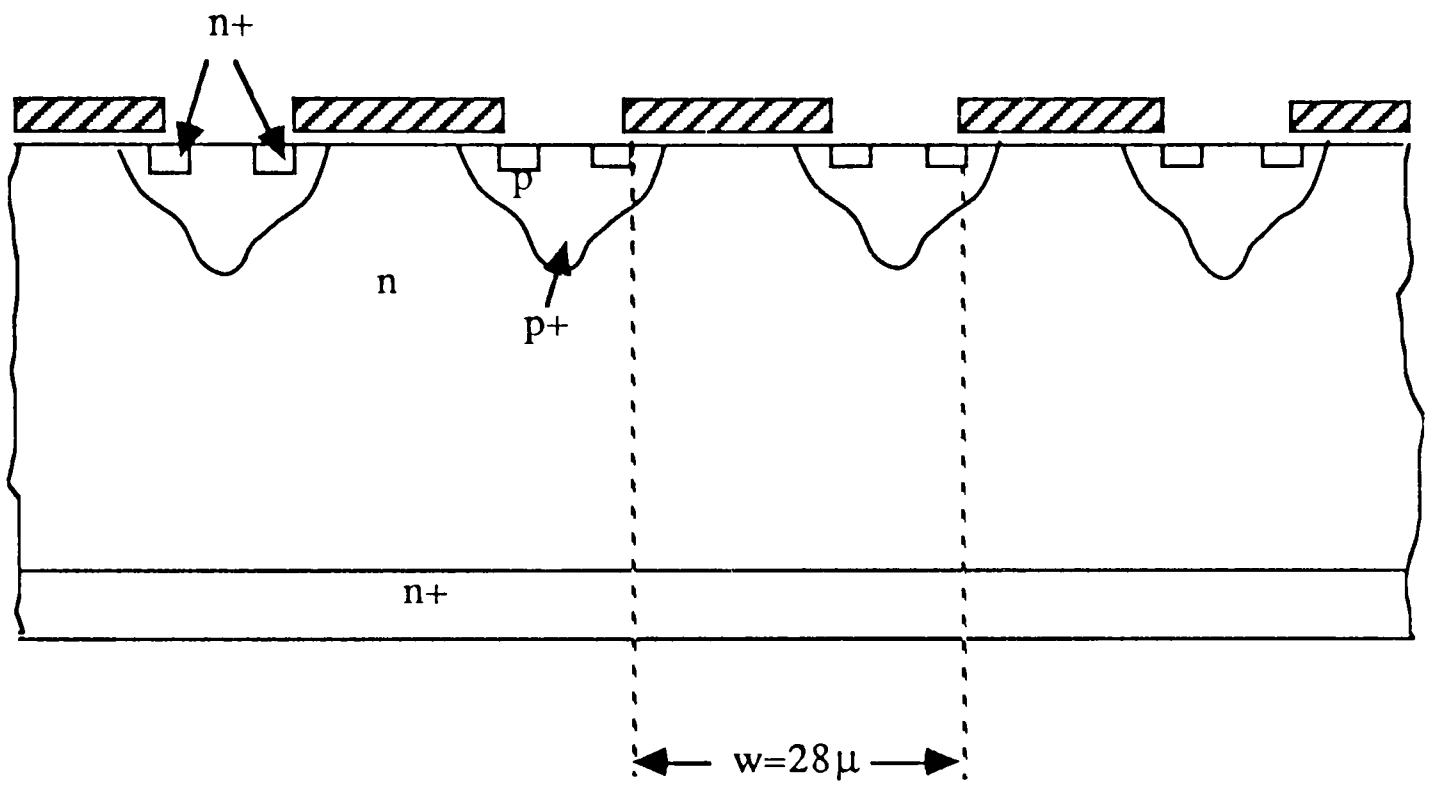


Figure 2.1. Side view of a vertical power MOSFET (VDMOS). W is the width of a unit cell

inversion takes place, the channel is always created near the interconnect. In the absence of the p+ region, as the source to drain voltage increases, the reverse biased diode of the body-drain junction can break down, and the device latches back.

As in other types of power MOSFET, the source, body, and drain of the vertical structure form a parasitic npn bipolar transistor; this transistor becomes active when the source-body junction is forward biased. When this happens, the power FET can undergo second breakdown. To inhibit turn-on, the emitter injection efficiency of the parasitic transistor is reduced by short circuiting the emitter (the source) and the base (the body) with a source metal. This technique is considered adequate at frequencies below 15 MHz; however, at higher frequencies the problem of the parasitic transistor still remains unresolved {2}.

Other problems associated with operation of this device, such as its high on-resistance and capacitance, have attracted attention in recent years, and considerable progress has been reported in the literature. For instance, in the design of the best geometry and arrangement of the cells to achieve the minimum on-resistance, two major divisions have emerged, namely, the cellular and linear geometries (figure 2.2). All cellular cells (e.g.,

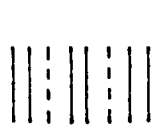
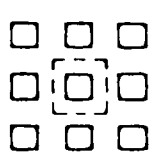
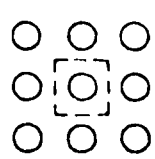
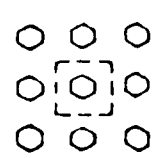
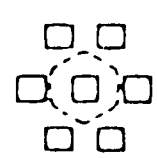
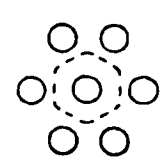
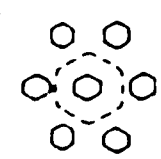
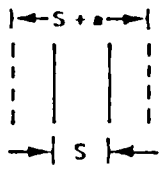
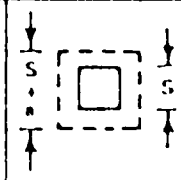
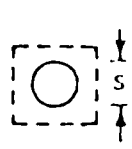
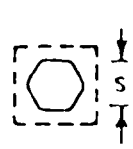
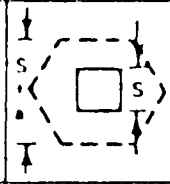
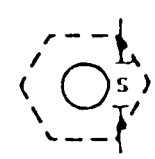
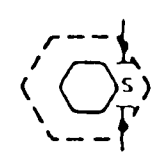
	LINEAR GEOMETRY	SQUARE ON SQUARE GRID	CIRCLE ON SQUARE GRID	HEXAGON ON SQUARE GRID	SQUARE ON HEXAGONAL GRID	CIRCLE ON HEXAGONAL GRID	HEXAGON ON HEXAGONAL GRID
SOURCE GEOMETRY AND GRID							
UNIT CELL							
COEFFICIENT G FOR CELLULAR GEOMETRIES	NOT APPLICABLE	1.0	0.8862	0.9306	1.0746	0.9523	1.0

Figure 2.2. Various power MOSFET surface geometries.

circular, hexagonal and rectanguar) provide equal and lower on-resistance than the linear geometry, assuming that the ratio of the neck area to the whole cell area is the same {2}, {3}.

Because the cells form a two-dimensional array of capacitors and resistors, corresponding to the gates and interconnects, respectively, a gate turn-on signal requires time to propagate through the array. This means that nearer cells will turn on while remote cells still remain off, so that excessive current densities occur, and propagation delays slow down switching action. This work was performed to improve understanding of the propagation effects, and to try to determine methods for enhancing turn-on.

2.2 Distributed Parameters

The high density of cells in the device permits a distributed treatment of the voltage, so as to avoid the intractable number of individual equations which would be required in a lumped parameter analysis. Then signal propagation through the interconnects will be characterized by a solution of a two-dimensional diffusion equation (derived in chapter III),

$$\frac{\partial^2 V(x,y,t)}{\partial x^2} + \frac{\partial^2 V(x,y,t)}{\partial y^2} = 4rc\frac{\partial V(x,y,t)}{\partial t} \qquad 2.1$$

where r is the resistance, V(x,y,t) is the gate voltage at position (x,y) and time t, and c the capacitance per unit length of the interconnect. The resistance r is determined from the resistivity and dimensions of the polysilicon. The capacitance depends on the oxide thickness and gate layers and also on the doping concentration of the device. In particular, the capacitance is heavily influenced by the lightly-doped n-type epitaxial layer. In the calculations discussed below, a square cell has been used for simplicity, inasmuch as all cellular cells give about the same results {3}, and the choice of the type of cells will not affect the results (to a good approximation).

2.2.1 Determination of the capacitance per unit length, c

The origin and magnitude of c can be understood by considering figure 2.3.

2.2.1a Gate-to-source capacitance

C_{gs}, in figure 2.3, consists of three capacitances:

1. the polysilicon-to-n+ source capacitance, C_{gs1}. This can be modeled as a parallel plate capacitance, with the area being the amount of polysilicon overlap beyond the channel onto the n+ source. To a first

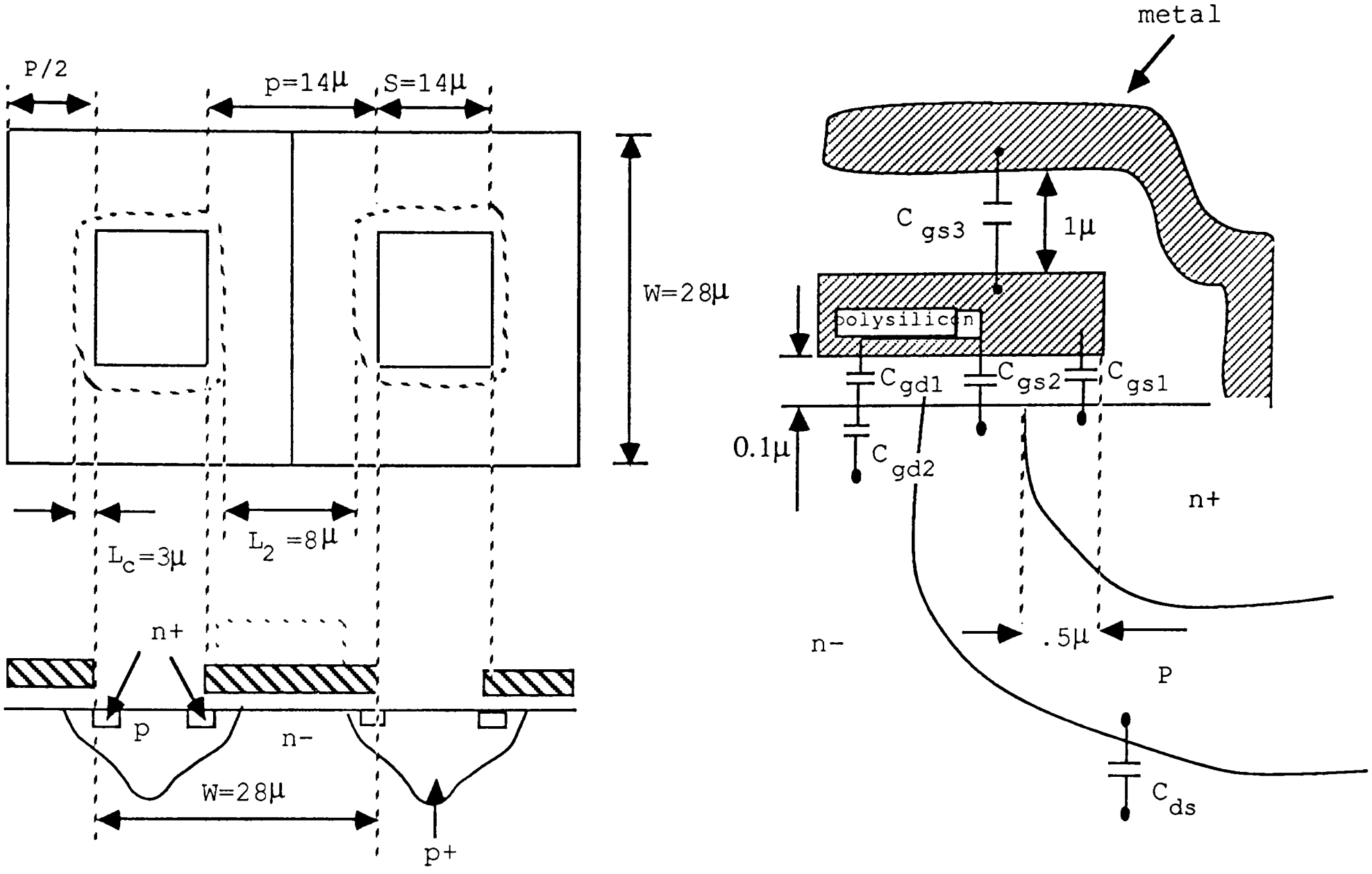


Figure 2.3. Cell structure and corresponding lumped circuit parameters. Two cells and their corresponding parameters are shown.

order approximation, this capacitance can be neglected, because it accounts for less than ten percent of the total capacitance;

2. the Polysilicon-to-channel capacitance, C_{gs2}. This depends on the mode of operation of the channel itself (inversion or depletion): However, the dependence of this capacitance on voltage is not strong, and it may be assumed constant before initial turn-on;

3. the Polysilicon-to-metal plate capacitance. The oxide thickness is assumed to be 10^{-4}cm. This value is consistent with manufacturing specifications. The relative permitivity of the oxide, ε_{ox} is 3.8.

C_{gs} is the parallel combination of all three capacitances; hence

$$C_{gs} = C_{gs1} + C_{gs2} + C_{gs3}. \qquad 2.2$$

In terms of the dimensions of the cell shown in figure 2.3, C_{gs} can be expressed as

$$C_{gs} = \frac{(S+2\times 0.5)^2 - S^2}{t_{ox}}\varepsilon_{ox} + \frac{(S+2Lc)^2 - S^2}{t_{ox}}\varepsilon_{ox}\,\frac{P^2}{T_{ox}}\varepsilon_{ox}. \qquad 2.3$$

Where t_{ox} is oxide thickness, and T_{ox} is metal-to-polysilicon spacing.

2.2.1b Source-to-drain capacitance

This capacitance consists of the parasitic junction diode capacitance. It has a 3rd root power dependence on the drain to source potential if a linearly graded junction is assumed {2}. Because of this weak dependence, it can be taken as constant with voltage to first order.

2.2.1c Gate-to-drain capacitance

The gate-to-drain capacitance, in figure 2.3, consists of the series combination of two capacitances;

1. the first one, C_{gd1}, is the parallel plate capacitance between the polysilicon and n-type epitaxial layer across the gate oxide (10^{-5}cm thick). The length of the plates corresponds to the n- region separating the channels;
2. the second component, C_{gd2}, is the result of accumulation or depletion of the surface of the n-type epitaxial layer under the oxide; the condition of the surface depends on the gate and drain potentials. When surface is accumulated, the capacitance increases, and when it is depleted, the capacitance decreases; the values can be orders of magnitude apart.

C_{gd} is the series combination of those two capacitances;

$$\text{hence } C_{gd} = \frac{C_{gd1}C_{gd2}}{(C_{gd1} + C_{gd2})}. \qquad 2.4$$

Where

$$C_{gd1} = \frac{W^2 - (S+2Lc)^2}{t_{ox}}\varepsilon_{OX} \qquad 2.5$$

and

$$C_{gd2} = \sqrt{(\frac{q\varepsilon_{Si}Nd}{2V})}(W^2 - (S+2Lc)^2). \qquad 2.6$$

The capacitance per unit length c, in terms of

C_{gs} and C_{gd}, is

$$C = \frac{C_{gs} + C_{gd}(1-Ar)}{W}, \qquad 2.7$$

where Ar is the amplification of the device. In these calculations, gate voltage propagation before turn-on is important, so that effects after turn-on (such as the miller effect, which increases the capacitance), may be neglected. Hence

$$C = \frac{C_{gs} + C_{gd}}{W}. \qquad 2.8$$

2.2.2 Calculation of the resistance per unit length, r

In order to calculate the resistance per unit length r, the interconnects of the device are partitioned into sections, each of which has the size of a cell. The

resistance per unit length is that of a square cell with a square hole in the center which provides access to the source. The equivalent resistance of this structure is obtained from resistors R_1, R_2, R_3, and R_4, as shown in figure 2.4. This equivalent gate resistance, R_w, of the cell is given by

$$R_w = R_1 + \frac{(R_2 R_3)}{R_2 + R_3} + R_4 \qquad 2.9$$

Because the cell is square,

$R_1 = R_4$, and $R_2 = R_3$.

Hence

$$R_W = 2R_1 + \frac{R_3}{2}. \qquad 2.10$$

And

$$r = \frac{2R_1 + \frac{R_3}{2}}{W} \qquad 2.11$$

where

$$R_1 = \frac{\rho \frac{P}{2}}{t_p W}, \text{ and } \quad R_3 = \frac{PS}{\frac{P}{2} T_P}.$$

The resistivity, ρ is 1.5 mohm-cm, and the parameters W, P, S, and t_p have the typical values shown in figure 2.3.

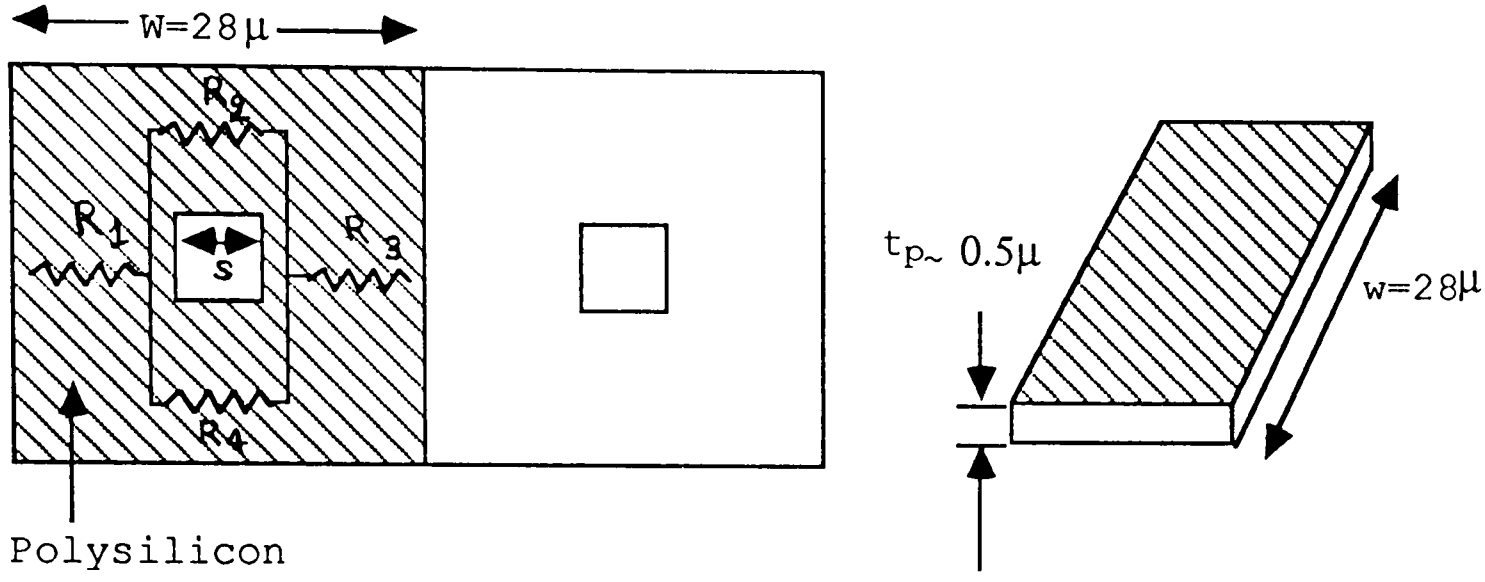


Figure 2.4. Gate resistance of a unit cell. The shaded region corresponds to the resistance.

In the case where the thickness of the interconnect is uniform, it is customary to specify the value of sheet resistance instead of the resistivity. By definition, sheet resistance is the resistivity per unit thickness; that is

$$\rho_s = \frac{\rho}{t_p} (\Omega/\square) \qquad 2.12$$

where $(\Omega/\square)$ represents the dimensions of ohms per square. In this case $\rho_s = 30\Omega/\square$

2.3 Choice of Interconnect Material

Device reliability and suppression of signal propagation delay play a major roll in selecting the interconnect material. In principle, the interconnect should not affect the overall device performance. However, physical dimensions and material properties control how the signal propagates through the interconnect. In order to reduce the adverse affects of the interconnect on device performance, it is therefore necessary that materials used as interconnect meet the following requirements:

1. low resistivity;
2. good adhesion to typical dielectrics;
3. resistance to electromigration;
4. adaptability to practical methods of deposition;
5. compatibility with bonding techniques.

Literature available on this subject {4}, confirms that the above requirements are needed to ensure the stability of the threshold voltage and satisfactory performance of the device.

In the search for materials which meet such requirements, many materials have had their properties studied. Aluminium is the most favored because it has good adhesion, low cost, and low resistivity. Other possible candidates, such as gold, copper, and silver, need an intermediate layer to enhance adhesion. In some cases, chromium, platinum, and tin-platinum have been used as buffer layers.

Nevertheless, aluminium is not suitable for devices with shallow p-n junctions because these junctions cannot withstand heat treatments above 500^{o}C which are performed after metalization. Otherwise, there would be interdiffusion of silicon and aluminium, which would result in instability of the threshold voltage.

Devices with shallow p-n junctions, among them, the power MOSFET, favor polysilicon as their interconnect. This is because polysilicon can easily be deposited by chemical vapor deposition techniques, is easily oxidized and adheres well to silicon dioxide, and, inhibits diffusions or implants from substantially degrading the gate oxide.

However, because polysilicon has a high resistivity, its use in interconnects increases the gate voltage propagation delay.

2.4 Cause of Propagation Delay

A power MOSFET is designed to handle very high currents. Because power dissipation within the device is directly propotional to the product of its on-resistance and square of the current, every effort is made to reduce its on-resistance to a minimum, to keep the device operating within safe limits. The on-resistance can be reduced by connecting the cells in parallel. The on-resistance of a single cell is

$$R_{on} = \frac{1}{\mu(C_{ox}(V_{gs} - V_t)W/L)}, \qquad 2.13$$

(where μ is electron mobility, C_{ox} is oxide capacitance, W, and L are width and length of the cells, and V_{gs}, V_t are gate and threshold voltages, respectively), then the over-all on-resistance for the N cells connected in parallel will be

$$R_{on(-N)} = \frac{1}{\mu(C_{ox}(V_{gs} - V_t)W \times N/L)} \qquad 2.14$$

$R_{on(-N)}$ is smaller than the individual R_{on} by a factor of 1/N. Accordingly, the forward voltage drop and conduction

power dissipation is reduced by the same factor. Figure 2.5 presents a typical MOSFET safe operating area (SOA) curve. The curve consists of four segments, which are maximum current (A-B); maximum power (B-C); maximum voltage (C-D); and the minimum on-resistance (E-A) of the device {2}. The device should always be operated within the SOA boundaries to avoid degradation or damage.

Although connecting cells in parallel reduces power dissipation, and increases current switching capability, this increases the input capacitance of the device. However, if square cells are used to make the device, the interconnect resistance can be controlled. In particular, its value remains constant so long as the ratio of its length to its width is unity. The interconnect resistance together with the input capacitance is responsible for gate voltage propagation delay through the interconnect; specifically, propagation delay is

$$t = RC \qquad 2.15$$

where C is the effective input capacitance, and R is the effective resistance of the interconnect.

The holes in the interconnect, which are provided to allow access to the source of each cell, will cause additional delay, probably because of reflections of the signal at the boundaries. In the following calculations,

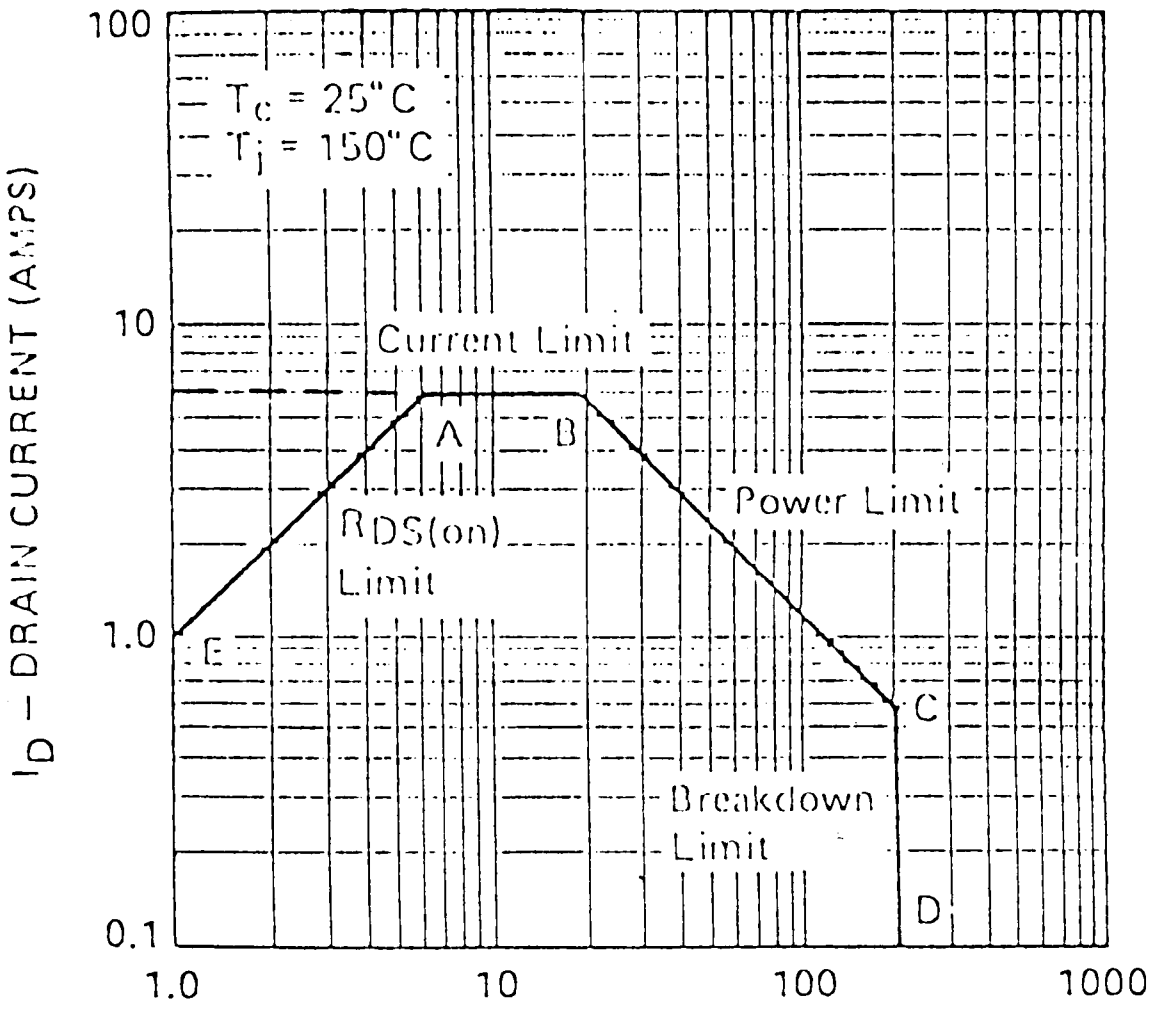


Figure 2.5. Typical MOSFET SOA curve.

the effects of the holes have been included by incorporating them into a lumped representation of the resistance, but their boundaries have not been explicitily considered. Otherwise, the solutions to the differential equations would be impracticably complex. Also the dependence of capacitance on time has been neglected. The results will then be correct to a first approximation.

CHAPTER III

BEHAVIOR OF A POWER FET AT TURN-ON

3.1 The Two-dimensional Model

When the interconnect has a uniform resistivity ρ, as it does here, a gate voltage pulse introduced at point A of figure 3.1, will propagate towards point B with circular wave front (neglecting the effect of the source access holes). Each cell will see a different time dependent gate voltage before steady-state is achieved. In particular, cells nearest point A experience the highest voltage, while those nearest point B, the lowest voltage. In order to analyze the distribution of the gate voltage through the polysilicon, it is first necessary to determine the parameters affecting the speed of propagation.

3.1.1 The diffusion equation

The equivalent circuit of a unit cell (figure 2.1) can be represented by figure 3.2, where C_{gd} is the gate-to-drain capacitance, C_{gs} is the gate-to-source capacitance, C_{ds} is the drain-to-source capacitance, R_o is the on-resistance of the cell, R is the interconnect resistance, and Y_{in} is the input admittance. The input admittance is given by

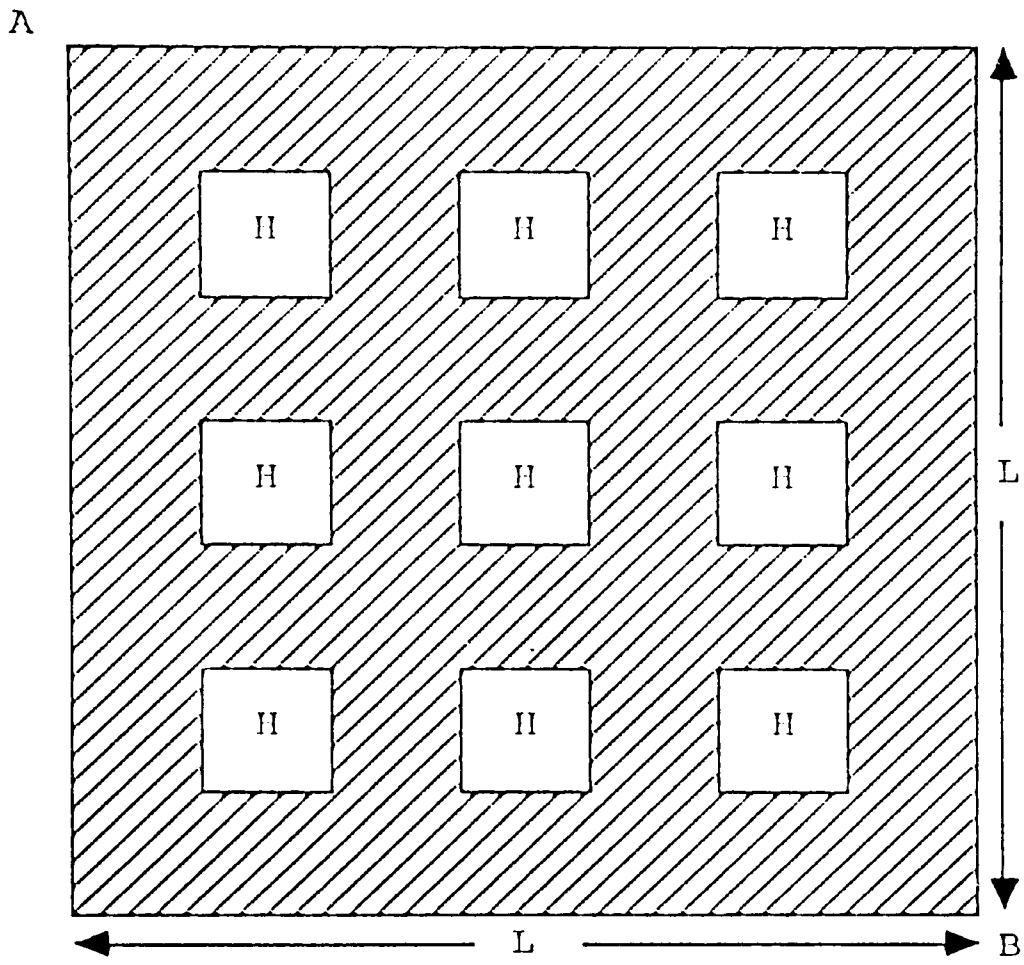


Figure 3.1. Top view of the interconnect.

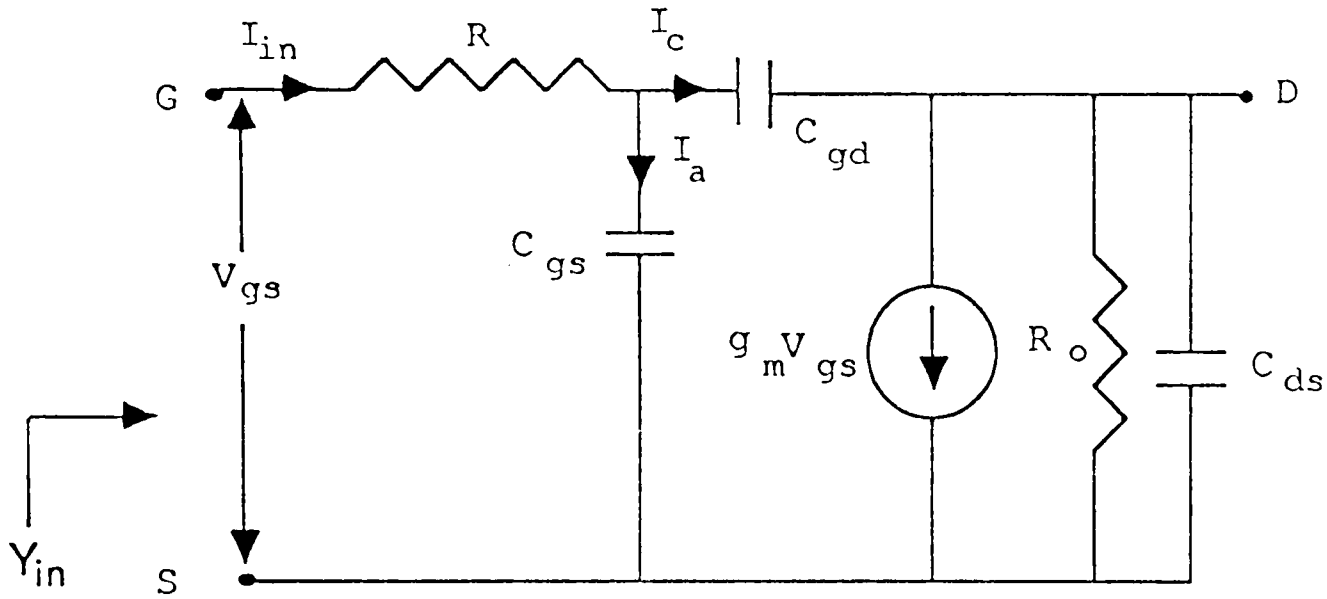


Figure 3.2. Equivalent circuit of a unit cell.

$$Y_{in} = \frac{I_{in}}{V_{gs}} = \frac{I_a + I_c}{V_{gs}} \qquad 3.1$$

$$= j\omega C_{gs} + j\omega Cgd\{1 - A_v(\omega)\},$$

where $A_v(\omega)$ is the amplification of the cell. If

$$A_v(\omega) = A_r + jA_x,$$

it can easily be shown that

$$Y_{in} = j\omega C_{gd}A_x + j\omega\{C_{gs} + C_{gd}\ (1 - A_r\ )\} \qquad 3.2$$

Before the cell starts to conduct, the amplification, $A_v(\omega)$, is zero. Consequently, equation 3.2 can be written as

$$Y_{in} = j\omega\{C_{gs} + C_{gd}\} = j\omega C_{in}. \qquad 3.3$$

The input equivalent circuit of the cell is then simply represented by the circuit in figure 3.3. The input equivalent circuit of the entire device, is obtained by combining all the cells in the closely packed device as shown in figure 3.4.

Figure 3.4a is a two-dimensional transmission line network; the details of each node are shown in figure 3.4b. The network consists of interconnected nodes, via gate resistance R, input capacitance C_1, and inherent inductance L_1, of the individual cells. The differential equations modelled by the network are

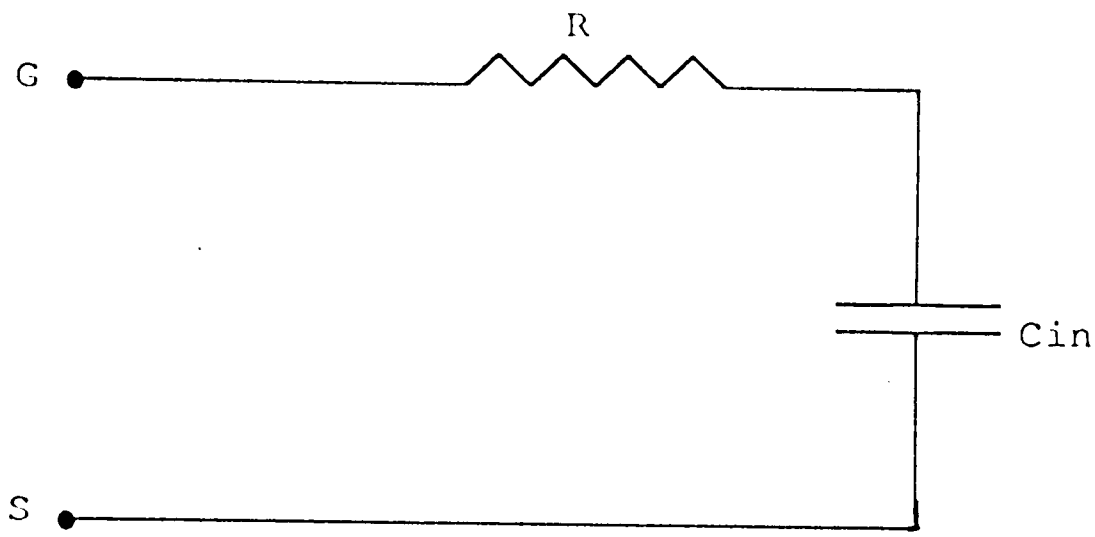


Figure 3.3. Input equivalent circuit of a unit cell.

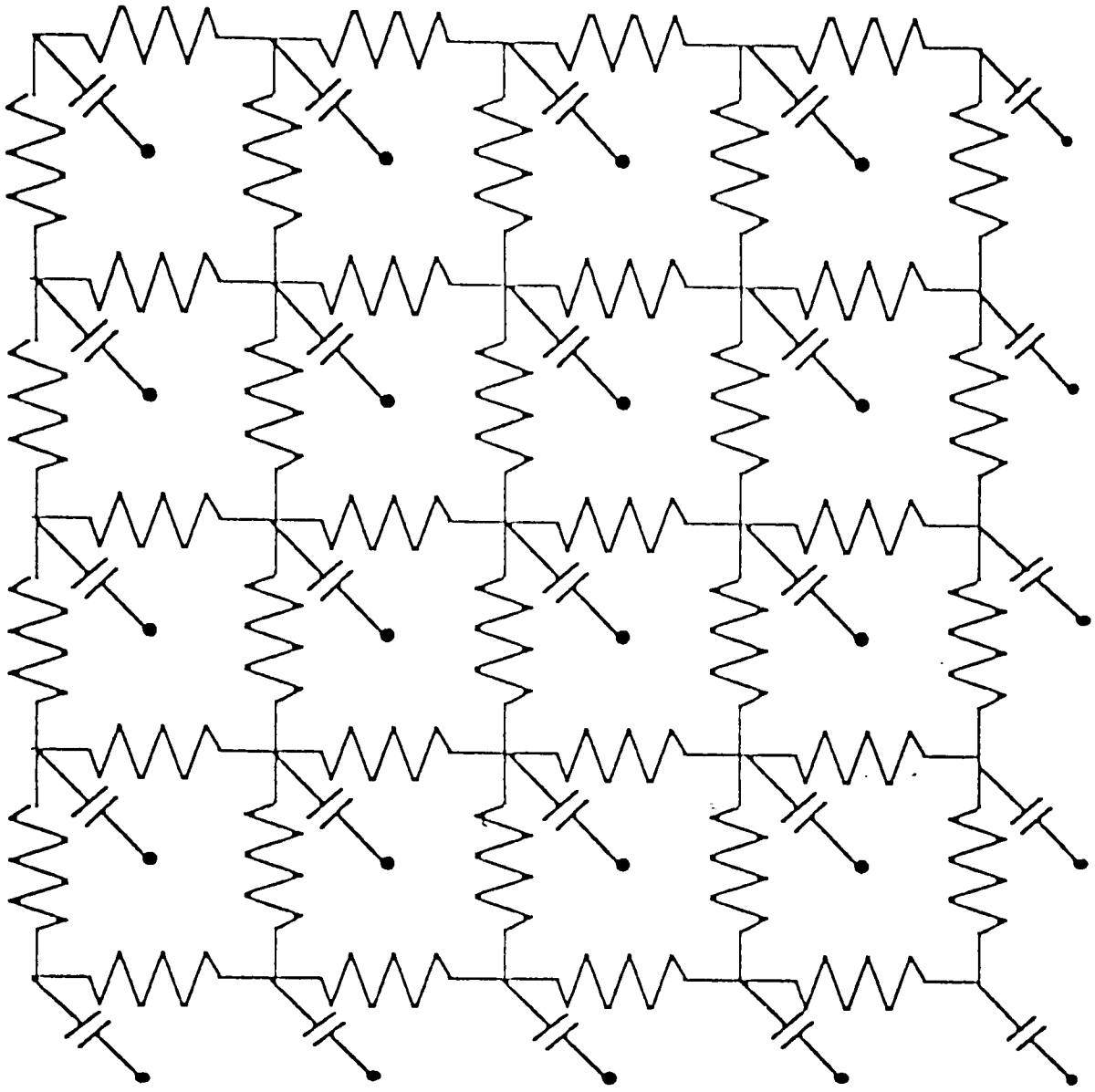


Figure 3.4a. Input equivalent circuit of the interconnect.

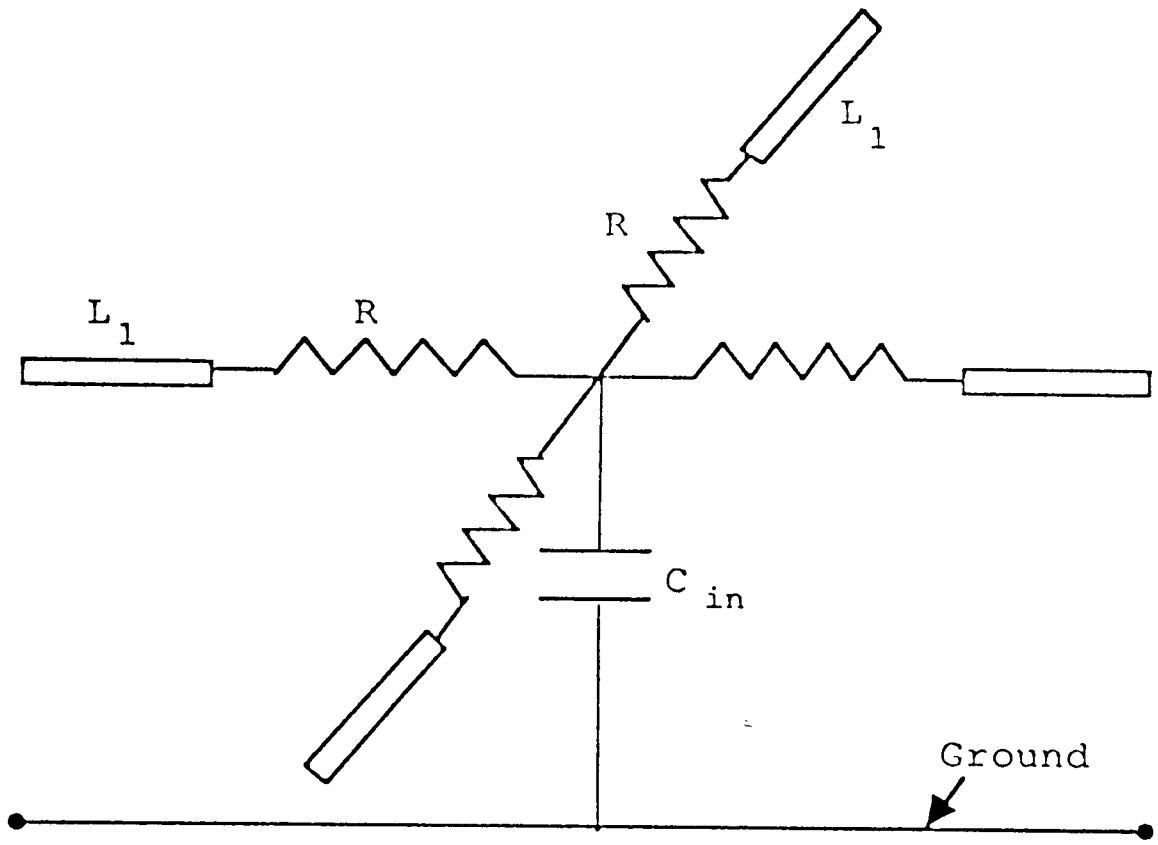


Figure 3.4b. Typical node of the interconnect.

$$\frac{\partial V}{\partial x} = -L\frac{\partial I_x}{\partial t} - 2rI_x \qquad 3.4a$$

$$\frac{\partial V}{\partial y} = -L\frac{\partial I_y}{\partial t} - 2rI_y \qquad 3.4b$$

$$\frac{\partial I_x}{\partial x} + \frac{\partial I_y}{\partial y} = -I_{xy} \qquad 3.4c$$

and

$$\frac{\partial V}{\partial t} = \frac{1}{2c\Delta l} I_{xy}. \qquad 3.4d$$

Where

$r = \frac{R}{\Delta l}$, $L = \frac{L_1}{\Delta l}$, $c = \frac{C_1}{\Delta l}$, and V is gate-to-source voltage. I_x, and I_y represent the diffusion fluxes in the x and y directions respectively. I_{xy} represents the current in the distributed capacitance, c per unit length which is assumed to be lumped at the node. Equations 3.4 can be combined to obtain

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 4rc\frac{\partial V}{\partial t} + 2Lc\frac{\partial^2 V}{\partial t^2}. \qquad 3.5$$

In semiconductor materials, inherent inductance, compared to their gate resistance, is neglegible {5}. Equations 3.5 can then be simplified such that

$$\frac{\partial^2 V}{\partial x^2} + \frac{\partial^2 V}{\partial y^2} = 4rc\frac{\partial V}{\partial t}. \qquad 3.6$$

Equation 3.6 is a diffusion equation, and its solution provides the propagation characteristics of the voltage wave.

3.1.2 Solution to the diffusion equation

Equation 3.6 can be rewritten as

$$\nabla^2 V(x,y,t) = 4rc\frac{\partial V}{\partial t}. \qquad 3.7$$

The voltage may be expressed as the sum of a steady-state and a time-dependent solution, that is

$$V(x,y,t) = M(x,y) + U(x,y,t), \qquad 3.8$$

where M is the steady-state, and U is the transient solution. Substituting Equation 3.8 into Equation 3.7,

$$\nabla^2 M(x,y) + \nabla^2 U(x,y,t) = 4rc\frac{\partial U(x,y,t)}{\partial t}. \qquad 3.9$$

The input voltage is a step of magnitude V_o, so that

$$M(x,y) + U(x,y,0) = 0 \qquad 3.10$$

and

$$M(0,0) + U(0,0,t) = V_o. \qquad 3.11$$

Because the edges of the interconnect are metal stripped, the electric fields are set to zero at the device boundaries.

$$\nabla_x M(L,y) + \nabla_x U(L,y,t) = 0 \qquad 3.12a$$

$$\nabla_y M(x,y) + \nabla_y U(x,L,t) = 0, \qquad 3.12b$$

where L is one side of the device. When the voltage in the interconnect reaches steady-state, the transient solution, U(x,y,t), and its derivative must vanish. Thus Equation 3.9 reduces to

$$\nabla^2 M(x,y) = 0, \qquad 3.13$$

with the boundary conditions

$$M(0,0) = V_o \qquad 3.14a$$

and

$$\nabla_x M(L,y) = 0; \quad \nabla_y M(x,L) = 0. \qquad 3.14b$$

For a uniformly distributed array, an input signal introduced at a corner gate will propagate as a circular wave, that is the wavefront will be a function of radius only. Equation 3.13 can be written as

$$\frac{\partial^2 M(x,y)}{\partial x^2} + \frac{\partial^2 M(x,y)}{\partial y^2} = 0; \qquad 3.15$$

letting $R = \sqrt{(x^2 + y^2)}$, Equation 3.15 can be written

$$\frac{d^2 M}{dR^2} + \frac{1}{R}\frac{dM}{dR} = 0, \qquad 3.16$$

and rewritten as

$$\frac{d}{dR}\left(R\frac{dM}{dR}\right) = 0.$$

Solving for M,

$$\frac{dM}{dR} = \frac{C_2}{R}, \text{ or } M = C_2 \ln R + C_1. \qquad 3.17$$

Finally,

$$M(x,y) = C_2 \ln\sqrt{x^2 + y^2} + C_1. \qquad 3.18$$

To evaluate Equation 3.18, the conditions given in Equations 3.14a and 3.14b are employed. The first condition determines the constant C_1. The second condition sets C_2 equal to zero. Hence the solution to Equation 3.13 is

$$M(x,y) = V_o \qquad \text{(steady-state solution)}. \qquad 3.19$$

It follows from Equation 3.9, and 3.10 that

$$\nabla^2 U(x,y,t) = 4rc\frac{\partial U(x,y,t)}{\partial t}, \qquad 3.20$$

with boundary conditions

$$\nabla_x U(L,y,t) = 0, \qquad \nabla_y U(x,L,t) = 0. \qquad 3.21$$

Initial condition

$$U(x,y,0) = -V_o, \qquad 3.22$$

because the sum of the initial conditions for steady-state and transient-state must add up to zero. Since Eq. (3.20) has homogeneous boundary conditions, the solution can be obtained by using separation of variables, so that

$$U(x,y,t) = \sum_{m=odd}^{\infty} C_m e^{\frac{-(m^2 \pi^2 t)}{32rcL^2}} \mathrm{Sin}\left(m\Pi\frac{\sqrt{(x^2 + y^2)/2}}{2L}\right). \qquad 3.23$$

The coefficients C_m are obtained by integrating Equation 3.15 over the limits of the polysilicon. However, since the

gate voltage within the holes is zero, the total integral must be reduced by the contribution due to those holes which are distributed uniformly throughout the entire interconnect. In that case, the C_m, can be expressed as

$$C_m = -\frac{4V_o}{\pi m}, \qquad 3.24$$

so that

$$U(x,y,t) = \sum_{m=odd}^{\infty} -\frac{4V_o}{\Pi m} e^{\frac{-(m^2 \Pi^2 t)}{32rcL^2}} \mathrm{Sin}\left(m\Pi \frac{\sqrt{(x^2 + y^2)/2}}{2L}\right). \qquad 3.25$$

But

$$V(x,y,t) = M(x,y) + U(x,y,t), \qquad 3.26$$

so that, the complete solution to Equation 3.7 is

$$V(x,y,t) = V_o\left(1 - \frac{4}{\pi} \sum_{m=odd}^{\infty} \frac{1}{m} \mathrm{Sin}\left(m\Pi \frac{\sqrt{(x^2+y^2)/2}}{2L}\right) e^{\frac{-(m^2 \Pi^2 t)}{32rcL^2}}\right). \qquad 3.27$$

The right-hand side of Equation 3.27 contains the steady-state and transient solutions, respectively, of the diffusion equation, subject to the boundary conditions.

3.2 Determination of the Threshold Voltage

Before a Power MOSFET can turn on, its gate voltage must reach a minimum voltage, its threshold value. The gate electric field induces charge into the conducting channel, so that current can flow. Figure 3.5 shows the

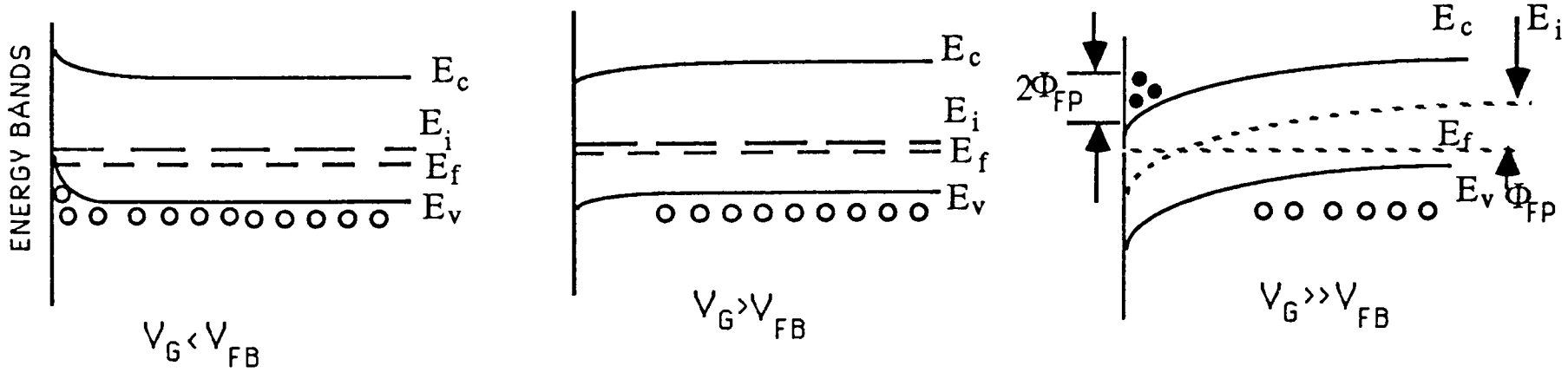


Figure 3.5. Energy bands at the oxide/semiconductor interface as the gate voltage increases.

energy bands at the oxide/semiconductor interface as the gate voltage increases. The gate voltage V_g, can be expressed as {6}

$$V_g = V_{fb} + \Phi_s - \Phi_B/C_{ox}, \quad 3.28$$

where

$$C_{ox} = \varepsilon_{siO_2}/t_{ox} \quad 3.29$$

is oxide capacitance,

Φ_s is the surface potential, and

$$V_{fb} = -0.55 + \Phi_{FP} - qN_f/C_{ox} \quad 3.30$$

is the flat band voltage. The charge Φ_B, in the channel is

$$\Phi_B = -\sqrt{2qNd\varepsilon_{si}(2|\Phi_{FP}| + V_{ds})}, \quad 3.31$$

where Nd is the substrate donor density and V_{ds} is the drain-source voltage. At the threshold voltage, the surface potential Φ_s becomes approximately twice the bulk potential, Φ_{FP}, so that Equation 3.28 can be re-written as

$$V_t=-0.55+ \Phi_{FP}-2qN_f/C_{ox}+2|\Phi_{FP}| + \sqrt{2qNd\varepsilon_{si}(2|\Phi_{FP}|+V)}/C_{ox}. \quad 3.32$$

When the gate voltage satisfies equation (3.32), the channel begins to conduct, that is, current can flow from the source across the channel to the drain when a drain-source is applied.

3.3 Application of the Model

When a voltage probe is supplied to the gate of the device, it begins to propagate through the polysilicon interconnect at a speed determined by the input capacitance and interconnect resistance. Because of gate voltage propagation delay, different parts of the interconnect will be at different voltages prior to steady-state. All the cells in a FET made using equal input capacitance values for each cell, have the same threshold voltage; as a result, cells near the gate electrode reach threshold voltage and start conducting before others more remote. However, all the cells can be made to turn on simultaneously by alteration in the process technology (see discussion in chapter IV).

Threshold voltage depends on {6}

1. the difference between the work functions of the gate and the substrate semiconductor;
2. both mobile and fixed charges in the insulator and at the semiconductor-oxide interface;
3. the doping concentrations of various layers, particularly the lightly doped drain layer.

Of these three factors, the threshold voltage is most heavily influenced by the doping concentration, Nd (Equation 3.32).

If the threshold voltage of each cell is established at

a value equal to that predicted by Equation 3.27, the cells can be made to turn on more or less simultaneously. At the present a power FET (built by Siliconix) consists of about 33124 cells; the size of each is 28μ by 28μ. Using these figures, and the resistivity and capacitance per unit length in chapter II, an algorithm and a written program, D2power, have been developed for predicting the gate voltage required at each node for simultaneous turn-on. The program and its use are described in Appendix A; the results of its application are described in chapter IV.

CHAPTER IV

RESULTS AND DISCUSSION

The continuous model developed in chapter III has been applied to obtain predicted values of the gate voltage, capacitance values, and substrate doping levels required for simultaneous turn-on of a square array of the power MOSFET. The times required for individual nodes to reach threshold voltages, using equal input capacitance values, have been calculated. Also, threshold voltage of individual nodes, using a modified technology in which the substrate doping level is varied as a function of position, have been determined. Inasmuch as the suggested modification is impractical to implement in its entirity, a reasonable procedure for varying the substrate resistivity would be to adjust the doping level in bands across the device, perhaps by ion implantation. This would not, of course, meet the requirements for simultaneous turn-on as the necessary condition would not have been fully implemented, but considerably enhanced switching speeds would be obtained.

In addition, simulation for the discrete nodel analysis, using a SPICE2 program, was obtained for comparison with the continuous model (for a manageable array

size). Finally, an experimental simulation was performed using a lumped RC network representation for the present and suggested device capacitance distributions. These calculations and measurements had a two-fold objective:

1. the time required for the first cell to reach an arbitrarily designated threshold voltage (in this case 2 volts), when a 2 volt signal was applied; and
2. distribution of the voltage throughout the network at that time.

A nine-by-nine array of resistors and capacitors was constructed on a double-sided copper-clad printed circuit board; one side was used as circuit common. In order to minimize strays, connections were made as short as laboratory conditions permitted. The arrangement of those components were illustrated in figure 3.4. The resistors formed a two-dimensional network, as seen from the circuit side of the board, and capacitors were fixed between each node and common.

4.2 Experimental measurements

The signal was introduced to the network at one of its four corners (figure 4.1); a Tektronik 7834 oscilloscope, with a 7A19 plug-in amplifier, a 7A18 time-delay unit, and a p6056 probe, were used in the measurements. A Systron-Donner 101D pulse generator provided a train of

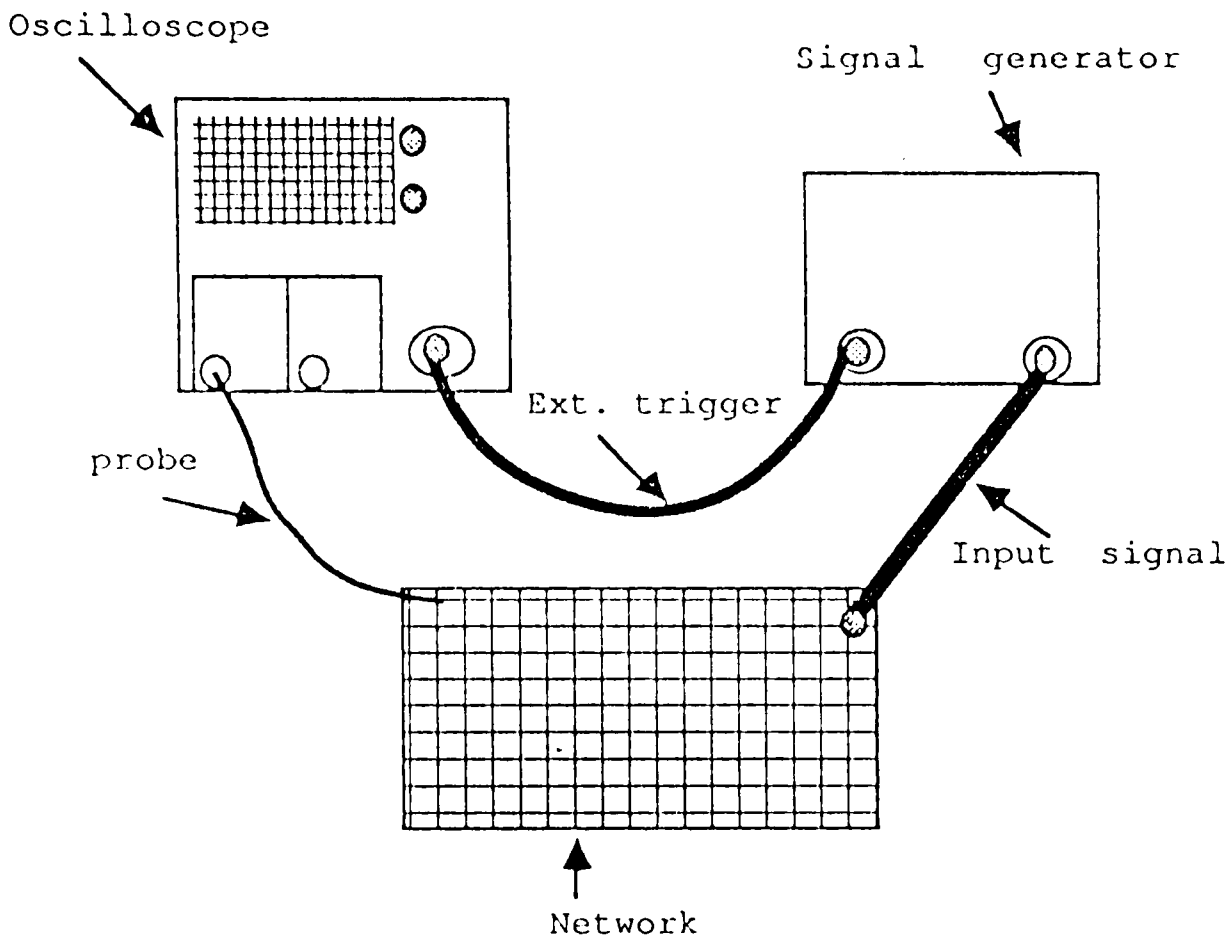


Figure 4.1. Experimental setup.

pulses, 2 volts in magnitude, with a rise time of 10 nanoseconds at a repetition rate of 10 kHz.

The threshold voltage of the first cell was chosen to be 2 volts. The voltages of interest of the other cells were specified to be their respective threshold voltages according to the proposed changes. Although the oscilloscope mainframe and amplifier were fast enough to obtain data at values of resistance and capacitance comparable to those in actual devices, it was not possible to obtain capacitors with those values. To circumvent this problem, the simulation circuits were scaled up in size by a factor of 1000. This permitted a simulation in which lumped resistance was not affected, but equivalent capacitances fell in range of practically obtainable values. As a result, the speed of propagation of the signal was slowed down.

Although a rectangular pulse was used as the circuit excitation, the capacitive load slowed down the rise-time of the signal; in the SPICE2 simulation, it was necessary that the input signal be piece-wise linearized. In general, the shape of the input signal influenced its speed through the network. The voltage measurements demonstrated a symmetrical signal spread, verifying the assumption, employed in the model, that the voltage waveform propagation is a circular front.

4.3 SPICE simulation

SPICE2 {7} is a standard circuit simulation program originally designed to analyze integrated circuits, but used for a large variety of discrete circuits. It has optional features, selected by using option cards for setting program control commands for specific simulation of DC, AC, and transient simulations. The SPICE2 program is flexible, and permits a number of calculations to be performed. The program used to calculate the nodal voltages of a nine by nine array is listed in Appendix B. The arrangement and values of the components are as described in Section 4.1.

In this work, transient voltages were to be obtained, and a transient card was used to specify computing intervals and step size. The initial simulation used a rectangular pulse with a linear rise time equal to the time required for the first node to reach 2 volts. In this case, the node voltages were found to be lower than those determined by experiment and predicted by the continuous model. When the signal fed into the network was piecewise linearized, corresponding to the actual input pulse observed experimentally, the results compared well with those obtained experimentally and predicted by the model.

4.4 Results

Samples of the results of the application of the continuous model, the SPICE2 simulation, and the

experimental measurements for a nine-by-nine array of discrete elements, are tabulated in Tables 4.1 and 4.2. Table 4.1 contains nodal voltages for a network of equal capacitances (in this case 114 pF), corresponding to present technology, PTECH. Table 4.2 is a tabulation of nodal voltages for specified bands of capacitance values, corresponding to suggested technology. Complete results of the nine-by-nine array as predicted by the continuous model for the present and modified technology are given in Appendices C and D, respectively.

The dots and the corresponding numbers, in figure 4.2, give the relative positions and the predicted gate voltages of the cells, respectively, at the time the first cell reaches 2 volts. The curves in figure 4.2 confirm that the gate signal propagates circularly down the simulated interconnect. This is a result of the array having uniformly distributed resistors and circularly distributed capacitances; the capacitance values vary from 114 pF to 112 pF, according to the prediction of the continuous model (Appendix D).

Figure 4.3 shows the voltage drops along the edge of the network (data taken from the first column) as determined by PTECH. The voltage difference is most pronounced between the first and second nodes, and continues to decrease away from the signal input point. Although the three curves are

TABLE 4.1

Sample nodal voltages, in volts, of a nine-by-nine array corresponding to the present technology (C=114 pF).

	FIRST ROW			SECOND ROW		
CELL #	MODEL	SPICE2	EXP	MODEL	SPICE2	EXP
1	2	2	2	1.907	1.913	1.911
2	1.907	1.913	1.911	1.885	1.879	1.879
3	1.863	1.862	1.863	1.845	1.847	1.837
4	1.827	1.829	1.826	1.813	1.821	1.816
5	1.801	1.806	1.800	1.791	1.802	1.795
6	1.783	1.789	1.784	1.778	1.787	1.779
7	1.773	1.777	1.779	1.770	1.774	1.774
8	1.771	1.769	1.768	1.768	1.768	1.763
9	1.769	1.766	1.763	1.766	1.764	1.761

TABLE 4.2

Sample nodal voltages, in volts, of a nine-by-nine array corresponding to the modified technology (C=114 pF to 112 pF).

	FIRST ROW			SECOND ROW		
CELL #	MODEL	SPICE2	EXP.	MODEL	SPICE2	EXP.
1	2	2	2	1.909	1.915	1.910
2	1.909	1.915	1.911	1.888	1.882	1.884
3	1.867	1.865	1.868	1.849	1.850	1.852
4	1.833	1.833	1.832	1.820	1.825	1.826
5	1.807	1.810	1.811	1.798	1.806	1.805
6	1.790	1.793	1.795	1.785	1.791	1.789
7	1.781	1.781	1.784	1.779	1.779	1.779
8	1.778	1.774	1.774	1.776	1.772	1.774
9	1.777	1.771	1.768	1.776	1.769	1.768

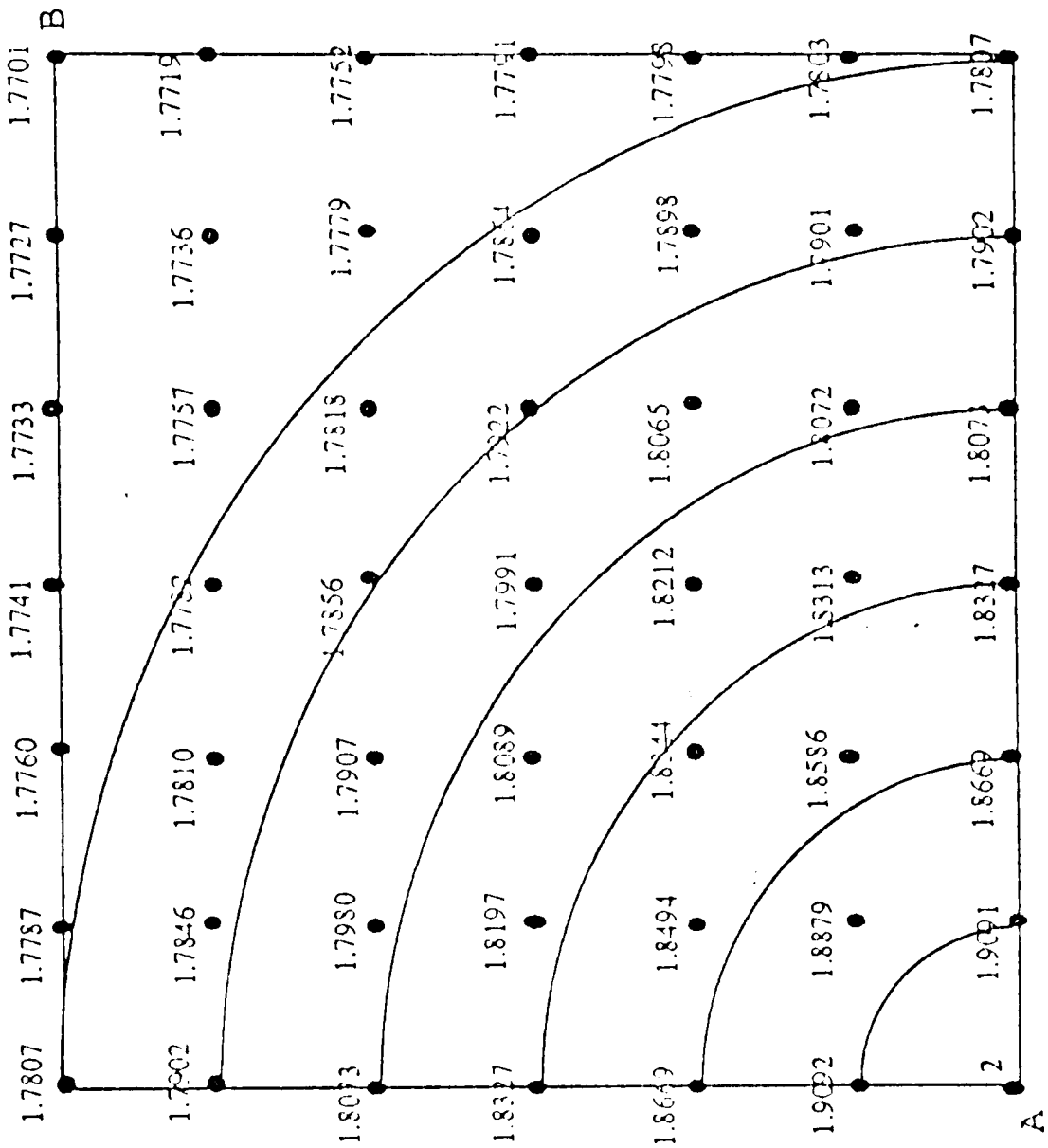


Figure 4.2. Propagation of the gate signal down the interconnect.

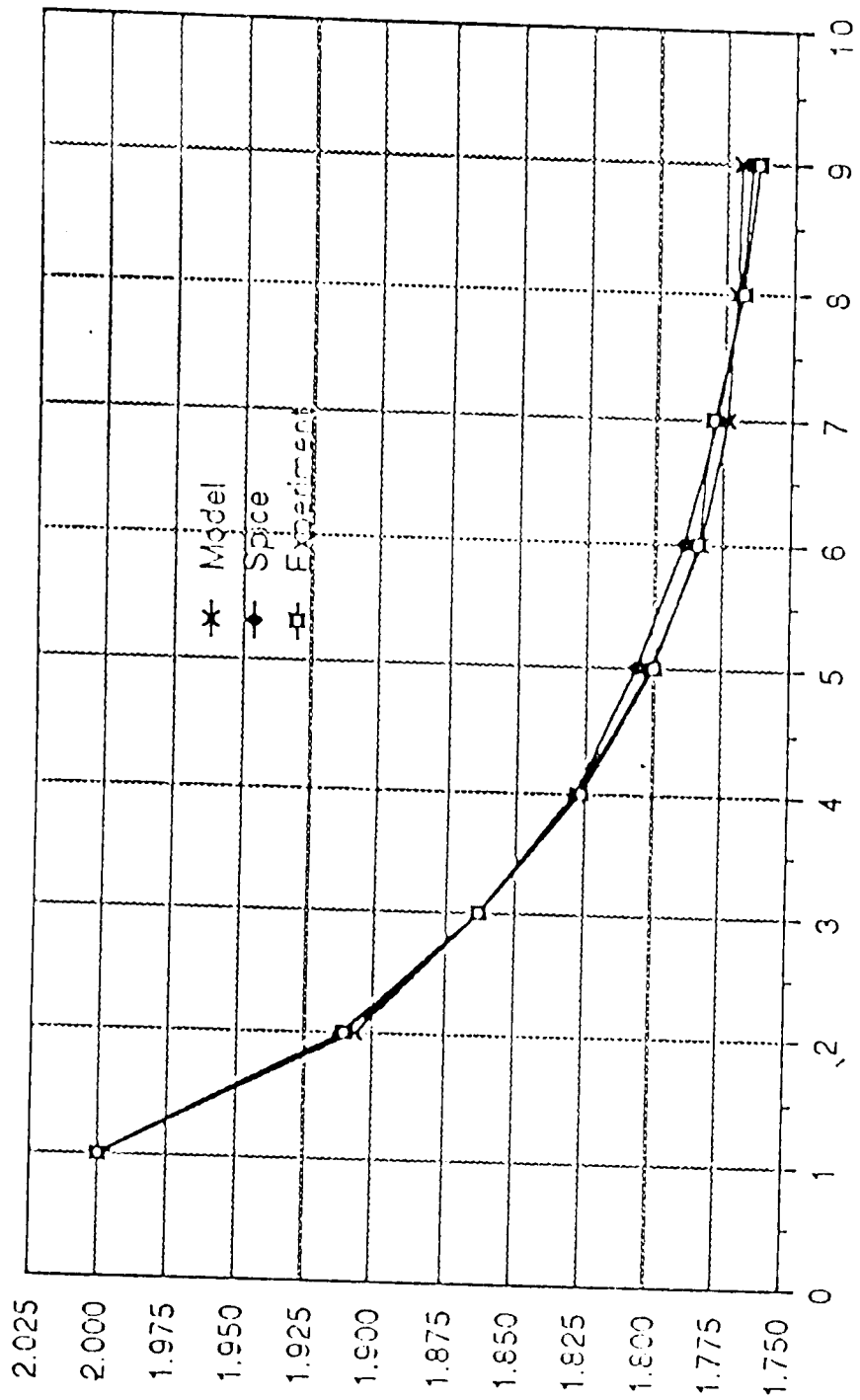


Figure 4.3. Node voltages along the edge of the network (present technology).

not exactly the same, their maximum difference at any cell is less than 0.8%.

The voltage values plotted in figure 4.4 are taken from along the edge of the network which incorporates the proposed changes. Basically the behavior of the signal is similar to that in figure 4.3. According to the proposed changes, however, the capacitance values of the network vary from 114 pF to 112 pF, as opposed to the present technology whose capacitance values are constant and equal to 114 pF. As a result, higher nodal voltages are obtained in figure 4.4 than in 4.3. Data obtained within the array by the modified technology are plotted in figure 4.5. The propagation delay within the network appears to be less pronounced than along the edges, probably because the gate signal along the edges is at the boundary, whereas an interior cell is surrounded by an array.

In general, the results are in good agreement. Variation between the data obtained from the model, the SPICE2 simulation, and the measurements is less than 1% for the entire array; which means, the model is a useful tool for predicting values of certain parameters.

Figure 4.6 shows how the voltage rises with time at arbitrarily chosen nodes of the array as predicted by the continuous model; in this case, voltages at nodes 1, 2, 3, 4, and 81 are shown. Before a steady-state is attained,

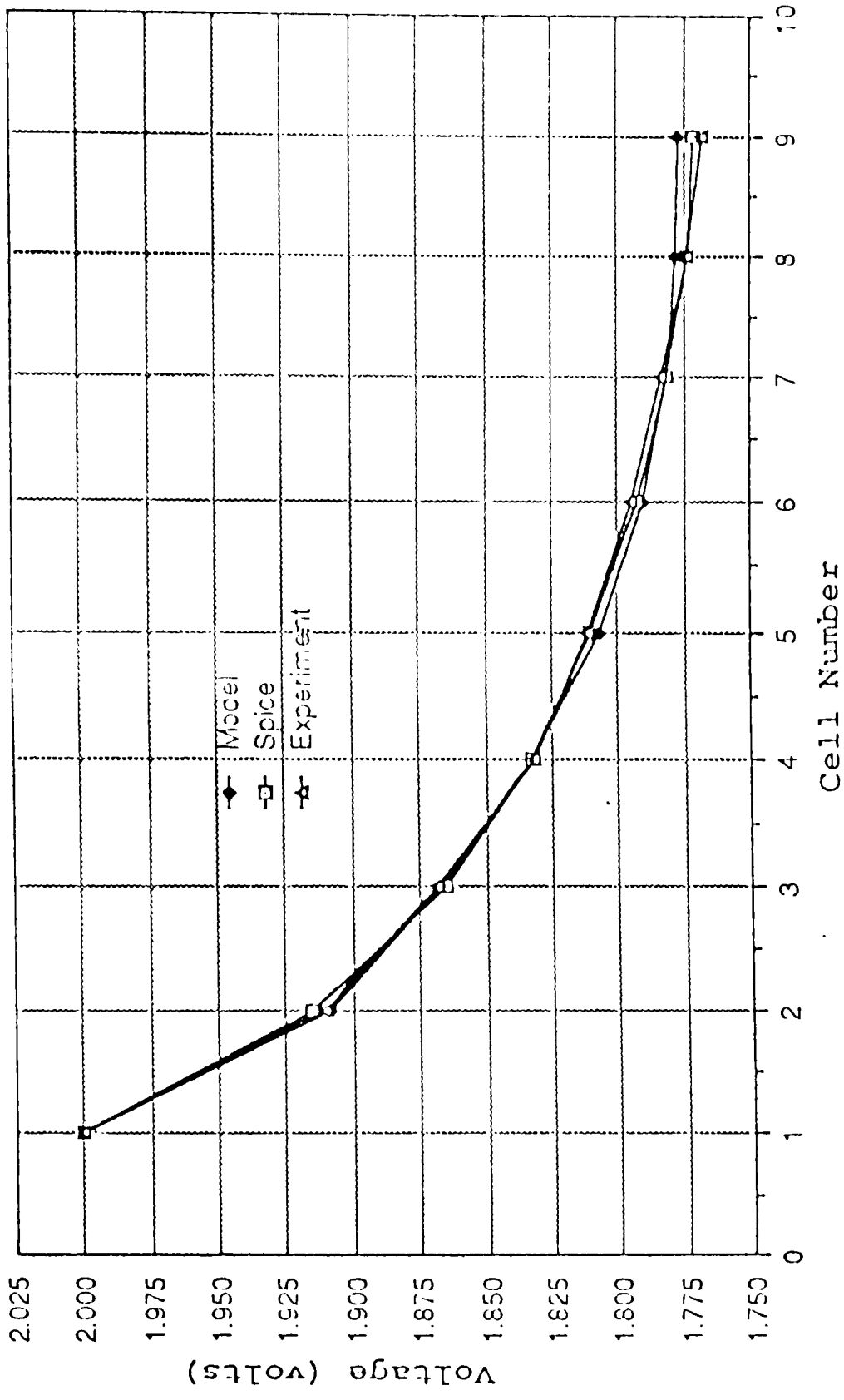


Figure 4.4. Node voltage along the edge of the array when the proposed changes are implemented.

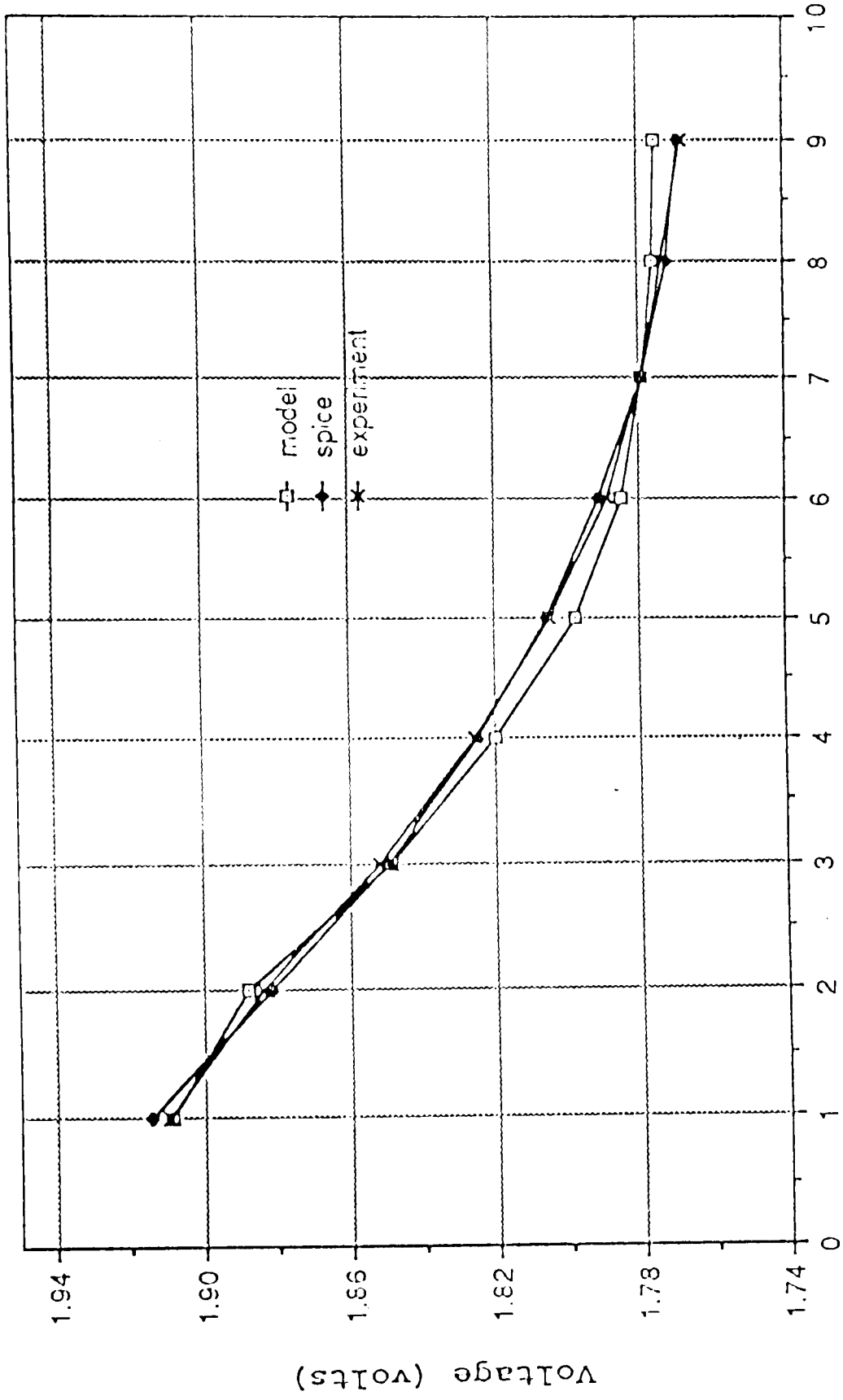


Figure 4.5. Node voltage within the array. The proposed changes are taken into account.

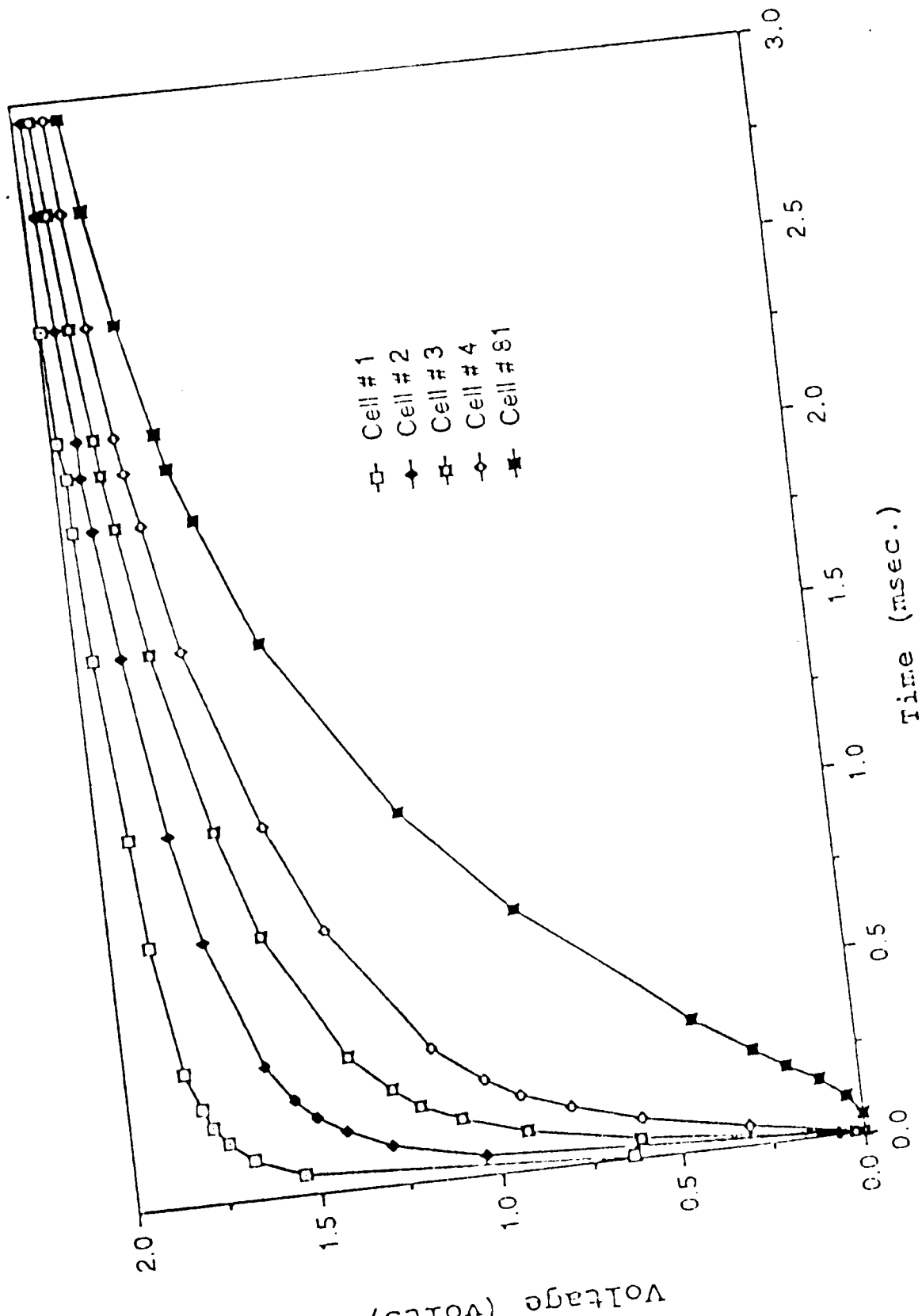


Figure 4.6. Voltage rise predicted by the model at arbitrarily chosen nodes of the array.

each node has a different gate voltage. The voltage at the first node rises fastest to reach the threshold voltage, and the voltage at the eighty-first node rises most slowly because of the distributed character of the array. When the input capacitance values of the network, EICN, are kept constant, cells near the input capacitance electrodes turn-on before those which are remote. Figures 4.7 and 4.8 show voltage rise, as determined by the SPICE2 simulation and the experimental measurements, respectively, at the same nodes as in figure 4.6 for comparison. Propagation effects appear here also, but these are not as important, inasmuch as the turn-on voltage of each cell decreases with distance.

In figure 4.9, the curve marked "pretech" gives the exact times when the nodes reach the threshold voltage (in this case 2 volts) within the EICN. The lower curves in figure 4.9 show the voltage at each node when the time the first node reaches 2 volts, according to the modified technology. If the respective threshold voltages at these nodes are set equal to those values (figure 4.9), the entire device will turn-on at the same time. In figure 4.10, the capacitances as a function of distance from the input point, A, (figure 3.1) required for these threshold voltages, is shown. The capacitive values decrease monotonically from point A to point B. In figure 4.11 the propagation of

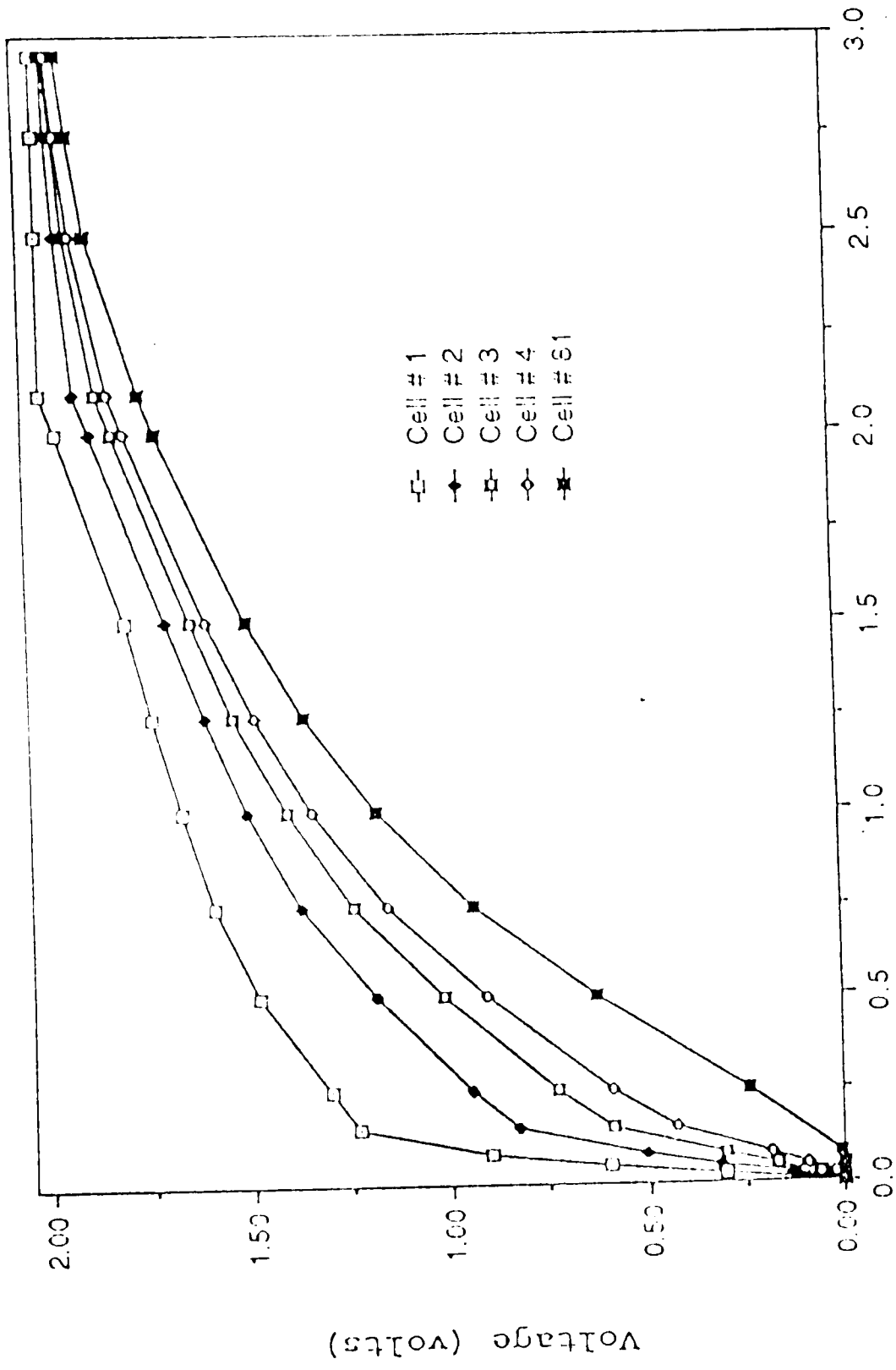


Figure 4.7. Voltage rise predicted by SPICE2 at arbitrarily chosen nodes of the network.

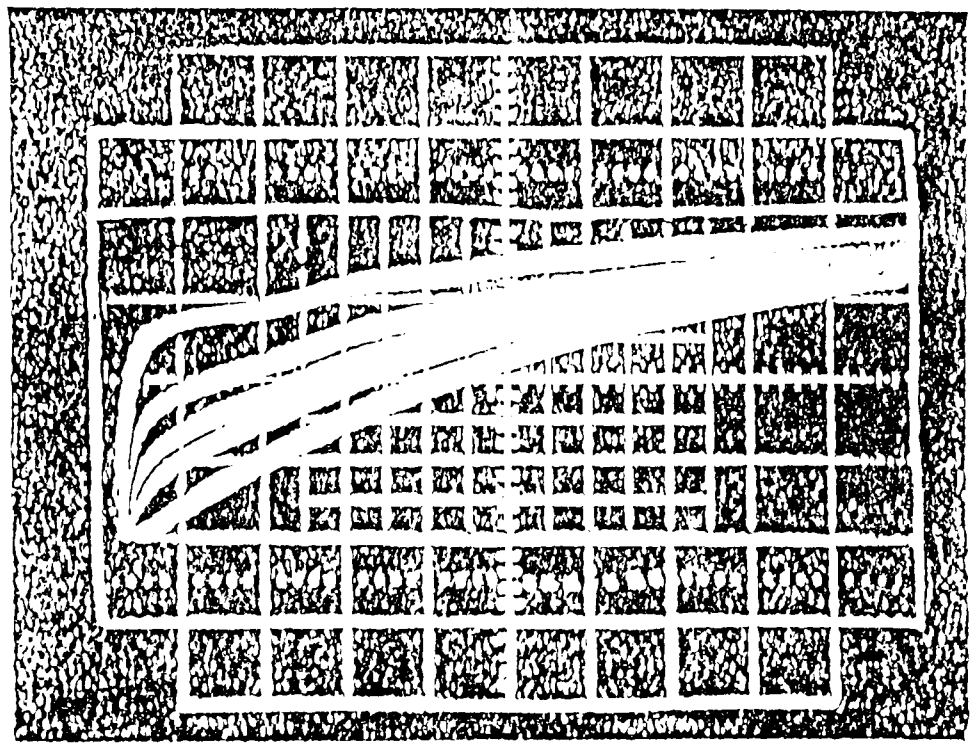


Figure 4.8. Experimentally observed voltage rise at different nodes of the array.

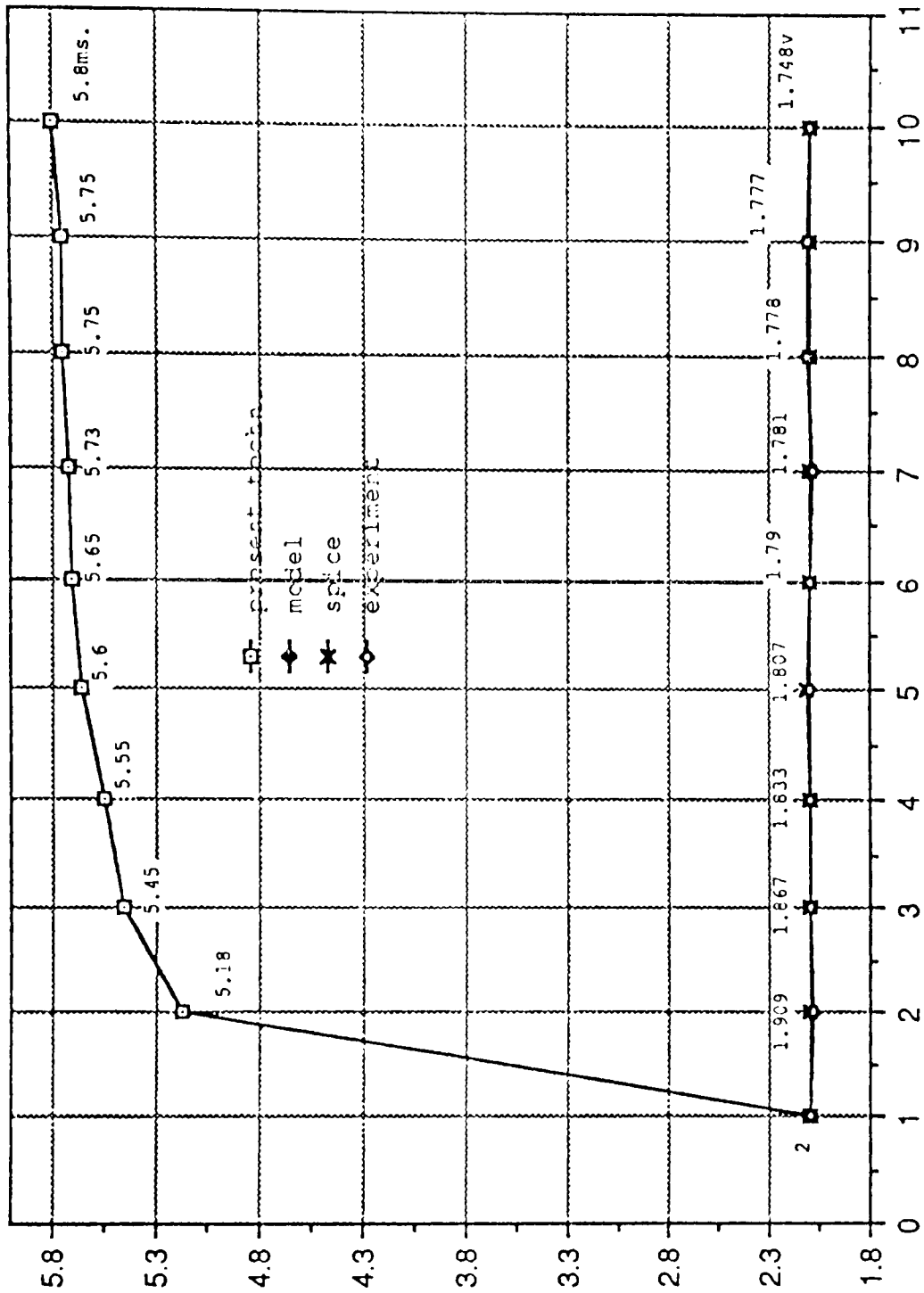


Figure 4.9. Switching times at arbitrarily chosen nodes of the array.

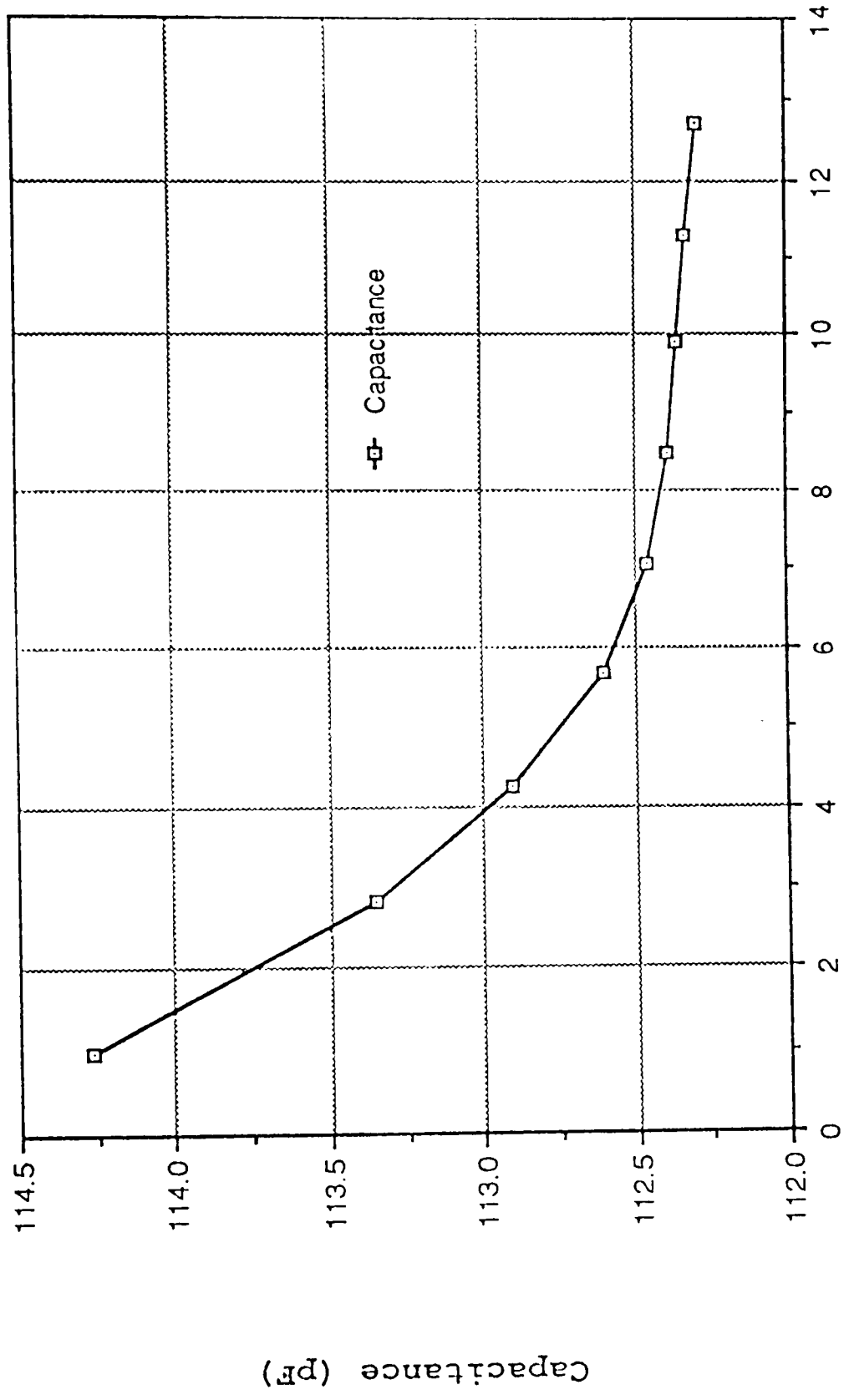


Figure 4.10. Proposed capacitance as a function of position.

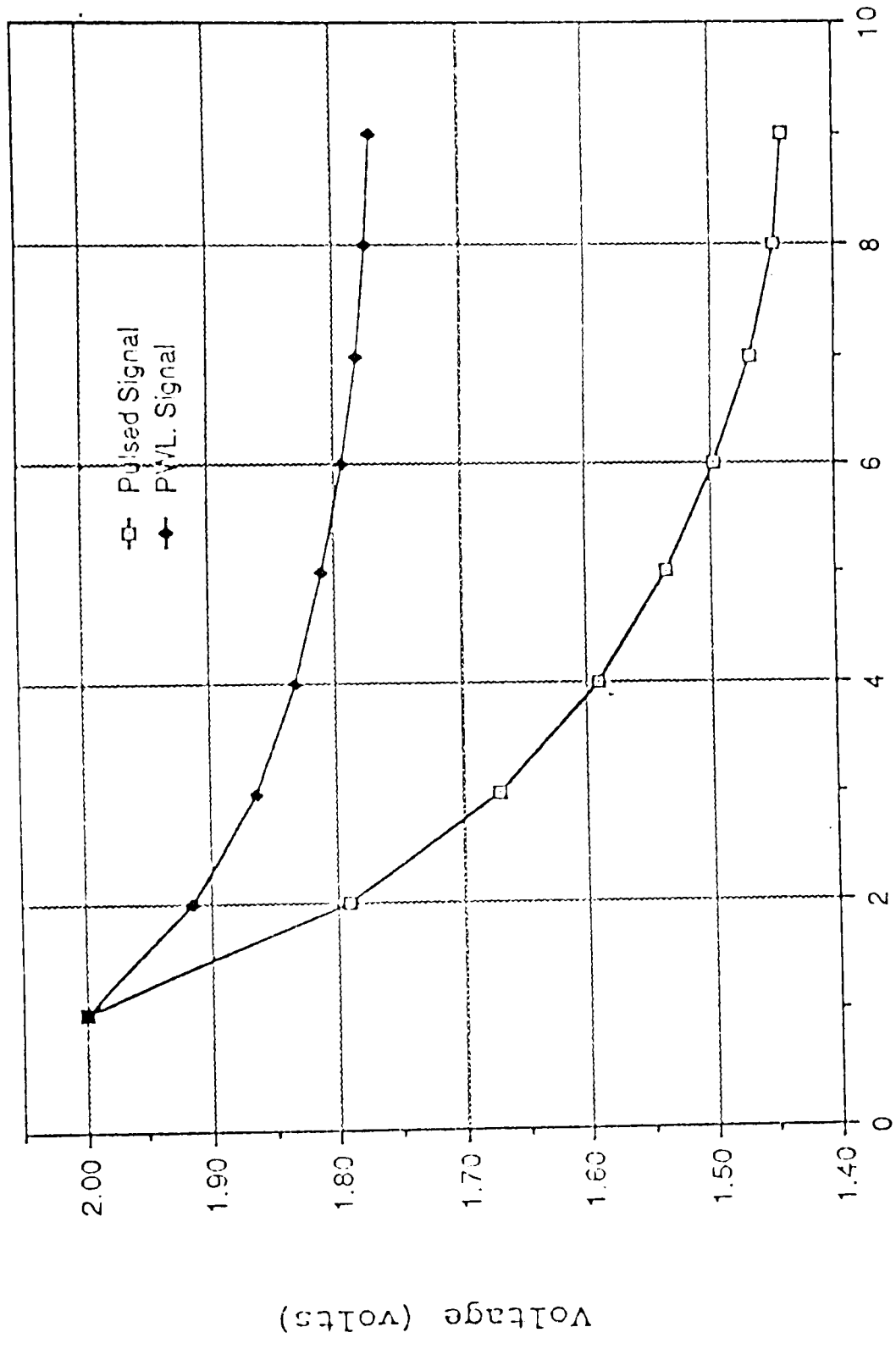


Figure 4.11. Node voltages within the proposed array for rectangular and piecewise linearized excitations.

piecewise linearized and rectangular signals across the proposed array are compared. The measured nodal voltages indicate that the piecewise linearized signal is faster than the rectangular signal.

CHAPTER V

CONCLUSIONS

The propagation of the gate voltage through the interconnect before the steady-state, has been analyzed. It has been confirmed that, as a result of the signal propagation delay during the transition period, each cell experiences a different gate voltage. According to the present technology, this causes some cells to turn-on before the others, which results in non-uniform drain current distributions and possible damage to the device. We propose that by adjusting the doping concentration of the lightly doped drain region, as demonstrated by the model, it would be possible for all the cells to reach their respective threshold voltages at the same time. The validity of the predictions of the model in the case of the voltages in the simulated device was demonstrated by comparison with the results from a SPICE2 program and experimental measurements. The results obtained in this work indicate that the developed model can be a useful tool for modifying the present power MOSFET technology to meet the requirements of enhanced turn-on.

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APPENDIX A

D2POWER PROGRAM

D2power program was developed to simulate the process of signal propagation down the interconnect. The algorithm was based on Equation 3.27, and polysilicon was invisaged as the interconnect material.

When running the program, specific questions appear on the screen which allow the following options:

1. Determination of the distribution of the voltage throughout the interconnect.
2. Examination of the voltage rise time at different points of the polysilicon.
3. Obtaining information about the doping concentration of lightly doped drain region and the corresponding threshold voltage of each cell.

Below is a complete list of the program

```
10  INPUT "GIVE THE DIMENSION OF THE ARRAY  "; CE
20  DIM R( 30, CE ) , VK( 30. CE )
30  REM IF CE=9 AND C=VARAIBLE THEN T=2100E-9, KY=.39, AND KX=.38
40  INPUT "TO ANALYSE VOLTAGE AS A FUNCTION OF TIME  type...3  "; M5
50  IF M5 <> 3 THEN 120
60  INPUT " GIVE CO-ORDINATES OF THE CELL, CO-ORDINATE...X= "; X1
70  INPUT "       CO-ORDINATE .............Y=  "; Y1
80  IF PL=0 THEN X1=.5    : IF PL=0 THEN Y1=.5
90  IF PL=0 THEN 140
100 INPUT" GIVE PRINTING TIME INTERVALS OF Vk VALUES....t= "; ST
110 INPUT " STARTING FROM TIME ....t= "; TI       : GOTO 280
120 INPUT "NUMBER OF COLUMNS TO BE PRINTED ARE ..... "; X1
130 INPUT "NUMBER OF CELLS IN A COLUMN TO BE PRINTED ARE..."; Y1
140 INPUT" GIVE THE COEFFECIENT OF Y...Ky= "; CY : REM CONTROLS THE ALGORITHM
150 INPUT"GIVE  THE COEFFICIENT OF X...Kx=  "; SX : REM CONTROLS THE ALGORITHM
160 REM
170 NI=1.45E+16  :  ESI=1.04E-10  : SIO = 3.45E-11
180 TOX = .0000001  :  K1=1.38E-23   : Q2 =1.602E-19 : PI=3.1415926#
190 NZ= 2.963E+22 :  T1= 300   : NF= 1.5E+15 : W=.000028
200 INPUT "GIVE switching time of cell # 1...TI= "; TI  : PRINT
210 INPUT "IF CAPACITANCE VALUE IS CONSTANT TYPE....2   "; KB
220 IF KB <> 2 THEN 250
230 INPUT" GIVE THE CAPACITANCE VALUE ...C= "; PP
240 INPUT" GIVE ANOTHER CAPACITANCE VALUE or press return...C= "; P9
250 PRINT: PRINT "PROGRAM D2POWER IS WRITTEN TO CALCULATE THE"
260 PRINT "VALUE OF THE THRESHOLD VOLTAGE OF EACH CELL "
270 PRINT "        FOR A  2-DIMENSIONAL MODEL        "  : PRINT
280 REM
290 KY=CY   :  KX=SX
300 FOR X=.5 TO X1
310 IF X=1.5 THEN KX=.51
320 FOR Y=.5 TO Y1
330 IF Y=.5 THEN NA= NZ
340 IF Y=1.5 THEN NZ= NA
350 V3=0        :   PM= 0
360 QF=-K1*T1*LOG( NA/NI)/Q2
370 QB=-SQR( 2*Q2*NA*ESI*( ABS( 2*QF)))
380 CX=SIO/TOX
390 QM= -.55
400 VF=QM - Q2*NF/CX
410 VT= VF + 2*ABS( QF) - QB/CX
420 REM ....... CALCULATION OF      R
430 W= .000028  : RO= .000015  : P= .000014
440 S= .000014  : TP= .0000005
450 R1= RO*P/( 2*W*TP)  : R4 = R1
460 R2= 2*RO*S/( P*TP)  : R3= R2
470 RW= R1 + R4 + R2*R3/( R2+R3)  : R= RW/W
480 REM  ...CALCULATION OF CAPACITANCE   C
490 LC= .000003  : TX= .000001
500 COX= 3.3645E-11  : PI=3.1415926#
510 C1= (( S+2*.0000005) ^2-S^2)*COX/TOX
520 C3= (( S + 2*LC) ^2 - S^2)*COX/TOX
530 C4= P^2*COX/TX
540 A4= ( W^2 - ( S +2*LC) ^2)
550 C5= A4*COX/TOX
560 C6= SQR( Q2*ESI*NA/( ABS( 2*QF) +50))*A4
570 C7= C5*C6/( C5+C6)
580 CIN= C1 + C3 + C4 + C7
```

```
590 C=CIN/W    : IF CE=9 AND KB <> 2 THEN  C=1000*C :  R=45/W
600 IF PM > 0 THEN  1130
610 IF KB <> 2 THEN 630
620 C=PP/W     :  R =46/W
630 R(X,Y) =R/((1+KY^Y/CE)^(1+KX^X/CE))
640 KY=1.01^KY
650 IF X=.5 THEN KY=1.01^KY
660 IF X=.5 AND Y=.5 THEN R(X,Y)=R
670 IF CE=9 AND Y > 2    AND P9<> 0 AND KB=2 THEN C=P9/W
680 TC= R(X,Y)^C          :  TS=PI^2*TI
690 IF M5 <> 3 THEN 730
700 IF X<> X1 AND Y<>Y1 THEN 730
710 FOR N=TI TO   1E+15     STEP  ST
720 TS= PI^2*N
730 TW= 32*(W*CE)^2*TC
740 MK= 0
750 FOR M= 1 TO 100000!
760 CP= PI*SQR((X^2 + Y^2)/2)
770 CJ=SIN((2*M-1)*CP/(2*CE))
780 NP= (2*M-1)^2*TS/TW     :  EX= EXP(-NP)
790 IF EX= 0 THEN  840
800 CK= CJ*EX/(2*M-1)
810 MK= MK + CK
820 NEXT M
830 REM
840 IF M5=3 AND Y=Y1 AND X=X1 THEN 1220
850 VO=2
860 VK(X,Y)= VO*(1-4*MK/PI)
870 IF Y=.5    THEN  1070
880 IF PZ=0 THEN KA=KY :IF PZ=0 THEN KR=KX      :PZ=PZ+1
890 IF VK(X,Y) > VK(X,Y-1)  AND KY >  .2  THEN KY=.97*KY
900 IF VK(X,Y) > VK(X,Y-1)  AND KY <= .22  THEN KX=.98*KX
910 IF VK(X,Y) > VK(X,Y-1)  THEN 610
920 IF X=.5 THEN 1070
930 IF VK(X,Y) > VK(X-1,Y)  AND KY > .2    THEN KY=.97*KY
940 IF VK(X,Y) > VK(X-1,Y)  AND KY <= .22  THEN KX=.98*KX
950 IF VK(X,Y) > VK(X-1,Y)    THEN  GOTO 610
960 V1=VK(X,Y-1) - VK(X,Y)     :   V2=VK(X-1,Y-1)-VK(X-1,Y)
970 IF V1 > V2      AND Y+.5= Y1 THEN KY=1.012*KY
980 IF  V1 > V2 AND KX < .23        THEN KX=1.01*KX
990  IF V1 > V2 +.0003 AND Y+.5=Y1 THEN 610
1000 IF Y+.5=Y1 THEN 1060
1010 IF VK(X,Y) < VK(X-1,Y) AND Y+.5=Y1 THEN 1060
1020 V3=(VK(X-1,Y)+VK(X-1,Y+1))/2
1030 IF VK(X,Y) > V3  AND KY > .18  THEN KY=.97*KY
1040 IF VK(X,Y) > V3  AND KY < .22 THEN KX=.98*KX
1050 IF VK(X,Y) > V3 AND KX > .18 THEN GOTO 610
1060 KN=KY     :  KY=KA    :  KX=KR  :  PZ=0
1070 IF X= .5 AND Y= .5  THEN VK(X,Y)= VO
1080 IF X <> .5 AND Y=.5  THEN VK(X,Y)= VK(Y,X)
1090 PRINT
1100 PM= PM +1
1110 IF KB= 2 AND M5<>3  THEN 1350
1120 IF M5=3    THEN 1360
1130 IF VK(X,Y)> VT THEN NA=NA+6E+17
1140 IF VK(X,Y)>VT THEN 1180
1150 IF ABS(VT - VK(X,Y)) < = .00008 THEN 1190
1160 IF ABS(VT - VK(X,Y)) > .001     THEN NA= NA - 2E+19
```

```
1170 IF ABS(VT - VK(X,Y)) < .001     THEN NA= NA - 7E+17
1180 GOTO 360
1190 N1= NA*.000001   :CA= C*W     :TT= TOX*100!
1200 PRINT"Vk("X+.5","; Y+.5")="; VK(X,Y)"; VL="; VT";  Na="; N1" ; C="; CA
1210 IF Y <> .5 THEN NA = NA - 6E+17
1220 IF KB <> 2 THEN 1360
1230 VO= 2
1240 VK(X,Y) = VO*(1-4*MK/PI)
1250 IF X=.5 AND Y=.5 AND PL=0 THEN VP=VO - VK(X,Y)
1260 IF  X=.5 AND Y=.5 AND PL=0 THEN VK(X,Y)= VO
1270 PRINT: PRINT"VK("; X+.5","; Y+.5")="; VK(X,Y)";  T="; N";  C="; C*W
1280 PL= PL +1
1290 IF VK(X,Y) + VP>= 1.99999 OR VK(X,Y)=2 THEN 1310
1300 NEXT N
1310 PRINT: PRINT" TO PLOT ANOTHER CELL TYPE....8 "   :PRINT
1320 INPUT "     PL=...."; PL
1330 IF PL= 8 THEN  60
1340 IF PL <> 8 THEN 1400
1350 IF KB= 2 THEN PRINT "Vk("; X+.5","; Y+.5")="; VK(X,Y)";  C="; C*W"
1360 NEXT Y
1370 KY=SX     :  KX=SX
1380 PRINT:  PRINT "     X =  "; (X+1.5)
1390 NEXT X
1400 PRINT  :  PRINT"          E N D    "
1410 END
```

APPENDIX B

SPICE2 PROGRAM LISTING

```
POWR FET EQUIVALENT CIRCUIT
.WIDTH IN=72
.OPTION LIMPTS=500
 *VIN 96  0  PULSE(0 2 050NS50NS50NS 2960NS)
VIN 96 0 PWL(0 0 .1U 1.2 .6U 1.55 1.1U 1.7 1.6U 1.83 2.1U 2)
*VIN 96 0 EXP(0  2  0 2.5US  2US  2.5US)
*DC VIN 0  2  0.1
.TRAN 25NS 5900NS
RS  96   1    .00001
R1   1   2     50
R2   2   3     50
R3   3   4     50
R4   4   5     50
R5   5   6     50
R6   6   7     50
R7   7   8     50
R8   8   9     50
R9   10  11    50
R10  11  12    50
R11  12  13    50
R12  13  14    50
R13  14  15    50
R14  15  16    50
R15  16  17    50
R16  17  18    50
R17  19  20    50
R18  20  21    50
R19  21  22    50
R20  22  23    50
R21  23  24    50
R22  24  24    50
R23  25  26    50
R24  26  27    50
R25  28  29    50
R26  29  30    50
R27  30  31    50
R28  31  32    50
R29  32  33    50
R30  33  34    50
R31  34  35    50
R32  35  36    50
R33  37  38    50
R34  38  39    50
R35  39  40    50
R36  40  41    50
R37  41  42    50
R38  42  43    50
R39  43  44    50
R40  44  45    50
R41  46  47    50
R42  47  48    50
R43  48  49    50
R44  50  51    50
R45  51  52    50
R46  52  53    50
R47  53  54    50
R48  54  55    50
R49  55  56    50
R50  56  57    50
R51  57  58    50
R52  58  59    50
R53  59  60    50
R54  60  61    50
R55  61  62    50
R56  62  63    50
R57  64  65    50
```

R58	65	66	50
R59	66	67	50
R60	67	68	50
R61	68	69	50
R62	69	70	50
R63	70	71	50
R64	71	72	50
R65	73	74	50
R66	74	75	50
R67	75	76	50
R68	76	77	50
R69	77	78	50
R70	78	79	50
R71	79	80	50
R72	80	81	50
R73	1	10	50
R74	2	11	50
R75	3	12	50
R76	4	13	50
R77	5	14	50
R78	6	15	50
R79	7	16	50
R80	8	17	50
R81	9	18	50
R82	10	19	50
R83	11	20	50
R84	12	21	50
R85	13	22	50
R86	14	23	50
R87	15	24	50
R88	16	25	50
R89	17	26	50
R90	18	27	50
R91	19	28	50
R92	20	29	50
R93	21	30	50
R94	22	31	50
R95	23	32	50
R96	24	33	50
R97	25	34	50
R98	26	35	50
R99	27	36	50
R100	28	37	50
R101	29	38	50
R102	30	39	50
R103	31	40	50
R104	32	41	50
R105	33	42	50
R106	34	43	50
R107	35	44	50
R108	36	45	50
R109	37	46	50
R110	38	47	50
R111	39	48	50
R112	40	49	50
R113	41	50	50
R114	42	51	50
R115	43	52	50
R116	44	53	50
R117	45	54	50
R118	46	55	50
R119	47	56	50
R120	48	57	50
R121	49	58	50
R122	50	59	50
R123	51	60	50

```
R124  52   61     50
R125  53   62     50
R126  54   63     50
R127  55   64     50
R128  56   65     50
R129  57   66     50
R130  58   67     50
R131  59   68     50
R132  60   69     50
R133  61   70     50
R134  62   71     50
R135  63   72     50
R136  64   73     50
R167  65   74     50
R168  66   75     50
R169  67   76     50
R170  68   77     50
R171  69   78     50
R172  70   79     50
R173  71   80     50
R174  72   81     50
C1     1    0    114PF
C2     2    0    114PF
C3     3    0    113PF
C4     4    0    113PF
C5     5    0    113PF
C6     6    0    113PF
C7     7    0    112PF
C8     8    0    112PF
C9     9    0    112PF
C10   10    0    114PF
C11   11    0    113PF
C12   12    0    113PF
C13   13    0    113PF
C14   14    0    113PF
C15   15    0    112PF
C16   16    0    112PF
C17   17    0    112PF
C18   18    0    112PF
C19   19    0    113PF
C20   20    0    113PF
C21   21    0    113PF
C22   22    0    113PF
C23   23    0    113PF
C24   24    0    112PF
C25   25    0    112PF
C26   26    0    112PF
C27   27    0    112PF
C28   28    0    113PF
C29   29    0    113PF
C30   30    0    113PF
C31   31    0    113PF
C32   32    0    112PF
C33   33    0    112PF
C34   34    0    112PF
C35   35    0    112PF
C36   36    0    112PF
C37   37    0    113PF
C38   38    0    113PF
C39   39    0    113PF
C40   40    0    113PF
C41   41    0    112PF
C42   42    0    112PF
C43   43    0    112PF
C44   44    0    112PF
C45   45    0    112PF
```

```
C46   46    0    113PF
C47   47    0    113PF
C48   48    0    113PF
C49   49    0    112PF
C50   50    0    112PF
C51   51    0    112PF
C52   52    0    112PF
C53   53    0    112PF
C54   54    0    112PF
C55   55    0    112PF
C56   56    0    112PF
C57   57    0    112PF
C58   58    0    112PF
C59   59    0    112PF
C60   60    0    112PF
C61   61    0    112PF
C62   62    0    112PF
C63   63    0    112PF
C64   64    0    112PF
C65   65    0    112PF
C66   66    0    112PF
C67   67    0    112PF
C68   68    0    112PF
C69   69    0    112PF
C70   70    0    112PF
C71   71    0    112PF
C72   72    0    112PF
C73   73    0    112PF
C74   74    0    112PF
C75   75    0    112PF
C76   76    0    112PF
C77   77    0    112PF
C78   78    0    112PF
C79   79    0    112PF
C80   80    0    112PF
C81   81    0    112PF
*PRINT DC V(96)  V(1)    I(VIN)
.PRINT TRAN V(1) V(2) V(3) V(4) V(5) V(6) V(7) V(8) V(9)
.PRINT TRAN V(10) V(11) V(12) V(13) V(14) V(15) V(16) V(17) V(18)
*.PRINT TRAN V(19) V(20) V(21) V(22) V(23) V(24) V(25) V(26) V(27)
.PRINT  TRAN V(9) V(18) V(27) V(81)
.END
```

APPENDIX C

NODAL VOLTAGES ACCORDING TO THE PRESENT TECHNOLOGY

```
GIVE THE DIMENSION OF THE ARRAY  ? 9
TO ANALYSE VOLTAGE AS A FUNCTION OF TIME  type...3  ? 1
NUMBER OF COLUMNS TO BE PRINTED ARE ..... ? 9
NUMBER OF CELLS IN A COLUMN TO BE PRINTED ARE...? 9
GIVE THE COEFFECIENT OF Y...Kv= ? .42
GIVE  THE COEFFICIENT OF X...Kx=  ? .39
GIVE switching time of cell # 1...T1= ? 2100e-9
IF CAPACITANCE VALUE IS CONSTANT TYPE....2   ? 2
 GIVE THE CAPACITANCE VALUE ...C= ? 114e-12
 GIVE ANOTHER CAPACITANCE VALUE or press return...C= ? 114e-12


  PROGRAM D2POWER IS WRITTEN TO CALCULATE THE
  VALUE OF THE THRESHOLD VOLTAGE OF EACH CELL
      FOR A 2-DIMENSIONAL MODEL: C=114pF

                                  X =   2

     Vk( 1 , 1 )= 2              Vk( 2 , 1 )= 1.906969

     Vk( 1 , 2 )= 1.906969       Vk( 2 , 2 )= 1.884655

     Vk( 1 , 3 )= 1.862641       Vk( 2 , 3 )= 1.844521

     Vk( 1 , 4 )= 1.827015       Vk( 2 , 4 )= 1.813285

     Vk( 1 , 5 )= 1.800514       Vk( 2 , 5 )= 1.791018

     Vk( 1 , 6 )= 1.782782       Vk( 2 , 6 )= 1.777759

     Vk( 1 , 7 )= 1.773139       Vk( 2 , 7 )= 1.770301

     Vk( 1 , 8 )= 1.770714       Vk( 2 , 8 )= 1.768032

     Vk( 1 , 9 )= 1.769365       Vk( 2 , 9 )= 1.766517

        X =   3                     X =   4

     Vk( 3 , 1 )= 1.862641       Vk( 4 , 1 )= 1.827015

     Vk( 3 , 2 )= 1.851936       Vk( 4 , 2 )= 1.82252 :

     Vk( 3 , 3 )= 1.828404       Vk( 4 , 3 )= 1.814484

     Vk( 3 , 4 )= 1.801827       Vk( 4 , 4 )= 1.792139

     Vk( 3 , 5 )= 1.783306       Vk( 4 , 5 )= 1.77759 :

     Vk( 3 , 6 )= 1.772622       Vk( 4 , 6 )= 1.769152

     Vk( 3 , 7 )= 1.768201       Vk( 4 , 7 )= 1.765642

     Vk( 3 , 8 )= 1.766385       Vk( 4 , 8 )= 1.765253

     Vk( 3 , 9 )= 1.764655       Vk( 4 , 9 )= 1.764341
```

```
    X =   5                    X =   6

Vk( 5 , 1 )= 1.800514      Vk( 6 , 1 )= 1.782782
Vk( 5 , 2 )= 1.798169      Vk( 6 , 2 )= 1.779752
Vk( 5 , 3 )= 1.797832      Vk( 6 , 3 )= 1.779423
Vk( 5 , 4 )= 1.783961      Vk( 6 , 4 )= 1.777479
Vk( 5 , 5 )= 1.77222       Vk( 6 , 5 )= 1.769036
Vk( 5 , 6 )= 1.766179      Vk( 6 , 6 )= 1.764992
Vk( 5 , 7 )= 1.764279      Vk( 6 , 7 )= 1.763167
Vk( 5 , 8 )= 1.763877      Vk( 6 , 8 )= 1.763029
Vk( 5 , 9 )= 1.762766      Vk( 6 , 9 )= 1.761711

    X =   7                    X =   8

Vk( 7 , 1 )= 1.773139      Vk( 8 , 1 )= 1.770714
Vk( 7 , 2 )= 1.767302      Vk( 8 , 2 )= 1.760501
Vk( 7 , 3 )= 1.766862      Vk( 8 , 3 )= 1.760378
Vk( 7 , 4 )= 1.766282      Vk( 8 , 4 )= 1.75981
Vk( 7 , 5 )= 1.765587      Vk( 8 , 5 )= 1.758817
Vk( 7 , 6 )= 1.763723      Vk( 8 , 6 )= 1.75788
Vk( 7 , 7 )= 1.761603      Vk( 8 , 7 )= 1.754229
Vk( 7 , 8 )= 1.759207      Vk( 8 , 8 )= 1.753715
Vk( 7 , 9 )= 1.757699      Vk( 8 , 9 )= 1.751968

    X =   9

Vk( 9 , 1 )= 1.769365
Vk( 9 , 2 )= 1.758863
Vk( 9 , 3 )= 1.758333
Vk( 9 , 4 )= 1.756875
Vk( 9 , 5 )= 1.755967
Vk( 9 , 6 )= 1.753083
Vk( 9 , 7 )= 1.749111
Vk( 9 , 8 )= 1.744867
Vk( 9 , 9 )= 1.744381

     E N D
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APPENDIX D

NODAL VOLTAGES ACCORDING TO THE MODIFIED TECHNOLOGY

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GIVE THE DIMENSION OF THE ARRAY  ? 9
TO ANALYSE VOLTAGE AS A FUNCTION OF TIME  type...3  ? 1
NUMBER OF COLUMNS TO BE PRINTED ARE ..... ? 9
NUMBER OF CELLS IN A COLUMN TO BE PRINTED ARE...? 9
GIVE switching time of cell # 1...TI= ? 2100e-9
IF CAPACITANCE VALUE IS CONSTANT TYPE....2   ? 1
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PROGRAM D2POWER IS WRITTEN TO CALCULATE THE
VALUE OF THE THRESHOLD VOLTAGE OF EACH CELL
FOR A 2-DIMENSIONAL MODEL: C=114pF to 112pF

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Vk( 1 , 1 )= 2 ; Vt= 2.000055 ;  Na= 2.9623E+16  ; C= 1.142718E-10

Vk( 1 , 2 )= 1.909176 ; Vt= 1.909247 ;  Na= 2.771245E+16  ; C= 1.135245E-10

Vk( 1 , 3 )= 1.866896 ; Vt= 1.866962 ,  Na= 2.684412E+16  ; C= 1.131726E-10

Vk( 1 , 4 )= 1.832698 ; Vt= 1.832755 ;  Na= 2.61516E+16  ; C= 1.128859E-10

Vk( 1 , 5 )= 1.807299 ; Vt= 1.807364 ;  Na= 2.564328E+16  ; C= 1.126721E-10

Vk( 1 , 6 )= 1.79021 ; Vt= 1.790211 ;  Na= 2.530267E+16  ; C= 1.12527E-10

Vk( 1 , 7 )= 1.780697 ; Vt= 1.78075 ;  Na= 2.511577E+16  ; C= 1.124469E-10

Vk( 1 , 8 )= 1.77789 ; Vt= 1.777943 ;  Na= 2.506046E+16  ; C= 1.124231E-10

Vk( 1 , 9 )= 1.777647 ; Vt= 1.7777 ;  Na= 2.505566E+16  ; C= 1.12421E-10

    X =   2

Vk( 2 , 1 )= 1.909176 ; Vt= 1.909247 ;  Na= 2.771245E+16  ; C= 1.135245E-10

Vk( 2 , 2.)= 1.887946 ; Vt= 1.888023 ,  Na= 2.727493E+16  ; C= 1.133482E-10

Vk( 2 , 3 )= 1.849435 ; Vt= 1.849496 ;  Na= 2.648941E+16  ; C= 1.130264E-10

Vk( 2 , 4 )= 1.819756 ; Vt= 1.819817 ;  Na= 2.589198E+16  ; C= 1.127771E-10

Vk( 2 , 5 )= 1.798019 ; Vt= 1.798085 ;  Na= 2.545877E+16  ; C= 1.125937E-10

Vk( 2 , 6 )= 1.784644 ; Vt= 1.784712 ;  Na= 2.519396E+16  ; C= 1.124805E-10

Vk( 2 , 7 )= 1.778703 ; Vt= 1.77876 ;  Na= 2.507655E+16  ; C= 1.1243E-10

Vk( 2 , 8 )= 1.775951 ; Vt= 1.776023 ;  Na= 2.502265E+16  ; C= 1.124068E-10

Vk( 2 , 9 )= 1.775478 ; Vt= 1.77553 ;  Na= 2.501294E+16  ; C= 1.124026E-10
```

X = 3

Yk(3 , 1) = 1.066896 ; Vl= 1.066957 ; Na= 2.684402E+16 ; C= 1.131725E-10

Yk(3 , 2) = 1.05858 ; Vl= 1.058645 ; Na= 2.667491E+16 ; C= 1.13103E-10

Yk(3 , 3) = 1.034403 ; Vl= 1.03446 ; Na= 2.61859E+16 ; C= 1.129003E-10

Yk(3 , 4) = 1.008868 ; Vl= 1.008944 ; Na= 2.567478E+16 ; C= 1.126054E-10

Yk(3 , 5) = 1.790689 ; Vl= 1.790756 ; Na= 2.531347E+16 ; C= 1.125317E-10

Yk(3 , 6) = 1.781016 ; Vl= 1.781084 ; Na= 2.512236E+16 ; C= 1.124497E-10

Yk(3 , 7) = 1.776018 ; Vl= 1.776069 ; Na= 2.502355E+16 ; C= 1.124072E-10

Yk(3 , 8) = 1.773483 ; Vl= 1.773542 ; Na= 2.497385E+16 ; C= 1.123857E-10

Yk(3 , 9) = 1.772859 ; Vl= 1.772907 ; Na= 2.496134E+16 ; C= 1.123803E-10

X = 4

Yk(4 , 1) = 1.032698 ; Vl= 1.032745 ; Na= 2.61514E+16 ; C= 1.128858E-10

Yk(4 , 2) = 1.031328 ; Vl= 1.031403 ; Na= 2.61244E+16 ; C= 1.128746E-10

Yk(4 , 3) = 1.021197 ; Vl= 1.021266 ; Na= 2.592099E+16 ; C= 1.127893E-10

Yk(4 , 4) = 1.799062 ; Vl= 1.799138 ; Na= 2.547968E+16 ; C= 1.126026E-10

Yk(4 , 5) = 1.785646 ; Vl= 1.785699 ; Na= 2.521347E+16 ; C= 1.124888E-10

Yk(4 , 6) = 1.778176 ; Vl= 1.778253 ; Na= 2.506657E+16 ; C= 1.124257E-10

Yk(4 , 7) = 1.77414 ; Vl= 1.774159 ; Na= 2.498596E+16 ; C= 1.12391E-10

Yk(4 , 8) = 1.773018 ; Vl= 1.773075 ; Na= 2.496466E+16 ; C= 1.123818E-10

Yk(4 , 9) = 1.772112 ; Vl= 1.77219 ; Na= 2.494725E+16 ; C= 1.123743E-10

X = 5

Yk(5 , 1) = 1.807299 ; Vl= 1.807348 ; Na= 2.564298E+16 ; C= 1.126719E-10

Yk(5 , 2) = 1.807153 ; Vl= 1.807208 ; Na= 2.564018E+16 ; C= 1.126707E-10

Yk(5 , 3) = 1.806519 ; Vl= 1.80658 ; Na= 2.562768E+16 ; C= 1.126654E-10

Yk(5 , 4) = 1.7922 ; Vl= 1.792275 ; Na= 2.534357E+16 ; C= 1.125445E-10

Yk(5 , 5) = 1.781835 ; Vl= 1.781915 ; Na= 2.513876E+16 ; C= 1.124568E-10

Yk(5 , 6) = 1.775715 ; Vl= 1.775795 ; Na= 2.501816E+16 ; C= 1.124049E-10

Yk(5 , 7) = 1.773309 ; Vl= 1.773376 ; Na= 2.497056E+16 ; C= 1.123843E-10

Yk(5 , 8) = 1.772266 ; Vl= 1.772327 ; Na= 2.494996E+16 ; C= 1.123754E-10

Yk(5 , 9) = 1.772089 ; Vl= 1.772154 ; Na= 2.494656E+16 ; C= 1.12374E-10

X = 6

Vk(6 , 1) = 1.79021 ; Vt= 1.790225 ; Na= 2.530298E+16 ; C= 1.125272E-10

Vk(6 , 2) = 1.790132 ; Vt= 1.79019 ; Na= 2.530228E+16 ; C= 1.125269E-10

Vk(6 , 3) = 1.78978 ; Vt= 1.789841 ; Na= 2.529537E+16 ; C= 1.125239E-10

Vk(6 , 4) = 1.786425 ; Vt= 1.786494 ; Na= 2.522917E+16 ; C= 1.124956E-10

Vk(6 , 5) = 1.777983 ; Vt= 1.778035 ; Na= 2.506226E+16 ; C= 1.124239E-10

Vk(6 , 6) = 1.773638 ; Vt= 1.773691 ; Na= 2.497675E+16 ; C= 1.12387E-10

Vk(6 , 7) = 1.772713 ; Vt= 1.77277 ; Na= 2.495865E+16 ; C= 1.123792E-10

Vk(6 , 8) = 1.772008 ; Vt= 1.772062 ; Na= 2.494474E+16 ; C= 1.123732E-10

Vk(6 , 9) = 1.771616 ; Vt= 1.771675 ; Na= 2.493714E+16 ; C= 1.123699E-10

X = 7

Vk(7 , 1) = 1.780697 ; Vt= 1.78076 ; Na= 2.511597E+16 ; C= 1.12447E-10

Vk(7 , 2) = 1.780308 ; Vt= 1.780369 ; Na= 2.510826E+16 ; C= 1.124437E-10

Vk(7 , 3) = 1.779799 ; Vt= 1.779877 ; Na= 2.509856E+16 ; C= 1.124395E-10

Vk(7 , 4) = 1.779126 ; Vt= 1.779171 ; Na= 2.508465E+16 ; C= 1.124335E-10

Vk(7 , 5) = 1.775161 ; Vt= 1.77524 ; Na= 2.500724E+16 ; C= 1.124002E-10

Vk(7 , 6) = 1.771856 ; Vt= 1.771909 ; Na= 2.494174E+16 ; C= 1.123719E-10

Vk(7 , 7) = 1.770074 ; Vt= 1.770148 ; Na= 2.490713E+16 ; C= 1.123569E-10

Vk(7 , 8) = 1.767712 ; Vt= 1.767759 ; Na= 2.486023E+16 ; C= 1.123366E-10

Vk(7 , 9) = 1.767146 ; Vt= 1.767193 ; Na= 2.484912E+16 ; C= 1.123318E-10

X = 8

Vk(8 , 1) = 1.77789 ; Vt= 1.777948 ; Na= 2.500056E+16 ; C= 1.124231E-10

Vk(8 , 2) = 1.774714 ; Vt= 1.774759 ; Na= 2.499776E+16 ; C= 1.123961E-10

Vk(8 , 3) = 1.774028 ; Vt= 1.774087 ; Na= 2.498455E+16 ; C= 1.123904E-10

Vk(8 , 4) = 1.773417 ; Vt= 1.773487 ; Na= 2.497275E+16 ; C= 1.123853E-10

Vk(8 , 5) = 1.770885 ; Vt= 1.770958 ; Na= 2.492305E+16 ; C= 1.123638E-10

Vk(8 , 6) = 1.770122 ; Vt= 1.770178 ; Na= 2.490774E+16 ; C= 1.123572E-10

Vk(8 , 7) = 1.766751 ; Vt= 1.766805 ; Na= 2.484153E+16 ; C= 1.123285E-10

Vk(8 , 8) = 1.766437 ; Vt= 1.766489 ; Na= 2.483533E+16 ; C= 1.123258E-10

Vk(8 , 9) = 1.765641 ; Vt= 1.765709 ; Na= 2.482002E+16 ; C= 1.123192E-10

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     X =    9

Vk(  9 ,  1 ) = 1.777647 ; Vl= 1.7777 ;  Na= 2.505566E+16  ; C= 1.12421E-10

Vk(  9 ,  2 ) = 1.773316 ; Vl= 1.773386 ;  Na= 2.497075E+16  ; C= 1.123844E-10

Vk(  9 ,  3 ) = 1.772998 ; Vl= 1.77307 ;  Na= 2.496455E+16  ; C= 1.123817E-10

Vk(  9 ,  4 ) = 1.768073 ; Vl= 1.768932 ;  Na= 2.488325E+16  ; C= 1.123466E-10

Vk(  9 ,  5 ) = 1.768229 ; Vl= 1.768295 ;  Na= 2.487074E+16  ; C= 1.123412E-10

Vk(  9 ,  6 ) = 1.765576 ; Vl= 1.765653 ;  Na= 2.481094E+16  ; C= 1.123187E-10

Vk(  9 ,  7 ) = 1.764007 ; Vl= 1.764138 ;  Na= 2.478923E+16  ; C= 1.123058E-10

Vk(  9 ,  8 ) = 1.762261 ; Vl= 1.762335 ;  Na= 2.475393E+16  ; C= 1.122905E-10

Vk(  9 ,  9 ) = 1.762096 ; Vl= 1.762161 ;  Na= 2.475052E+16  ; C= 1.12289E-10


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