| **Schottky clamps** | | Marks allocated (40) |
|---|---|---|
| 1.4 | Schematic of the RTL logic circuit | 2 |
| 1.4 | Simulated plot of the RTL gate when for an input pulse amplitude of 5V and duration of 200 ns | 1 |
| 1.4 | Estimate (1) Turn-on delay, (2) Fall time, (3) Charge storage delay, (4) Rise time. | 4 |
| 1.5 | Simulated plot of the RTL gate when for pulse durations of 300 ns, 400 ns, and 500 ns and estimate the charge storage delay based on these measurements | 3 |
| 1.5 | Calculate charge storage delay for 300 ns, 400 ns, and 500 ns and estimate the charge storage delay based on these measurements | 4 |
| 1.5 | Explain why shorter pulse duration have different charge storage delay | 2 |
| 1.6 | Calculate charge recovery time constant $\tau_x$<br>**Important: this should clearly show the steps in calculating the steady state base currents** | 4 |
| 1.7 | Simulated plot of the RTL gate when the base resistor is doubled | 1 |
| 1.7 | Calculate charge storage delay | 2 |
| 1.7 | Calculate the charge recovery time constant $\tau_x$ and discuss if this value is as same as that obtained in 1.6 | 3 |
| 1.8 | Schematic with the Schottky diode | 2 |
| 1.8 | Simulated plot of the RTL gate with the Schottky diode at 200 ns | 1 |
| 1.8 | Estimate the charge storage delay for 200 ns, 300 ns, 400 ns and 500 ns | 4 |
| 1.8 | Comment on how these time delays compare with the unclamped circuit. | 2 |
| 1.9 | Measure the Schottky diode current and the collector current, summarize the role of the Schottky diode in the circuit when the BJT nears saturation. | 5 |

| **Transistor Transistor Logic (TTL) and Low Power Schottky TTL (LSTTL)** | | Marks allocated (40) |
|---|---|---|
| 2.2 | Schematic of the TTL logic circuit | 1 |
| 2.2 | Simulated plot of the TTL logic gate output | 1 |
| 2.2 | Measure the high-to-low (output) propagation time, $t_{PHL,}$ and the low-to-high propagation time, $t_{PLH.}$ | 2 |
| 2.2 | Explain why the low-to-high propagation time dominates the switching speed in TTL circuits. | 2 |
| 2.3 | State of each transistor $Q_1$ - $Q_4$<br>**Important: You should support your answer with the calculated currents/voltages**<br>**0.5 marks for the state and 0.5 marks for supporting your answer with the voltages/currents for each transistor** | 4 |
| 2.3 | Explain the purpose of the diode $D_1$ and determine when it is forward or reverse biased<br>**(2 marks for the purpose and 1 mark each for determining when it is forward and reversed biased)** | 4 |
| 2.4 | Calculate the instantaneous and average power | 2 |
| 2.5 | Simulated plot of the LSTTL logic gate output | 1 |
| 2.5 | Measure the high-to-low (output) propagation time, $t_{PHL,}$ and the low-to-high propagation time, $t_{PLH.}$ | 2 |
| 2.5 | Compare these propagation delays with those obtained for the TTL case. Discuss your findings | 2 |
| 2.6 | Calculate the instantaneous and average power | 2 |
| 2.6 | Compare the power dissipation of the LSTTL inverter with the TTL inverter. Discuss your answer | 2 |
| 2.6 | Compare the overall performance of LSTTL compared with TTL circuits. Discuss the propagation delay and power consumption performance | 4 |
| 2.7 | With the aid of appropriate measurements, explain why all the transistors except Q5 are Schottky transistors. | 3 |
| 2.8 | Using appropriate measurements, show the circuit shown in Figure 3 act as an active pull down | 5 |
| 2.8 | Explain how this active pull down circuit helps in the switching of the output stage BJT Q2. | 3 |

| **Emitter Coupled Logic (ECL)** | | Marks allocated (40) |
|---|---|---|
| 3.1 | Schematic of the ECL logic circuit | 1 |
| 3.1 | Explain if Is this a NECL or PECL logic gate circuit. | 2 |
| 3.1 | Are the two resistors RT1 and RT2 typically part of the logic gate or external to it? | 2 |
| 3.1 | Explain why might ECL gates be useful for driving terminated transmission lines | 2 |
| 3.1 | Explain the purpose of the sub-circuit shown in Figure 6 | 2 |
| 3.2 | Identify the possible High and Low voltage values for the input from the datasheet | 1 |
| 3.2 | Simulated output values at Q1 and Q2 for different VA and VB combinations, i.e VAVB = LL, LH,HL,HH | 4 |
| 3.2 | Determine the logic function based on the input/output values | 1 |
| 3.3 | Simulated plot of voltage transfer characteristics from input VA to the outputs defined by the emitter voltages of Q1 and Q2 | 2 |
| 3.3 | Determine the input voltage for which the two output voltages are equal | 1 |
| 3.3 | Determine the high / low output / input voltages (denoted $V_{OH}$, $V_{OL}$, $V_{IH}$, $V_{IL}$) | 4 |
| 3.3 | The high / low noise margins (denoted $NM_H$ and $NM_L$). | 2 |
| 3.3 | Comparison of simulated values and values given in the datasheet | 1 |
| 3.3 | Discuss the factors or assumptions that may contribute to any differences you observe | 2 |
| 3.4 | Simulated plot of the transient analysis | 1 |
| 3.4 | Measure the high-to-low (output) propagation time, $t_{PHL,}$ and the low-to-high propagation time, $t_{PLH}$. | 2 |
| 3.4 | Compare the high-to-low (output) propagation time, $t_{PHL,}$ and the low-to-high propagation time, $t_{PLH}$ of TTL, SLTTL, and ECL logic circuits | 2 |
| 3.4 | Explain the essential feature of ECL operation that results in the switching performance of the ECL compared to the other two | 2 |
| 3.5 | Calculate the instantaneous and average power | 2 |
| 3.5 | Compare the average power of ECL circuit against TTL and SLTTL logic circuits. Discuss your answer | 2 |
| 3.6 | Explain if the average power dissipation is frequency dependant or not | 2 |

| **CMOS** | | Marks allocated (15) |
|---|---|---|
| 4.1 | Schematic of the CMOS inverter | 1 |
| 4.2 | Simulated plot of the transient analysis | 1 |
| 4.2 | Measure the high-to-low (output) propagation time, $t_{PHL,}$ and the low-to-high propagation time, $t_{PLH}$. | 2 |
| 4.2 | Compare the propagation delays against TTL, LSTTL and ELC logic inverters | 2 |
| 4.3 | Simulated plot of the current flowing from the output of the first gate | 1 |
| 4.3 | Discuss the nature of the steady state current flowing through the first gate and why | 2 |
| 4.4 | Calculate the instantaneous power | 1 |
| 4.4 | Discuss when during the transient, power is dissipated | 1 |
| 4.4 | Compare the power consumption of TTL, LSTTL, ECL, and CMOS | 2 |
| 4.5 | Discuss how the performance changes if signal MOSFETs are used in place of the IRF MOSFETs | 2 |

| **BiCMOS** | | Marks allocated (45) |
|---|---|---|
| 5.1.1 | Schematic of the BiCMOS inverter | 1 |
| 5.1.2 | Simulated plot of the input and output voltages as a function of time | 1 |
| 5.1.2 | Determine the logic function | 1 |
| 5.1.3 | Simulated plots of the input and outputs as a function of time for Cload = 0.1 pF, 1 pf, and 1 pF. | 3 |
| 5.1.3 | Measure the high-to-low (output) propagation time, $t_{PHL,}$ and the low-to-high propagation time, $t_{PLH}$ for Cload = 0.1 pF, 1 pf, and 1 pF. | 3 |
| 5.1.3 | Discuss the ability of this circuit to drive difference capacitive loads | 2 |
| 5.2.1 | Schematic of the BiCMOS inverter with push pull circuit | 2 |
| 5.2.1 | Simulated plot of the input and output voltages as a function of time | 1 |
| 5.2.1 | Verify the logic function using the simulated plot | 2 |
| 5.2.2 | Simulated plots of the input and outputs as a function of time for Cload = 0.1 pF, 1 pf, and 1 pF. | 3 |
| 5.2.2 | Measure the high-to-low (output) propagation time, $t_{PHL,}$ and the low-to-high propagation time, $t_{PLH}$ for Cload = 0.1 pF, 1 pf, and 1 pF. | 3 |
| 5.2.2 | Explain the performance improvement and trade-off | 2 |
| 5.2.3 | Explain the purpose of resistor R1 in the BiCMOS logic gate of Figure 9<br>Important: your answer should include simulated plots for the logic output with and without the resistor | 4 |
| 5.3.1 | Schematic of the BiCMOS logic gate with push-pull output stage and auxiliary inverters | 1 |
| 5.3.1 | Simulated plot of the input and output voltages for the inputs specified in the schematic | 1 |
| 5.3.1 | Verify the logic function using the simulated plot | 1 |
| 5.3.2 | Compare the steady state HIGH and LOW output voltages generated by the BiCMOS logic gates of Figures 8, 9 and 10 | 2 |
| 5.3.3 | Determine the purpose of the auxiliary CMOS inverter | 3 |

| | | |
|---|---|---|
| 5.3.3 | Determine the instantaneous power delivered by the supply rails in this circuit | 1 |
| 5.3.3 | Compare the power dissipation of this BiCMOS logic gate compare with the CMOS logic function of Figure 8 | 2 |
| 5.3.4 | Discuss if the average power dissipation of this BiCMOS logic gate to be frequency dependent | 2 |
| 5.3.4 | Determine the average power consumption for different signal periods to support your answer | 4 |

| **Discussion** | | Marks allocated (20) |
|---|---|---|
| 6.1 | Discuss which of the families considered is best suited to low power applications. | 5 |
| 5.1.2 | Discuss which families are suited to high switching speeds | 5 |
| 5.1.2 | Discuss which families are suited to driving low impedance loads | 5 |
| 5.1.3 | Discuss if there is any apparent trade-off between switching speed and current drive. Discuss which families are designed for both | 5 |

**Important**

- Where possible, try to include the schematics, relevant simulated voltage/current plots to support your answer and to make your report more comprehensive.
- Clearly indicate the equations and steps used in calculations.