ELEN90062 High Speed Electronics

Workshop Four

Single-stage Transistor Amplifier Design for Maximum Gain

Welcome to Workshop 4 for High Speed Electronics. The objective of this workshop is to design input and output matching networks for a single-stage transistor amplifier using a single-stub matching technique.

Instructions

- The workshop is worth 2.5% of your final subject mark.
- You must complete the pre-lab exercise before coming to the class
- You must show the completed tasks to your workshop demonstrator.
- The report should have a brief executive summary detailing the objective of the workshop. The remaining part of the report should consist of the outcome of the tasks below (calculations, plots, discussions etc.).
- The report should clearly show the equations used in calculations.
- The report is due on 14/09/2018.
- Submit one report per group.

Background

Microwave Amplifier

A microwave amplifier is one of the most basic and critical components in modern RF and microwave systems. The modern microwave amplifiers use transistor devices such as Si or SiGe BJTs, GaAs HBTs, GaAs or InP FETs, or GaAs HEMTs. The microwave amplifiers are rugged, low-cost, and reliable and can be easily integrated in both hybrid and monolithic integrated circuitry. The figure-of-merits related to the performance of microwave amplifiers are gain, noise-figure, bandwidth, power, and size. In this lab we will focus on the design of a microwave amplifier for maximum gain. The principle of the design relies on the two-port characteristics of a transistor as represented by its S parameters usually provided by the manufacturer. We will derive the input and output matching networks for conjugate matching in order to maximize the gain and implement them with a single-stub configuration.

Theoretical background of amplifier design for maximum gain

A microwave amplifier can be considered as a special case of two-port network shown in Figure 1. Its gain can be represented with the so-called transducer power gain G_T defined as follows:

$$G_T = \frac{G_L}{G_{avs}} \tag{1}$$

where G_L and G_{avs} represent the power dissipated at the load and power available at the source, respectively. It has been shown that the transducer gain can also represented as a function of reflection coefficients and S-parameters as follows:

$$G_T = \frac{G_L}{G_{avs}} = \frac{|S_{21}|^2(1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{(|1-\Gamma_{in}\Gamma_s|^2)(|1-\Gamma_L S_{22}|^2)}) \tag{2}$$

Where S_{ij} is the S parameters for the two-port network and Γ_s, Γ_L, and Γ_{in} are the reflection coefficients for the source, load, and the input port he two-port network, respectively. Lets first assume that the amplifier is

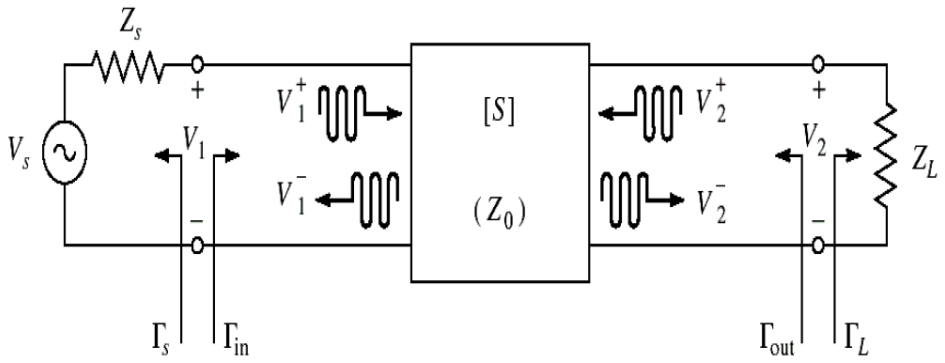


Figure 1: Two port network model for microwave amplifier

unconditionally stable. Maximum gain can be obtained when the conjugate matching condition is satisfied. If the transistor appears as a significant impedance mismatch (large S11 and S22), the resulting frequency response will be narrow band.
From the principle of the conjugate matching, the maximum power transfer from the input matching network to the transistor will occur when

$$\Gamma_{in} = \Gamma_s^* \tag{3}$$

and the maximum power transfer from the transistor to the output matching network will occur when

$$\Gamma_{out} = \Gamma_L^* \tag{4}$$

These conditions will maximize the overall transducer gain. From eqn. 2, the maximum gain reduces to:

$$G_{max} = \frac{|S_{21}|^2(1-|\Gamma_L|^2)}{(1-|\Gamma_s|^2)(|1-\Gamma_L S_{22}|^2}) \tag{5}$$

It can be easily shown that assuming $S_{12} = 0$, we obtain the so-called maximum unilateral power gain, G_{UM} defined as follows:

$$G_{UM} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \tag{6}$$

which is often quoted in the data sheet provide by the transistor manufacturer.

From the congugating conditions given in eqns. (3) and (4), we can explicitly derive solutions for Γ_s and Γ_L as follows;

$$\Gamma_s = \frac{B_1 \pm \sqrt{B_1^2 - 4C_1^2}}{2C_1} \tag{7}$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4C_2^2}}{2C_2} \tag{8}$$

$$where \tag{9}$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{10}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{11}$$

$$C_1 = S_{11} - \Delta S_{22}^* \tag{12}$$

$$C_2 = S_{22} - \Delta S_{11}^* \tag{13}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{14}$$

Designing a microwave amplifier for a maximum gain

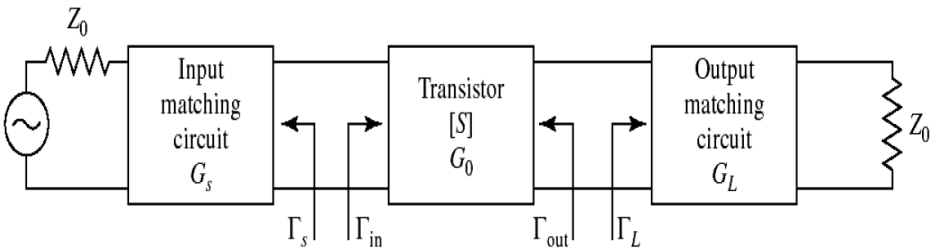


Figure 2: The general transistor amplifier circuit

A single-stage microwave transistor amplifier can be modeled in the circuit shown in Figure 2 [1]. For the particular application of achieving maximum gain relevant to this lab, the input/output matching circuit is to transfer source reflection coefficient Γ_s^0 to the desired Γ_s/Γ_L expressed by eqns. (7) and (8).

Input and output impedance matching circuits

In addition to the application of maximizing the gain for a microwave amplifier, matching circuits are useful in other applications including impendence matching for antenna and low-noise amplifier to improve the signal-to-noise ratio, and impedance matching for power distribution network to reduce amplitude and phase errors. Many choices are available influenced by some practical factors such as complexity, bandwidth, and adjustability.

We will consider for the lab a single-stub matching technique that uses a single open-circuit or short-circuited length of transmission line shown in Figure 3, where shunt and serial matching network are used to transform arbitrary load Y_L (impedance Z_L) into the characteristic admittance Y_0 (impedance Z_0).

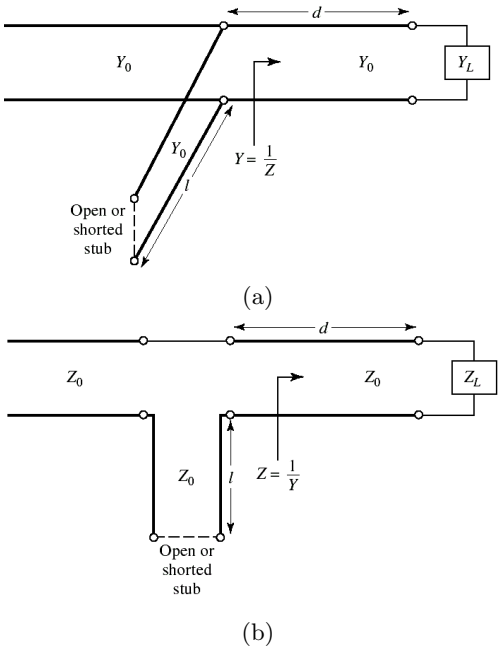


Figure 3: Single-stub matching circuits. (a) Shunt stub. (b) Series stub

For the amplifier design, we can provide a similar solution with some modifications. Figure 4 shows the matching network design for the input matching where the output admittance is transformed from Y_0 to Y_s, where Y_s is the source admittance that satisfies the conjugate matching corresponding to the Γ_s computed in eqn. (7). A point at length d from the generator will have impedance Y_1 with a real part of the admittance equal to the characteristic admittance Y_0, which is

$$Y_1 = Y_0 + jS \tag{15}$$

The imaginary component is provided by the open or shorted stub with appropriate length l and we have:

$$Y_{stub} = jS \tag{16}$$
$$Y_1 = Y_0 + Y_{stub} \tag{17}$$

where Y_{stub} stands for the admittance looking into the open or shorted stub with length l. The output impedance circuit can be obtained in almost identical manner.

The transmission line for the lab is implemented in microstrip circuits. These have a dielectric thinness of 1.2 mm and use a composite epoxy-fiberglass material call FR-4 that has relative permittivity of $\varepsilon_r = 4.3$ at 2.4 GHz. The transmission line made of 1oz copper (which has a thickness of 35 micron) and is designed to have a characteristic impedance of 50 ohm by setting the transmission line width to a specific value. You will need to calculate this width as part of this workshop.

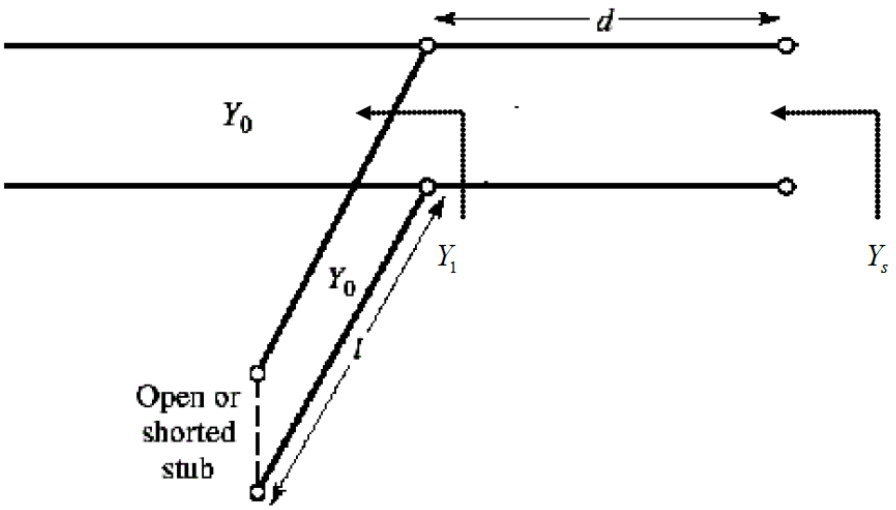


Figure 4: Single-stub circuit for input impedance matching

Bipolar Junction Transistor

The transistor used for the lab is the ATF50189. The datasheet for this component will be made available on the LMS. (Please note that you are expected to know how to obtain datasheets for such components by searching through the websites of suppliers such as Element14, Mouser or Digikey.) Figure 5 shows the bias characteristics for the transistor in common-emitter configuration. For this lab, both the RF signals and DC biases are fed through input and output transmissions lines. The input and output bias voltages, V^1_{bias} and V^2_{bias} are provided by the Bias-Ts inside the vector network analyzer. The gain of the transistor can be set by Collector current I_c and can be tuned by varying V^1_{bias}.

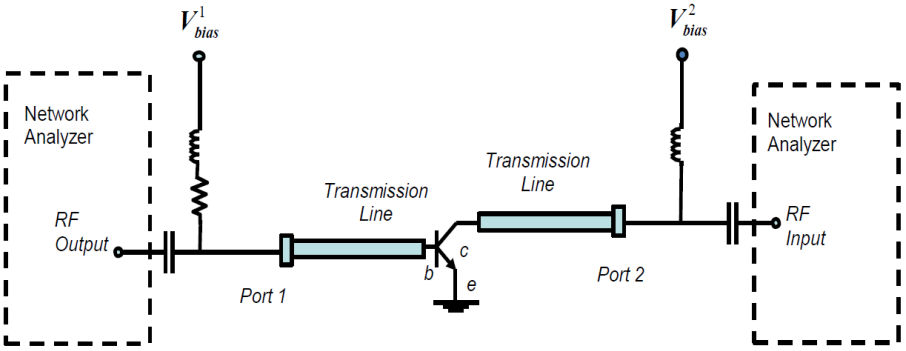


Figure 5: Biasing and decoupling circuit for BJT

Microwave Vector Network Analyser

The S parameters of passive and active networks can be measured with a vector network analyzer as shown in Figure 6. The incident signals (A1, A2) and reflection signals (B1 and B2) for the two-port device under test (DUT) can be measured and related to the S parameters as follows:

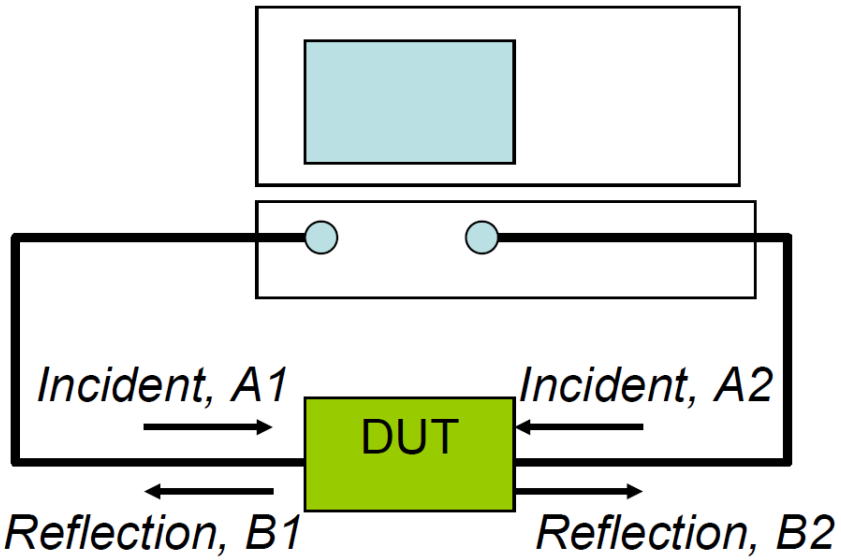


Figure 6: Vector Network Analyser

$$\begin{bmatrix} B_1 \\ B_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \end{bmatrix}$$

The measured voltages are complex values with both amplitude and phase, and so are the S parameters derived from the measurement. The vector network analyzer can therefore display the S parameters in magnitude and phase, as well as the Smith chart for S_{11} and S_{22}. Please take note that the network analyzer measurement result is dependent on at which point the measurement is being measured. The analyzer can add or subtract a differential delay to calibrate out the transmission line phase delay including measurement cables and on-board transmission lines.

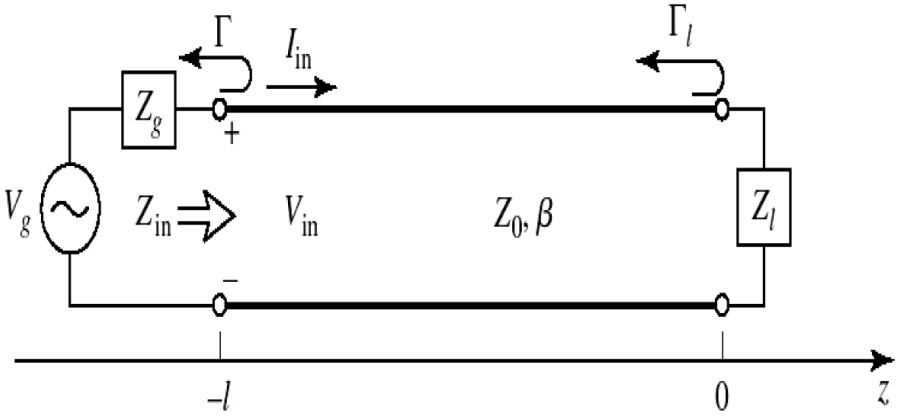


Figure 7: Transmission line circuit for arbitrary generator and load impedances

Task 1: Figure 8 shows a transmission line circuit with arbitrary generator and load impedances.

- Derive an equation for the power delivered to the load P_L in terms of V_g, R_g, R_{in}, X_{in} and X_g where R_g and X_g are the real and imaginary components of Z_g, while R_{in} and X_{in} are the real and imaginary components of Z_{in}.
- With the reference to the equation derived in (1), show that P_L is maximized when the conjugating matching condition is satisfied, which is:

$$Z_{in} = Z_g^* \tag{18}$$

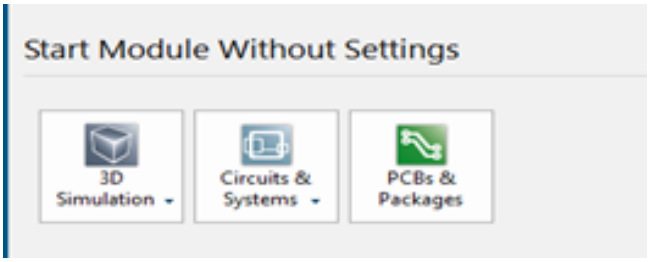
Task 2: Assume the following S parameters for a BJT transistor at 2.4 GHz
$S_{11} = 0.912\angle 127.1$
$S_{12} = 0.041\angle 26.0$
$S_{21} = 1.721\angle 35.6$
$S_{22} = 0.75\angle 143.9$

- Compute Γ_s and Γ_L using eqns. 7 and 8 under which the conjugating conditions are met.
- What is the gain improvement by using conjugate matching circuits?
- With the aid of the Smith Chart, derive the lengths of the transmission lines for the shunt single-stub circuits as shown in Figure 4, for both input and output matching circuits. Using Equations 3.195-3.197 in [1] to calculate the corresponding wavelength at 2.4 GHz for 50 ohm transmission line on the PCB used for the lab.

(19)

CST Simulation

Start CST and select Circuits and Systems and then select the Schematic view. The schematic view will allow us to place microstrip(tracks and tuning stubs) and discrete components (amplifier) through numerous import file types, in this case it will be a s2p file.

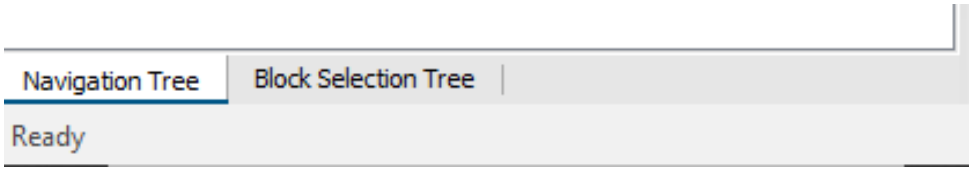


Stage 1: Designing a microstrip with an optimized width

In this stage we will create a schematic with a simple microstrip track and two external ports. Using our Block parameter list we will be able to parameterize our basic circuit design features such as copper thickness and dielectric constants.

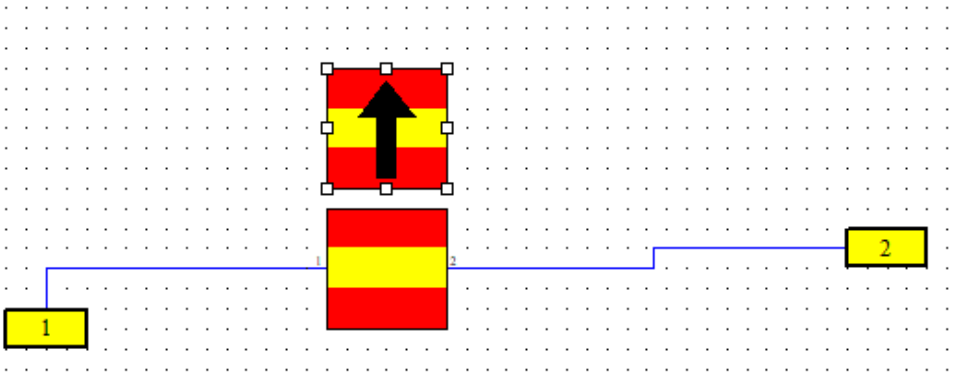
To begin we will start placing our two external ports as well as our simple microstrip track connecting them over FR4 circuit board material.

Place two external ports 1 and 2 (they will label themselves). In the bottom left of our screen we want to swap from Navigation tree to Block Selection tree.

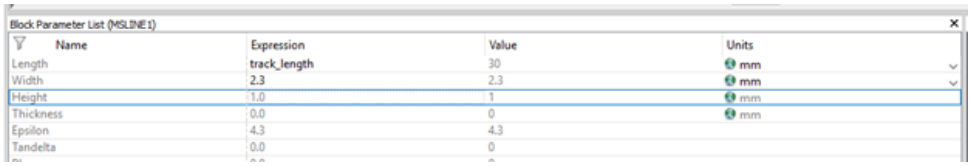


If we now look on the left hand side there will be a number of pre-defined blocks which we can use. For the purpose of this workshop obviously the microstrip section is of interest to us!

When this is selected there is a group of more common microstrip components that appears. Track is one of them, select this and drag it onto the schematic as shown.

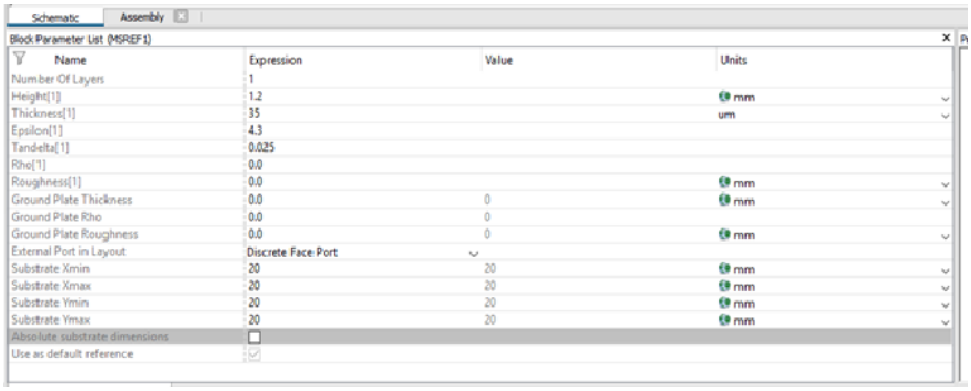


We now want to connect our external ports to each end of the stripline. Youll notice that a Microstrip Reference block has also appeared. This is where we will have to enter our parameters for the reference plane for our microstrip components like size, distance from microstrip and dielectric constant. Click on the track component first and enter the parameters as shown.



When you enter track_length as a parameter as it has no numerical value it becomes a variable parameter which we can tune later. A prompt will appear asking for a numerical value and a description, enter 30 and a description of your choosing.

Now click on the Microstrip Reference block and alter the parameters to below. Note that for the Thickness you will also have to change the units from mm to um.

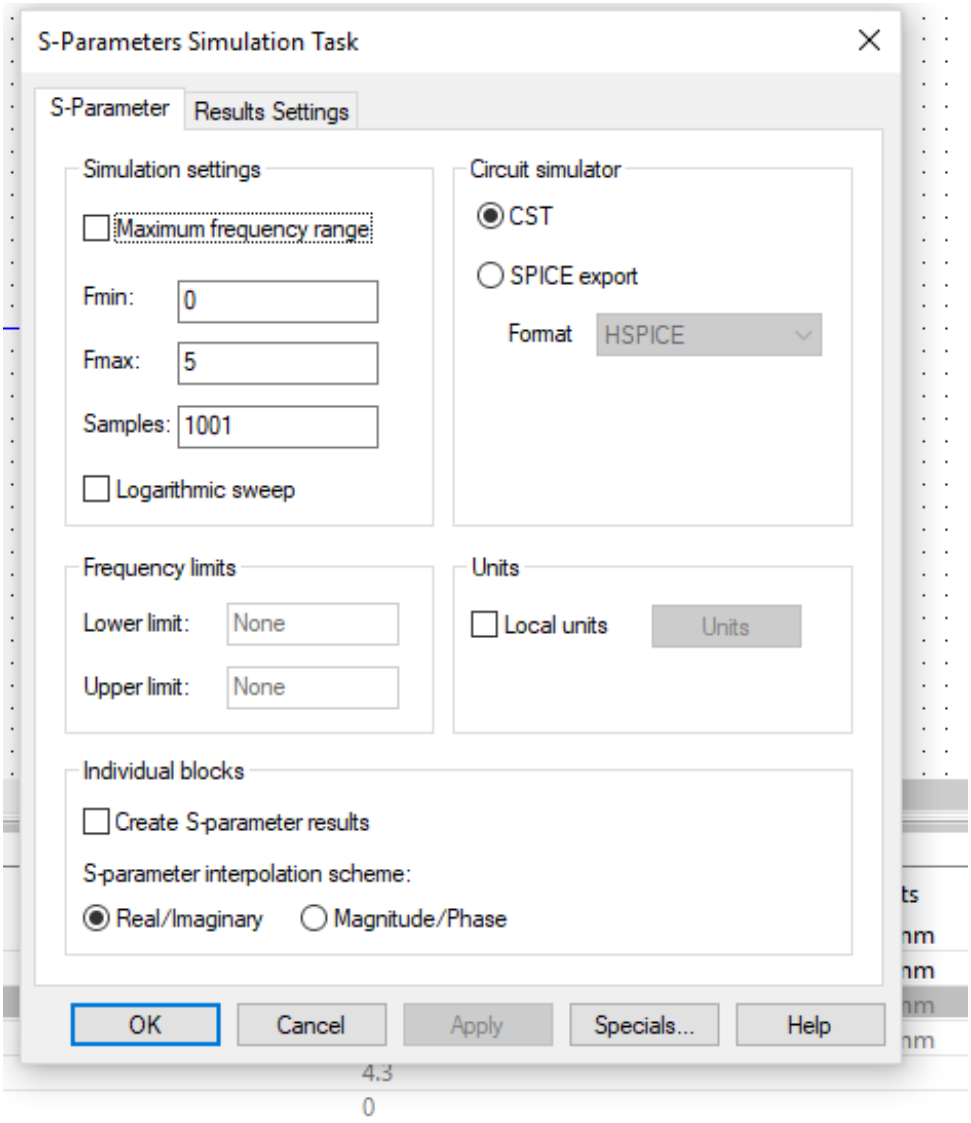


The power of the schematic design is that we can run simple simulations very quickly here, or if we want more complex results we can create a 3D representation of our drawing with the information we have included and use the 3D model to perform other simulations.

If we now go back to the bottom left of CST and select the Navigation tree we can see that it has sorted our placed components for us including our ports, stripline and reference block. There is also a section there labelled Task this is where we can undertake S-parameter calculations DC point calculations, Amplifier/assembly designs and so-on.

We want to eventually add two tasks to our list, the first is a S-parameter task. Select the Task button, and New Task, in the prompt select S-Parameters and click ok. Simply change the 1 to a 5 as below, this will allow us to see results from DC-5GHz as opposed to 1GHz where we might miss important features.

Before we add our second task lets update and see the S-parameter results and how close the port impedances are to 50 Ohm. NOTE Port Impedences



At this stage we are not going to add our second task as we want to get or characteristic impedance as close to 50 Ohm as possible. To make this slightly easier lets parameterize another variable, this time make it the width of the track. To do this lets go back to the Schematic view and select the Track block and change the width field from 2.3 to track width as we did with the length and enter 2.3 as the numerical value. We can now setup a parameter sweep which will very quickly calculate our characteristic impedance at each change in variable.

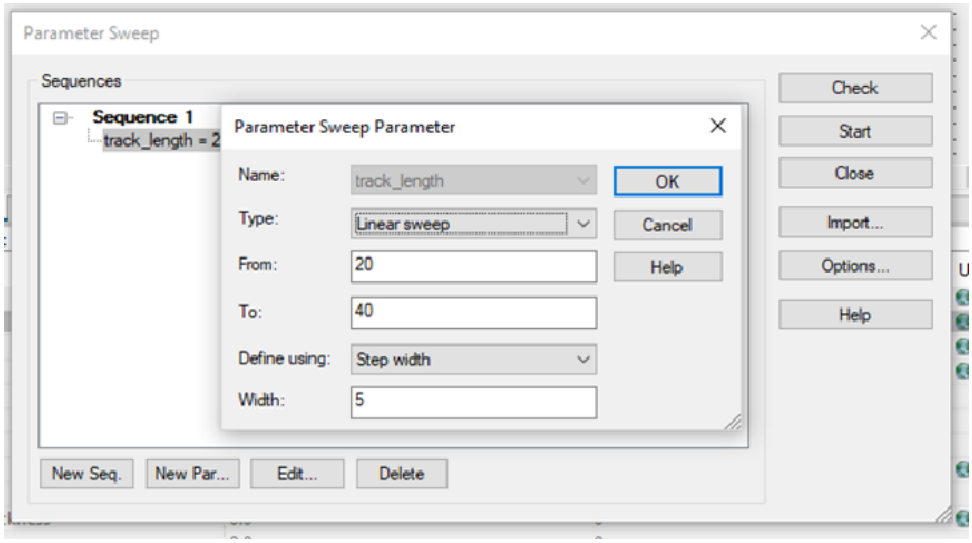
In our ribbon on the top next to Update is a Par. Sweep button, select this. We want to setup a new Sequence and under that sequence add a New Parameter to sweep, in this case it will be track length. Here we can alter the length of the stripline track and see how each change in a sweep changes our response. Lets change it From 20 to 40 in Step Widths of 5mm.

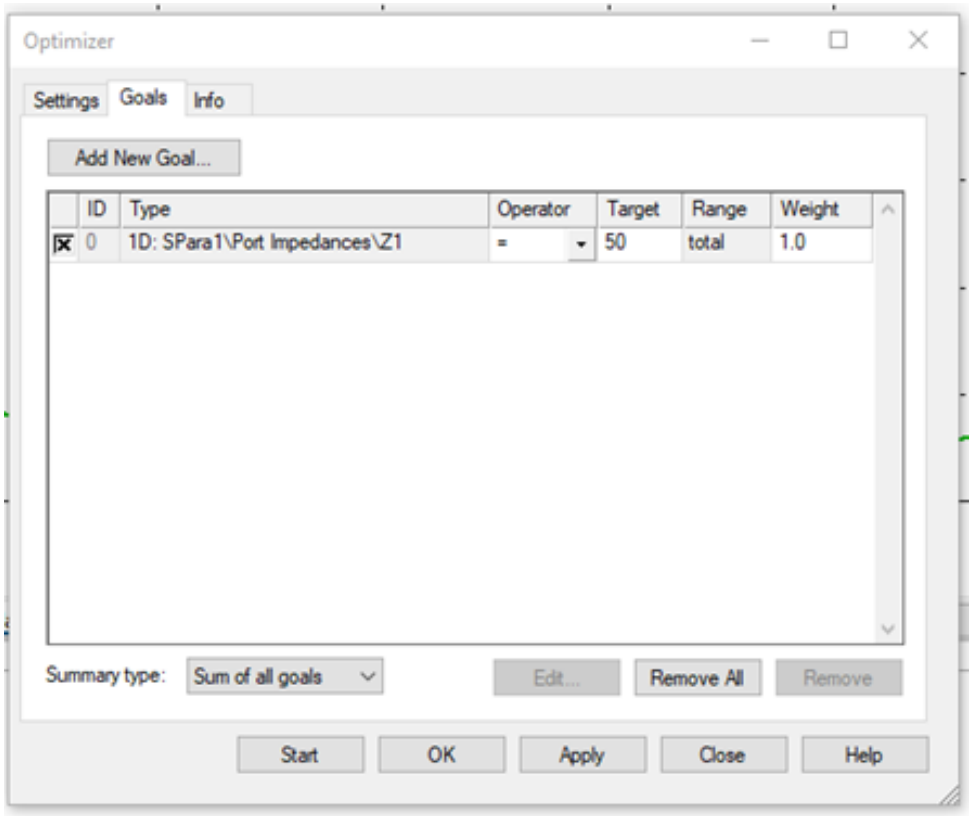
If we now press Start, CST will alter the schematic and sweep those parameters for us. NOTE whether this improves the response of the circuit.

Another feature of CST is its inbuilt optimizer. Located just above the Par. Sweep button. We want to add a new goal for the optimizer to try and achieve, in this case we want Z1 the impedance of port 1 to be equal to 50 Ω.

We then need to set the optimizer some variables to change. We currently only have two variables, track_length and track_width, select track_width this time and set the minimum and maximum values to some reasonable values 1.7→2.7. This gives the optimizer a wide range to work with and will hopefully end up with a much improved match.

If we now just click start the optimizer will use the Trust Region Framework method and arrive at a more optimized result.





Task 3:

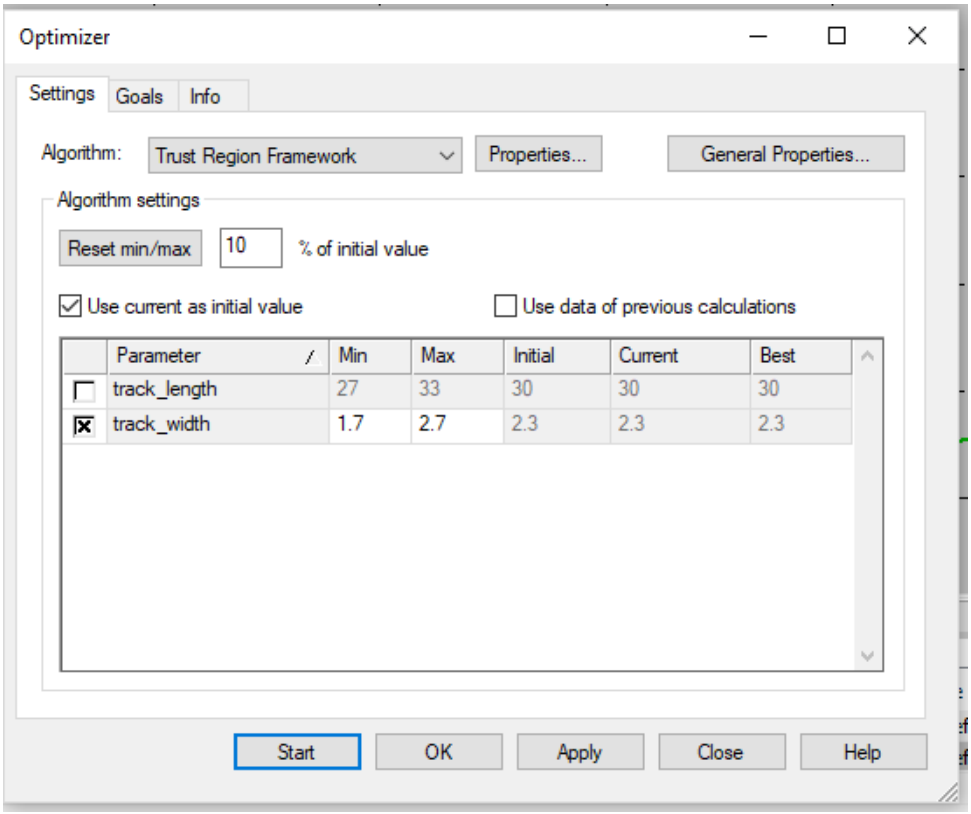
- What is the optimized microstrip width w determined by the simulation?
- The microstrip width w and impedance Z_0 follows the following relationship;

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} ln(\frac{5.98h}{0.8w + T}) \tag{20}$$

where $\varepsilon_r = 4.3$, thickness $T = 35\mu m$, and $h = 1.2mm$. Calculate the microstrip width w that will result in an Z_0 of 50 Ω

2.2mm

- Compare the calculated value against the simulated value. Discuss your answer.

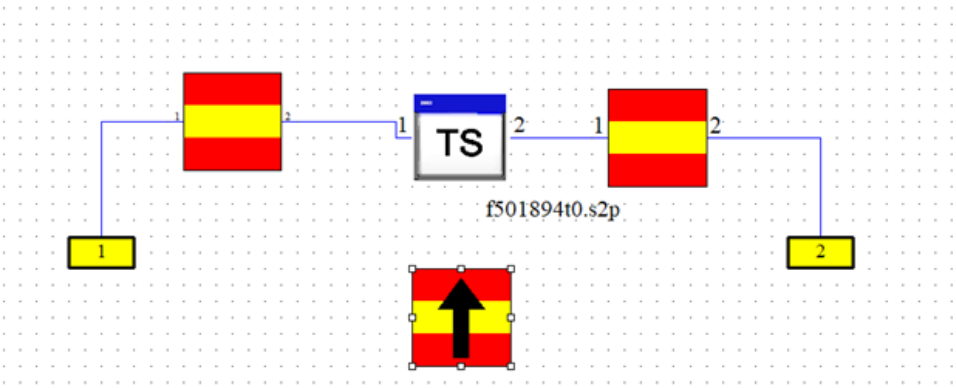


Stage 2: Implementing the power amplifier

We are now going to take that initial schematic and now include the s-parameter details of our op-amp. Firstly, we are going to delete the connection between our stripline and port 2. Then drag a new microstrip track into the schematic and connect it to port 2. Well set it up similarly to the first track with two variables, for the length lets set that as track_length2 a new variable and give it a value of 30 for now. Set the width to track width the same variable as the original track.

Now we want to drag our op-amp details as a s2p file/block into the middle. Use the file provided by your demonstrator and drag it into your schematic into between the two tracks. Join each side to a the open end of the track.

Your schematic should now look something like this. Lets update our simulation to see what changes this has had on our port impedances.

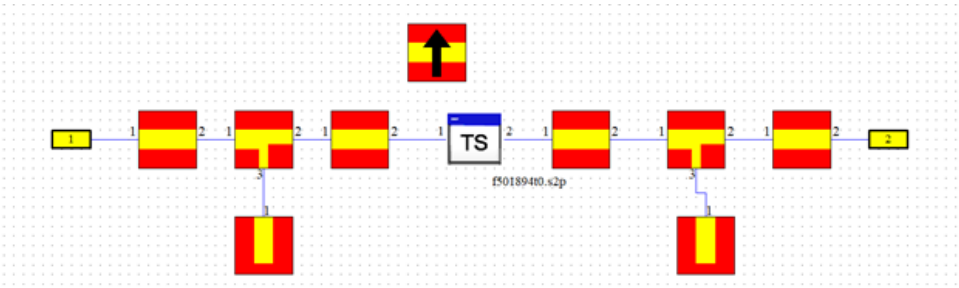


Task 4:

- What are the simulated S_{11} and S_{22} values?
- What is the amplifier gain?
- Are your S-parameters measured at the connector or at the power amplifier? Where do you want the S-parameters to be measured from for your calculations?

Stage 3: Power amplifier with Stub matching

Lets now add in some T-junctions and some open tuning stubs to get a better match for our op-amp.



Your overall circuit should look like the above now. With two t-junctions, an input stub and an output stub and some extra track lengths leading into the op-amp and out of the op-amp.

When inputting these into your circuit use the below variable parameters so we can tune the stubs to suit.

Parameter List

Name	Expression	Value	Description	Type
track_length	30	30		Undefined
track_width	2.3	2.3		Undefined
track_length2	30	30		Undefined
l_in	25	25		Undefined
stub_in	21	21		Undefined
l_out	1	1		Undefined
stub_out	7.5	7.5		Undefined

Where l_in and l_out are the lengths of the tracks into and out of the op-amp and the stub_in and stub_out matching their respective stub lengths. All tracks should have the same width of 2.3 still.

Update your task and see how the port impedances look. Optimise the stub lengths to get a port impedance of 50 Ω.

Task 5:

- What are the simulated values for d and l (as shown in Figure 4) at the input and the output of the power amplifier. Compare with the values calculated in Task 2.
- What are the new simulated S_{11} and S_{22} values?
- What is the new amplifier gain (S_{21})? Has your gain maximised? What Gain do you expect?

Task 6 (optional): Make a 3D version of your schematic and assembly to explore the effects the tuning has on 2D and 3D farfields or E and H fields of your circuit.

References

[1] Pozar, D.M., Microwave Engineering John Wiley & Sons Inc. 1998
[2] Schrader, D. Microstrip Circuit Analysis, Prentice Hall, 1995.