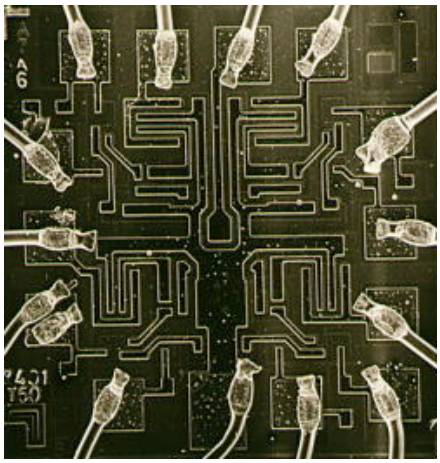
ELEN90062 High Speed Electronics

Workshop 1 - Logic Gates

Logic gate architecture, transient behaviour, and design tradeoffs

Logic gates are ubiquitous in modern electronics, finding application in mobile phones, computers, televisions, MP3 players, microwave ovens, and so on. Typical microprocessors employed in these applications consist of interconnections of millions of logic gates. Understanding the transient behaviour of logic gates, along with the various tradeoffs associated with their design, is essential in realizing high performance digital systems.



(a) An SEM image of a logic gate. `sciencephoto.com`

(b) A 74HC04 high speed CMOS inverter IC. `philips.com`

This workshop investigates the logic function implementation, transient behaviour and power dissipation of various logic gate circuits. Several circuit capture and simulation exercises provide the basis of this investigation. The software package LTspice will be used. The following specific issues will be considered:

1) Reduction of switching time via the use of Schottky clamped transistors;
2) The transient behaviour and power dissipation of a TTL vs LSTTL circuit;
3) Comparison with an ECL circuit;
4) Comparison with a CMOS circuit; and
5) Comparison with a number of BiCMOS circuits.

The main steps involved in the analysis of each logic gate circuit typically involve (i) the schematic capture of each circuit; (ii) simulation using a variety of compatible input signals; (iii) a DC sweep; (iv) approximation of power consumption; and (v) interpretation of results.

1 The Schottky clamp

Schottky clamps can be used to improve the switching speed of BJTs by limiting the forward bias of the BC junction. In order to demonstrate this improvement, an LTspice simulation will be constructed.

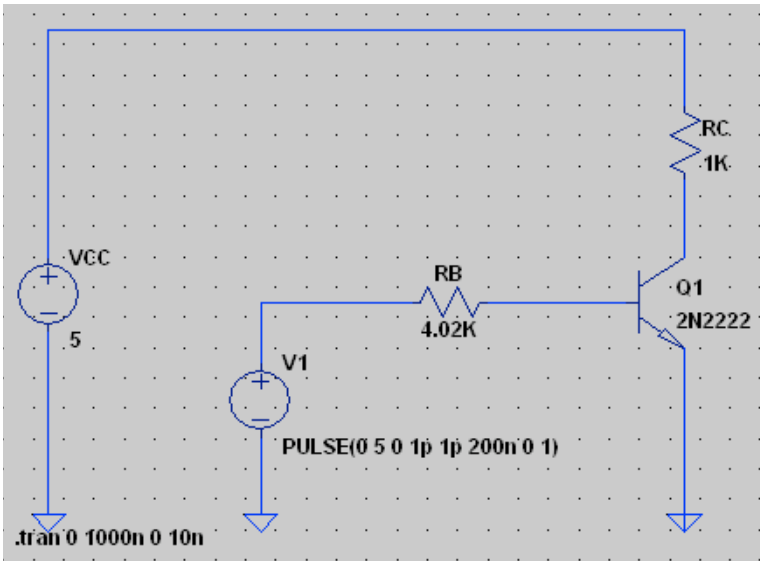


Figure 1: Unclamped resistor-transistor logic gate.

Tasks

1.1. Start the LTspice software from the Start Menu.

1.2. Create a schematic by selecting File > New Schematic. Save this schematic with a useful name, for example, Clamp.

> IMPORTANT: Make sure that you do **not** save your files on the local hard disk, as these files will automatically be erased when you log out!! Instead, save your files on the network drive (i.e. in your allocated account).

1.3. Construct the unclamped common emitter BJT amplifier circuit shown in Figure 1. Note that the resistor values, supply voltage and transistor used must be as indicated in the schematic.

1.4. In order to simulate the transient behaviour of this circuit, you will first to create a simulation profile. To do this, select Simulate > Edit Simulation Cmd. The pop-up window requires that you select some simulation properties. In this case, a guide would be to select the Transient tab, and enter

Stop Time : 1000 n
Maximum Timestep : 100 p

To simulate, click on the run symbol, or select Simulate > Run.

Using a voltage input pulse of amplitude 5 V and duration 200 ns, determine via simulation each of the following time delays: (1) Turn-on delay, (2) Fall time, (3) Charge storage delay, (4) Rise time.

1.5. Repeat the above measurement of the charge storage delay for input pulse durations of 300 ns, 400 ns and 500 ns. What is your estimate of the charge storage delay in light of these measurements? Explain why the shorter input pulse lengths give rise to different charge storage delay measurements.

1.6. Using your revised measurement of the charge storage delay, determine an approximation for the charge recovery time constant τ_X. For this you will need to know some steady state base currents — see the lecture notes for details. Also, you will need to know the forward active mode current gain for the Q2N2222. Assume that this is 160. (By the way, LTspice can be used to determine this current gain. Any ideas how? HINT: DC sweep.)

1.7. Replace the series base resistor with double the resistance. Repeat the above measurement of the charge storage delay. Repeat the computation of the charge recovery time constant τ_X. Is this value the same as you obtained earlier? Explain.

1.8. Restore the original series base resistance of 4 kΩ. The objective here will be to add a specific Schottky clamping diode across the base-collector junction of the BJT. A model for this diode will need to be specified. To this end, first add a generic Schottky diode across the base collector junction of the BJT. Make sure that the diode is connected in the correct direction so as to limit the forward biased BC junction voltage. Edit the diode label on the schematic, changing D to Dmbd101. Next, in the directory in which you have saved your schematic, create a text file named MBD101.lib. Copy the following text into this file (and save it):

```
.MODEL Dmbd101 d
+IS=1e-07 RS=2.51244 N=1.71158 EG=0.63401
+XTI=4 BV=1000 IBV=0.0001 CJO=9.20838e-13
+VJ=1.5 M=0.2 FC=0.5 TT=0
+KF=0 AF=1
```

Back in LTspice, add a SPICE directive to your schematic by selecting Edit > Text. Select the SPICE directive option, and enter .inc MBD101.lib in the text window provided. Select any location on your schematic to add this directive (and click the mouse button to complete the operation).

Repeat your determination of the time delays (but not the time constant) from 1.5 above. Comment on how these time delays compare with the unclamped circuit.

1.9. By measuring the Schottky diode current and the collector current, summarize the role of the Schottky diode in the circuit when the BJT nears saturation.

2 Transistor Transistor Logic (TTL) and Low Power Schottky TTL (LSTTL)

TTL is a "very old" logic family that utilizes bipolar technology. It is slow and consumes plenty of power. A faster, lower power variant of TTL is based on the Schottky clamping technique examined in the preceding section.This variant is called LSTTL. In this section, a circuit for a TTL inverter will be analyzed via simulation and compared with the corresponding LSTTL circuit. In particular, the transient response and power consumption will be of interest.

Tasks

2.1. Close your schematic from Section 1 and create a new one called TTL inverter. Construct the TTL circuit shown in Figure 2, being careful to use the resistor values provided. Note that here we have substituted the Q2N2222 for the actual BJTs used in a TTL inverter circuit. Resistor RL is used to model a load. The input pulse voltage should be 0 - 5 V with duration 500 ns.

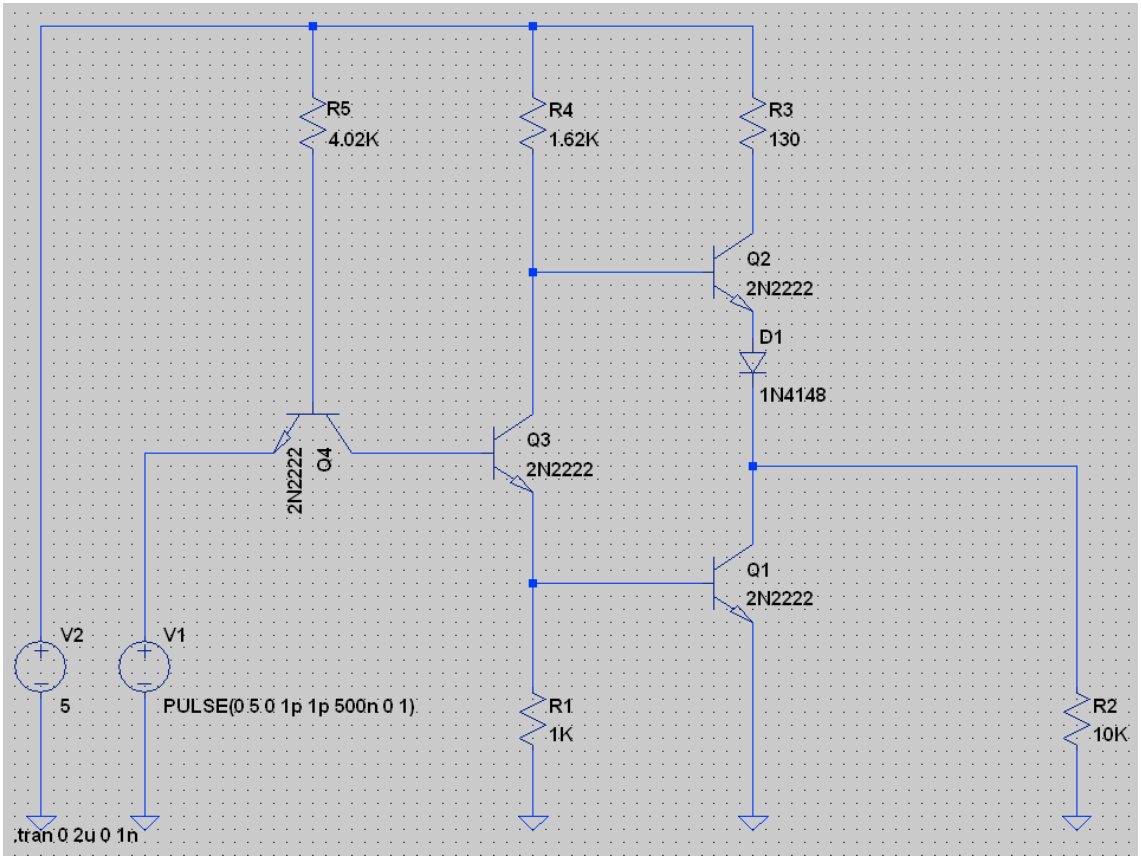


Figure 2: TTL inverter logic gate.

2.2. Create a new transient simulation profile for this schematic. Enter a stop time of 2 us. Simulate the circuit to obtain a measure of the following times:

(i) The high-to-low (output) propagation time, denoted by t_{PHL};
(ii) The low-to-high propagation time, t_{PLH}.

Explain why the low-to-high propagation time dominates the switching speed in TTL circuits.

2.3. By examining the various BJT currents and voltages, determine the mode of operation (i.e. cutoff, forward active, reverse active or saturation) for each of the BJTs for the two input levels. Does this agree with theory? Also, explain the purpose of the diode D1 and determine when it is forward or reverse biased.

2.4. Plot the instantaneous power supplied via the supply rails. To do this, select the traces icon in the horizontal menu bar. Then, press Alt-[double click] to bring up the Expression Editor. Now type in the product of traces for the supply voltage and current. Determine the peak instantaneous power supplied via the supply rails over the duration of the input (i.e. over the 2 us). Assuming that the input is periodic with period 2 us, compute the approximate average power consumed by this circuit.

2.5. Save and close your TTL inverter schematic. Create a new schematic called "Schottky TTL Inverter". Construct the LSTTL circuit shown in Figure 4. Use the MBD101.lib library created in Section 1 to implement the Schottky diodes. As in the TTL case, measure the low-to-high and high-to-low output propagation delays t_{PLH} and t_{PHL}. Compare these propagation delays with those obtained for the TTL case.

2.6. As in the TTL case, measure the instantaneous power supplied by the supply rails over the course of the input pulse. Assuming that the input is periodic with period 2 us, compute the approximate average power consumed by this circuit. Compare the power dissipation of the LSTTL inverter with the TTL inverter considered earlier. In view of your conclusions, what can you say about the performance of LSTTL compared with TTL circuits?

2.7. All of the BJTs in the LSTTL inverter circuit are Schottky transistors with the exception of Q5 (see the Figure 4). With the aid of appropriate measurements, explain why this is the case. Does this conform with the theory?

2.8. Consider the sub-circuit shown of Figure 4 shown in Figure 3. Connect a single DC voltage source from the unconnected wires to ground. By conducting a DC input voltage sweep and measuring the corresponding current, show that this circuit performs the role of an active pull-down. Explain what this means in terms of resistance versus voltage, and how this helps in the switching of the output stage BJT Q2.

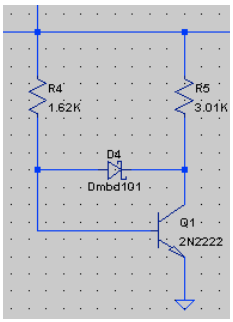


Figure 3: LSTTL inverter active pull-down subcircuit.

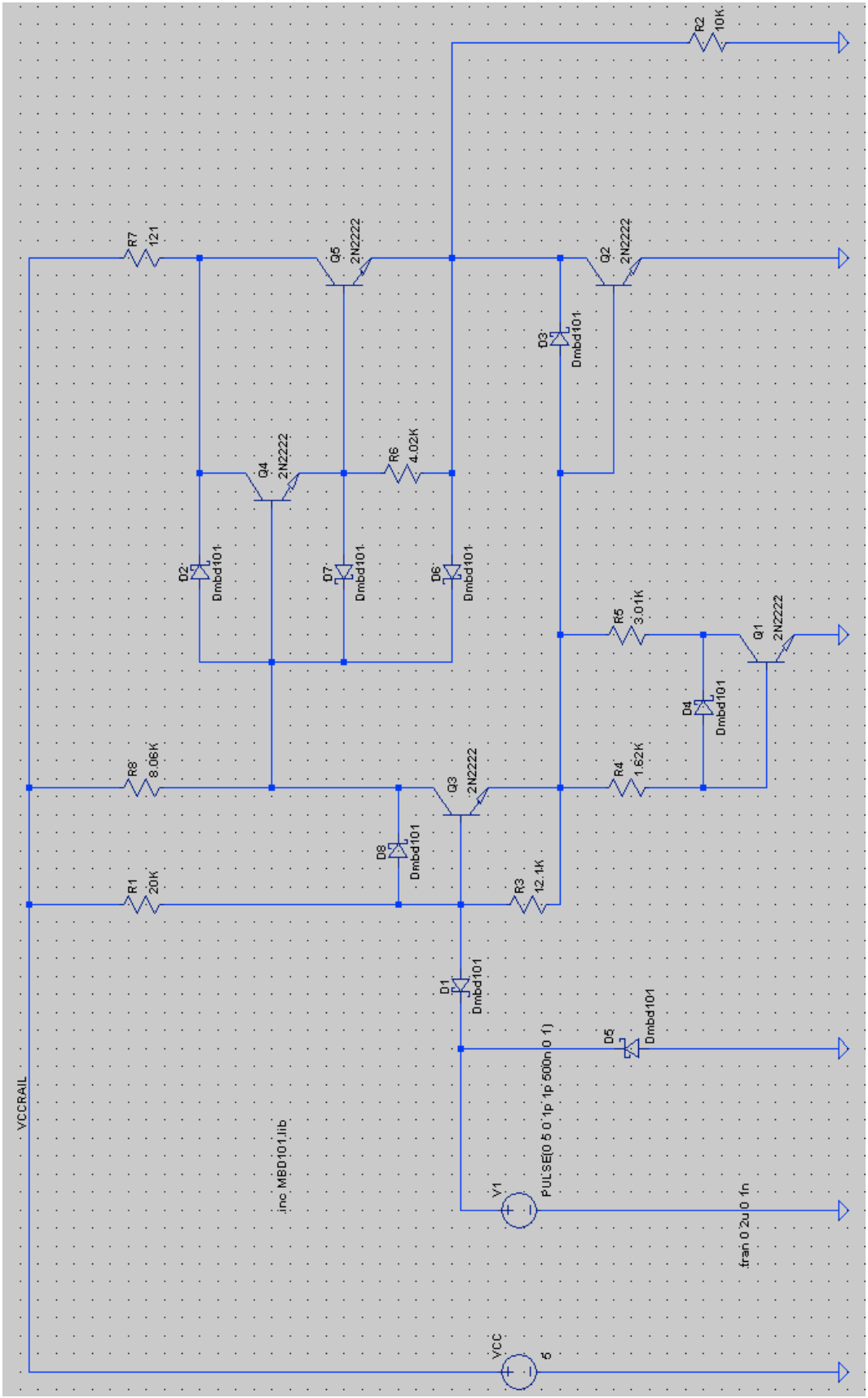


Figure 4: LSTTL inverter logic gate.

3 Emitted coupled logic (ECL)

Emitter coupled logic (ECL) is another logic gate technology based on BJTs. Common ECL families include 10KH, 100KH and ECLinPS Plus. ECL is fast. For example, the ECLinPS Plus family exhibits typical propagation delays of 200 ps, with switching speeds of up to more than 3 GHz! (Compare that with LSTTL, which struggles at 40 MHz.)

In this section, the behaviour of a common ECL structure is examined by simulation. In particular, transient response and power dissipation will be considered.

(Note that an added peculiarity of ECL is the supply rail setup. Using positive supply rails in ECL is given the acronym PECL, while negative supply rails yield NECL. In fact, the principle of operation of the two is identical.)

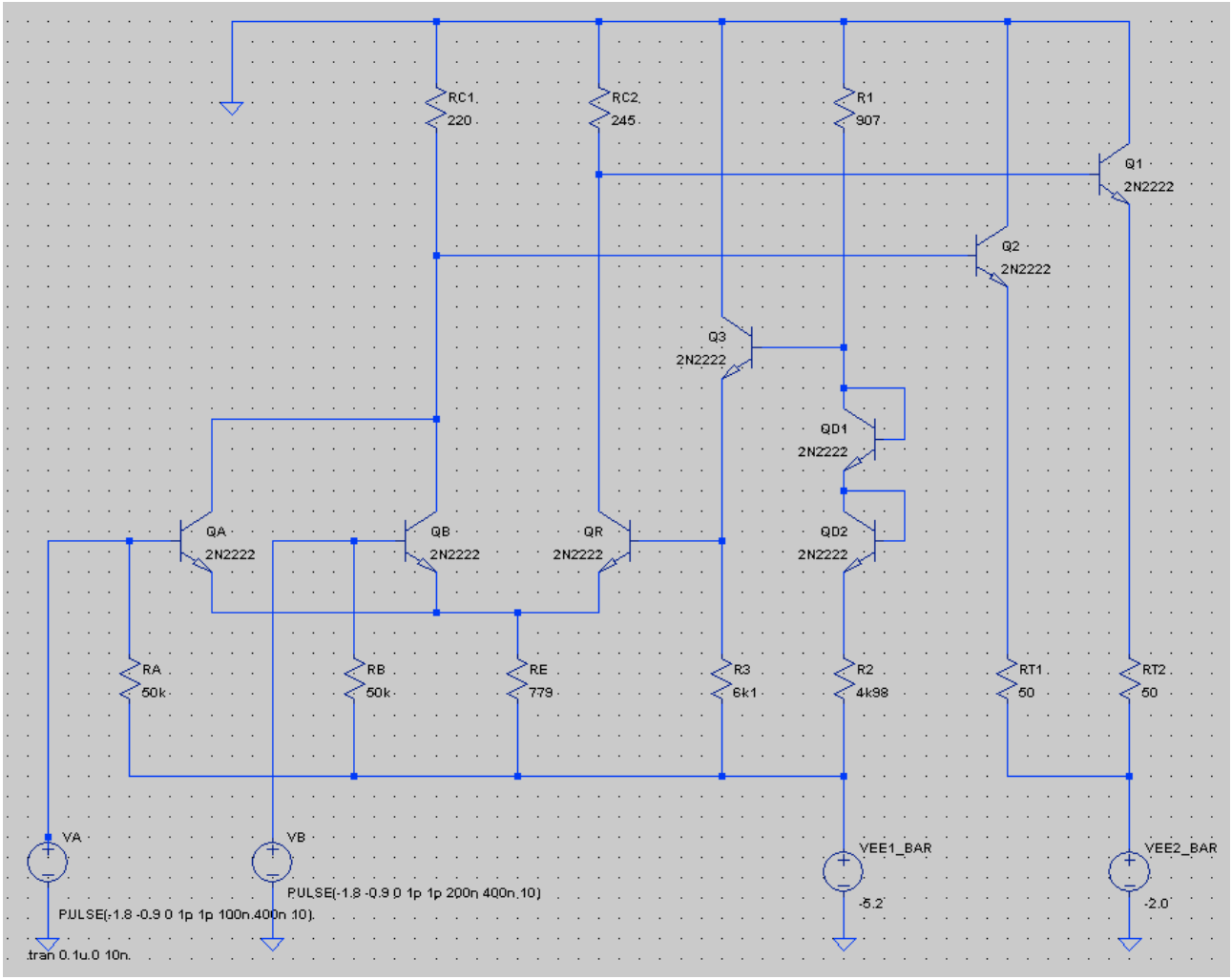


Figure 5: ECL logic gate and load.

Tasks

3.1. Construct the 10K ECL circuit shown in Figure 5.

(i) Is this a NECL or PECL logic gate circuit? Explain.

(ii) Are the two resistors RT1 and RT2 typically part of the logic gate or external to it? (HINT: Termination.)
(iii) Why might ECL gates be useful for driving terminated transmission lines?
(iv) What is the purpose of the sub-circuit consisting of components QD1, QD2 and R2 shown in Figure 6 (see also Figure 5)? Explain.

3.2. By applying the appropriate logic signals to the two inputs VA and VB and examining the outputs corresponding to the emitter voltages of Q1 and Q2, determine the logic function of this gate. Make sure that you examine both outputs. (You will need to look up a 10K ECL datasheet to find out what voltage levels are appropriate.)

3.3. Remove source VB and connect this input voltage to VA. (This will be the case for the remainder of this section.) Using a DC sweep, determine the voltage transfer characteristic from input VA to the outputs defined by the emitter voltages of Q1 and Q2. From this voltage transfer characteristic, determine the following:

(i) The input voltage for which the two output voltages are equal;
(ii) The high / low output / input voltages (denoted V_{OH}, V_{OL}, V_{IH}, V_{IL});
(iii) The high / low noise margins (denoted NM_{H} and NM_{L}).

How do the obtained values compare to that specified in the datasheet? What factors or assumptions may contribute to any differences you observe?

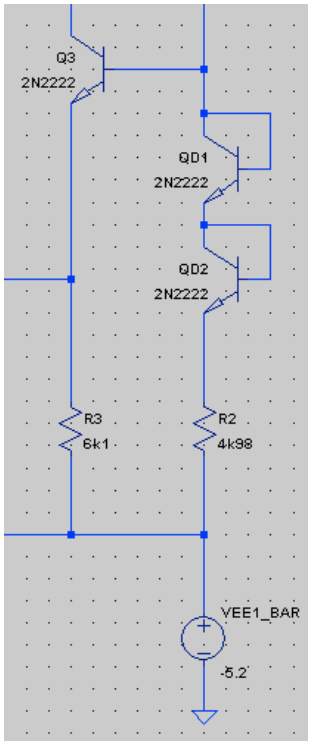


Figure 6: ECL subcircuit.

3.4. By conducting a transient analysis, determine the high-to-low and low-to-high output propagation times t_{PHL} and t_{PLH}. Use a pulse input which remains high for 500 ns. How do these propagation times compare to the TTL and LSTTL cases? What is the essential feature of ECL operation that gives rise to this switching performance?

3.5. Determine the instantaneous power delivered by the supply rails in this circuit. Assuming that the input is periodic with period 2 us, compute the approximate average power consumed by this circuit. How does this compare with your earlier measurements for the TTL and LSTTL families?

3.6. Do you expect the average power dissipation to be frequency dependent? Explain.

4 CMOS

CMOS circuits are by far the most commonly used in the implementation of logic gates. This section investigates some of the transient properties of a CMOS circuit.

Tasks

4.1. Construct the circuit shown in Figure 7 for a cascade of CMOS inverters. Note that the capacitors C1 and C2 are used to model the parasitic capacitance of the interconnects seen by the output of each gate.

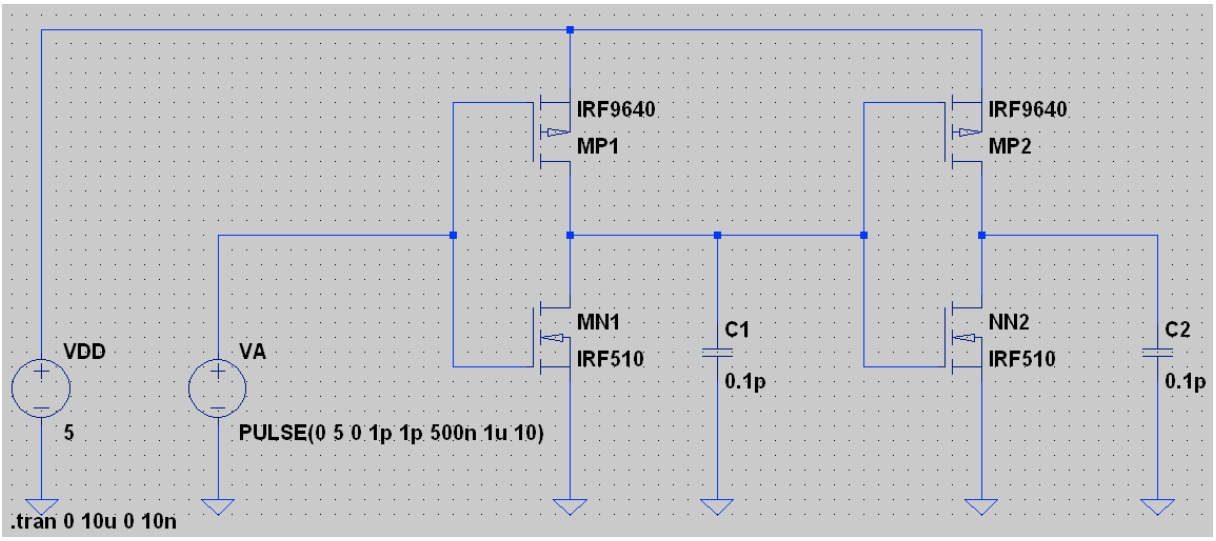


Figure 7: CMOS circuit.

4.2. By conducting a transient analysis, determine the high-to-low and low-to-high output propagation times t_{PHL} and t_{PLH}. Use a pulse input which remains high for 500 nS. How do these propagation times compare to the TTL, LSTTL and ECL cases?

4.3. Measure the current flowing from the output of the first gate. What is the steady state value of this current (i.e. between transients)? Explain why this is the case.

4.4. Determine the instantaneous power delivered by the supply rails in this circuit. Indicate where during the transient power is dissipated and explain why. How does the power dissipation of CMOS compare with TTL, LSTTL and ECL?

4.5. IRF MOSFETs as used in this experiment are typically used for power switching applications. How would your results be different if signal MOSFETs were used instead? (HINT: propagations delays, power dissipation, etc.)

5 BiCMOS

BiCMOS describes a logic gate technology that utilizes both bipolar and CMOS aspects in gate circuit design. In particular, BiCMOS combines the low power, high density and high input impedance of CMOS with the high current drive of bipolar technology. A number of BiCMOS logic gates are considered here, all of which utilize the same single CMOS logic gate to implement a particular logic function. This CMOS logic gate is cascaded with a variety of BJT/ CMOS output stages to implement current gain and other features at the output. Specific models for the transistors required will be created.

5.1 CMOS logic function

A schematic of the CMOS logic function to be implemented in the various BiCMOS logic gates of interest is shown in Figure 8. The first objective is to capture this schematic, determine the CMOS logic function by simulation, and to understand the ability of CMOS logic gates to drive capacitive loads.

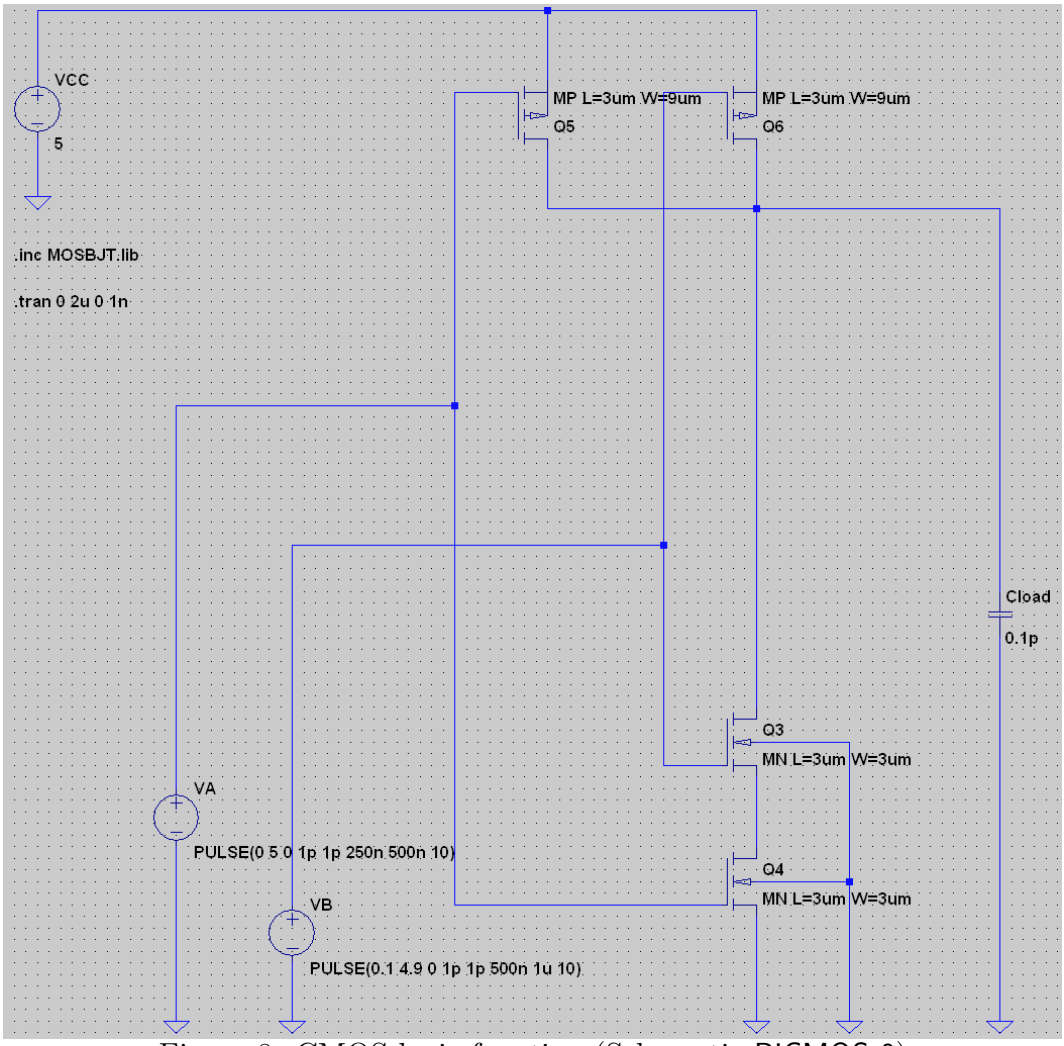


Figure 8: CMOS logic function (Schematic BiCMOS-0).

Tasks

5.1.1. Create a new schematic called BiCMOS-0. Save this (empty) schematic to your working directory. Following the same steps as per Section 1, create a new text file called MOS-BJT.lib In the same directory as your saved schematic file above. In that file, define four transistor models via the following SPICE directives:

```
.MODEL MN NMOS (level=3 vto=.7 kp=4.e-5 gamma=1.1 phi=.6
+ rd=40 rs=40 pb=.7 cgso=3.e-10 cgdo=3.e-10 cgbo=5.e-10
+ rsh=25 cj=.00044 mj=.5 mjsw=.3 js=1.e-5 tox=5.e-8 nsub=1.7e16
+ nss=0 nfs=0 tpg=1 xj=6.e-7 ld=3.5e-7 uo=755 vmax=100000
+ theta=.11 eta=.05 kappa=1)
.MODEL MP PMOS (level=3 vto=-.8 kp=1.2e-5 gamma=.6 phi=.6
+ rd=100 rs=100 pb=.6 cgso=2.5e-10 cgdo=2.5e-10 cgbo=5.e-10
+ rsh=25 cj=.00044 mj=.5 mjsw=.3 js=1.e-5 tox=5.e-8 nsub=5.e15
+ nss=0 nfs=0 tpg=1 xj=5.e-7 ld=2.5e-7 uo=250 vmax=70000
+ theta=.13 eta=.3 kappa=1)
.MODEL QN NPN (Is=10fA Bf=100 Br=1 Tf=1.0ns Cje=1pF Cjc=1.5pF
Va=100)
.MODEL QP PNP (Is=10fA Bf=100 Br=1 Tf=1.0ns Cje=1pF Cjc=1.5pF
Va=100)
```

Make sure you save this file in the same location as your schematic BiCMOS-0 created above. In order to include these models in your schematic, add a SPICE directive to your schematic by selecting Edit > Text. Select the SPICE directive option, and enter .inc MOSBJT.lib in the text window provided. Select any location on your schematic to add this directive (and click the mouse button to complete the operation). Using these new models, construct the CMOS logic gate circuit shown in Figure 8. In specifying the model to be used for each MOSFET, ensure that you include the dimensions provided, as these are employed by SPICE in the simulation. In particular, the models for the n-channel and p-channel MOSFETs should be recorded as "MN L=3um W=3um" and "MP L=3um W=9um" respectively, without the quotes. (Note that these dimensions refer to the gate length and width for each MOSFET, and hence are vital to determining capacitance and resistance of each device.)

5.1.2. Simulate this CMOS logic function for a period of $2\,\mu$s. Plot the input and output voltages as a function of time. By inspection of these plots, determine the CMOS logic function implemented.

5.1.3. Determine the high-to-low and low-to-high output propagation delays t_{PHL} and t_{PLH} for the following load capacitances:

(i) Cload $= 0.1\,$pF.

(ii) Cload $= 1\,$pF.

(iii) Cload $= 10\,$pF.

What can you conclude about the ability of this circuit to drive difference capacitive loads?

5.2 BiCMOS logic gate with push-pull output stage

Using the CMOS logic function of Figure 8, a BiCMOS gate may be constructed by cascading a BJT push-pull output stage at the output, as shown in Figure 9.

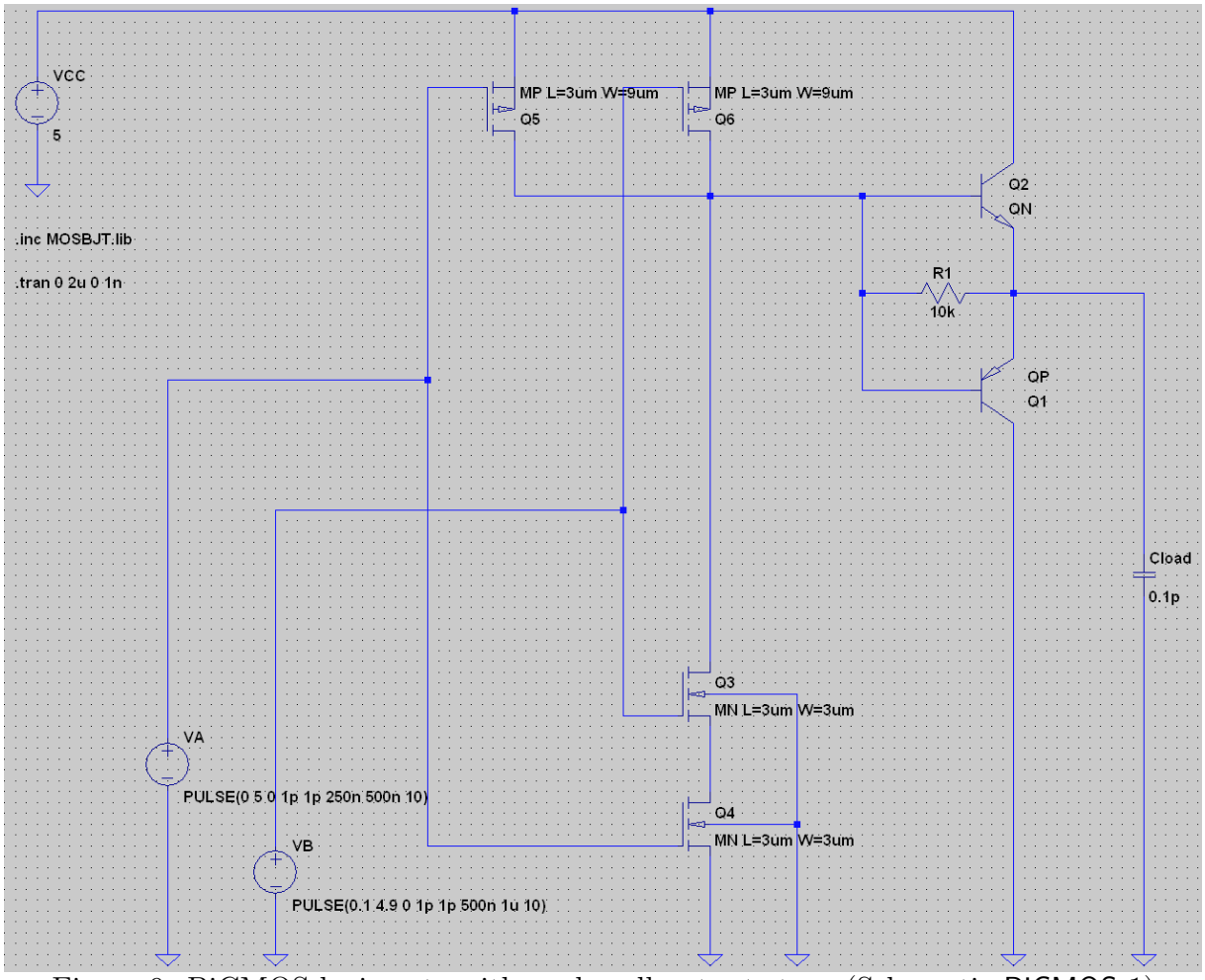


Figure 9: BiCMOS logic gate with push-pull output stage (Schematic BiCMOS-1).

5.2.1. With your previous schematic saved, create a copy by selecting File > Save As and using the new schematic name BiCMOS-1. Modify your schematic by adding the BJT output stage as shown in Figure 9. Confirm that the logic function of this BiCMOS gate is retained from the CMOS logic function of Figure 8.

5.2.2. Repeat Task 5.1.3 above and compare the performance of the logic gates of Figures 8 and 9 based on their ability to drive capacitive loads. Explain any performance improvement observed, and what tradeoffs (if any) have been made in establishing this improvement.

5.2.3. What is the purpose of resistor R1 in the BiCMOS logic gate of Figure 9? Justify your answer by observing the effect of varying its value. (HINT: try observing the steady state HIGH and LOW output voltages with and without resistor R1.)

5.3 BiCMOS logic gate with push-pull output stage and auxiliary inverters

Based on the schematic of Figure 9, a revised BiCMOS logic gate design that does not employ resistor R1 is illustrated in Figure 10.

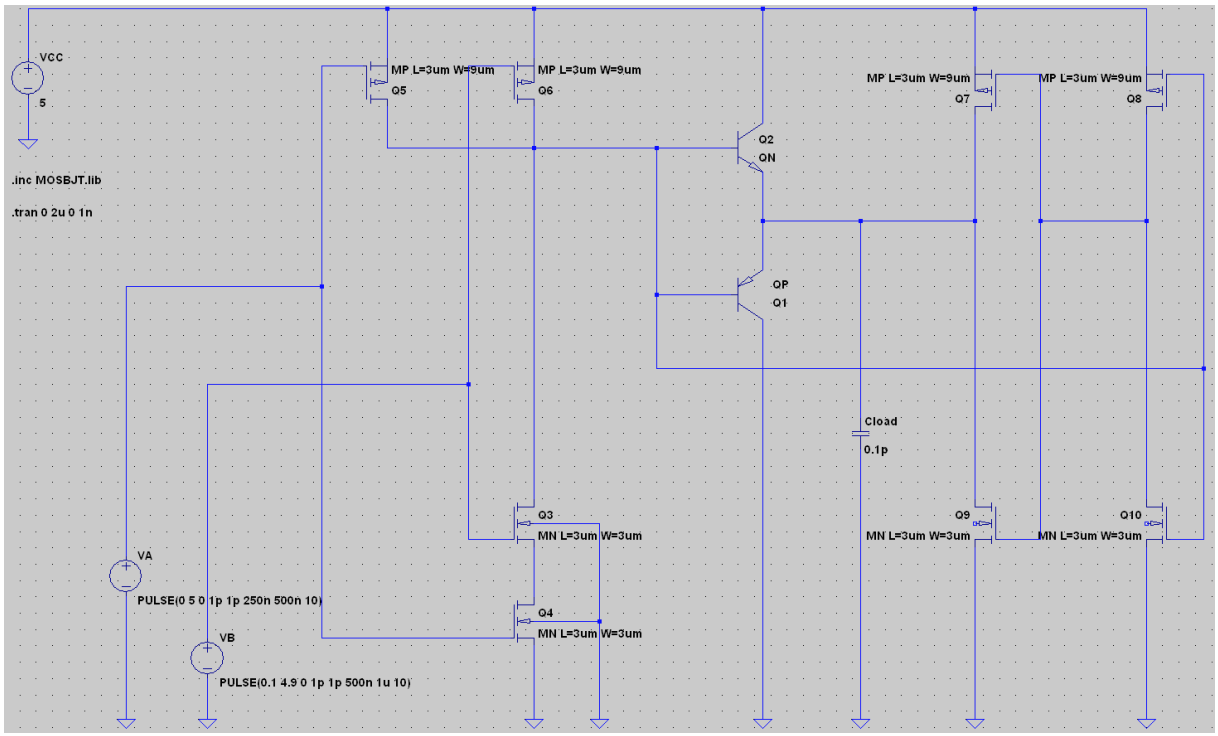


Figure 10: BiCMOS logic gate with push-pull output stage and auxiliary inverters (Schematic BiCMOS-2).

5.3.1 Again with your previous schematic saved, create a copy by selecting File > Save As and using the new schematic name BiCMOS-2. Modify your schematic by modifying the output stage as shown in Figure 10. Plot the input and output voltages for the inputs specified in the schematic. Confirm that the logic function this BiCMOS gate is retained from the original CMOS logic function of Figure 8.

5.3.2 Compare the steady state HIGH and LOW output voltages generated by the BiCMOS logic gates of Figures 8, 9 and 10. Determine the purpose of the auxiliary CMOS inverters implemented by Q7 – Q10 in Figure 10.

5.3.3 Determine the instantaneous power delivered by the supply rails in this circuit. How does the power dissipation of this BiCMOS logic gate compare with the CMOS logic function of Figure 8?

5.3.4 Do you expect the average power dissipation of this BiCMOS logic gate to be frequency dependent? By varying the period of the input waveforms, investigate this dependence.

6 Summary

TTL, LSTTL, ECL, CMOS and BiCMOS logic families have different electrical characteristics and offer a range of advantages and disadvantages. The following tasks involve drawing conclusions on the basis of the experiments undertaken. Make sure that you justify your answers.

Tasks

6.1. On the basis of the studies conducted, indicate which of the families considered is best suited to low power applications.

6.2. Which families are suited to high switching speeds?

6.3. Which families are suited to driving low impedance loads?

6.4. Is there any apparent tradeoff between switching speed and current drive? Which families are designed for both?

7 Report

Your report is a important part of this experiment, as it documents your results and your conclusions. The report should include (but is not limited to) the following:

1. Any preparation work, for example circuit analysis, calculations, etc.
2. Documentation of each of the tasks completed.
3. Answers to all questions in each of the above tasks.