BG96-QuecOpen

Hardware Design

LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2017-10-20	Lyndon LIU	Initial
1.1	2018-02-05	Lyndon LIU	1. Updated the key features of BG96-QuecOpen module in Table 2. 2. Updated the definition of main UART pins in Figure 2. 3. Updated the pin description in Table 4. 4. Updated the multiplexing pins in Table 5. 5. Updated the description of UART interfaces in Chapter 3.10. 6. Updated the description of I2C interfaces in Chapter 3.11. 7. Updated the description of SPI interfaces in Chapter 3.12. 8. Updated the description of ADC function interfaces in Chapter 3.13. 9. Updated the module bottom dimensions in figure 33. 10. Updated the recommended footprint (Top View) in figure 34. 11. Updated the storage information in Chapter 8.1.
1.2	2018-04-04	Lyndon LIU	1. Updated the description of UART interfaces in Table 2 and Chapter 10. 2. Updated pin definition of the (U)SIM interface in Table 11. 3. Updated timing of the turning on module in Figure 8. 4. Updated timing of the turning off module in Figure 9. 5. Updated GNSS performance in Table 23. 6. Updated BG96-QuecOpen Current Consumption in Table 38. 7. Updated GNSS Current Consumption of BG96-QuecOpen Module in Table 39.

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1 Introduction

This document defines the BG96-QuecOpen module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of BG96-QuecOpen module. Associated with application note and user guide, customers can use BG96-QuecOpen module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating BG96-QuecOpen module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals,clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.
	Cellular terminals or mobiles operatingover radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid USIM/SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

QuecOpen™ is an application solution where the module acts as a main processor. With the development of communication technology and the ever-changing market demands, more and more customers have realized the advantages of QuecOpen™ solution. Especially, its advantage in reducing the product cost is greatly valued by customers. With QuecOpen™ solution, development flow for wireless application and hardware design will be simplified. Main features of QuecOpen™ solution are listed below:

- Simplifies the development of embedded applications, and shortens product development cycle
- Simplifies circuit design, and reduces product cost
- Decreases the size of terminal products
- Reduces power consumption
- Supports remote upgrade of firmware wirelessly
- Improves products' cost-performance ratio, and enhances products' competitiveness

BG96-QuecOpen module is a baseband processor platform based on ARM Cortex A7. The maximum dominant frequency is up to 1.3GHz. Customers can use BG96-QuecOpen modules as the basis for development of QuecOpen™ applications.

BG96-QuecOpen is an embedded IoT (LTE Cat M1, LTE Cat NB1 and EGPRS) wireless communication module. It provides data connectivity on LTE-TDD/LTE-FDD/GPRS/EDGE networks, and supports half-duplex operation in LTE networks. It also provides GNSS[1)] to meet customers' specific application demands. The following table shows the frequency bands of BG96-QuecOpen module.

Table 1: Frequency Bands of BG96-QuecOpen Module

Mode	Description
LTE Bands	LTE-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B26/B28 LTE-TDD: B39 (for Cat M1 only)
GSM [2)]	GSM850/EGSM900/DCS1800/PCS1900
GNSS [1)]	GPS, GLONASS, BeiDou/Compass, Galileo, QZSS

NOTES

1. [1] GNSS function is optional.
2. [2] BG96 GSM only supports Packet Switch.

With a compact profile of 22.5mm × 26.5mm × 2.3mm, BG96-QuecOpen can meet almost all requirements for M2M applications such as automotive, smart metering, tracking system, wireless POS, etc.

BG96-QuecOpen is an SMD type module which can be embedded into applications through its 102 LGA pads.

2.2. Key Features

The following table describes the detailed features of BG96-QuecOpen module.

Table 2: Key Features of BG96-QuecOpen Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 3 (23dBm±2dB) for LTE-FDD bands Class 3 (23dBm±2dB) for LTE-TDD bands Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for EGSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for PCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for PCS1900 8-PSK
LTE Features	Support LTE Cat M1 and LTE Cat NB1 Support 1.4MHz RF bandwidth for LTE Cat M1 Support 200KHz RF bandwidth for LTE Cat NB1 Support SISO in DL direction Cat M1: Max. 300kbps (DL)/375kbps (UL) Cat NB1: Max. 32kbps (DL)/70kbps (UL)
GSM Features	**GPRS:** Support GPRS multi-slot class 33 (33 by default) Coding scheme: CS-1, CS-2, CS-3 and CS-4

	Max. 107Kbps (DL), Max. 85.6Kbps (UL) **EDGE:** Support EDGE multi-slot class 33 (33 by default) Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) Downlink coding schemes: CS 1-4 and MCS 1-9 Uplink coding schemes: CS 1-4 and MCS 1-9 Max. 296Kbps (DL), Max. 236.8Kbps (UL)
Internet Protocol Features	Support TCP/PPP/UDP/IP/PING/NITZ/SSL/TLS/HTTP(S)/FILE/MQTT protocols Support the protocols PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) usually used for PPP connections
(U)SIM Interface	Support USIM/SIM card: 1.8V, 3.0V
USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NEMA output, software debugging and firmware upgrade Support USB serial drivers for Windows XP, Windows Vista, Windows 7, Windows 8/8.1, Windows 10, Windows CE 5.0/6.0/7.0, Linux 2.6/3.x/4.1, Android 4.x/5.x/6.x/7.x
I2C Interfaces	Support two I2C interfaces Multi-master is not supported
SPI Interfaces	Support two SPI interfaces for master mode only Maximum clock frequency rate: 50MHz
UART Interfaces	**Main UART:** Used for AT command communication **UART1/UART2/UART3:** Used for communication and data transmission with peripherals
Network Indication	One NETLIGHT pin for network connectivity status indication
GNSS Features	Gen8C-Lite of Qualcomm Protocol: NMEA 0183
Antenna Interface	Including main antenna (ANT_MAIN) and GNSS antenna (ANT_GNSS) interfaces
Physical Characteristics	Size: (26.5±0.15)mm × (22.5±0.15)mm × (2.3±0.2)mm Weight: approx. 3.1g
Temperature Range	Operation temperature range: -35°C ~ +75°C [1)] Extended temperature range: -40°C ~ +85°C [2)] Storage temperature range: -40°C ~ +90°C
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within operation temperature range, the module is 3GPP compliant.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of BG96-QuecOpen and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

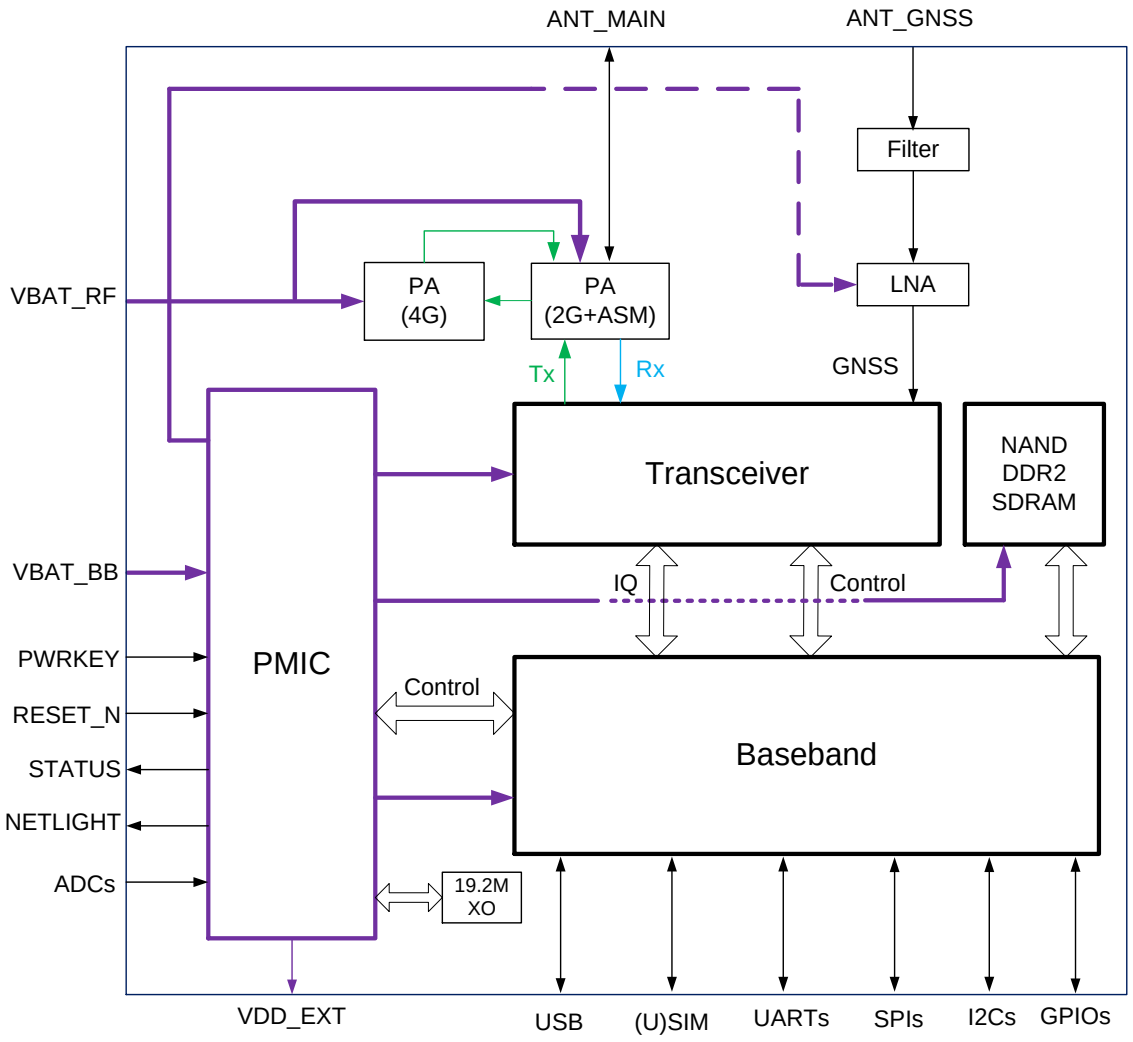


Figure 1: Functional Diagram

2.4. Evaluation Board

In order to help customers develop applications conveniently with BG96-QuecOpen module, Quectel supplies the evaluation board (EVB), USB data cable, antenna and other peripherals to control or test the module.

3 Application Interfaces

3.1. General Description

BG96-QuecOpen is equipped with 102-pin LGA pads. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- I2C interfaces
- SPI interfaces
- ADC interfaces
- Status indication interfaces
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of BG96-QuecOpen module.

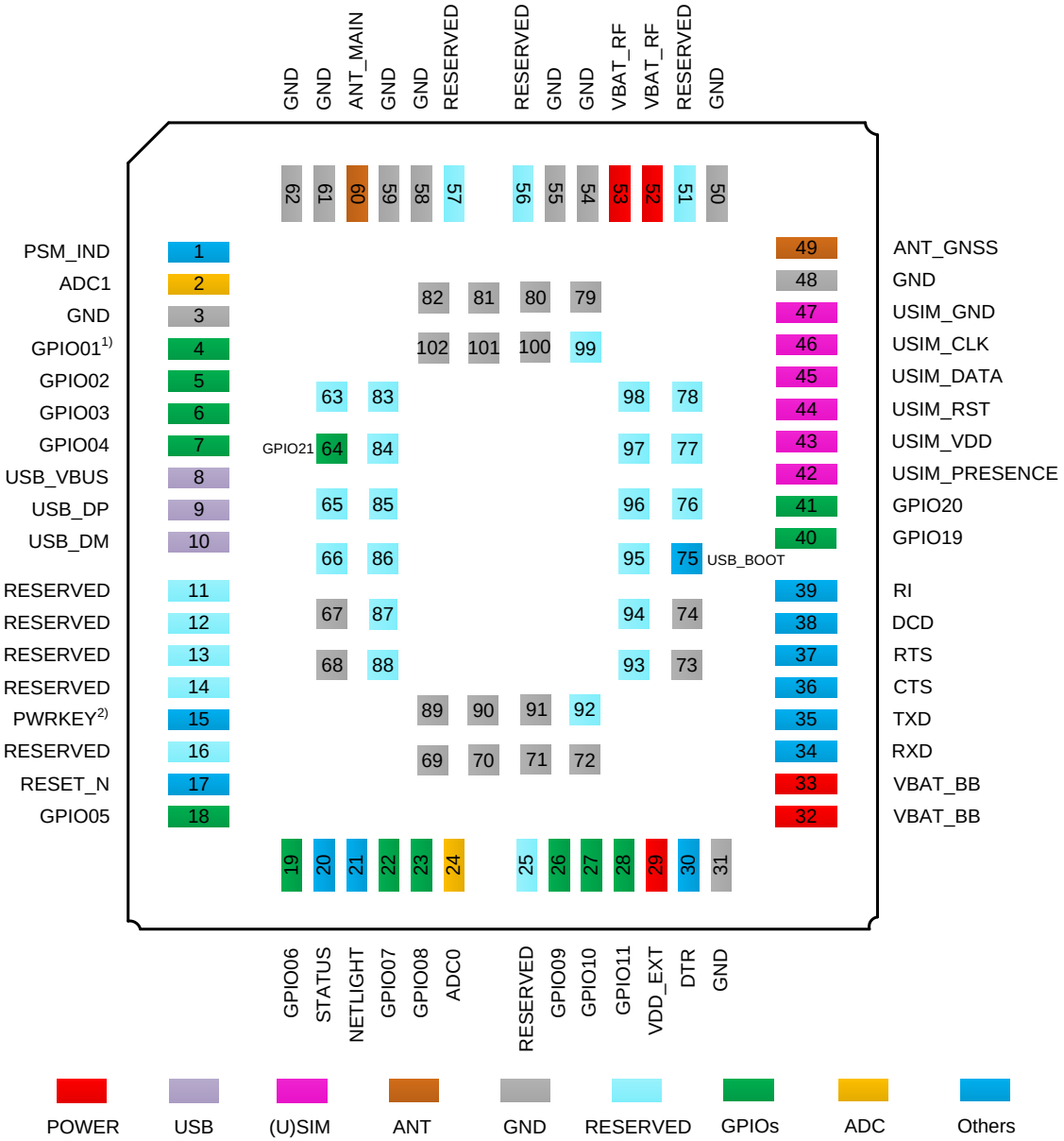


Figure 2: Pin Assignment (Top View)

NOTES

1. [1)] means this pin comes with BOOT function, and cannot be pulled up before startup.
2. [2)] PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
3. Keep all RESERVED pins and unused pins unconnected.

3.3. Pin Description

The following tables show the pin definition, alternate function and GPIO pull up/down resistance of BG96-QuecOpen module.

Table 3: I/O Parameters Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain
B	Bidirectional digital with CMOS input
BH	High-voltage tolerant bidirectional digital with CMOS input
PU	Pull up
PD	Pull down
H	High level
L	Low level

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for module's baseband part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	

VBAT_RF	52, 53	PI	Power supply for module's RF part	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	
VDD_EXT	29	PO	Provide 1.8V for external circuit	Vnorm=1.8V $I_O$max=50mA	Power supply for external GPIO's pull up circuits.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~102		Ground		

Turn on/off

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	15	DI	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
RESET_N	17	DI	Reset signal of the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	If unused, keep this pin open.

Status Indications

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PSM_IND	1	DO	Power saving mode indicator	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep this pin open.
STATUS	20	DO	Indicate the module's operation status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep this pin open.
NETLIGHT	21	DO	Indicate the module's network activity status	V_{OH}min=1.35V V_{OL}max=0.45V	1.8V power domain. If unused, keep this pin open.

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	8	PI	USB detection	Vmax=5.25V Vmin=3.0V	

				Vnorm=5.0V	
USB_DP	9	IO	USB differential data bus (+)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
USB_DM	10	IO	USB differential data bus (-)	Compliant with USB 2.0 standard specification.	Require differential impedance of 90Ω.
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_ PRESENCE	42	DI	(U)SIM card insertion detection	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep it open.
USIM_VDD	43	PO	Power supply for (U)SIM card	**For 1.8V (U)SIM:** Vmax=1.9V Vmin=1.7V **For 3.0V (U)SIM:** Vmax=3.05V Vmin=2.7V $I_O$max=50mA	Either 1.8V or 3.0V is supported by the module automatically.
USIM_RST	44	DO	Reset signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_DATA	45	IO	Data signal of (U)SIM card	**For 1.8V (U)SIM:** V_{IL}max=0.6V V_{IH}min=1.2V V_{OL}max=0.45V V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{IL}max=1.0V V_{IH}min=1.95V V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_CLK	46	DO	Clock signal of (U)SIM card	**For 1.8V (U)SIM:** V_{OL}max=0.45V	

				V_{OH}min=1.35V **For 3.0V (U)SIM:** V_{OL}max=0.45V V_{OH}min=2.55V	
USIM_GND	47		Specified ground for (U)SIM card		
UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DTR	30	DI	Data terminal ready	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
RXD	34	DI	Receive data	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
TXD	35	DO	Transmit data	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
CTS	36	DO	Clear to send	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
RTS	37	DI	Request to send	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
DCD	38	DO	Data carrier detection	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
RI	39	DO	Ring indicator	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC1	2	AI	General purpose analog to digital converter	Voltage range: 0.3V to 1.8V	If unused, keep this pin open.

			interface		
ADC0	24	AI	General purpose analog to digital converter interface	Voltage range: 0.3V to 1.8V	If unused, keep this pin open.
USB_BOOT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	75	DI	Force the module to enter into emergency download mode	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
RF Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	IO	Main antenna interface		50Ω impedance.
ANT_GNSS	49	AI	GNSS antenna interface		50Ω impedance. If unused, keep this pin open.
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	11~14, 16, 25, 51, 56, 57, 63, 65, 66, 76~78, 83~88, 92~99		Reserved		Keep these pins open.
GPIO Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO01	4	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open. This pin cannot be pulled up before startup.
GPIO02	5	IO	General-purpose	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain. If unused, keep this pin

			input/output interface	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	open.
GPIO03	6	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO04	7	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO05	18	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO06	19	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO07	22	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO08	23	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO09	26	IO	General-purpose input/output	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V	1.8V power domain. If unused, keep this pin open.

			interface	V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	
GPIO10	27	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO11	28	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO19	40	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO20	41	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.
GPIO21	64	IO	General-purpose input/output interface	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain. If unused, keep this pin open.

NOTE

Keep all RESERVED pins and unused pins open.

Table 5: Multiplexing Pins

Pin Name	Pin No.	Mode 1	Mode 2	Mode 3	Mode 4	Reset[1)]	Interrupt*	Remark
GPIO01	4	GPIO_23	GPIO_23	SPI1_CLK	/	B-PU	No	BOOT_ CONFIG_4
GPIO02	5	GPIO_20	UART1_TX	SPI1_MOSI	/	B-PD	Yes	
GPIO03	6	GPIO_21	UART1_RX	SPI1_MISO	/	B-PD	Yes	
GPIO04	7	GPIO_22	GPIO_22	SPI1_CS_N	/	B-PD	Yes	
GPIO05	18	GPIO_11	/	SPI2_CLK	I2C2_SCL	B-PU	Yes	
GPIO06	19	GPIO_10	/	SPI2_CS_N	I2C2_SDA	B-PD	No	
GPIO07	22	GPIO_09	UART2_RX	SPI2_MISO	/	B-PD	Yes	
GPIO08	23	GPIO_08	UART2_TX	SPI2_MOSI	/	B-PD	Yes	
GPIO09	26	GPIO_15	GPIO_15	/	/	B-PD	No	
GPIO10	27	GPIO_12	UART3_TX	/	/	B-PD	Yes	
GPIO11	28	GPIO_13	UART3_RX	/	/	B-PD	Yes	
GPIO19	40	GPIO_19	/	/	I2C1_SCL	B-PD	No	
GPIO20	41	GPIO_18	/	/	I2C2_SDA	B-PD	No	
GPIO21	64	GPIO_07	/	/	/	B-PD	No	

NOTES

1. The pin functions in Model 1/2/3/4 take effect only after software configuration.
2. [1)] Please refer to ***Table 3*** for more details about the symbol description.
3. The BOOT_CONFIG pin (GPIO01) cannot be pulled up before startup.
4. "*" means under development.
5. "/" means not supported.

Table 6: Pull up/down Resistance of GPIO

Symbol	Description	Min	Max	Unit
R_{PU}	Pull-up resistance	55	390	kohm
R_{PD}	Pull-down resistance	55	390	kohm

3.4. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on network, and it is ready to send and receive data.
	Talk/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Extended Idle Mode DRX (e-I-DRX)	The module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN** command can set the module into airplane mode. In this case, RF function will be invalid.	
Minimum Functionality Mode	**AT+CFUN** command can set the module into a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Power Saving Mode (PSM)	The module may enter into Power Saving Mode for reducing its power consumption. PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections.	
Power OFF Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. But operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

During e-I-DRX, it is recommended to use UART interface for data communication, as the use of USB interface will increase power consumption.

3.5. Power Saving

3.5.1. Airplane Mode

When the BG96-QuecOpen module enters into airplane mode, the RF function does not work, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following ways.

Software:

AT+CFUN=<fun> command provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTE

The execution of **AT+CFUN** command will not affect GNSS function.

3.5.2. Power Saving Mode (PSM)

BG96-QuecOpen module can enter into PSM for reducing its power consumption. The mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. So BG96-QuecOpen module in PSM cannot immediately respond users' requests.

When the module wants to use the PSM it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM and accepts that the module uses PSM, the network confirms usage of PSM by allocating an Active Time value to the module. If the module wants to change the Active Time value, e.g. when the conditions are changed in the module, the module consequently requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+CPSMS=1** command.

Either of the following methods will wake up the module from PSM:

- Drive PWRKEY pin to low level will wake up the module.
- When the T3412 timer expires, the module will be automatically woken up.

NOTE

Please refer to ***document [2]*** for details about **AT+CPSMS** command.

3.5.3. Extended Idle Mode DRX (e-I-DRX)

The BG96-QuecOpen module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what was requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

If e-I-DRX is supported by the network, then it can be enabled by **AT+CEDRXS=1** command.

NOTE

Please refer to ***document [2]*** for details about **AT+CEDRXS** command.

3.6. Power Supply

3.6.1. Power Supply Pins

BG96-QuecOpen provides the following four VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

Table 8: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	32, 33	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67~74, 79~82, 89~91, 100~102	Ground	-	-	-	-

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in LTE networks.

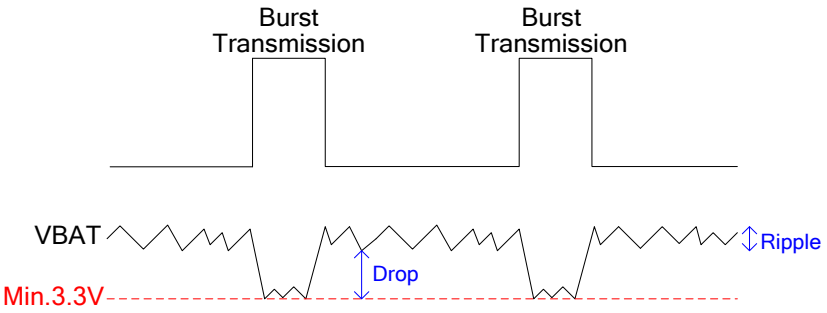


Figure 3: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be used due to its low ESR. It is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm, and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested to use a zener diode with reverse zener voltage of 5.1V and dissipation power more than 0.5W, and place it as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

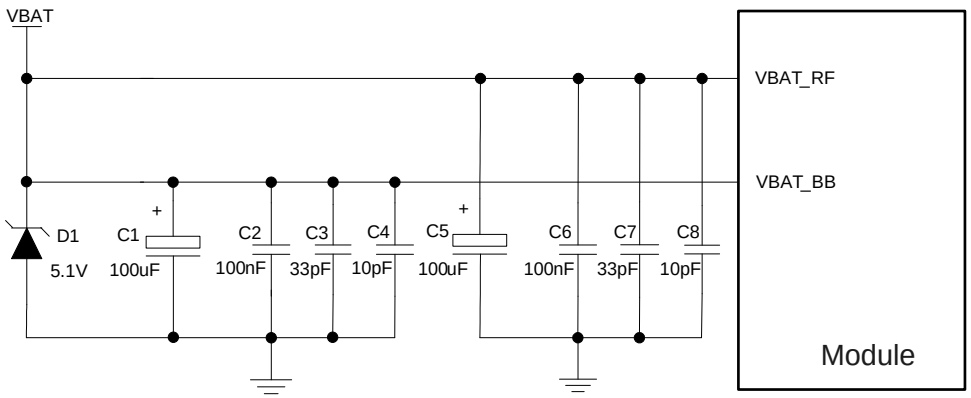


Figure 4: Star Structure of the Power Supply

3.6.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply for BG96-QuecOpen should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The designed output for the power supply is about 3.8V and the maximum rated current is 3A.

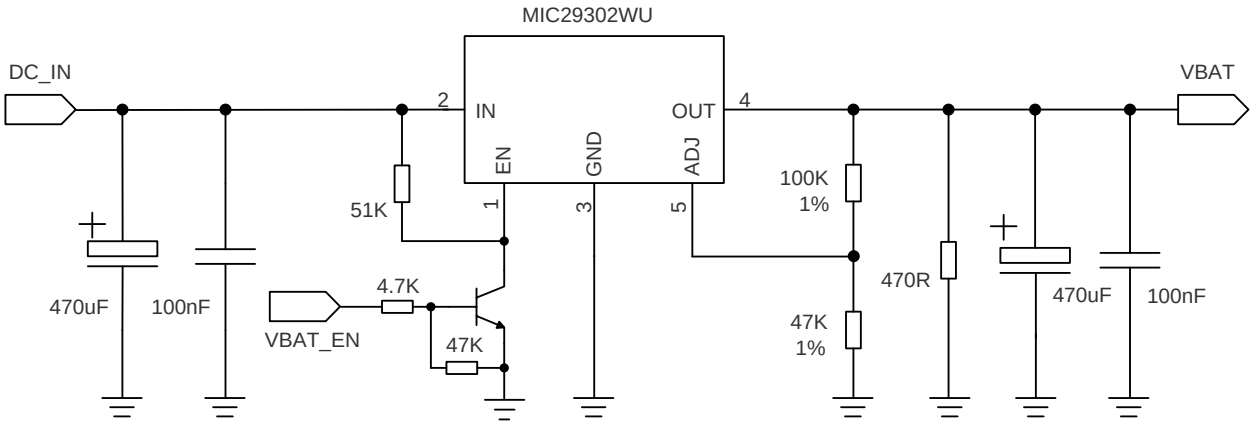


Figure 5: Reference Circuit of Power Supply

3.6.4. Monitor the Power Supply

AT+CBC command can be used to monitor the VBAT_BB voltage value. Please refer to ***document [2]*** for more details.

3.7. Turn on and off Scenarios

3.7.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 9: PWRKEY Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
PWRKEY	15	Turn on/off the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When BG96-QuecOpen is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin outputting a high level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

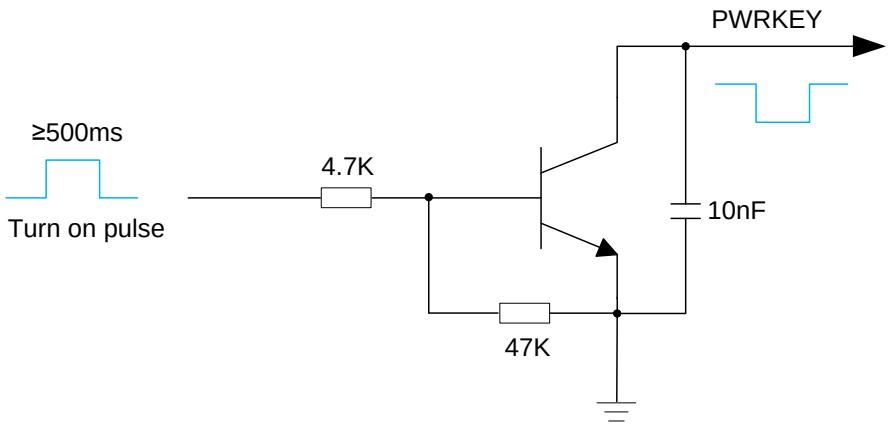


Figure 6: Turn on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When pressing the key, electrostatic strike may generate from finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

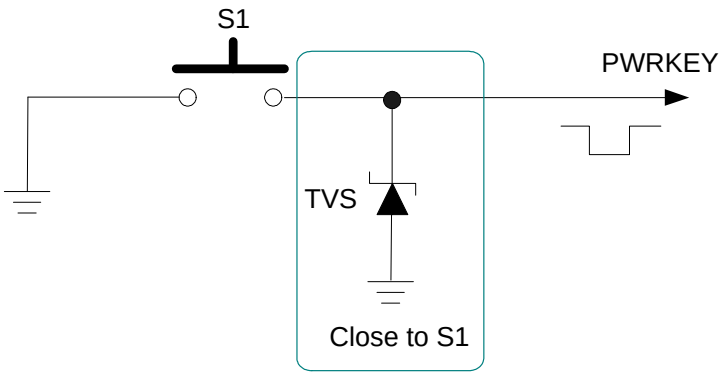


Figure 7: Turn on the Module Using Keystroke

The turn on scenario is illustrated in the following figure.

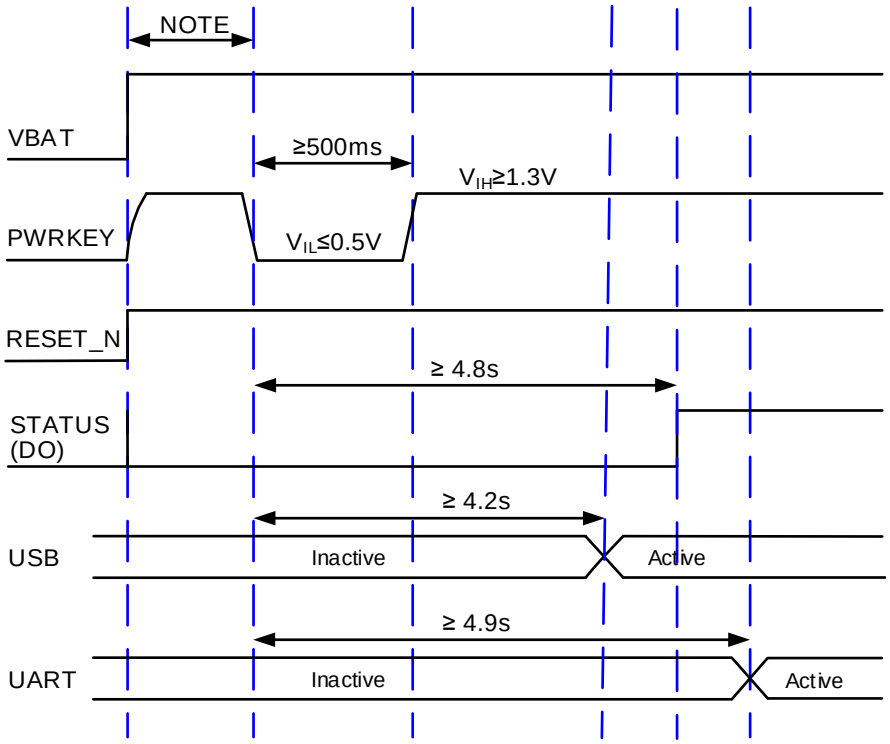


Figure 8: Timing of Turning on Module

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them is no less than 30ms.

3.7.2. Turn off Module

Either of the following methods can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using AT command or API interface.

3.7.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

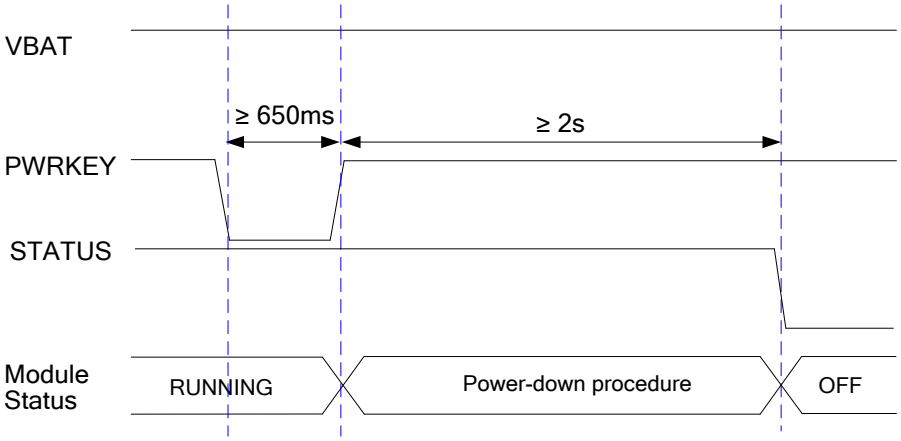


Figure 9: Timing of Turning off Module

3.7.2.2. Turn off Module Using AT Command or API Interface

It is also a safe way to use AT command or API interface to turn off the module, which is similar to turning off the module via PWRKEY Pin.

Please refer to ***document [2]*** for more details about the AT command.

NOTES

1. In order to avoid damaging the internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command or API interface, the power supply can be cut off.
2. When turn off module with AT command or API, please keep PWRKEY at high level after the execution of power off command. Otherwise the module will be turned on again after successfully turn-off.

3.7.3. Reset the Module

The RESET_N can be used to reset the module. The module can be reset by driving the RESET_N to a low level voltage for time between 150ms and 460ms. As the RESET_N pin is sensitive to interference, the routing trace on the interface board of the module is recommended to be as short as possible and totally ground shielded.

Table 10: RESET_N Pin Description

Pin Name	Pin No.	Description	DC Characteristics	Comment
RESET_N	17	Reset the module	V_{IH}max=2.1V V_{IH}min=1.3V V_{IL}max=0.5V	Pull-up to 1.8V internally. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

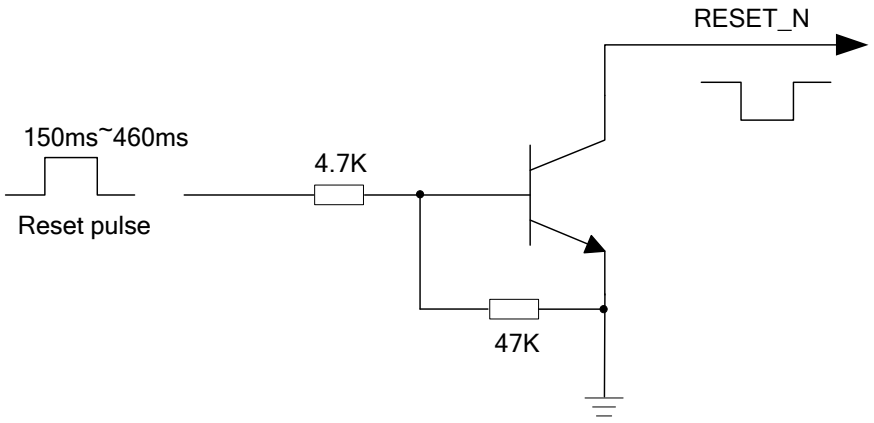


Figure 10: Reference Circuit of RESET_N by Using Driving Circuit

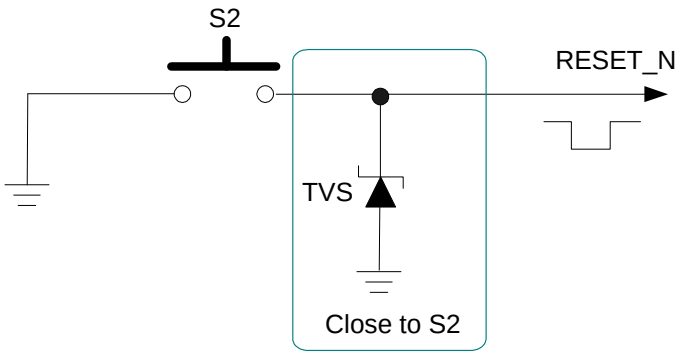


Figure 11: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

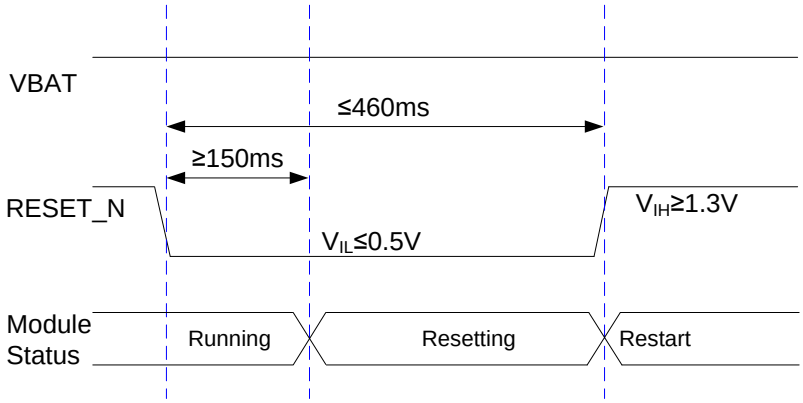


Figure 12: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by AT command, API interface and PWRKEY pin all failed.
2. Please assure that there is no large capacitance on PWRKEY and RESET_N pins.

3.8. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 SIM interface requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 11: Pin Definition of the (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_ PRESENCE	42	DI	(U)SIM card insertion detection	1.8V power domain.
USIM_VDD	43	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_RST	44	DO	Reset signal of (U)SIM card	
USIM_DATA	45	IO	Data signal of (U)SIM card	
USIM_CLK	46	DO	Clock signal of (U)SIM card	
USIM_GND	47		Specified ground for (U)SIM card	

BG96-QuecOpen supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and is disabled by default. Please refer to ***document [2]*** about **AT+QSIMDET** command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

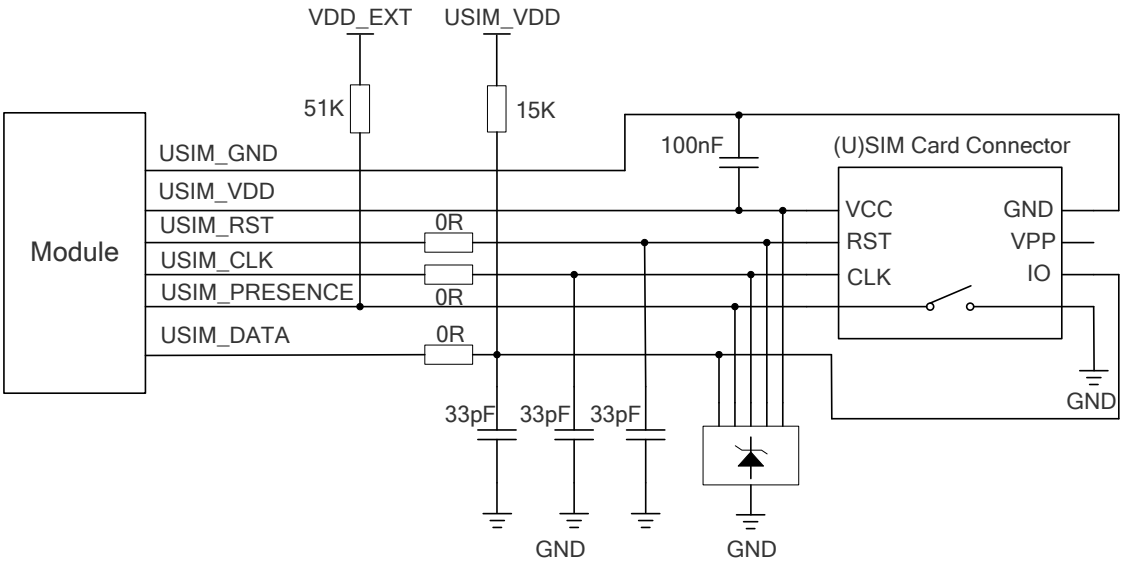


Figure 13: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, then USIM_PRESENCE can be used for other function. Please refer to ***Table 5*** for more details. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

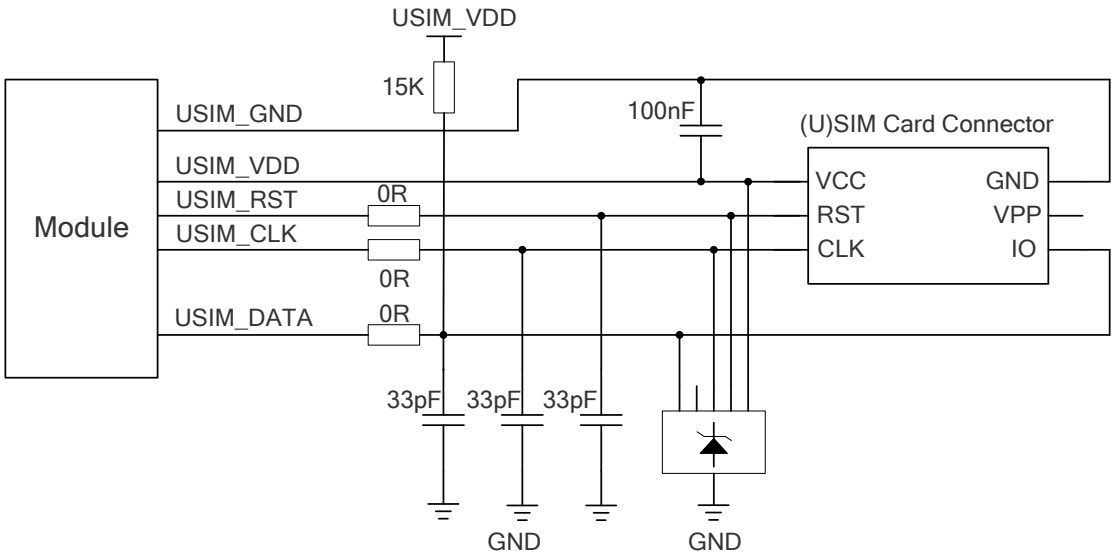


Figure 14: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. Also please make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1uF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be ground shielded.
- In order to offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15pF. In order to facilitate debugging, it is recommended to reserve series resistors for (U)SIM signals of the module. The 33pF capacitors are used for filtering interference of GSM 900MHz. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.9. USB Interface

BG96-QuecOpen contains one integrated Universal Serial Bus (USB) transceiver which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB Signal Part				
USB_VBUS	8	PI	USB connection detection	Typically 5.0V
USB_DP	9	IO	USB differential data bus (+)	Require differential impedance of 90Ω
USB_DM	10	IO	USB differential data bus (-)	Require differential impedance of 90Ω
GND	3		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in application design. The following figure shows a reference circuit of USB interface.

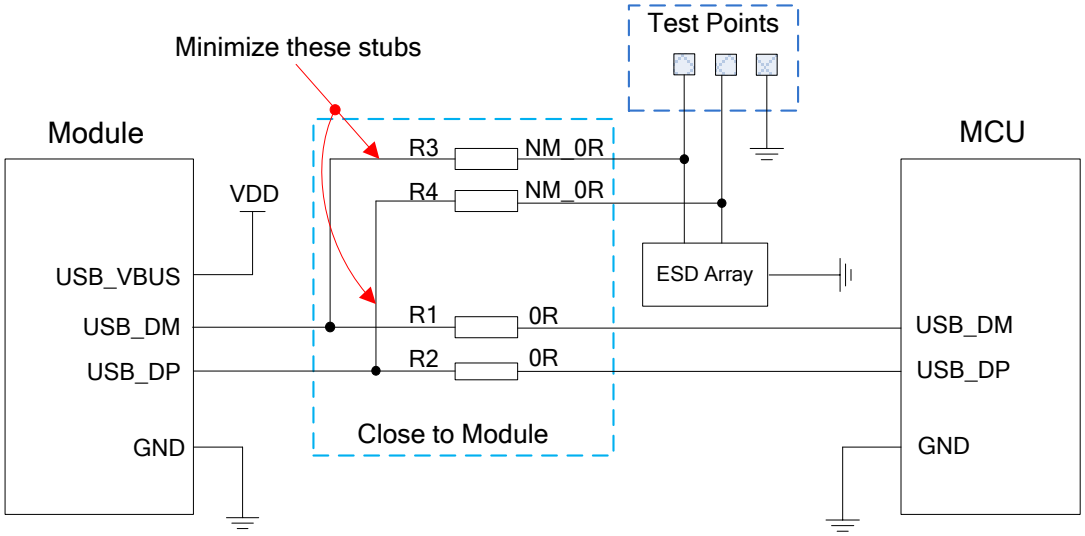


Figure 15: Reference Circuit of USB Application

In order to ensure the integrity of USB data line signal, components R1, R2, R3 and R4 must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 ohm.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components as close to the USB connector as possible.

NOTE

BG96-QuecOpen module can only be used as a slave device.

3.10. UART Interfaces

The module provides four UART interfaces: Main UART, UART1, UART2 and UART3.

- Main UART interface can only be used for AT command communication.
- UART1, UART2 and UART3 interfaces are used for communication and data transmission with peripherals, and can also be multiplexed into other functions.

The following tables show the pin definition of the four UART interfaces.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DTR	30	DI	Data terminal ready	1.8V power domain
RXD	34	DI	Receive data	1.8V power domain
TXD	35	DO	Transmit data	1.8V power domain
CTS	36	DO	Clear to send	1.8V power domain
RTS	37	DI	Request to send	1.8V power domain
DCD	38	DO	Data carrier detection	1.8V power domain
RI	39	DO	Ring indicator	1.8V power domain

Table 14: Pin Definition of UART1 Interface

Pin Name	Pin No.	I/O	Mode 1	Mode 2	Mode 3	Mode 4	Remark
GPIO01	4	IO	GPIO_23	GPIO_23	SPI1_CLK	/	1.8V power domain. Cannot be pulled up before startup.
GPIO02	5	IO	GPIO_20	UART1_TX	SPI1_MOSI	/	1.8V power domain.
GPIO03	6	IO	GPIO_21	UART1_RX	SPI1_MISO	/	1.8V power domain.
GPIO04	7	IO	GPIO_22	GPIO_22	SPI1_CS_N	/	1.8V power domain.

Table 15: Pin Definition of UART2 Interface

Pin Name	Pin No.	I/O	Mode 1	Mode 2	Mode 3	Mode 4	Remark
GPIO05	18	IO	GPIO_11	/	SPI2_CLK	I2C2_SCL	1.8V power domain.
GPIO06	19	IO	GPIO_10	/	SPI2_CS_N	I2C2_SDA	1.8V power domain.
GPIO07	22	IO	GPIO_09	UART2_RX	SPI2_MISO	/	1.8V power domain.
GPIO08	23	IO	GPIO_08	UART2_TX	SPI2_MOSI	/	1.8V power domain.

Table 16: Pin Definition of UART3 Interface

Pin Name	Pin No.	I/O	Mode 1	Mode 2	Mode 3	Mode 4	Remark
GPIO10	27	IO	GPIO_12	UART3_TX	/	/	1.8V power domain.
GPIO11	28	IO	GPIO_13	UART3_RX	/	/	1.8V power domain.

NOTE

The pin functions in Model 1/2/3/4 take effect only after software configuration.

The logic levels of the four UART interfaces are described in the table below.

Table 17: Logic Levels of Digital I/O

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

The module provides 1.8V UART interfaces. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by Texas Instrument is recommended. The following figure shows a reference design.

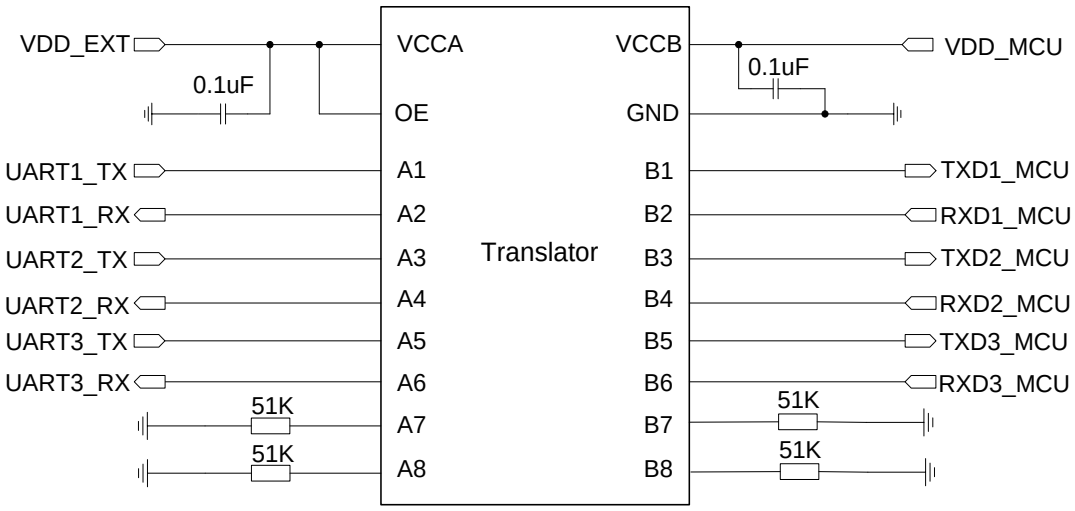


Figure 16: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module input and output circuit designs, but please pay attention to the direction of connection.

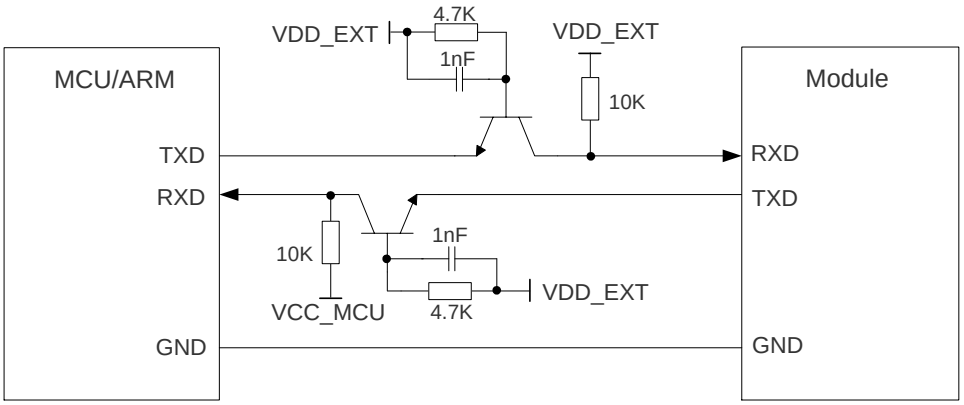


Figure 17: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.11. I2C Interfaces

BG96-QuecOpen provides two Inter-Integrated Circuit (I2C) interfaces for communication, which support high-speed mode and not support multi-master. I2C interfaces uses GPIOs configured as open-drain outputs, and the pull-up resistors should be provided externally.

The following table shows the pin definition.

Table 18: Pin Definition of the I2C1 Interface

Pin Name	Pin No.	I/O	Mode 1	Mode 2	Mode 3	Mode 4	Remark
GPIO19	40	IO	GPIO_19	/	/	I2C1_SCL	1.8V power domain.
GPIO20	41	IO	GPIO_18	/	/	I2C2_SDA	1.8V power domain.

Table 19: Pin Definition of the I2C2 Interface

Pin Name	Pin No.	I/O	Mode 1	Mode 2	Mode 3	Mode 4	Remark
GPIO05	18	IO	GPIO_11	/	SPI2_CLK	I2C2_SCL	1.8V power domain.
GPIO06	19	IO	GPIO_10	/	SPI2_CS_N	I2C2_SDA	1.8V power domain.

NOTES

1. I2C interfaces are open-drain outputs that must be pulled up to 1.8V.
2. The pin functions in Model 1/2/3/4 take effect only after software configuration.

The following figure shows a reference design of I2C interfaces with an external I2C interface sensor.

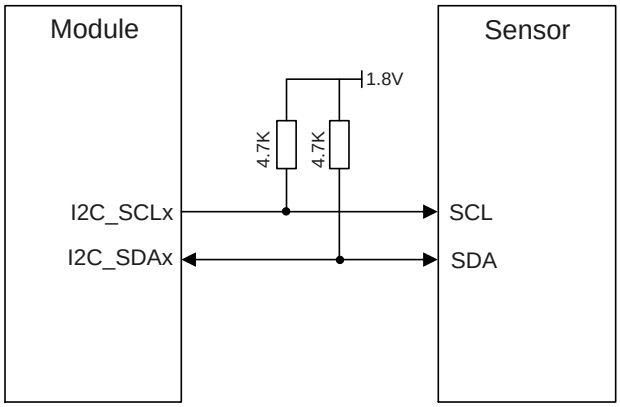


Figure 18: Reference Circuit of I2C Interfaces with an External I2C Interface Sensor

3.12. SPI Interfaces

BG96-QuecOpen provides two SPI interfaces which support only master mode with a maximum clock frequency up to 50MHz.

The following table shows the pin definition.

Table 20: Pin Definition of the SPI1 Interface

Pin Name	Pin No.	I/O	Mode 1	Mode 2	Mode 3	Mode 4	Remark
GPIO01	4	IO	GPIO_23	GPIO_23	SPI1_CLK	/	1.8V power domain. Cannot be pulled up before startup.
GPIO02	5	IO	GPIO_20	UART1_TX	SPI1_MOSI	/	1.8V power domain.
GPIO03	6	IO	GPIO_21	UART1_RX	SPI1_MISO	/	1.8V power domain.
GPIO04	7	IO	GPIO_22	GPIO_22	SPI1_CS_N	/	1.8V power domain.

Table 21: Pin Definition of the SPI2 Interface

Pin Name	Pin No.	I/O	Mode 1	Mode 2	Mode 3	Mode 4	Remark
GPIO05	18	IO	GPIO_11	/	SPI2_CLK	I2C2_SCL	1.8V power domain.
GPIO06	19	IO	GPIO_10	/	SPI2_CS_N	I2C2_SDA	1.8V power domain.
GPIO07	22	IO	GPIO_09	UART2_RX	SPI2_MISO	/	1.8V power domain.
GPIO08	23	IO	GPIO_08	UART2_TX	SPI2_MOSI	/	1.8V power domain.

NOTE

The pin functions in Model 1/2/3/4 take effect only after software configuration.

The following figure shows the timing relationship of SPI interfaces. The related parameters of SPI timing is shown in the table below.

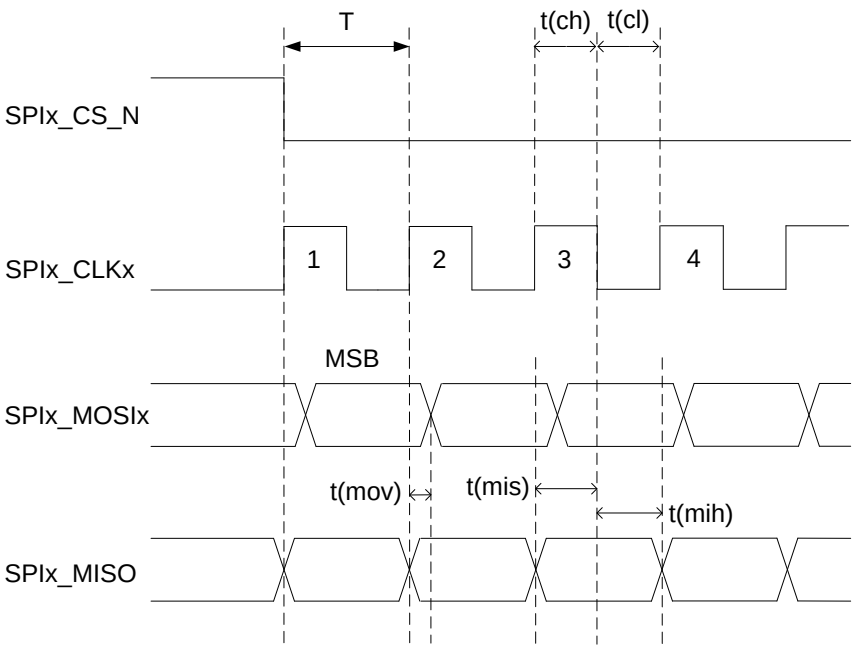


Figure 19: SPI Timing

Table 22: Parameters of SPI Interface Timing

Parameter	Description	Min	Typical	Max	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high level time	9.0	-	-	ns
t(cl)	SPI clock low level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

NOTE

The module provides 1.8V SPI interface. A level translator should be used between the module and the host if customers' application is equipped with a 3.3V processor or device interface.

3.13. ADC Function

The module provides two analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read via **AT+QADC=<port>** command, through setting **<port>** into 0, 1. For more details about the AT command, please refer to ***document [2]***.

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

In order to improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 23: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC1	2	AI	General purpose analog to digital converter	
ADC0	24	AI	General purpose analog to digital converter	

The following table describes characteristics of ADC interfaces.

Table 24: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		1.8V	V
ADC1 Voltage Range	0.3		1.8V	V
ADC Resolution		15		bits

NOTES

1. ADC input voltage must not exceed 1.8V.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

3.14. Network Status Indication

BG96-QuecOpen provides one network indication pin: NETLIGHT. The pin is used to drive a network status indication LED.

The following tables describe the pin definition and logic level changes of NETLIGHT in different network status.

Table 25: Pin Definition of Network Status Indicator

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	21	DO	Indicate the module's network activity status.	1.8V power domain

Table 26: Working State of the Network Status Indicator

Pin Name	Indicator Status (Logic Level Changes)	Network Status
NETLIGHT	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle

	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

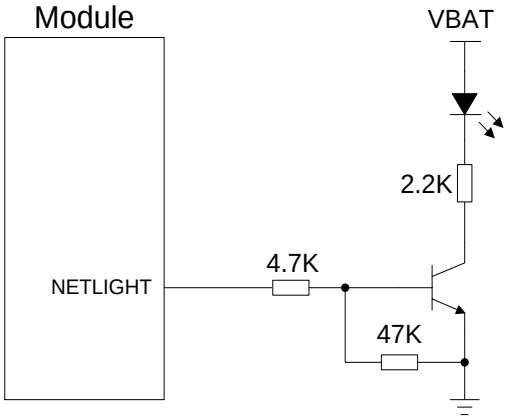


Figure 20: Reference Circuit of the Network Status Indicator

3.15. STATUS

The STATUS pin is a digital output for indicating the module's operation status. When the module is turned on normally, the STATUS will present high-impedance state. Otherwise, the STATUS will present a low level state.

Table 27: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8V power domain

The following figure shows a reference circuit of STATUS.

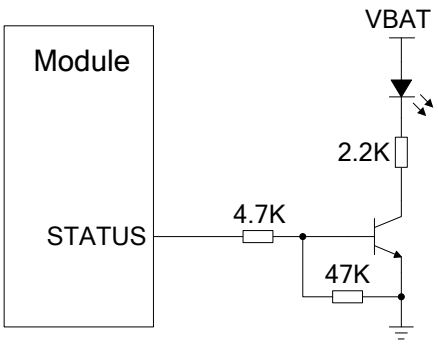


Figure 21: Reference Circuits of STATUS

3.16. USB_BOOT Interface

BG96-QuecOpen provides a USB_BOOT pin. Developers can pull up the USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into forced download mode when it is powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 28: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module to enter into emergency download mode	1.8V power domain. Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

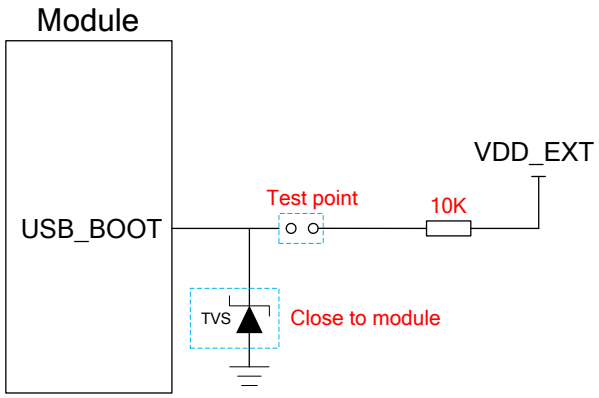


Figure 22: Reference Circuit of USB_BOOT Interface

4 GNSS Receiver

4.1. General Description

BG96-QuecOpen includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

BG96-QuecOpen supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, GNSS engine of the module is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of BG96-QuecOpen.

Table 29: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	31	s
		XTRA enabled	11.54	s
	Warm start @open sky	Autonomous	21	s
		XTRA enabled	2.52	s

	Hot start @open sky	Autonomous	2.7	s
		XTRA enabled	1.82	s
Accuracy (GNSS)	CEP-50	Autonomous @open sky	< 2.5	m

NOTES

1. Tracking sensitivity: the lowest GNSS signal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application design.

- Maximize the distance between the GNSS antenna and the main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Control the characteristic impedance for ANT_GNSS trace as 50Ω.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

BG96-QuecOpen include a main antenna interface and a GNSS antenna interface. The antenna ports have an impedance of 50Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

The pin definition of main antenna interface is shown below.

Table 30: Pin Definition of the RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	IO	Main antenna interface	50Ω impedance

5.1.2. Operating Frequency

Table 31: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B2/PCS1900	1850~1910	1930~1990	MHz
LTE-FDD B3/DCS1800	1710~1785	1805~1880	MHz
LTE-FDD B4	1710~1755	2110~2155	MHz
LTE-FDD B5/GSM850)	824~849	869~894	MHz
LTE-FDD B8/EGSM900)	880~915	925~960	MHz
LTE-FDD B12	699~716	728~746	MHz

LTE-FDD B13	777~787	746~757	MHz
LTE-FDD B18	815~829.9	860~874.9	MHz
LTE-FDD B19	830~844.9	875~889.9	MHz
LTE-FDD B20	832~862	791~821	MHz
LTE-FDD B26	814~848.9	859~893.9	MHz
LTE-FDD B28	703~748	758~803	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of main antenna interface is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

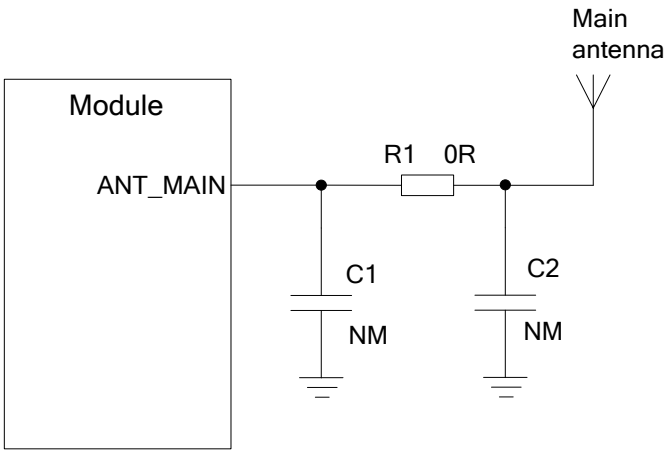


Figure 23: Reference Circuit of RF Antenna Interface

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures.

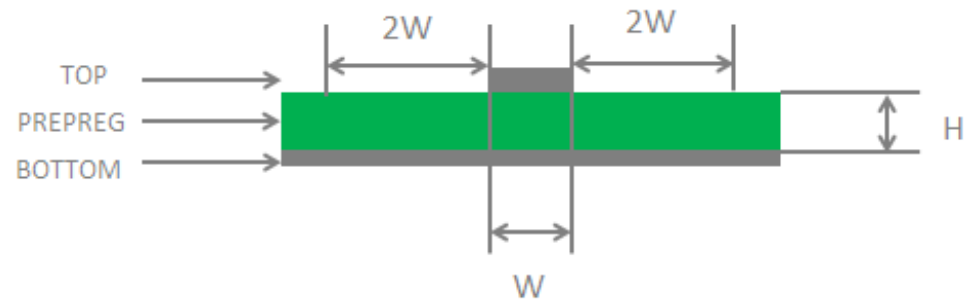


Figure 24: Microstrip Line Design on a 2-layer PCB

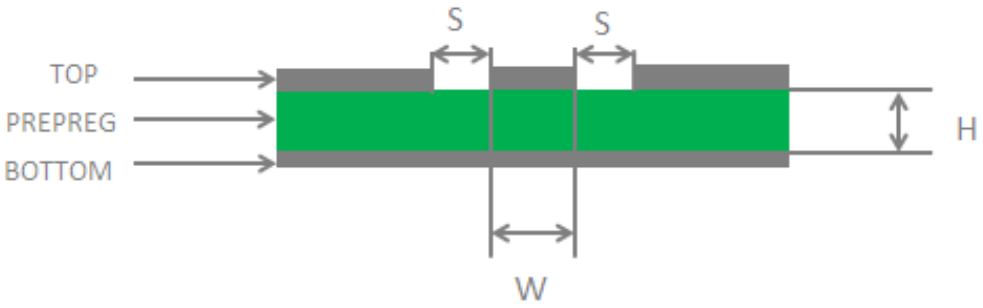


Figure 25: Coplanar Waveguide Line Design on a 2-layer PCB

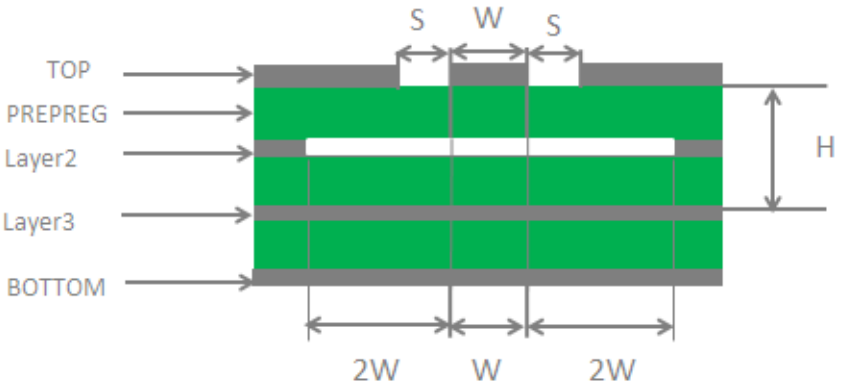


Figure 26: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

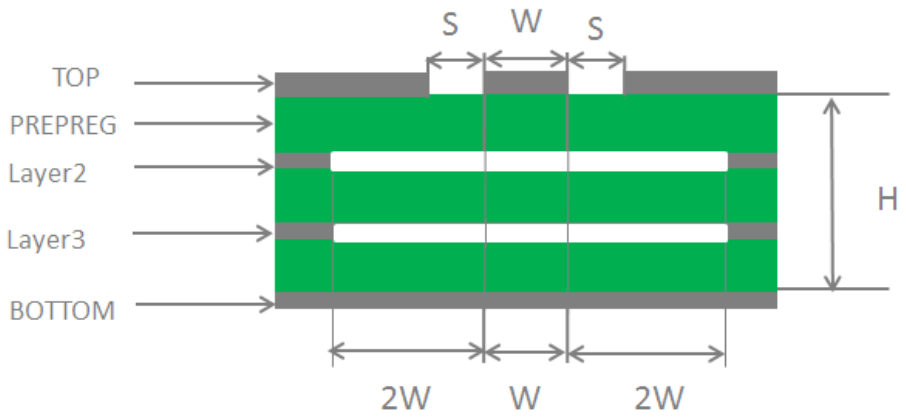


Figure 27: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to control the characteristic impedance of RF traces as 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times of the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

Table 32: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50Ω impedance

Table 33: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

A reference design of GNSS antenna is shown as below.

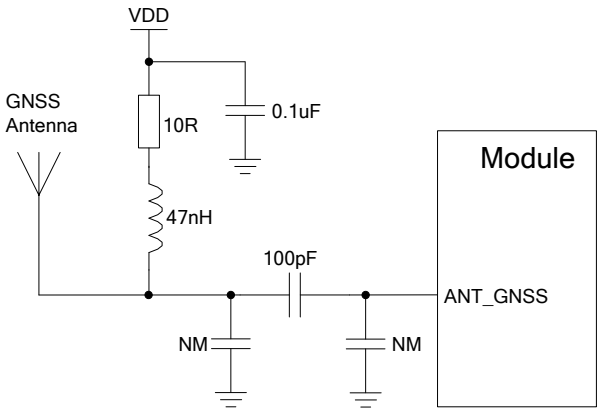


Figure 28: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna and GNSS antenna.

Table 34: Antenna Requirements

Type	Requirements
LTE/GSM Antenna	VSWR: ≤ 2 Gain (dBi): 1 Max Input Power (W): 50 Input Impedance (Ω): 50 Polarization Type: Vertical Cable Insertion Loss: < 1dB (LTE B5/B8/B12/B13/B18/B19/B20/B26/B28 GSM850/EGSM900) Cable Insertion Loss: < 1.5dB (LTE B1/B2/B3/B4/B39, DCS1800/PCS1900)
GNSS Antenna	Frequency range: 1561~1615MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > -2dBi Active antenna embedded LNA gain: 20dB (Typ.) Active antenna total gain: > 18dBi (Typ.)

5.3.2. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by HIROSE.

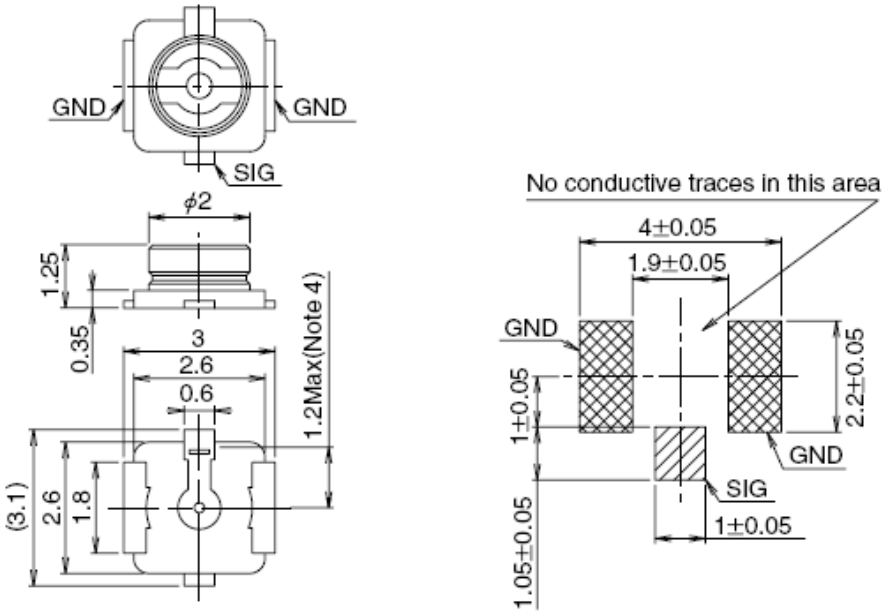


Figure 29: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connector listed in the following figure can be used to match the U.FL-R-SMT.

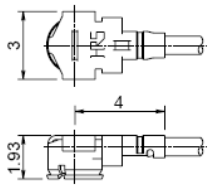
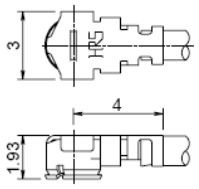
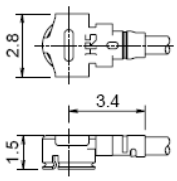
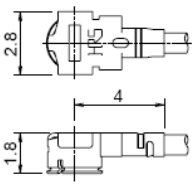
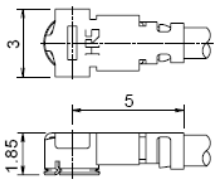
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 30: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

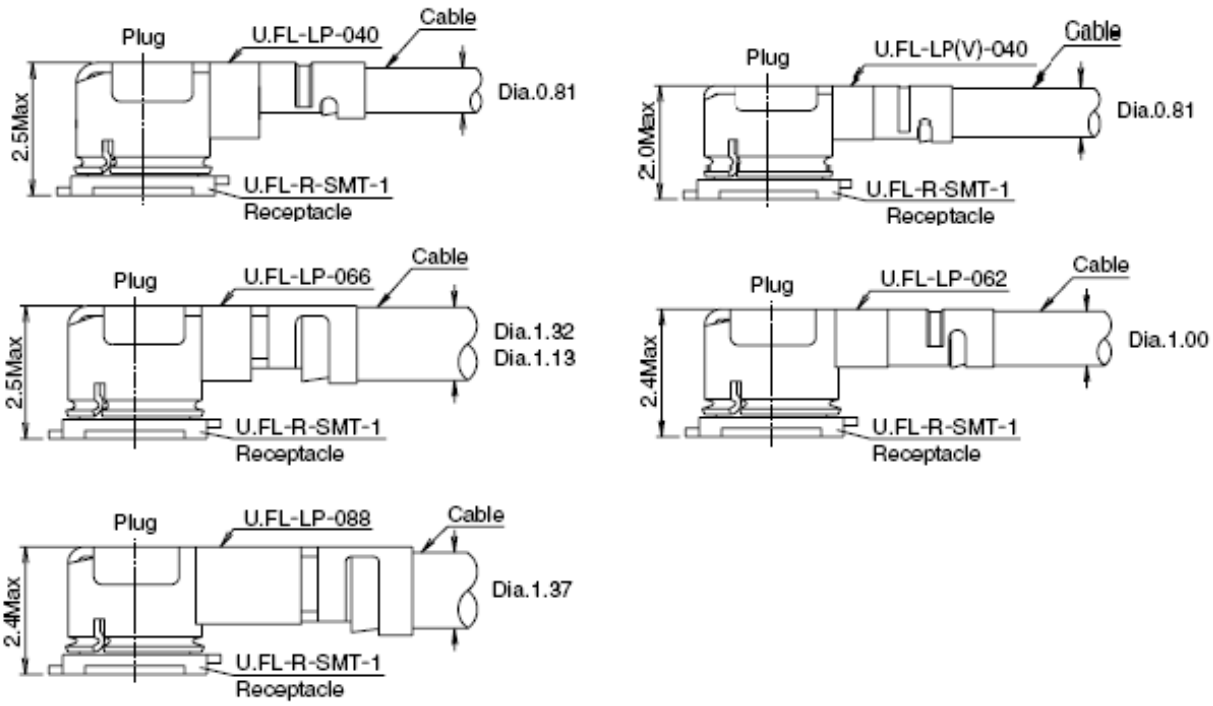


Figure 31: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 35: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.3	4.7	V
VBAT_RF	-1.2	6	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.3	V
Voltage at Digital Pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 36: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V

	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900		1.8	2.0	A
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

Table 37: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage temperature range	-40		+90	°C

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The following table shows current consumption of BG96-QuecOpen module.

Table 38: BG96-QuecOpen Current Consumption

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF State	Power down	8	uA
	PSM	Power Saving Mode @Real Network	10	uA
	Quiescent Current	**AT+CFUN=0**	0.8 [1]	mA
	Sleep State	DRX=1.28s @Real LTE Cat M1 Network	1.7 [2]	mA
		DRX=1.28s @Real LTE Cat NB1 Network	2.3 [2]	mA
		e-I-DRX=20.48s @Real LTE Cat M1 Network	1.1 [2]	mA
		e-I-DRX=20.48s @Real LTE Cat NB1 Network	1.7 [2]	mA
		@Real 2G Network	2.0 [2]	mA
	Standby State	DRX=1.28s @Real LTE Cat M1 Network	16 [3]	mA
		DRX=1.28s @Real LTE Cat NB1 Network	16 [3]	mA
		e-I-DRX=20.48s @Real LTE Cat M1 Network	15 [3]	mA
		e-I-DRX=20.48s @Real LTE Cat NB1 Network	15 [3]	mA
	LTE Cat M1 data transfer (GNSS OFF)	LTE-FDD B1 @23.21dBm	217	mA
		LTE-FDD B2 @22.29dBm	211	mA
		LTE-FDD B3 @23.05dBm	223	mA
		LTE-FDD B4 @23.2dBm	227	mA
		LTE-FDD B5 @23.35dBm	211	mA
		LTE-FDD B8 @23.05dBm	213	mA
		LTE-FDD B12 @23.83dBm	217	mA
		LTE-FDD B13 @23.39dBm	225	mA
		LTE-FDD B18 @23.58dBm	217	mA
		LTE-FDD B19 @23.26dBm	212	mA
		LTE-FDD B20 @23.46dBm	215	mA

		LTE-FDD B26 @23.34dBm	226	mA
		LTE-FDD B28 @23.67dBm	236	mA
		LTE-TDD B39 @TBD	TBD	mA
	LTE Cat NB1 data transfer (GNSS OFF)	LTE-FDD B1 @23.5dBm	170	mA
		LTE-FDD B2 @23.3dBm	175	mA
		LTE-FDD B3 @23.5dBm	188	mA
		LTE-FDD B4 @23.6dBm	185	mA
		LTE-FDD B5 @23.5dBm	185	mA
		LTE-FDD B8 @23.1dBm	173	mA
		LTE-FDD B12 @23.6dBm	189	mA
		LTE-FDD B13 @23.3dBm	182	mA
		LTE-FDD B18 @23.6dBm	185	mA
		LTE-FDD B19 @23.4dBm	187	mA
		LTE-FDD B20 @23.4dBm	189	mA
		LTE-FDD B26 @23.4dBm	190	mA
		LTE-FDD B28 @23.2dBm	183	mA
	GPRS data transfer (GNSS OFF)	GSM850 4UL1DL @30.55dBm	603	mA
		GSM850 3UL2DL @31.87dBm	527	mA
		GSM850 2UL3DL @32.21dBm	380	mA
		GSM850 1UL4DL @32.41dBm	220	mA
		EGSM900 4UL1DL @30.57dBm	564	mA
		EGSM900 3UL2DL @31.79dBm	489	mA
		EGSM900 2UL3DL @32.47dBm	372	mA
		EGSM900 1UL4DL @32.61dBm	209	mA
		DCS1800 4UL1DL @29.95dBm	534	mA

		DCS1800 3UL2DL @30.15dBm	418	mA
		DCS1800 2UL3DL @30.34dBm	303	mA
		DCS1800 1UL4DL @30.54dBm	183	mA
		PCS1900 4UL1DL @29.58dBm	497	mA
		PCS1900 3UL2DL @29.72dBm	388	mA
		PCS1900 2UL3DL @29.91dBm	282	mA
		PCS1900 1UL4DL @30.11dBm	171	mA
	EDGE data transfer (GNSS OFF)	GSM850 4UL1DL @26.35dBm	415	mA
		GSM850 3UL2DL @26.47dBm	320	mA
		GSM850 2UL3DL @26.69dBm	230	mA
		GSM850 1UL4DL @26.88dBm	140	mA
		EGSM900 4UL1DL @26.05dBm	390	mA
		EGSM900 3UL2DL @26.46dBm	301	mA
		EGSM900 2UL3DL @26.33dBm	217	mA
		EGSM900 1UL4DL @26.69dBm	133	mA
		DCS1800 4UL1DL @24.95dBm	370	mA
		DCS1800 3UL2DL @25.12dBm	282	mA
		DCS1800 2UL3DL @25.25dBm	204	mA
		DCS1800 1UL4DL @25.43dBm	127	mA
		PCS1900 4UL1DL @25.24dBm	375	mA
		PCS1900 3UL2DL @25.37dBm	290	mA
		PCS1900 2UL3DL @25.49dBm	210	mA
		PCS1900 1UL4DL @25.72dBm	130	mA
	LTE Voice (GNSS OFF)	Voice @LTE Cat M1 network	108	mA

NOTES

1. [1] Typical value with USB and UART disconnected.
2. [2] Sleep state with UART connected and USB disconnected. The module can enter into sleep state through executing **AT+QSCLK=1** command via UART interface and then controlling the module's DTR pin. For details, please refer to ***Chapter 3.4.4***.
3. [3] Standby state with UART connected and USB disconnected.

Table 39: GNSS Current Consumption of BG96-QuecOpen Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @Passive Antenna	41.7	mA
		Lost state @Passive Antenna	42	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	21.7	mA
		Open Sky @Passive Antenna	36	mA
		Open Sky @Active Antenna	35	mA

6.5. RF Output Power

The following table shows the RF output power of BG96-QuecOpen module.

Table 40: RF Output Power

Frequency	Max.	Min.
LTE-FDD B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B26/B28	23dBm±2dB	<-39dBm
LTE-TDD B39	23dBm±2dB	<-39dBm
GSM850/EGSM900	33dBm±2dB	5dBm±5dB
DCS1800/PCS1900	30dBm±2dB	0dBm±5dB
GSM850/EGSM900 (8-PSK)	27dBm±3dB	5dBm±5dB
DCS1800/PCS1900 (8-PSK)	26dBm±3dB	0dBm±5dB

6.6. RF Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of BG96-QuecOpen module.

Table 41: BG96-QuecOpen Conducted RF Receiving Sensitivity

Network	Band	Primary	Diversity	Sensitivity (dBm)	
				Cat M1/3GPP	Cat NB1[1)]/3GPP
LTE	LTE-FDD B1	Supported	Not Supported	-107.0/-102.7	-112.5/-107.5
	LTE-FDD B2			-106.7/-100.3	-112.5/-107.5
	LTE-FDD B3			-106.8/-99.3	-113/-107.5
	LTE-FDD B4			-106.9/-102.3	-112.5/-107.5
	LTE-FDD B5			-107.0/-100.8	-114/-107.5
	LTE-FDD B8			-107.3/-99.8	-113/-107.5
	LTE-FDD B12			-107.7/-99.3	-113.5/-107.5
	LTE-FDD B13			-106.5/-99.3	-112/-107.5
	LTE-FDD B18			-107.5/-102.3	-113.5/-107.5
	LTE-FDD B19			-107.1/-102.3	-114/-107.5
	LTE-FDD B20			-107.2/-99.8	-114/-107.5
	LTE-FDD B26			-107.1/-100.3	-113/-107.5
	LTE-FDD B28			-107.2/-100.8	-113/-107.5
	LTE-TDD B39			TBD /-103	Not Supported
Network	**Band**	**Primary**	**Diversity**	**Sensitivity (dBm)**	
				GSM/3GPP	
GSM	GSM850/EGSM900	Supported	Not Supported	-109/-102	
	DCS1800/PCS1900			-108.5/-102	

NOTE

[1] LTE Cat NB1 receiving sensitivity without repetitions.

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatic discharge characteristics.

Table 42: Electrostatic Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±10	±15	kV
Main/GNSS Antenna Interfaces	±10	±15	kV

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the Module

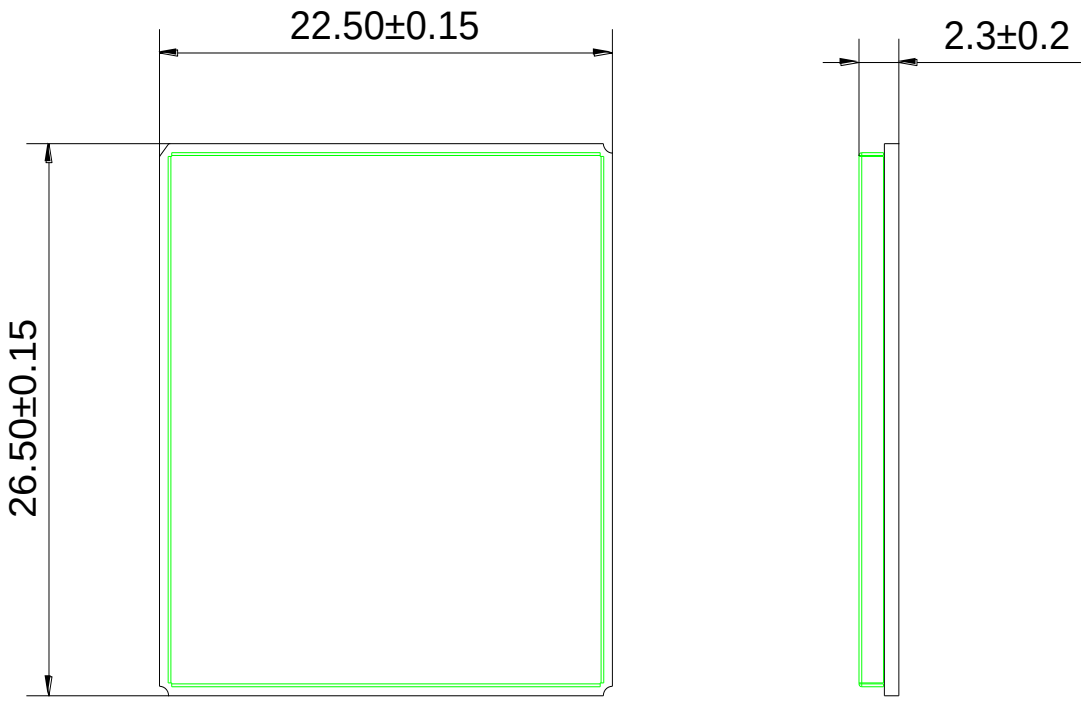


Figure 32: Module Top and Side Dimensions

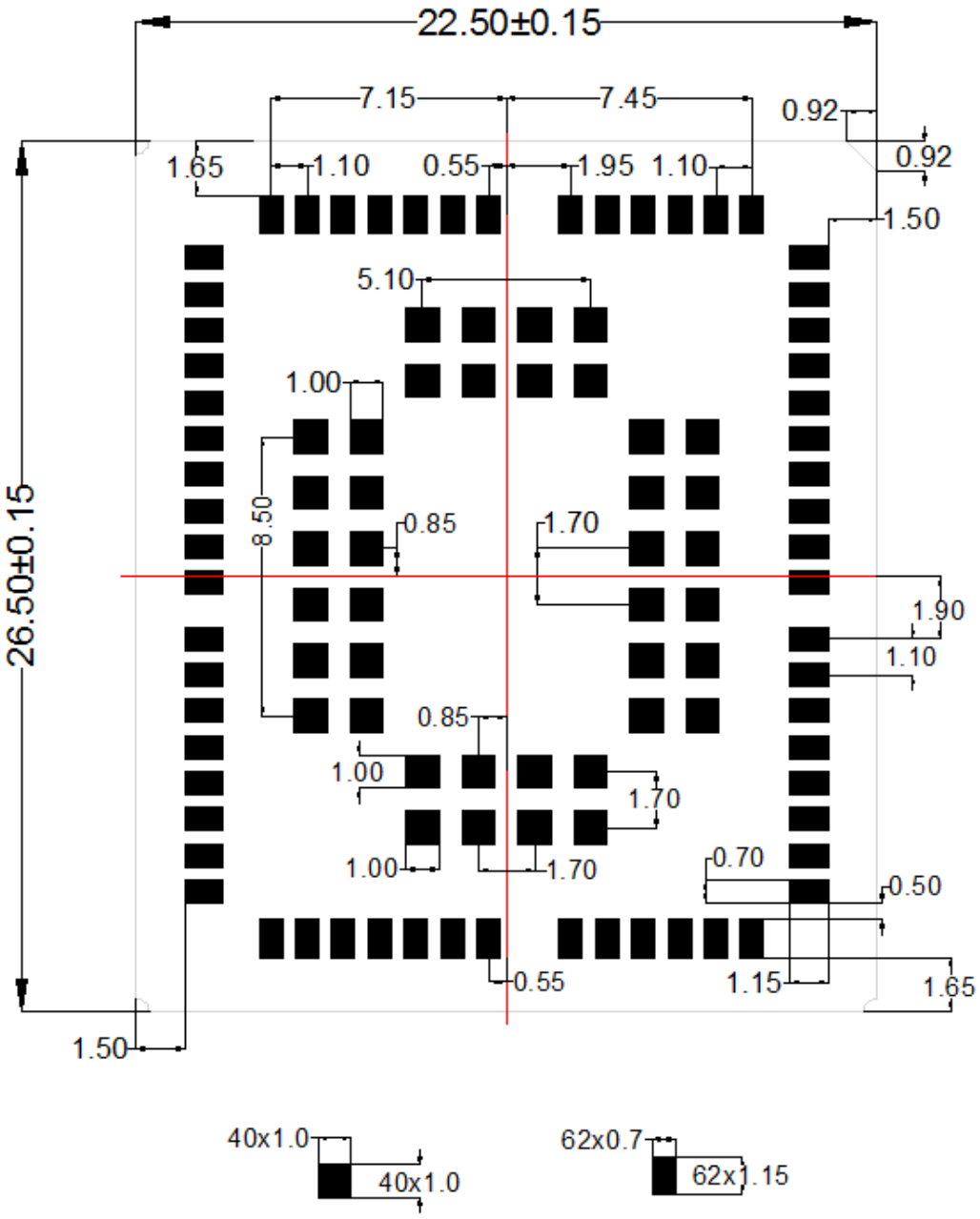


Figure 33: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

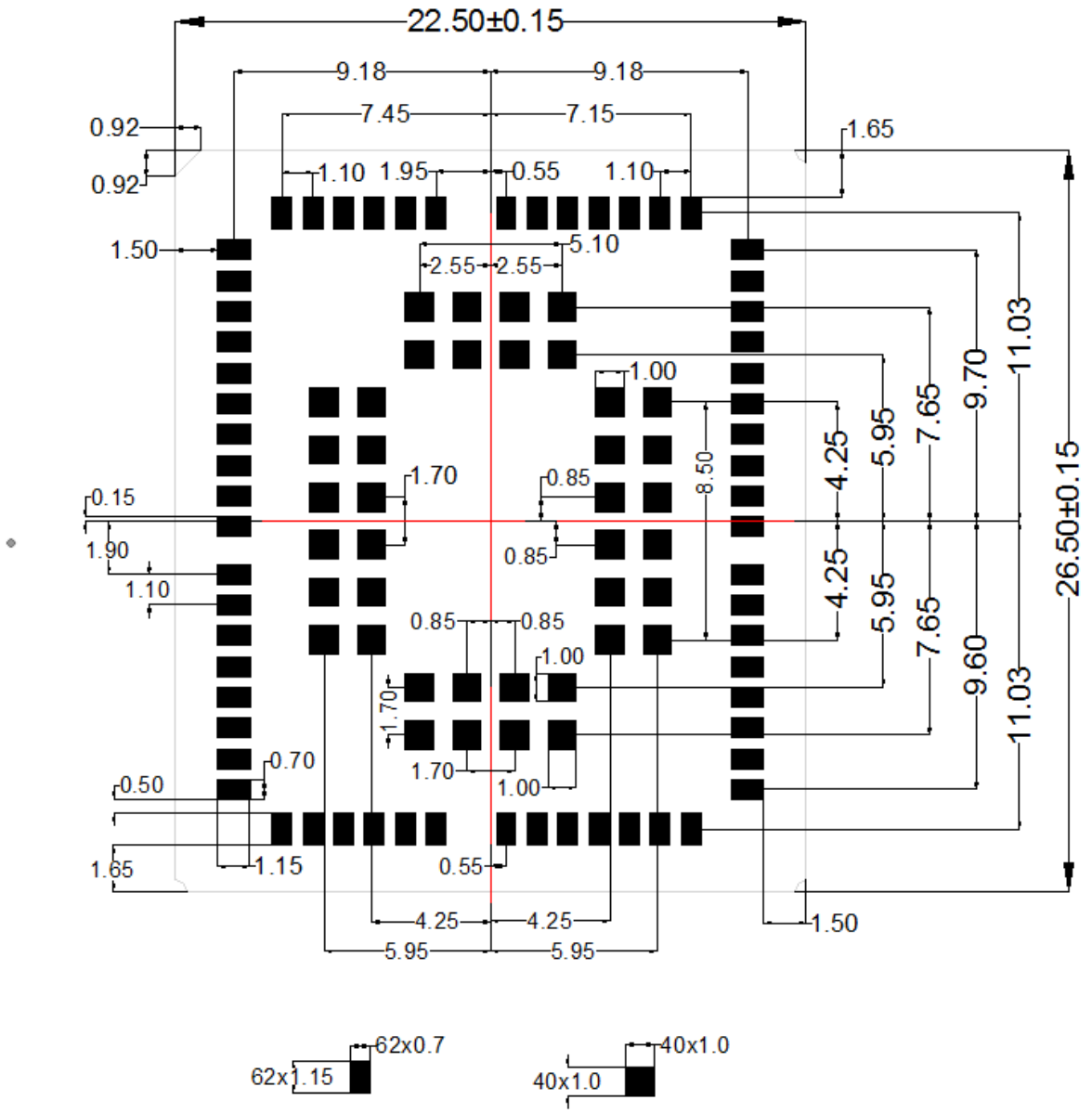


Figure 34: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, please keep about 3mm between the module and other components on the host PCB.
2. All reserved pins must be kept open.

7.3. Design Effect Drawings of the Module

Figure 35: Top View of the Module

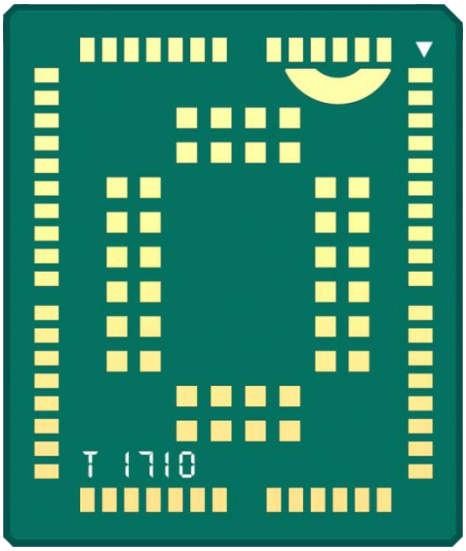


Figure 36: Bottom View of the Module

NOTE

These are design effect drawings of BG96-QuecOpen module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

BG96-QuecOpen is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10% RH.

3. Devices require bake before mounting, if any circumstances below occurs:

   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.
   - Stored at >10% RH after the vacuum-sealed bag is opened.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic container cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm. For more details, please refer to ***document [5]***.

It is suggested that the peak reflow temperature is 235~245ºC (for SnAg3.0Cu0.5 alloy). The absolute max reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below.

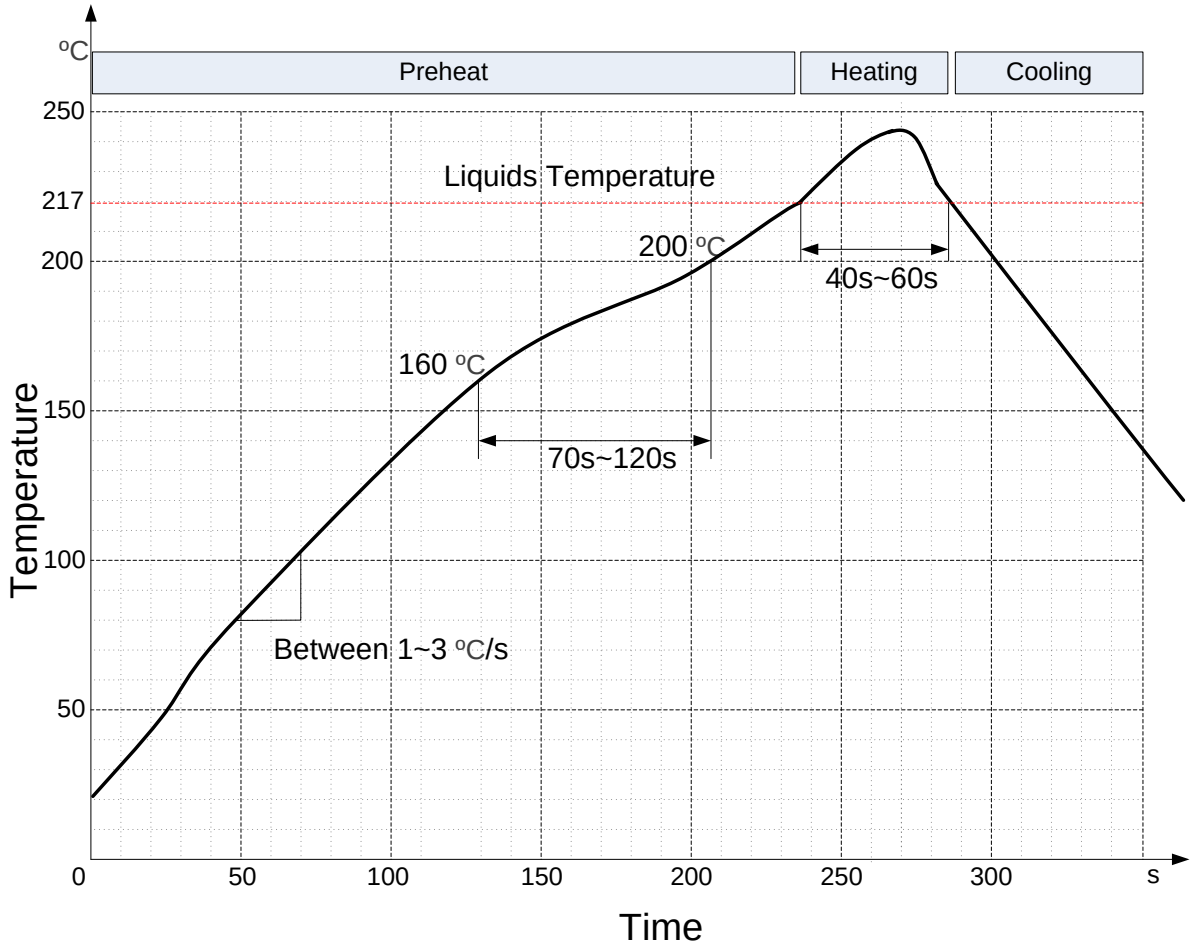


Figure 37: Reflow Soldering Thermal Profile

8.3. Packaging

BG96-QuecOpen is packaged in a vacuum-sealed bag which is ESD protected. The bag should not be opened until the devices are ready to be soldered onto the application.

The reel is 330mm in diameter and each reel contains 250 modules. The following figures show the packaging details, measured in mm.

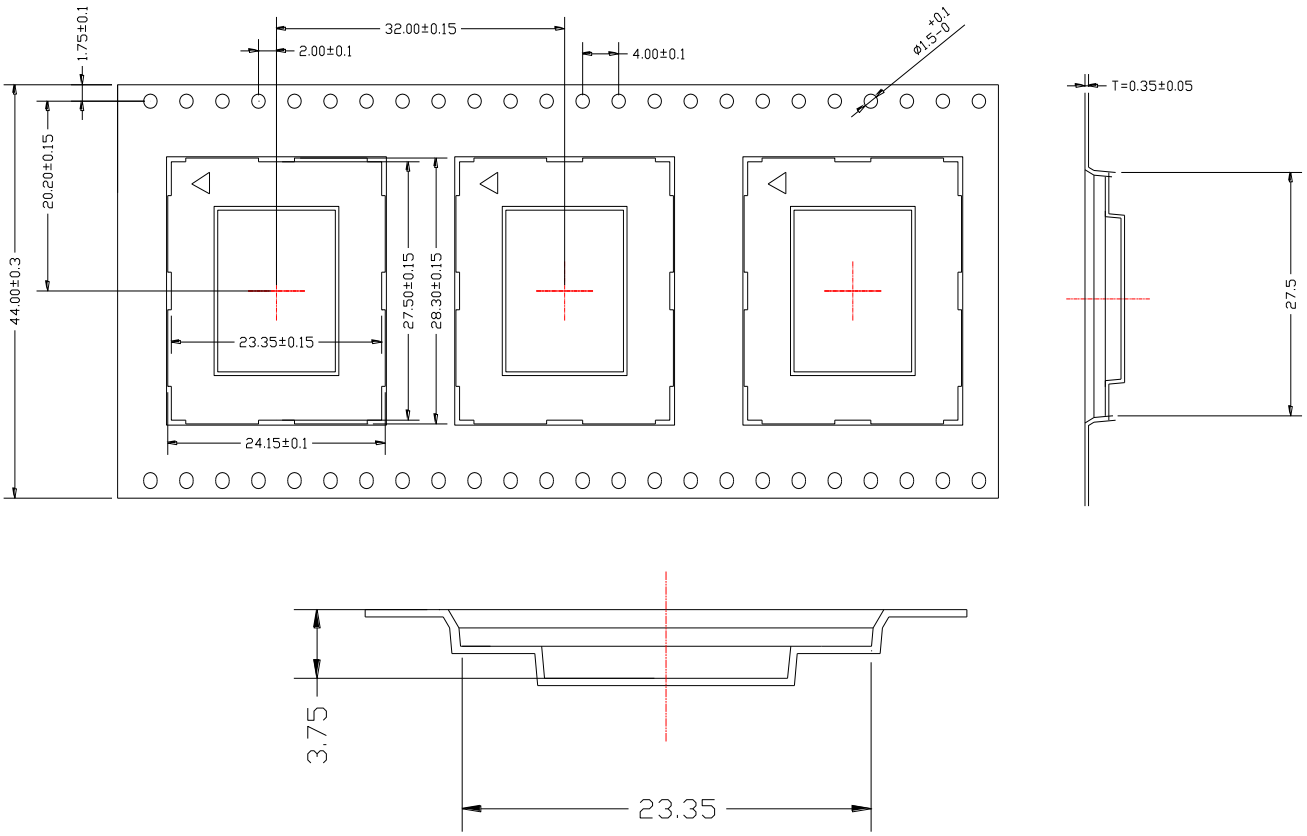


Figure 38: Tape Dimensions

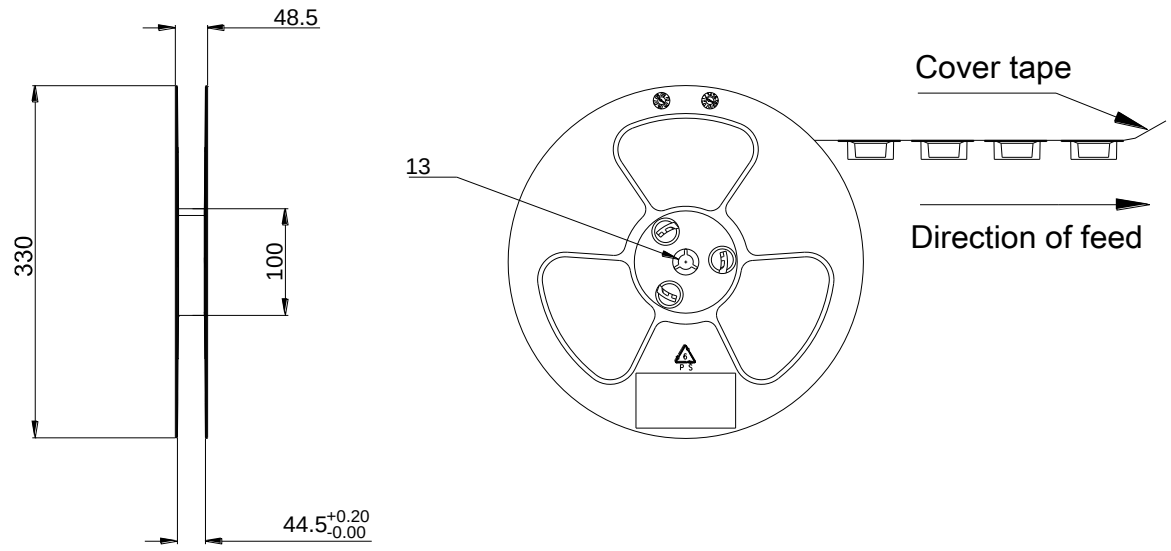


Figure 39: Reel Dimensions

Table 43: Reel Packaging

Model Name	MOQ for MP	Minimum Package: 250pcs	Minimum Package x 4=1000pcs
BG96	250pcs	Size: 370mm × 350mm × 56mm N.W: 0.78kg G.W: 1.46kg	Size: 380mm × 250mm × 365mm N.W: 3.1kg G.W: 6.45kg

9 Appendix A References

Table 44: Related Documents

SN	Document Name	Remark
[1]	Quectel_UMTS&LTE_EVB_User_Guide	UMTS&LTE EVB User Guide
[2]	Quectel_BG96_AT_Commands_Manual	BG96 AT Commands Manual
[3]	Quectel_BG96_GNSS_AT_Commands_Manual	BG96 GNSS AT Commands Manual
[4]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[5]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

Table 45: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core

ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSS	Home Subscriber Server
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SISO	Single Input Single Output
SMS	Short Message Service
TDD	Time Division Duplexing
TX	Transmitting Direction
UL	Uplink

UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
$V_I$max	Absolute Maximum Input Voltage Value
$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio

10 Appendix B GPRS Coding Schemes

Table 46: Description of Different Coding Schemes

Scheme	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

11 Appendix C GPRS Multi-slot Classes

Twenty-nine classes of GPRS multi-slot modes are defined for MS in GPRS specification. Multi-slot classes are product dependent, and determine the maximum achievable data rates in both the uplink and downlink directions. Written as 3+1 or 2+2, the first number indicates the amount of downlink timeslots, while the second number indicates the amount of uplink timeslots. The active slots determine the total number of slots the GPRS device can use simultaneously for both uplink and downlink communications.

The description of different multi-slot classes is shown in the following table.

Table 47: GPRS Multi-slot Classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
13	3	3	NA
14	4	4	NA

15	5	5	NA
16	6	6	NA
17	7	7	NA
18	8	8	NA
19	6	2	NA
20	6	3	NA
21	6	4	NA
22	6	4	NA
23	6	6	NA
24	8	2	NA
25	8	3	NA
26	8	4	NA
27	8	4	NA
28	8	6	NA
29	8	8	NA
30	5	1	6
31	5	2	6
32	5	3	6
33	5	4	6

12 Appendix D EDGE Modulation and Coding Schemes

Table 48: EDGE Modulation and Coding Schemes

Coding Schemes	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.60kbps	35.20kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps