[Microprocessor Applications]
Course Overview

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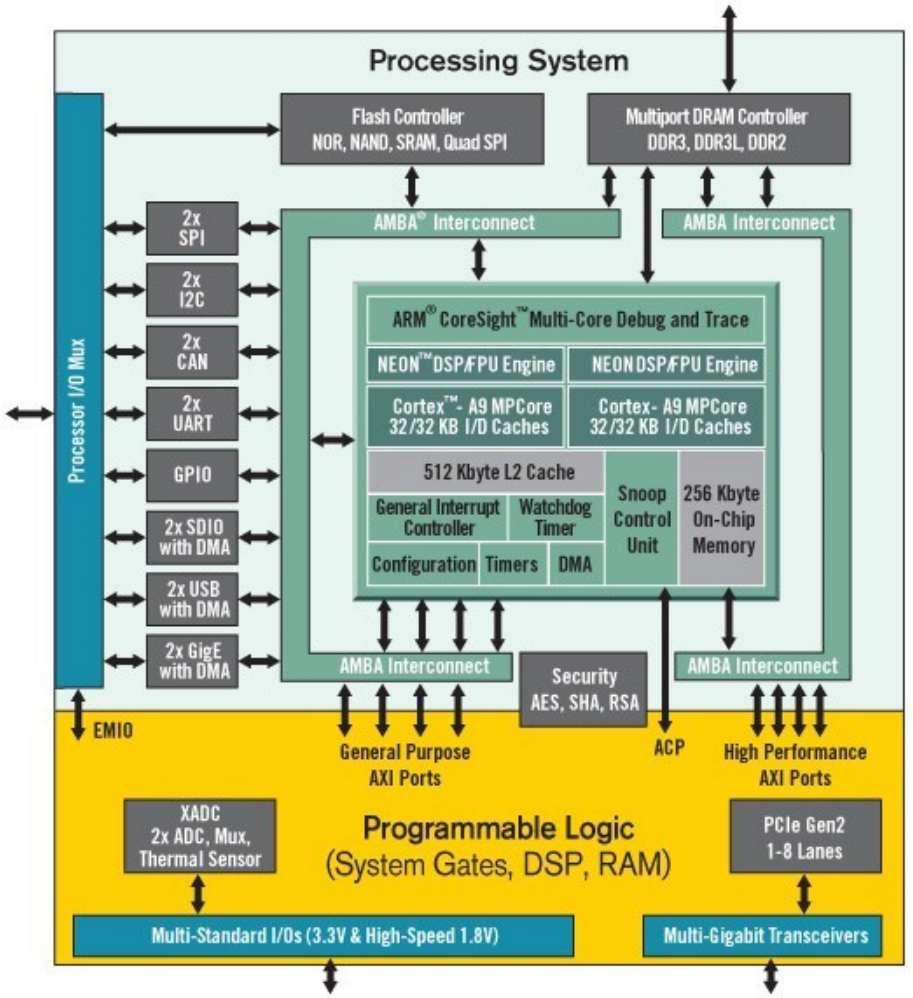
Objectives

- You should be able to
  - Understand the architecture of microprocessors from the programmers' point of view
    - ✓ Instruction set, coprocessor (SIMD), bus, memory, I/O peripherals, interrupt etc.
  - Understand the architecture of the target microcontroller (Xilinx ZYNQ – PS)
  - Optimize a program running on the target microcontroller in terms of speed, size etc.
  - Implement your own microprocessor-based system (e.g., neural networks for hand-writing recognition)

Target Microcontroller

- Xilinx ZYNQ7020 (PS)



Target Microcontroller

- Xilinx ZYNQ7020 (PS) (cont'd)

Vivado

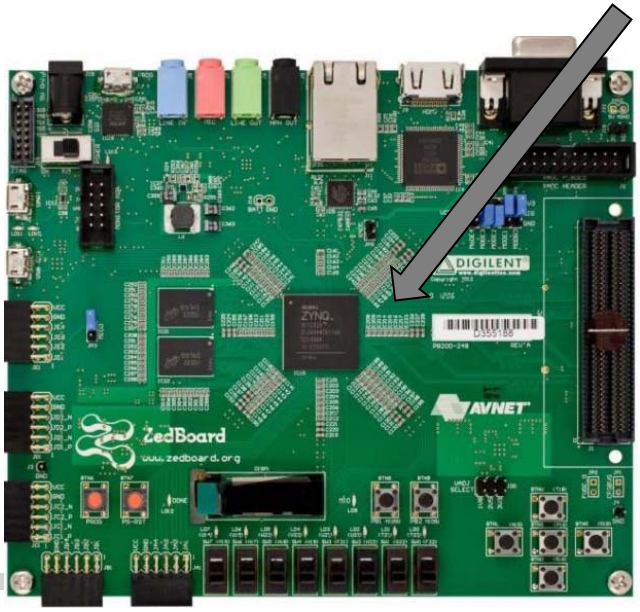
1. Launch Vivado
2. Create IP block [IP integrator]
3. Configuration PS settings
4. Add IP
5. Add Top-Level HDL
6. Add Constraints file
7. Add Generate Bitstream
8. Export hardware to SDK

SDK

9. Specify hardware built from Vivado
10. Add software project & build
11. Program bitstream

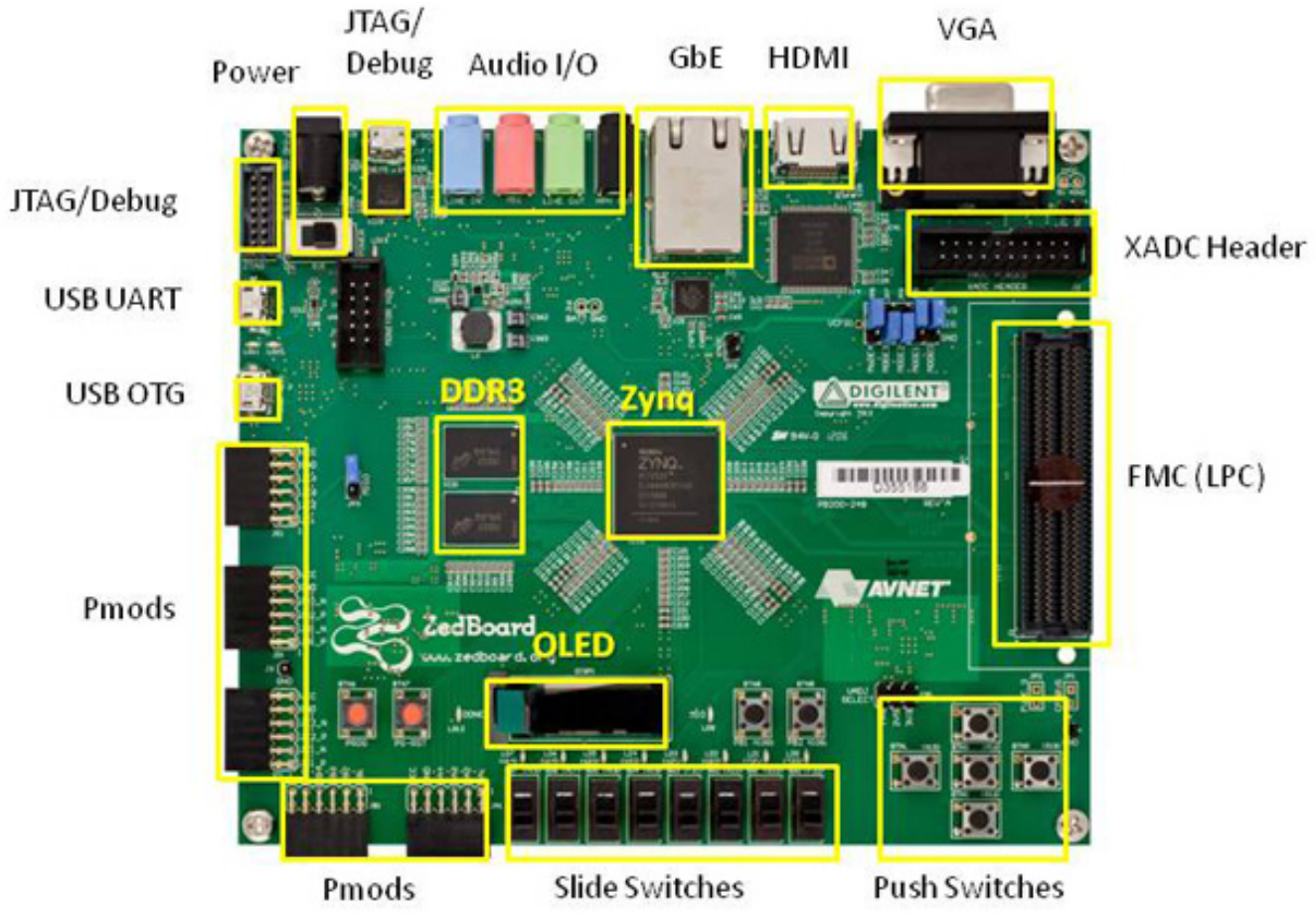
SDK
Xilinx SDK

ZYNQ/ZedBoard



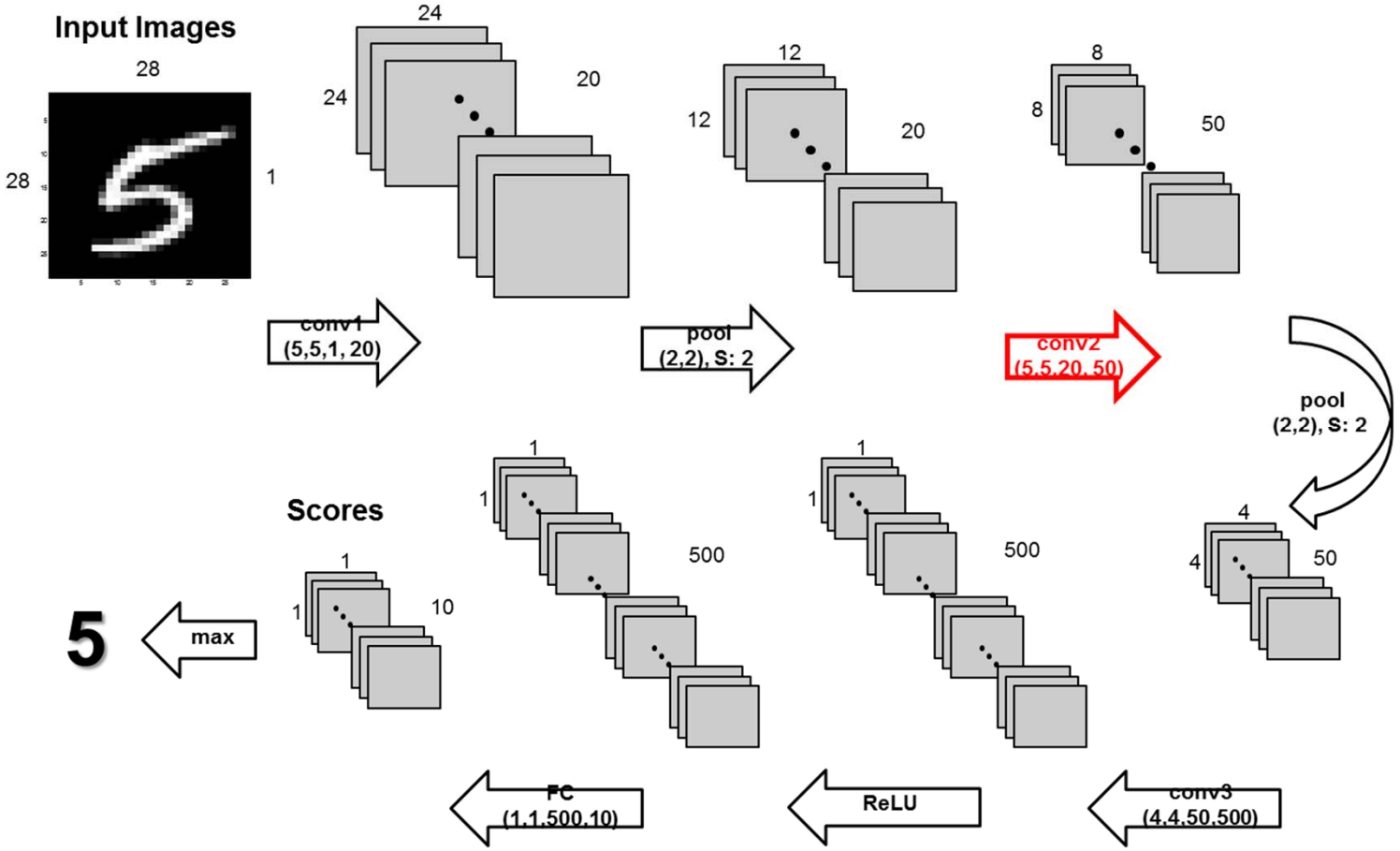
Target Board

- Avnet Zedboard



Microprocessor-Based System

- Example: neural network for hand-writing recognition

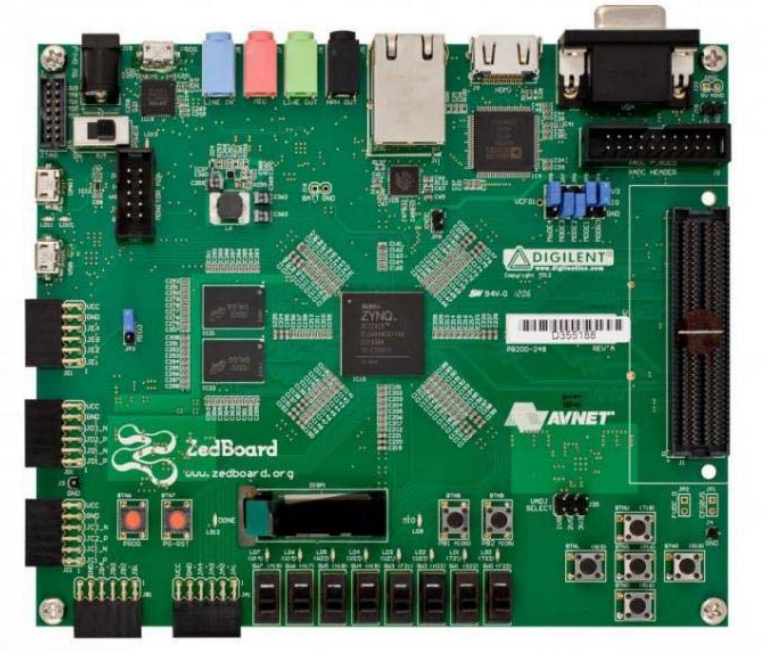


Lectures

- Focus on the topics relevant to the labs
  - Instruction set
  - Coprocessor
  - Memory/cache
  - Interrupt/DMA
  - I/O peripherals
- Knowledge of computer architectures considered as a plus
  - In particular, how every instruction of a program is executed on a *cache-based* microprocessor

Labs

- Focus on the topics that are useful to your term project
  - Assembly programming (ARM)
  - Code optimization (ARM)
  - Memory/cache (ZYNQ)
  - Interrupt/DMA (ARM/ZYNQ)
  - I/O peripherals (ZYNQ)
  - Bus (AXI)



Term Project - Presentation & Demo

- Presentation & Demo
  - Team-presentation with exactly the same **slideset file** as submitted before the due date
  - Team-demo with exactly the same **SDK folder** as submitted before the due date

1. *Bring a storage device (e.g., HDD) having the entire **project folder** just in case (e.g., when the SDK folder does not work)*
2. *Note that any progress made later than **the due date** can**not** be counted for evaluation*

Demo (SoC Design 2017):
https://www.sites.google.com/site/kusocdesignlab/demos/cnnacceleratoronzynq