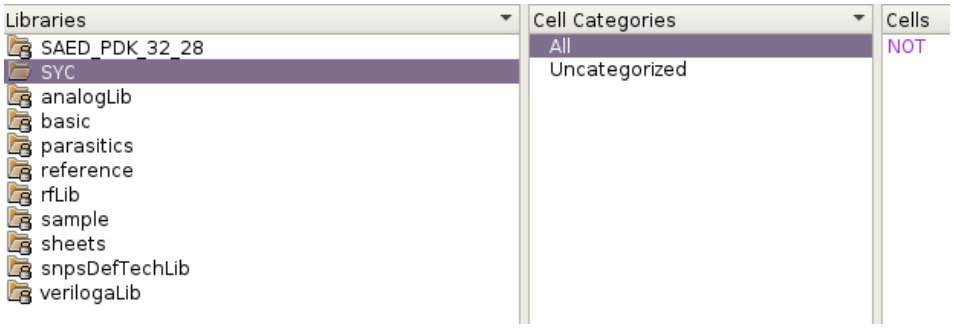
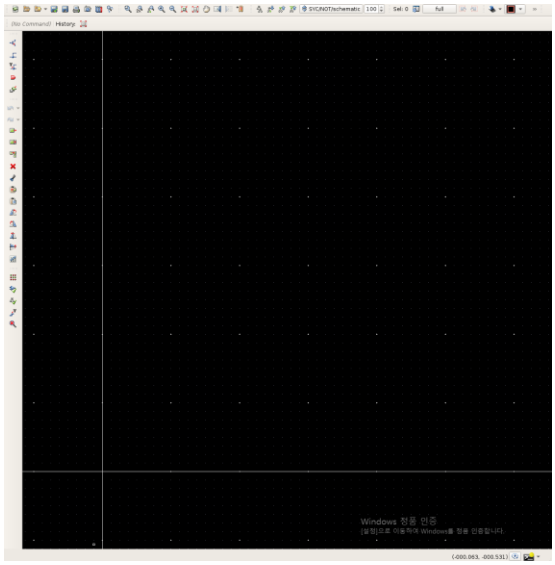
250616

```
[aedu21@kccisynop2 /home/aedu21] source /home/env/env_tools.csh
[aedu21@kccisynop2 /home/aedu21] custom_compiler &
[1] 1729722
[aedu21@kccisynop2 /home/aedu21]
```

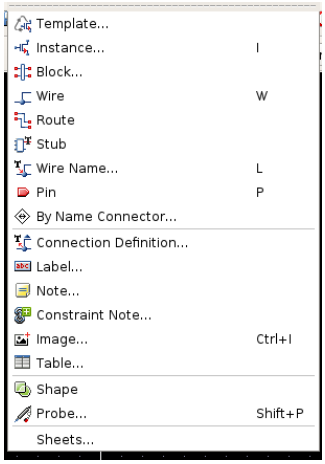
⇨ Custom compiler 실행


=> library 생성(SYC) cf) 32nm 환경에서 실습할 예정



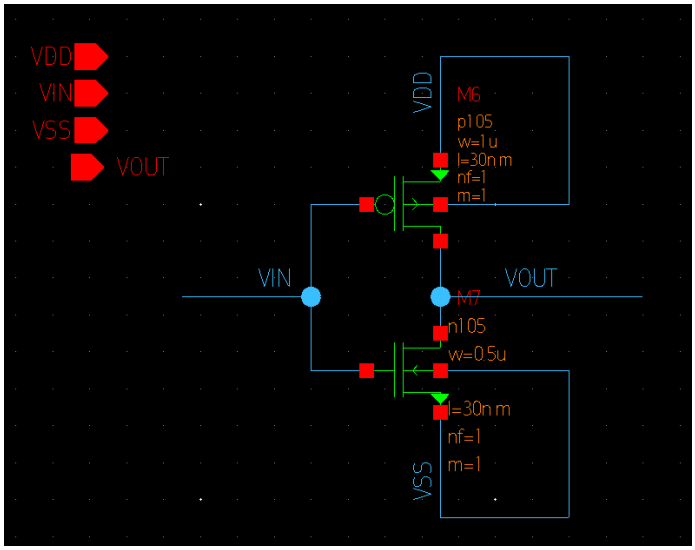
=> F : 화면 가운데로 보여줌



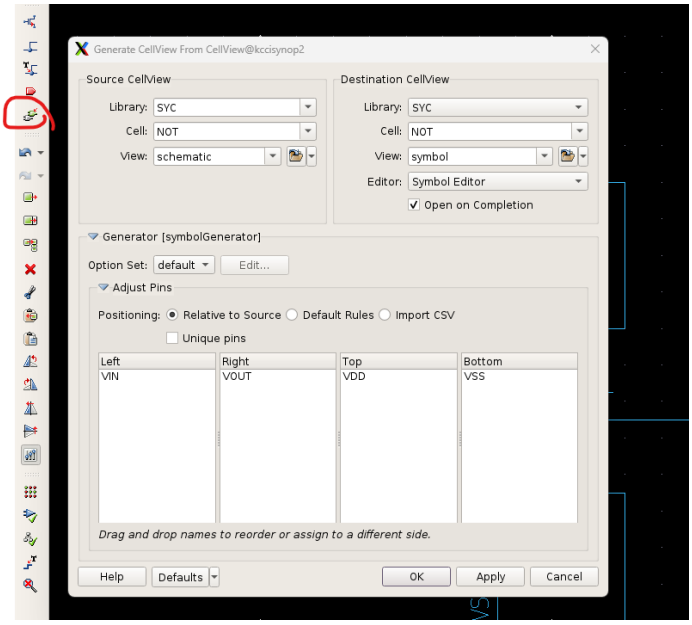

참고: 단축키

```
[aedu21@kccisynop2 /home/aedu21] cd SYC
total 12
drwxr-xr-x  3 aedu21 aedu21   62 Jun 16 15:16 .
drwxr-xr-x 12 aedu21 aedu21 4096 Jun 16 15:27 ..
-rw-r--r--  1 aedu21 aedu21  142 Jun 16 15:13 .oalib
drwxr-xr-x  3 aedu21 aedu21   23 Jun 16 15:16 NOT
-rw-r--r--  1 aedu21 aedu21 3220 Jun 16 15:13 data.dm
[aedu21@kccisynop2 /home/aedu21/SYC] cd NOT
total 0
drwxr-xr-x 3 aedu21 aedu21  23 Jun 16 15:16 .
drwxr-xr-x 3 aedu21 aedu21  62 Jun 16 15:16 ..
drwxr-xr-x 2 aedu21 aedu21 126 Jun 16 15:16 schematic
[aedu21@kccisynop2 /home/aedu21/SYC/NOT] cd schematic/
total 24
drwxr-xr-x 2 aedu21 aedu21  126 Jun 16 15:16 .
drwxr-xr-x 3 aedu21 aedu21   23 Jun 16 15:16 ..
-rw-r--r-- 1 aedu21 aedu21   35 Jun 16 15:16 master.tag
-rw-r--r-- 1 aedu21 aedu21 6124 Jun 16 15:16 sch.oa
-rw-r--r-- 2 aedu21 aedu21  647 Jun 16 15:16 sch.oa.cdslck
-rw-r--r-- 2 aedu21 aedu21  647 Jun 16 15:16 sch.oa.cdslck.RHEL30.kccisynop2.1729722
-rw-r--r-- 1 aedu21 aedu21  411 Jun 16 15:16 snapshot.png
[aedu21@kccisynop2 /home/aedu21/SYC/NOT/schematic] rm sch.oa.cdslck
[aedu21@kccisynop2 /home/aedu21/SYC/NOT/schematic]
```

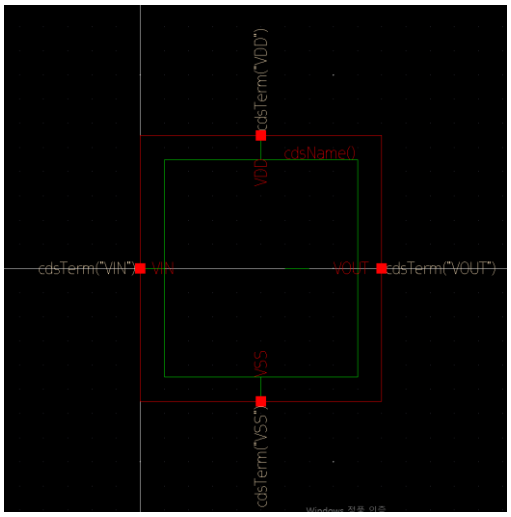
=> 파일에서 read only라는 warning이 발생했을 경우 해결방안. Lock file remove



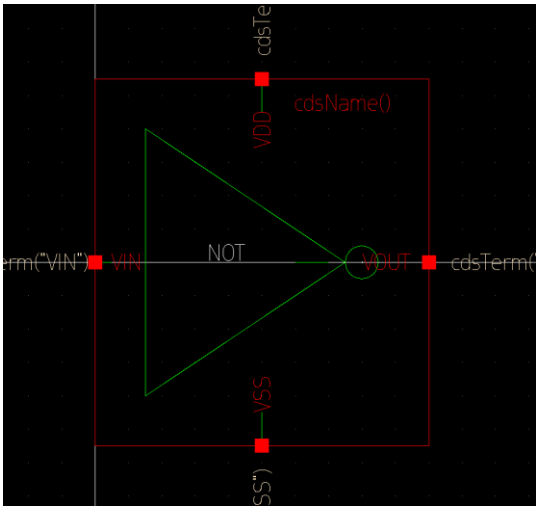

=> label을 이용해서 pin(input, output)에 직접 연결하지 않고 진행



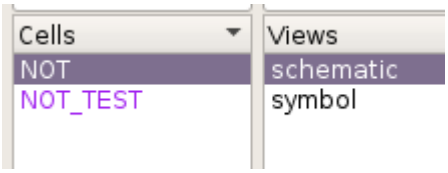

=> generate cellview => symbol 생성



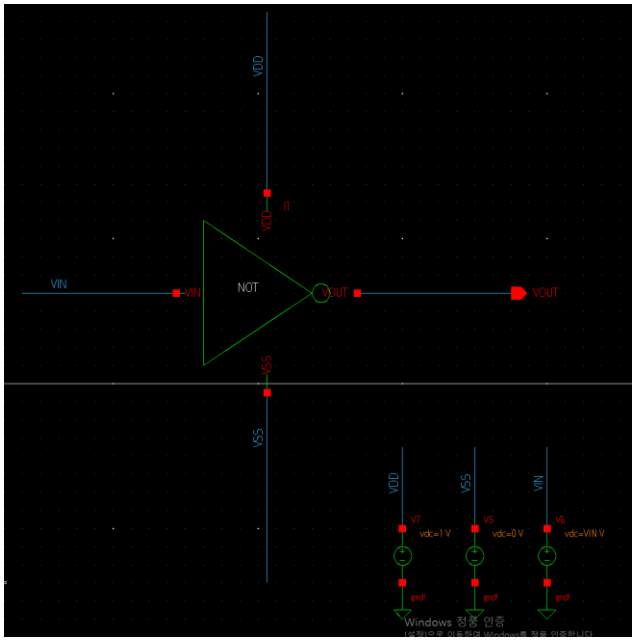

=>



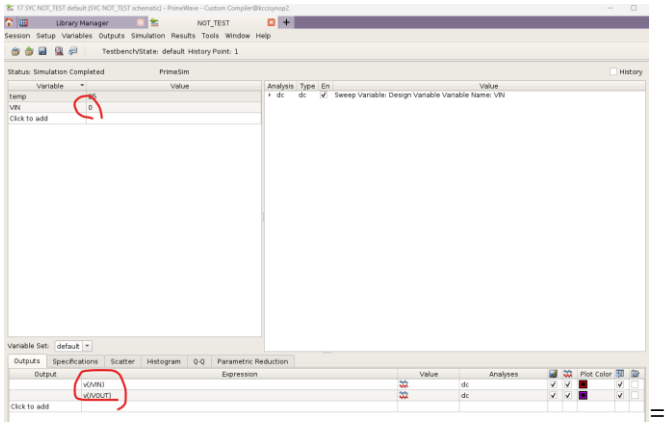

=> NOT gate symbol 생성 (초록색 모양 조정가능)




=> + layout 추가할 예정




Vdc를 누르고 Q입력 => 전압조정가능

=> dc sweep 0~1V 0.01씩 증가