

과제구현내용

제출자:서윤철

개요

- I. 소개
- II. Button debounce
- III. FSM
- IV. 전자레인지

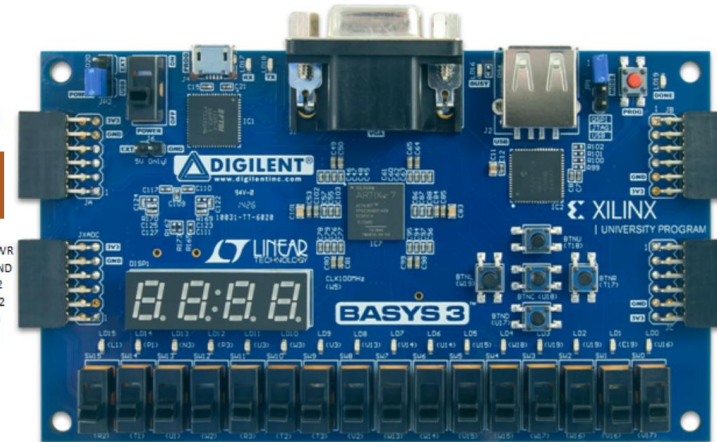
소개



Down CNT

사용한 핀

JA12: J1	JA6: PWR
JA11: GND	JA5: GND
JA10: G3	JA4: G3
JA9: H2	JA3: J2
JA8: K2	JA2: L2
JA7: H1	JA1: J1
JXAC12: PWR	JXAC6: PWR
JXAC11: GND	JXAC5: GND
JXAC10: N1	JXAC4: N2
JXAC9: M1	JXAC3: M2
JXAC8: M3	JXAC2: L3
JXAC7: K3	JXAC1: J3



JB1: A14	JB7: A15
JB2: A16	JB8: A17
JB3: B15	JB9: C15
JB4: B16	JB10: C16
JB5: GND	JB11: GND
JB6: PWR	JB12: PWR
JC1: K17	JC7: L17
JC2: M18	JC8: M19
JC3: N17	JC9: P17
JC4: P18	JC10: R18
JC5: GND	JC11: GND
JC6: PWR	JC12: PWR

FPGA TEST

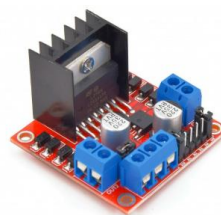
Verilog

• Design



Vivado

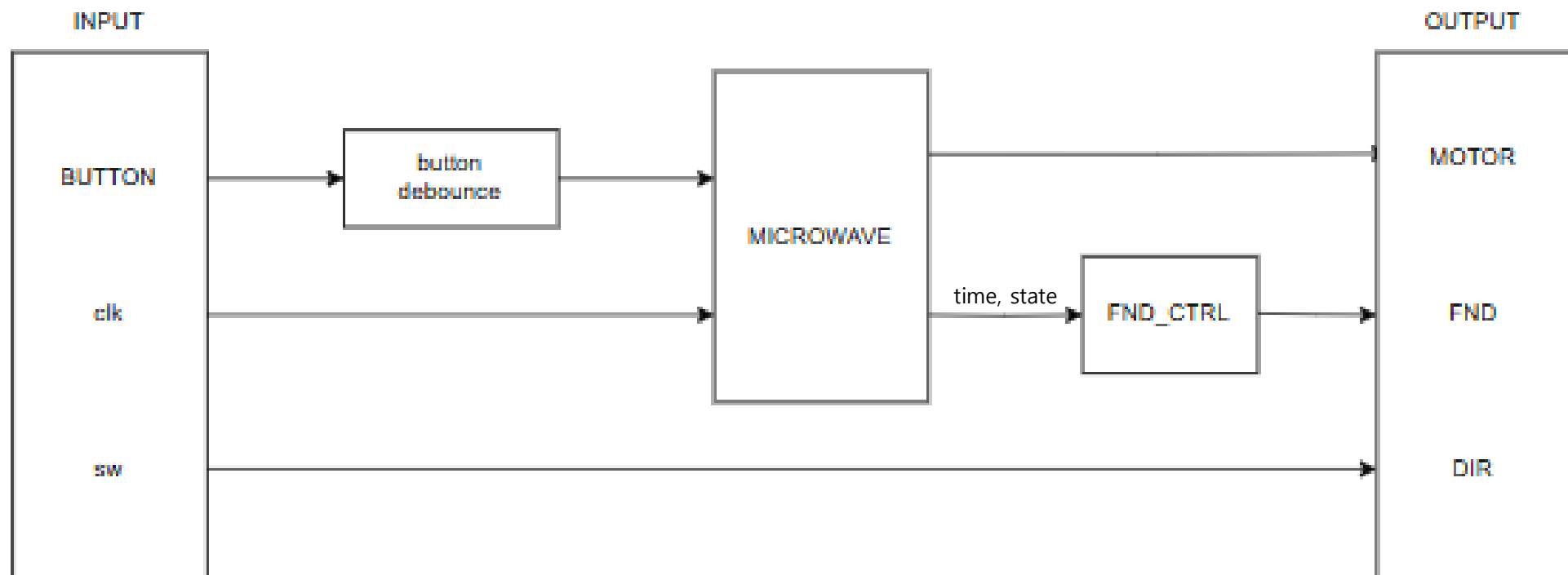
- Simulation
- Synthesis
- Bitstream



L298N Dual H-Bridge Motor Controller

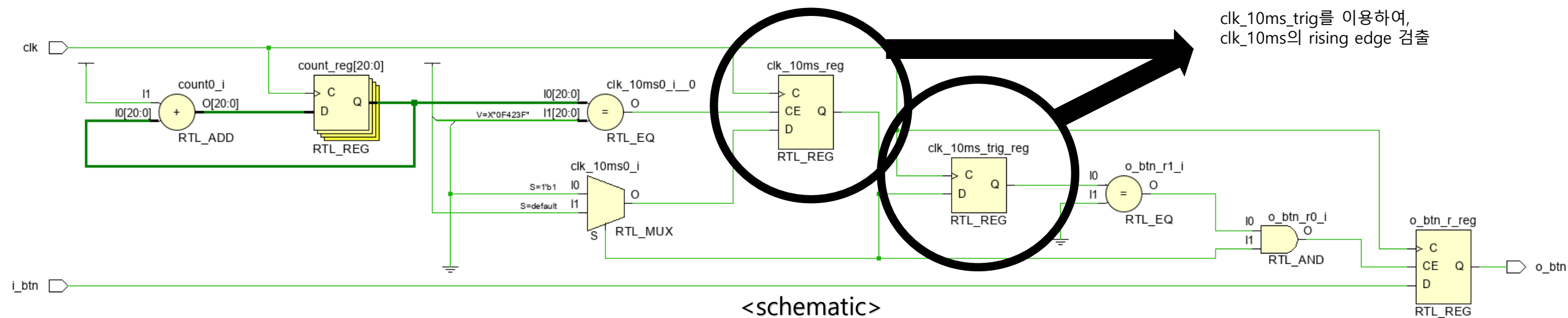
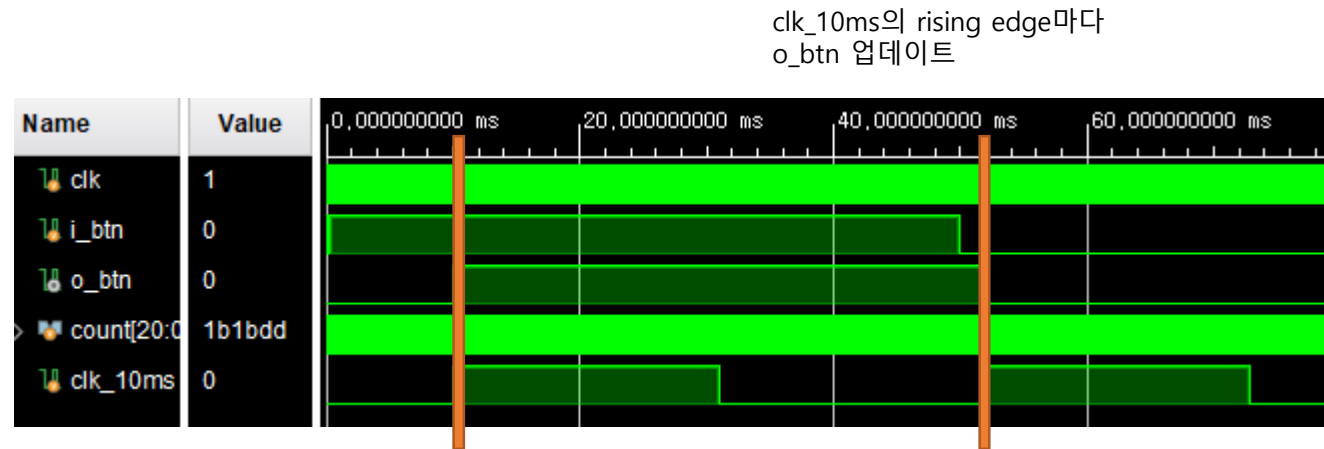
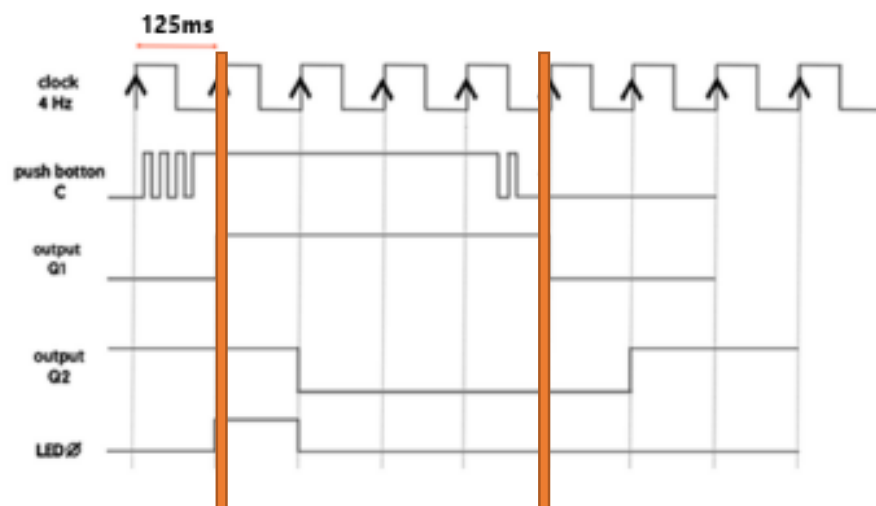


FAN

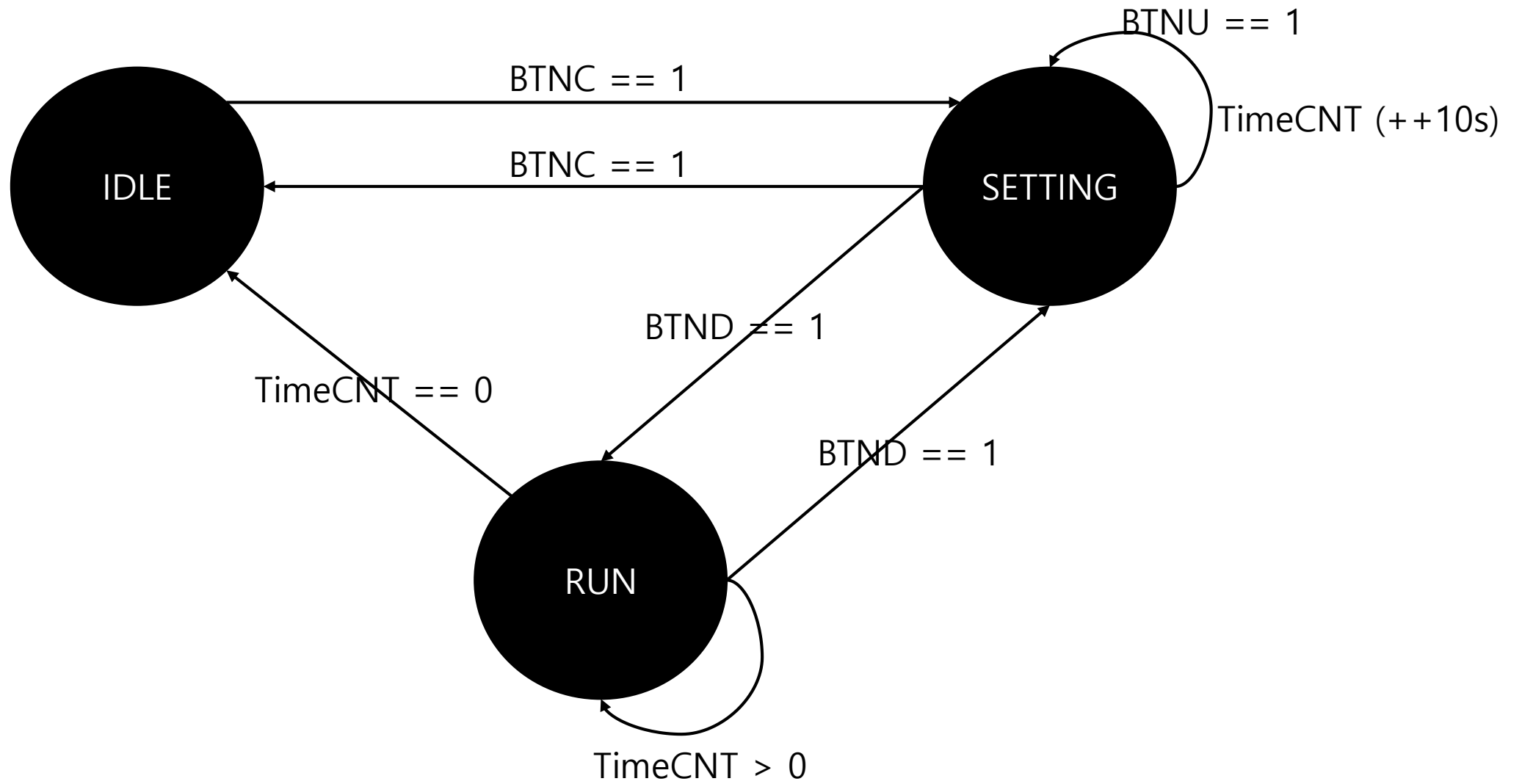


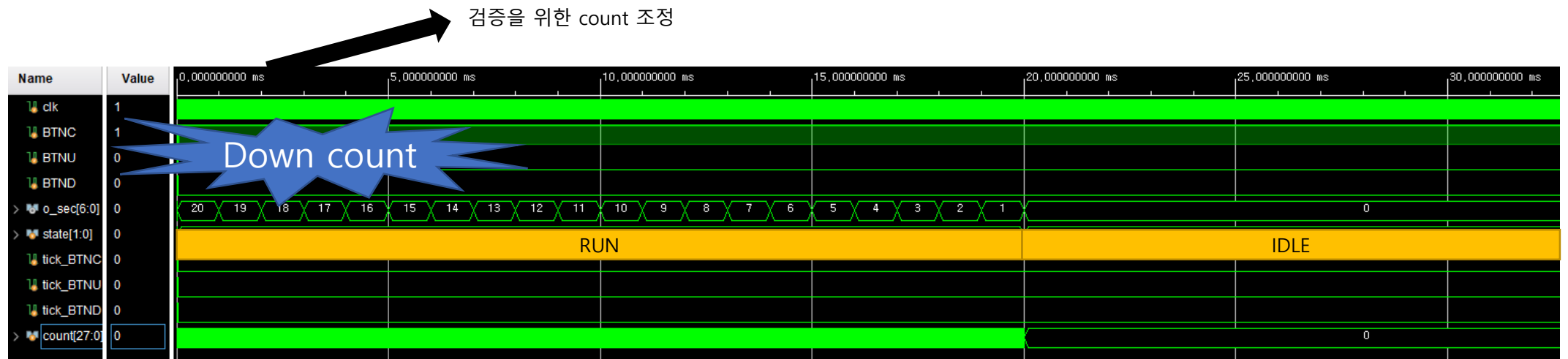
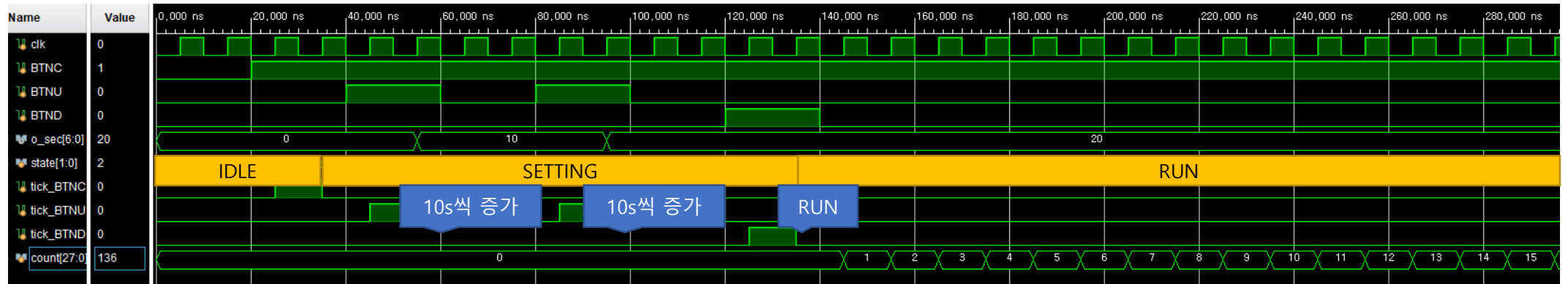
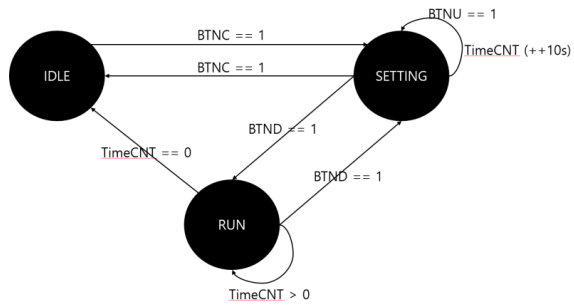
<architecture>

Button debounce



FSM





<simulation>

전자레인지



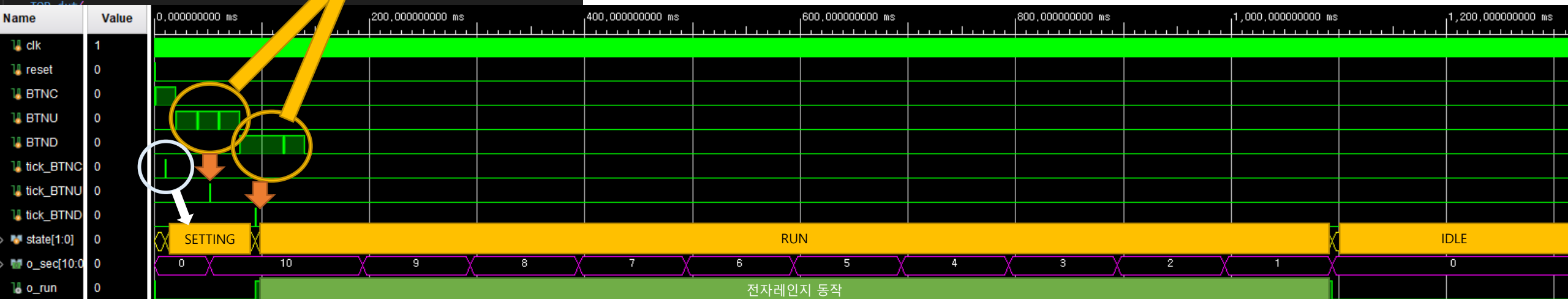
timescale 1ns / 1ps

```
module tb_TOP();
  reg clk;
  reg [1:0] motor_direction;
  reg reset;
  reg BTNC;
  reg BTNU;
  reg BTND;
  wire o_run;
  wire [3:0] o_state;
  wire [1:0] in1_in2;
  wire [7:0] fnd_data;
  wire [3:0] fnd_com;

  TOP dut(

```

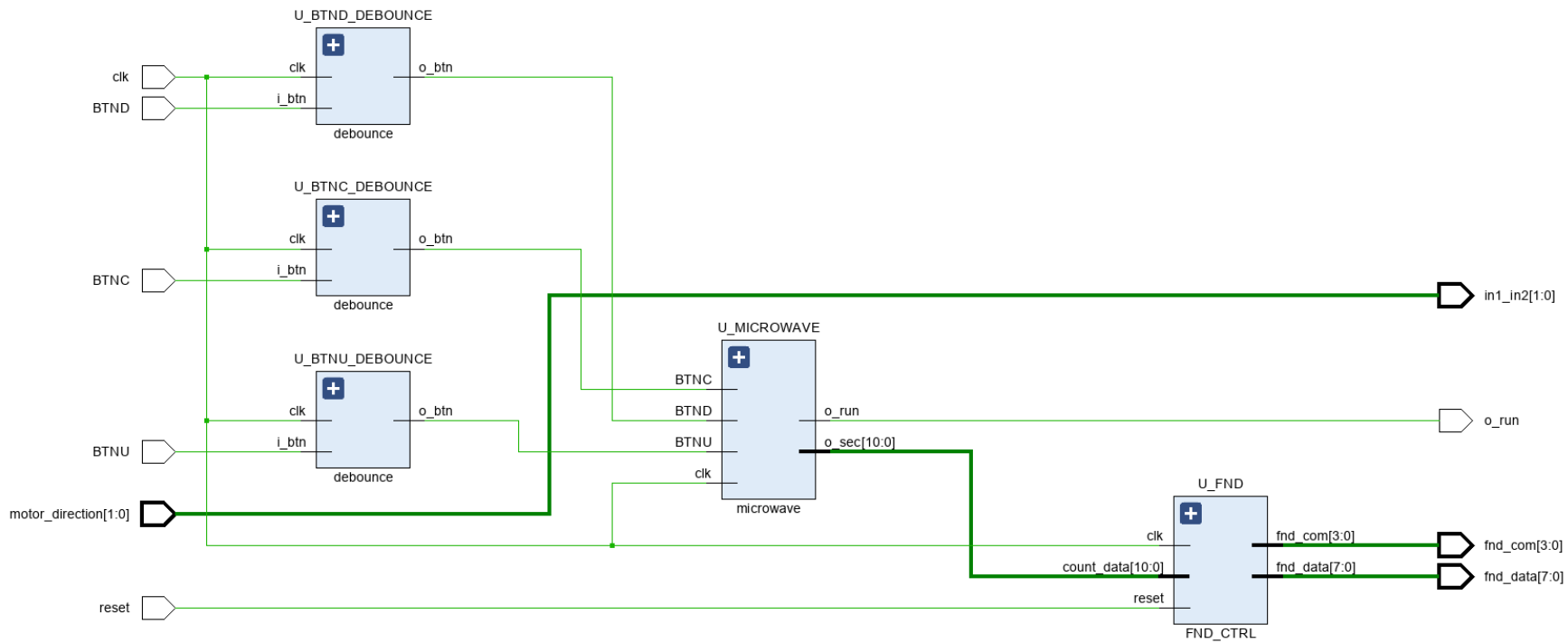
버튼 디바운스와 tick_gen을 이용하여
틱 한번 발생.



<simulation>

```
#20; reset = 0;
#1000; BTNC = 1;
#20000000; BTNC = 0;
#100; BTNU = 1;
#20000000; BTNU = 0;
#100; BTNU = 1;
#20000000; BTNU = 0;
#100; BTNU = 1;
#20000000; BTNU = 0;
#100; BTND = 1; //RUN
#20000000; BTND = 0;
#(3000000*1000); BTND = 1;
#20000000; BTND = 0;
#100; BTND = 1;
#20000000; BTND = 0;
#(2000000*1000); //IDLE
$stop;
end
endmodule
```

<testbench>



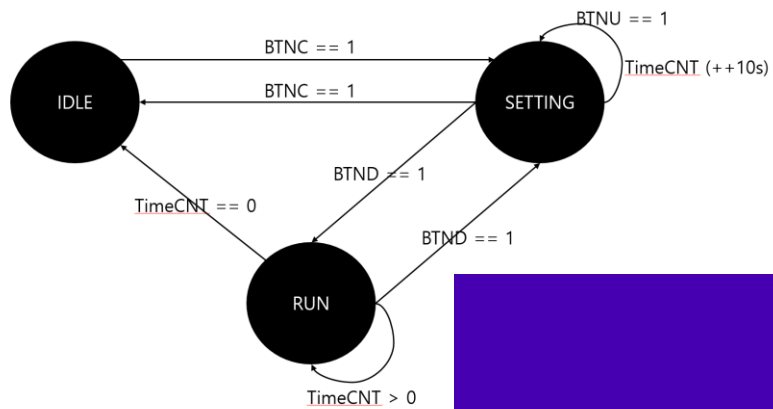
<schematic>

## Clock signal	
set_property -dict { PACKAGE_PIN W5 IOSTANDARD LVCMOS33 }	[get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5}	[get_ports clk]
## Switches	
set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 }	[get_ports {a[0]]
	[get_ports {a[1]]
	[get_ports {motor_direction[0]]
	[get_ports {motor_direction[1]]
	[get_ports {a[4]]
set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 }	[get_ports {a[5]]
set_property -dict { PACKAGE_PIN W14 IOSTANDARD LVCMOS33 }	[get_ports {a[6]]
set_property -dict { PACKAGE_PIN W13 IOSTANDARD LVCMOS33 }	[get_ports {a[7]]
set_property -dict { PACKAGE_PIN V2 IOSTANDARD LVCMOS33 }	[get_ports {b[0]]
set_property -dict { PACKAGE_PIN T3 IOSTANDARD LVCMOS33 }	[get_ports {b[1]]
set_property -dict { PACKAGE_PIN T2 IOSTANDARD LVCMOS33 }	[get_ports {b[2]]
set_property -dict { PACKAGE_PIN R3 IOSTANDARD LVCMOS33 }	[get_ports {b[3]]
set_property -dict { PACKAGE_PIN W2 IOSTANDARD LVCMOS33 }	[get_ports {b[4]]
set_property -dict { PACKAGE_PIN U1 IOSTANDARD LVCMOS33 }	[get_ports {b[5]]
set_property -dict { PACKAGE_PIN T1 IOSTANDARD LVCMOS33 }	[get_ports {b[6]]
set_property -dict { PACKAGE_PIN R2 IOSTANDARD LVCMOS33 }	[get_ports {b[7]]
## LEDs	
	[get_ports {o_state[0]]
State 확인용(LED)	
	[get_ports {o_state[1]]
	[get_ports {o_state[2]]
	[get_ports {o_state[3]]
set_property -dict { PACKAGE_PIN W18 IOSTANDARD LVCMOS33 }	[get_ports {cout}]
set_property -dict { PACKAGE_PIN U15 IOSTANDARD LVCMOS33 }	[get_ports {led[5]]
set_property -dict { PACKAGE_PIN U14 IOSTANDARD LVCMOS33 }	[get_ports {led[6]]
set_property -dict { PACKAGE_PIN V14 IOSTANDARD LVCMOS33 }	[get_ports {led[7]]
set_property -dict { PACKAGE_PIN V13 IOSTANDARD LVCMOS33 }	[get_ports {led[8]]
set_property -dict { PACKAGE_PIN V3 IOSTANDARD LVCMOS33 }	[get_ports {led[9]]
set_property -dict { PACKAGE_PIN W3 IOSTANDARD LVCMOS33 }	[get_ports {led[10]]
set_property -dict { PACKAGE_PIN U3 IOSTANDARD LVCMOS33 }	[get_ports {led[11]]
set_property -dict { PACKAGE_PIN P3 IOSTANDARD LVCMOS33 }	[get_ports {led[12]]
set_property -dict { PACKAGE_PIN R3 IOSTANDARD LVCMOS33 }	[get_ports {led[13]]
set_property -dict { PACKAGE_PIN P1 IOSTANDARD LVCMOS33 }	[get_ports {led[14]]
set_property -dict { PACKAGE_PIN L1 IOSTANDARD LVCMOS33 }	[get_ports {led[15]]
##7 Segment Display	
	[get_ports {fnd_data[0]]
	[get_ports {fnd_data[1]]
	[get_ports {fnd_data[2]]
	[get_ports {fnd_data[3]]
	[get_ports {fnd_data[4]]
	[get_ports {fnd_data[5]]
	[get_ports {fnd_data[6]]
	[get_ports {fnd_data[7]]
FND COM	
	[get_ports {fnd_com[0]]
	[get_ports {fnd_com[1]]
	[get_ports {fnd_com[2]]
	[get_ports {fnd_com[3]]
##Buttons	
	[get_ports BTNC]
	[get_ports BTNU]
	[get_ports reset]
	[get_ports sw[1]]
	[get_ports BTND]
##DC Motor PWM control	
	[get_ports {o_run}];#Sch name = JA1
	[get_ports {in1_in2[0]};#Sch name = JA2
	[get_ports {in1_in2[1]};#Sch name = JA3
	[get_ports {JA[3]};#Sch name = JA4
	[get_ports {JA[4]};#Sch name = JA5

<constraint>

시연영상



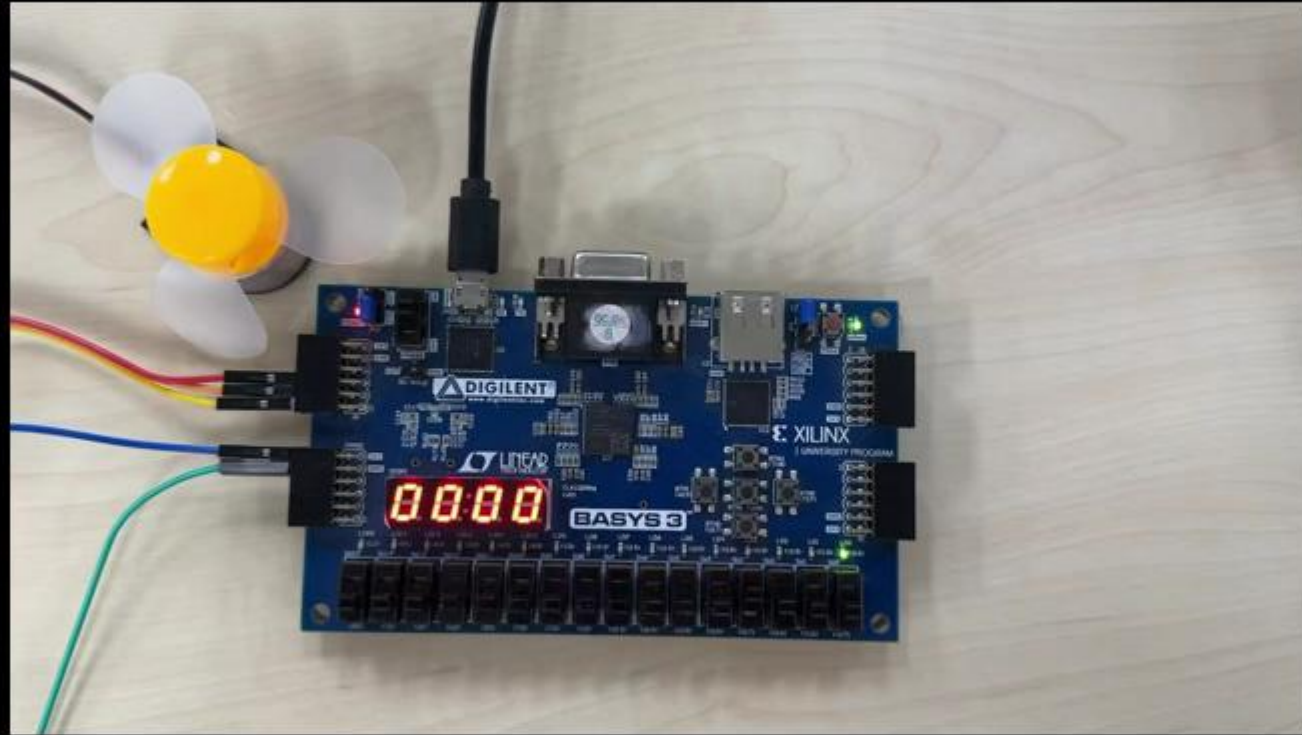
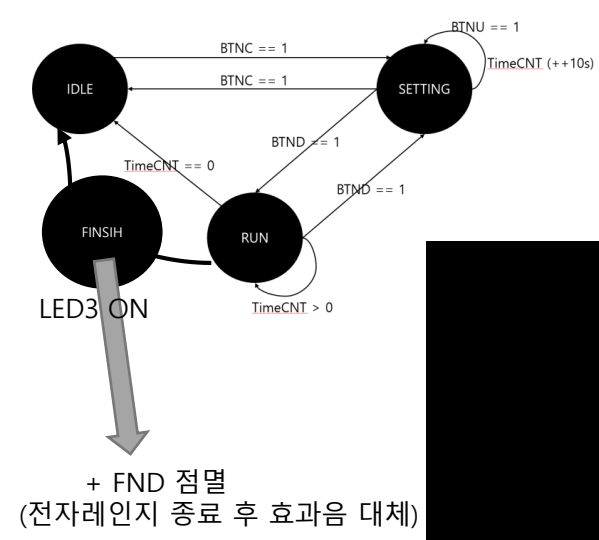


전자렌지 시연영상

서윤철

전자레인지.v2





추가 모듈

