

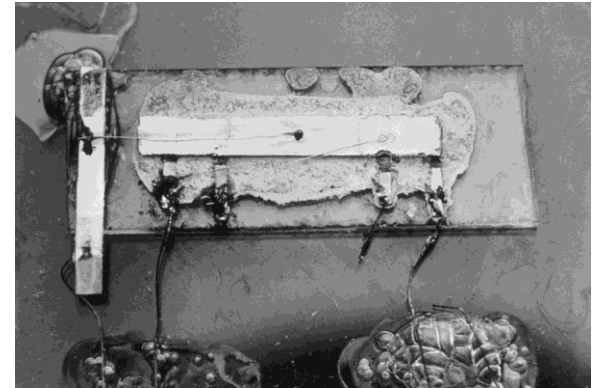
Lecture 1: Circuits & Layout

Outline

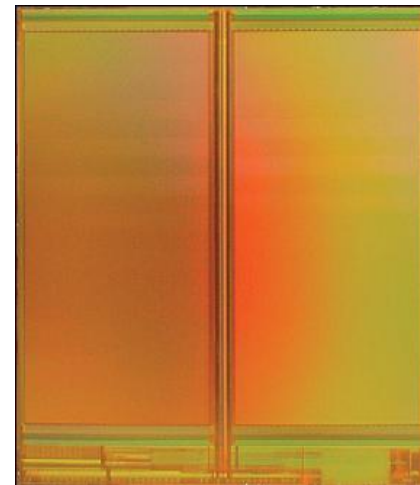
- ☐ A Brief History
- ☐ CMOS Gate Design
- ☐ Pass Transistors
- ☐ CMOS Latches & Flip-Flops
- ☐ Standard Cell Layouts
- ☐ Stick Diagrams

A Brief History

- ❑ 1958: First integrated circuit
 - Flip-flop using two transistors
 - Built by Jack Kilby at Texas Instruments
- ❑ 2010
 - Intel Core i7 μ processor
 - 2.3 billion transistors
 - 64 Gb Flash memory
 - > 16 billion transistors



Courtesy Texas Instruments



[Trinh09]
© 2009 IEEE

Growth Rate

- ❑ 53% compound annual growth rate over 50 years
 - No other technology has grown so fast so long
- ❑ Driven by miniaturization of transistors
 - Smaller is cheaper, faster, lower in power!
 - Revolutionary effects on society

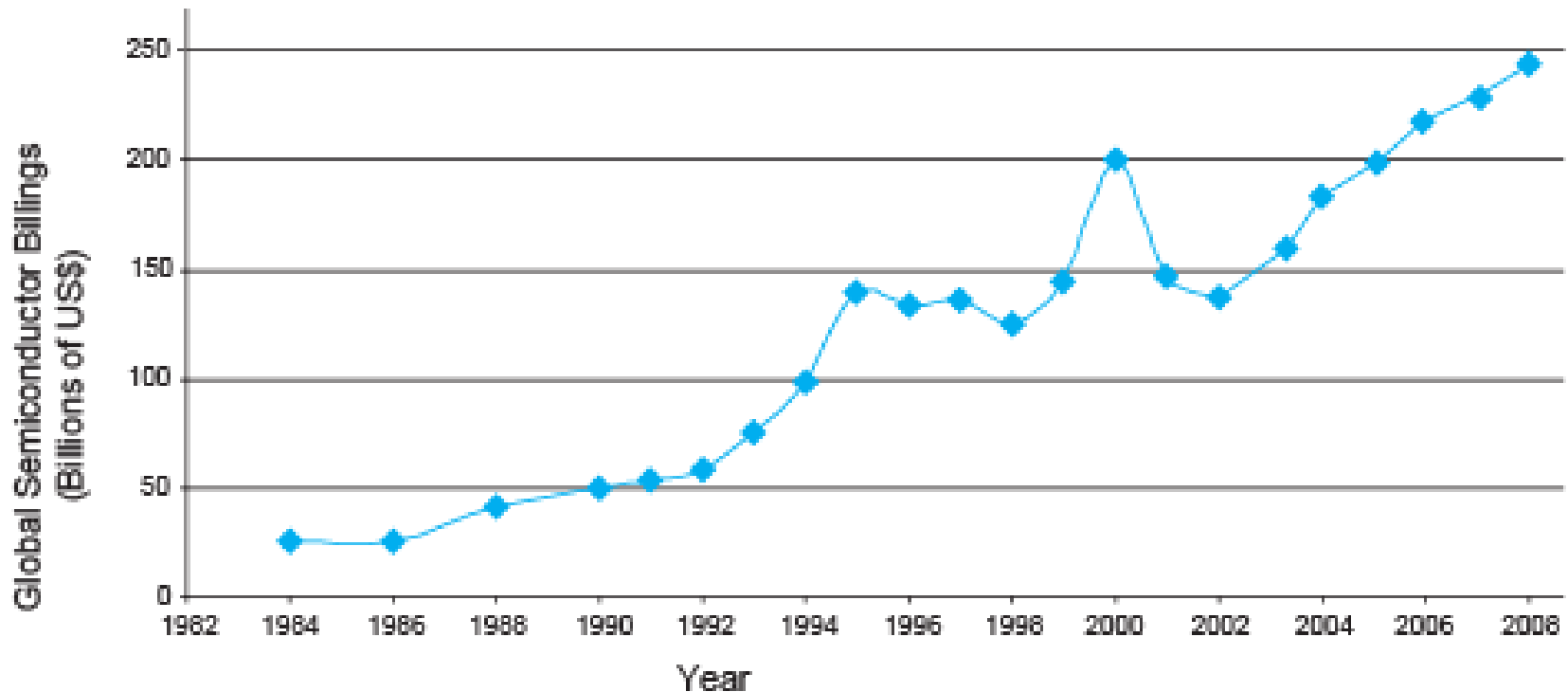


[Moore65]

Electronics Magazine

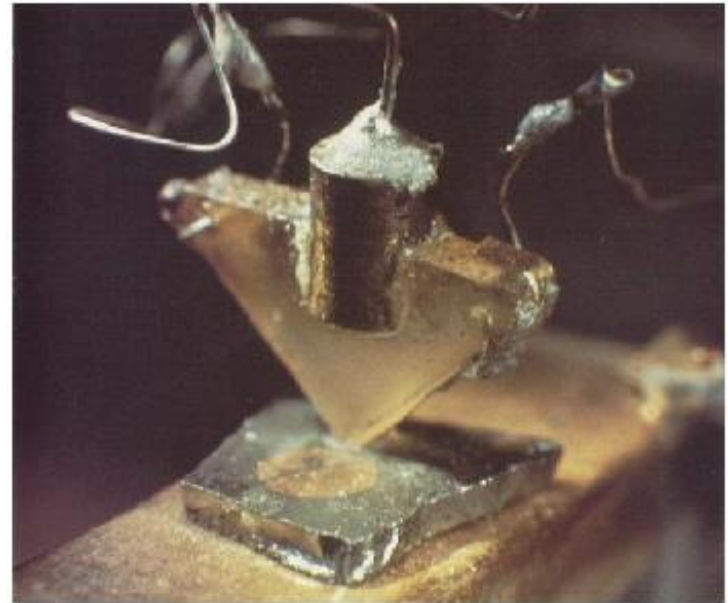
Annual Sales

- ❑ $>10^{19}$ transistors manufactured in 2008
 - 1 billion for every human on the planet



Invention of the Transistor

- ❑ Vacuum tubes ruled in first half of 20th century Large, expensive, power-hungry, unreliable
- ❑ 1947: first point contact transistor
 - John Bardeen and Walter Brattain at Bell Labs
 - See *Crystal Fire* by Riordan, Hodgeson



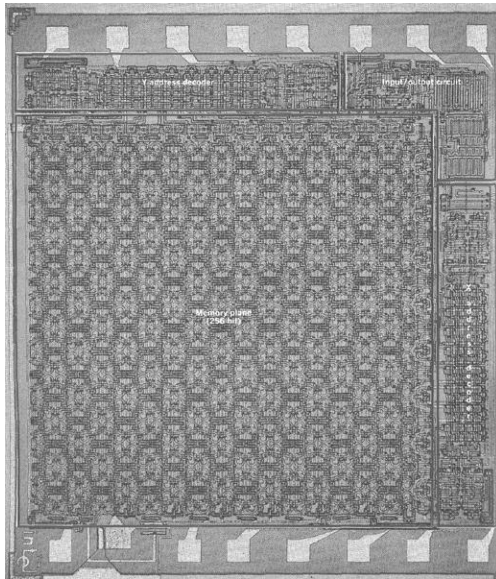
AT&T Archives.
Reprinted with
permission.

Transistor Types

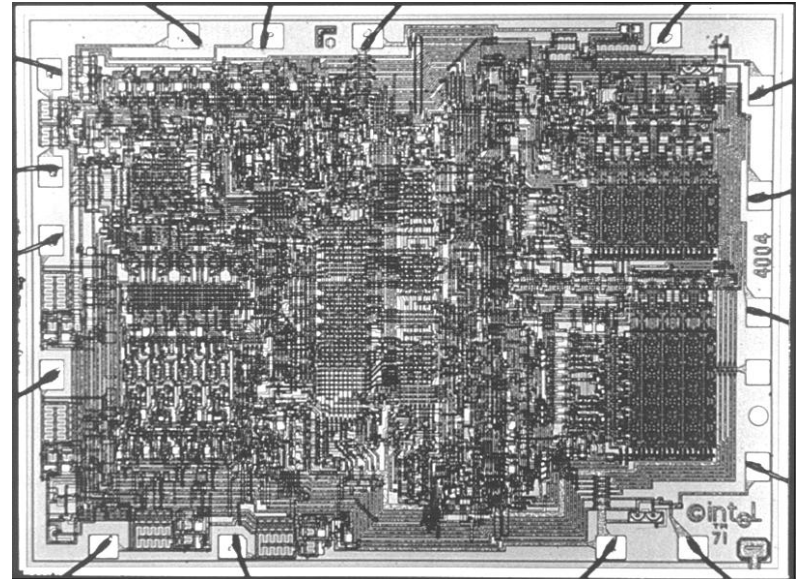
- ❑ Bipolar transistors
 - npn or pnp silicon structure
 - Small current into very thin base layer controls large currents between emitter and collector
 - Base currents limit integration density
- ❑ Metal Oxide Semiconductor Field Effect Transistors
 - nMOS and pMOS MOSFETS
 - Voltage applied to insulated gate controls current between source and drain
 - Low power allows very high integration

MOS Integrated Circuits

- ❑ 1970's processes usually had only nMOS transistors
 - Inexpensive, but consume power while idle



[Vadasz69]
© 1969 IEEE.



Intel
Museum.
Reprinted
with
permission.

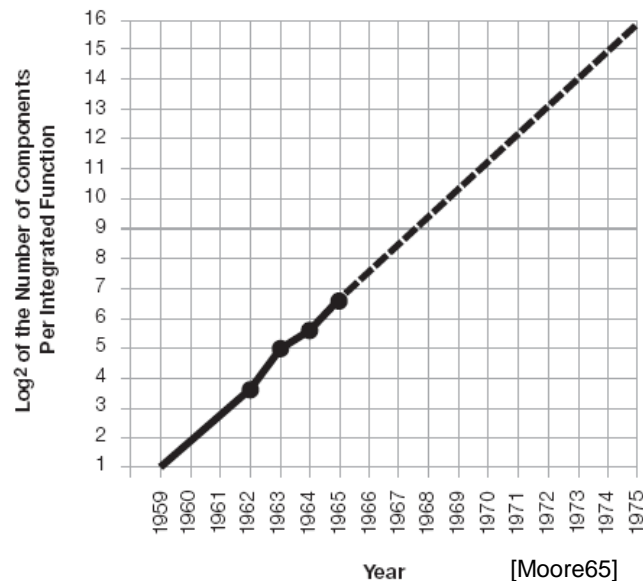
Intel 1101 256-bit SRAM

Intel 4004 4-bit μ Proc

- ❑ 1980s-present: CMOS processes for low idle power

Moore's Law: Then

- ❑ 1965: Gordon Moore plotted transistor on each chip
 - Fit straight line on semilog scale
 - Transistor counts have doubled every 26 months



Electronics Magazine

Integration Levels

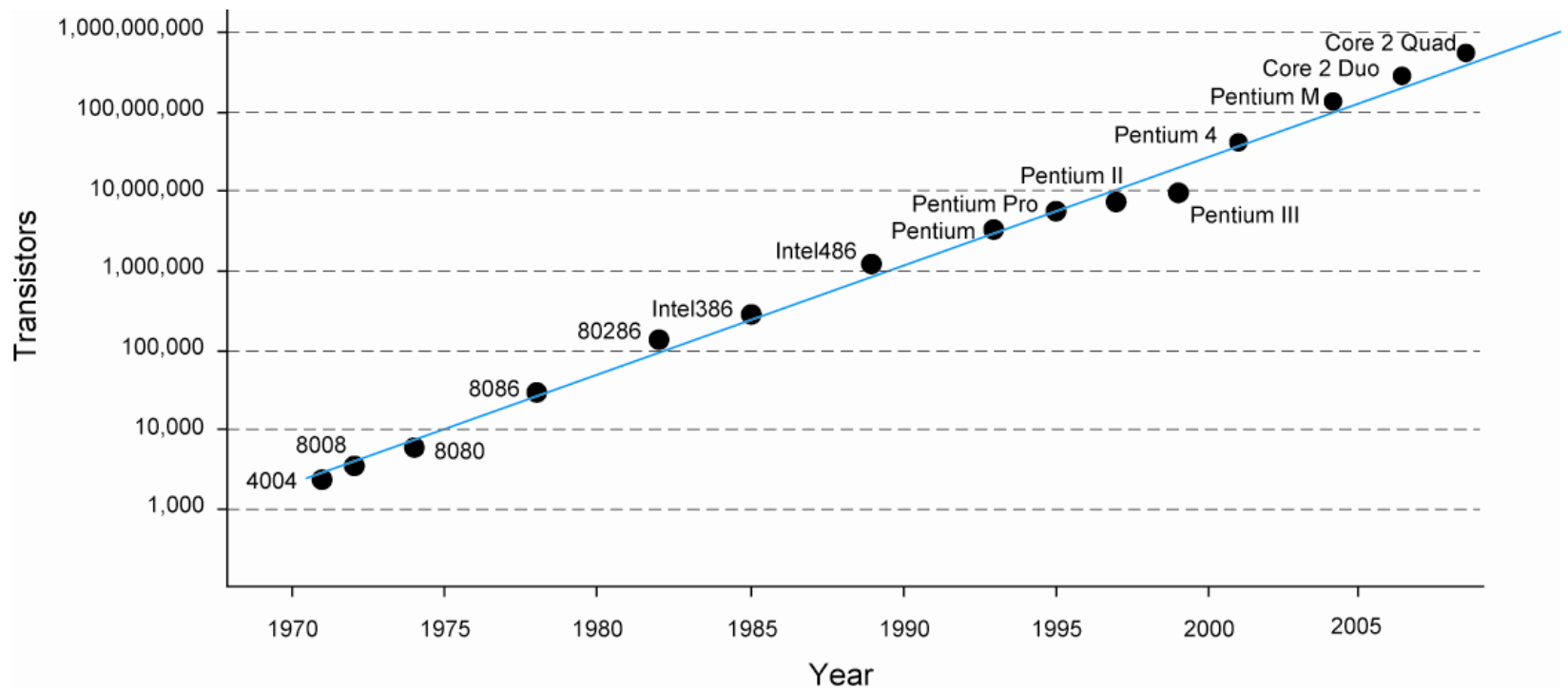
SSI: 10 gates

MSI: 1000 gates

LSI: 10,000 gates

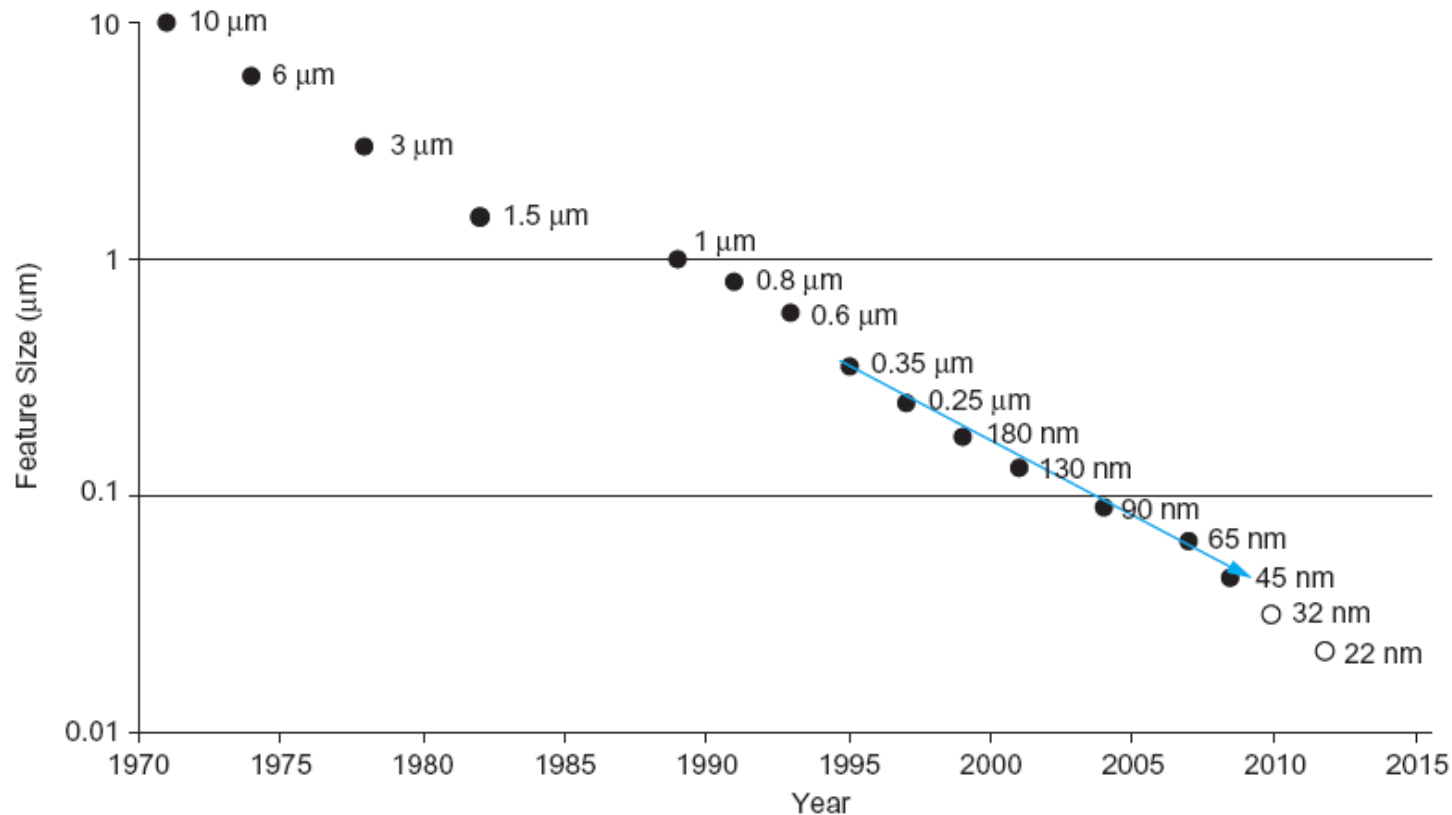
VLSI: > 10k gates

And Now...



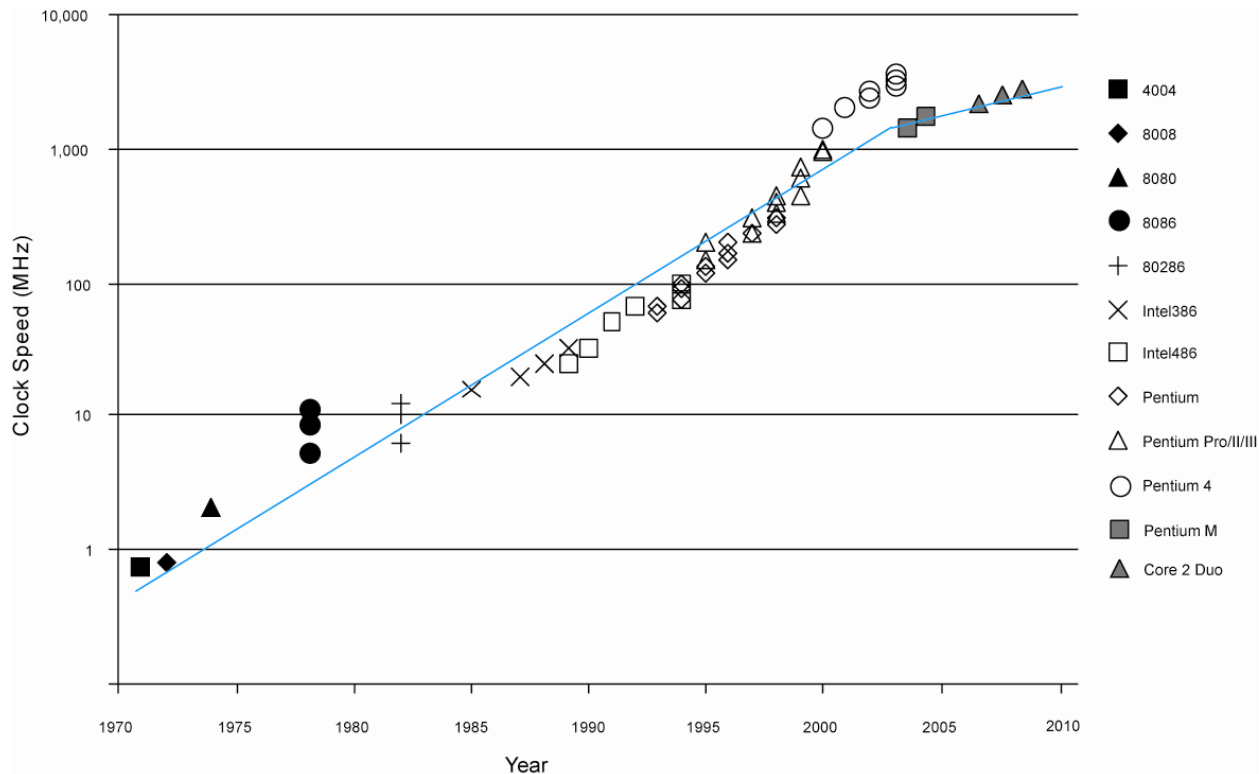
Feature Size

- ❑ Minimum feature size shrinking 30% every 2-3 years



Corollaries

- Many other factors grow exponentially
 - Ex: clock frequency, processor performance

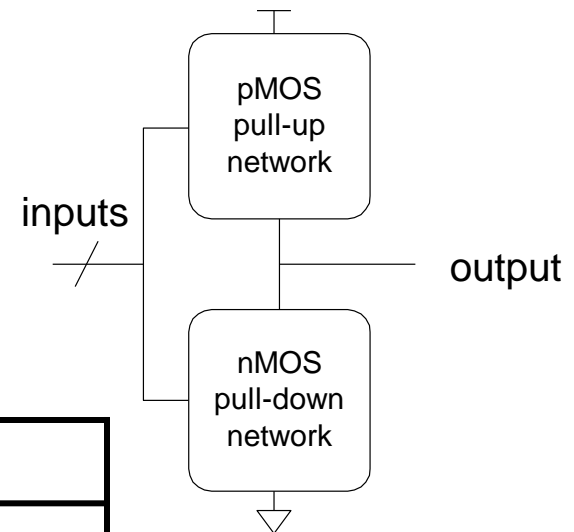


CMOS Gate Design

- Activity:
 - Sketch a 4-input CMOS NOR gate

Complementary CMOS

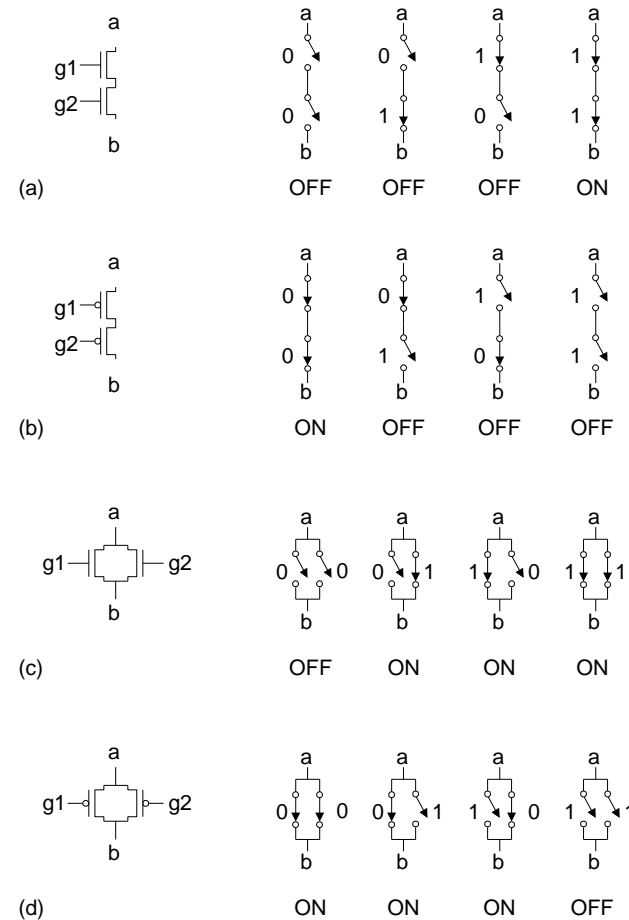
- ❑ Complementary CMOS logic gates
 - nMOS *pull-down network*
 - pMOS *pull-up network*
 - a.k.a. static CMOS



	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

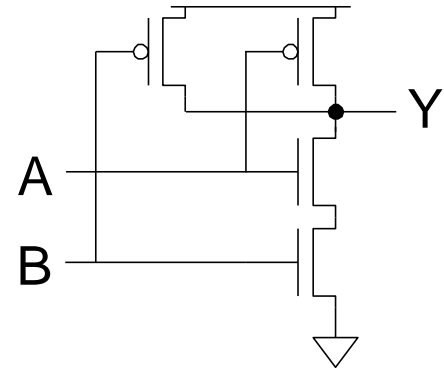
Series and Parallel

- ❑ nMOS: 1 = ON
- ❑ pMOS: 0 = ON
- ❑ *Series*: both must be ON
- ❑ *Parallel*: either can be ON



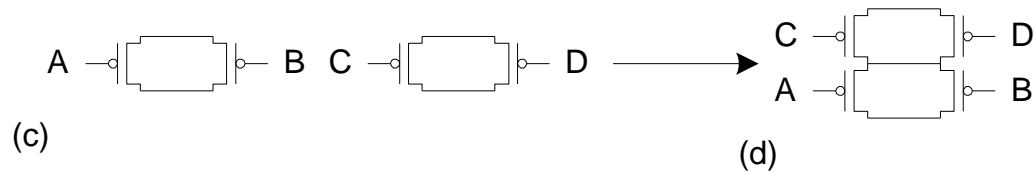
Conduction Complement

- ❑ Complementary CMOS gates always produce 0 or 1
- ❑ Ex: NAND gate
 - Series nMOS: $Y=0$ when both inputs are 1
 - Thus $Y=1$ when either input is 0
 - Requires parallel pMOS
- ❑ Rule of *Conduction Complements*
 - Pull-up network is complement of pull-down
 - Parallel \rightarrow series, series \rightarrow parallel



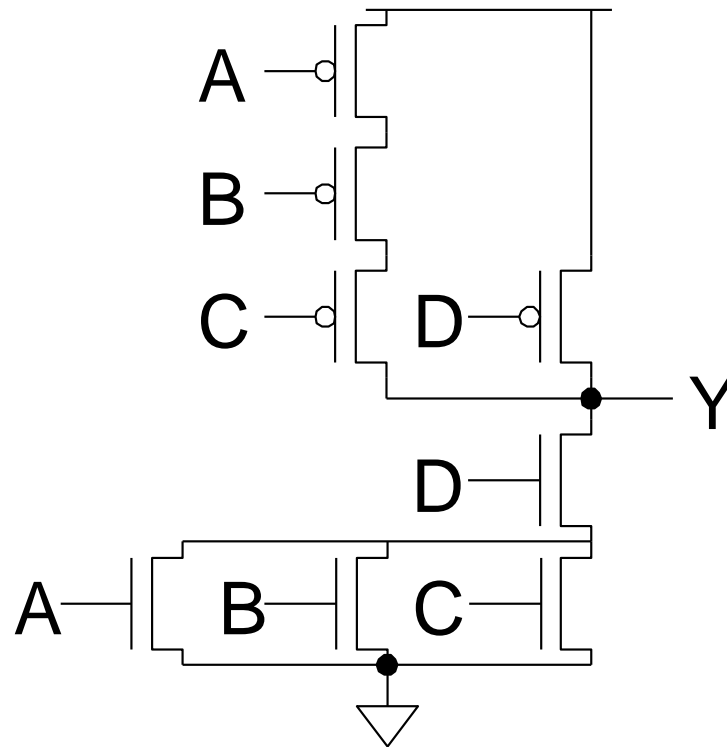
Compound Gates

- ❑ *Compound gates can do any inverting function*
- ❑ Ex: $Y = \overline{A \square B + C \square D}$ (AND-AND-OR-INVERT, AOI22)



Example: O3AI

$$\square Y = \overline{(A + B + C)} \square D$$

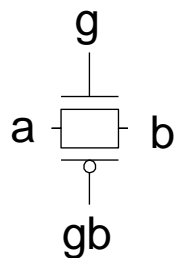


Signal Strength

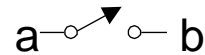
- ❑ *Strength* of signal
 - How close it approximates ideal voltage source
- ❑ V_{DD} and GND rails are strongest 1 and 0
- ❑ nMOS pass strong 0
 - But degraded or weak 1
- ❑ pMOS pass strong 1
 - But degraded or weak 0
- ❑ Thus nMOS are best for pull-down network

Transmission Gates

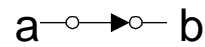
- ❑ Pass transistors produce degraded outputs
- ❑ *Transmission gates* pass both 0 and 1 well



$g = 0, gb = 1$



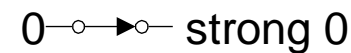
$g = 1, gb = 0$



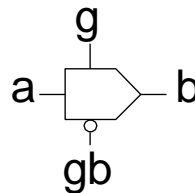
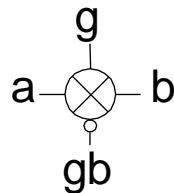
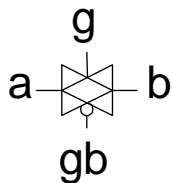
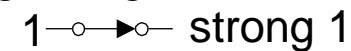
Input

Output

$g = 1, gb = 0$

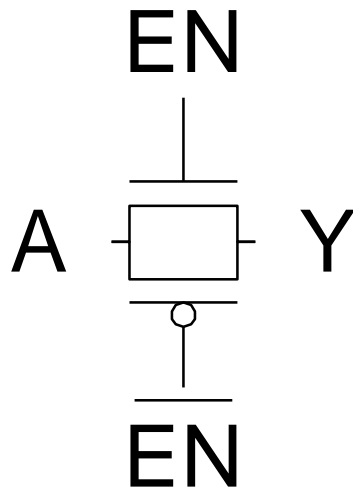


$g = 1, gb = 0$



Nonrestoring Tristate

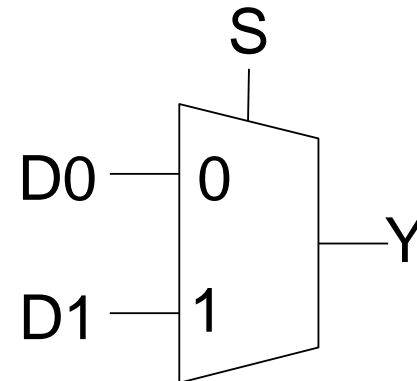
- ❑ Transmission gate acts as tristate buffer
 - Only two transistors
 - But *nonrestoring*
 - Noise on A is passed on to Y



Multiplexers

- ❑ 2:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	
0	X	1	
1	0	X	
1	1	X	

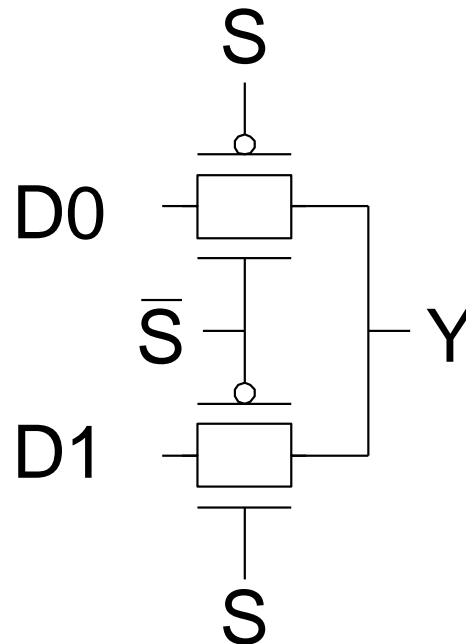


Gate-Level Mux Design

- ❑ $Y = SD_1 + \bar{S}D_0$ (too many transistors)
- ❑ How many transistors are needed?

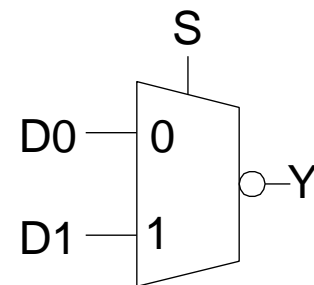
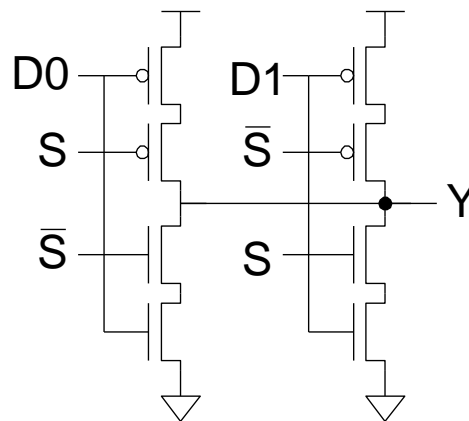
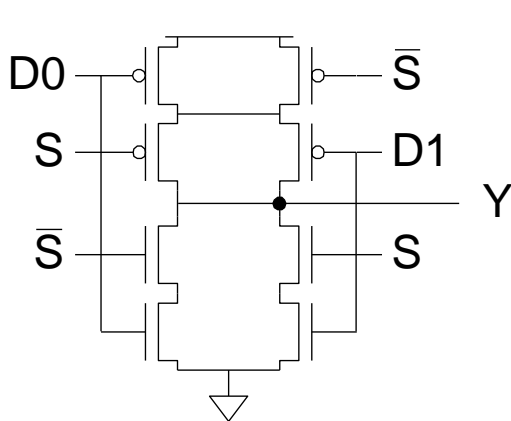
Transmission Gate Mux

- ❑ Nonrestoring mux uses two transmission gates
 - Only 4 transistors



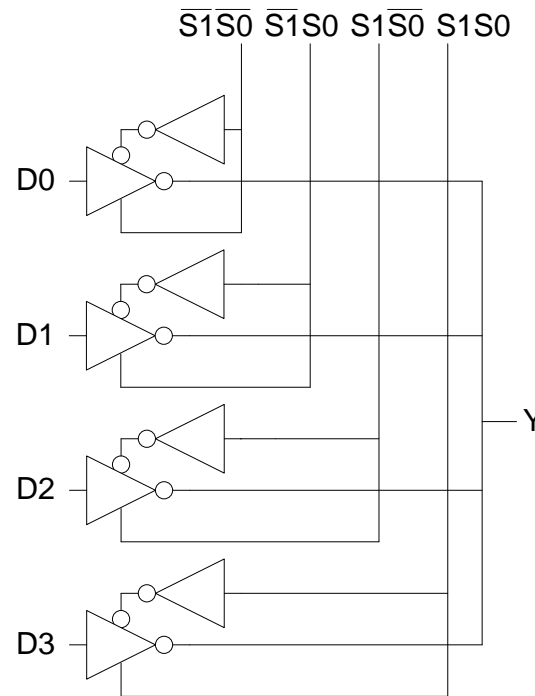
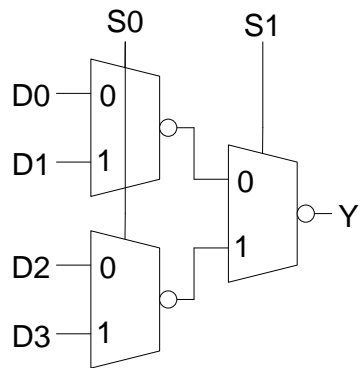
Inverting Mux

- ❑ Inverting multiplexer
 - Use compound AOI22
 - Or pair of tristate inverters
 - Essentially the same thing
- ❑ Noninverting multiplexer adds an inverter



4:1 Multiplexer

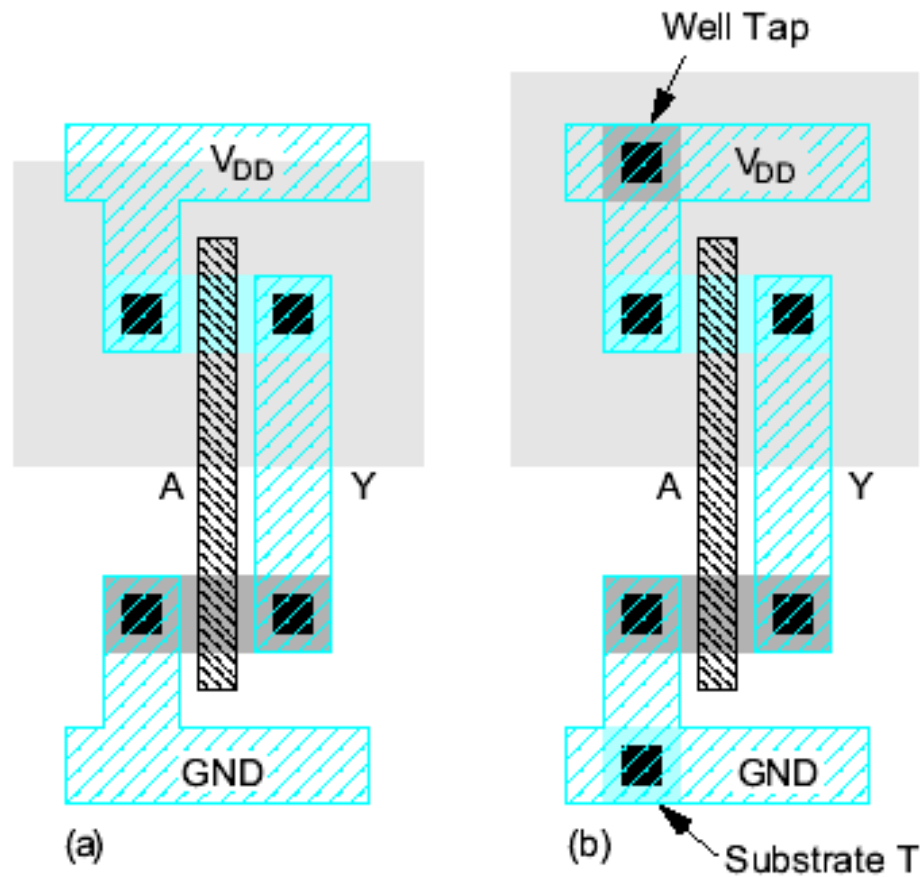
- ❑ 4:1 mux chooses one of 4 inputs using two selects
 - Two levels of 2:1 muxes
 - Or four tristates



Gate Layout

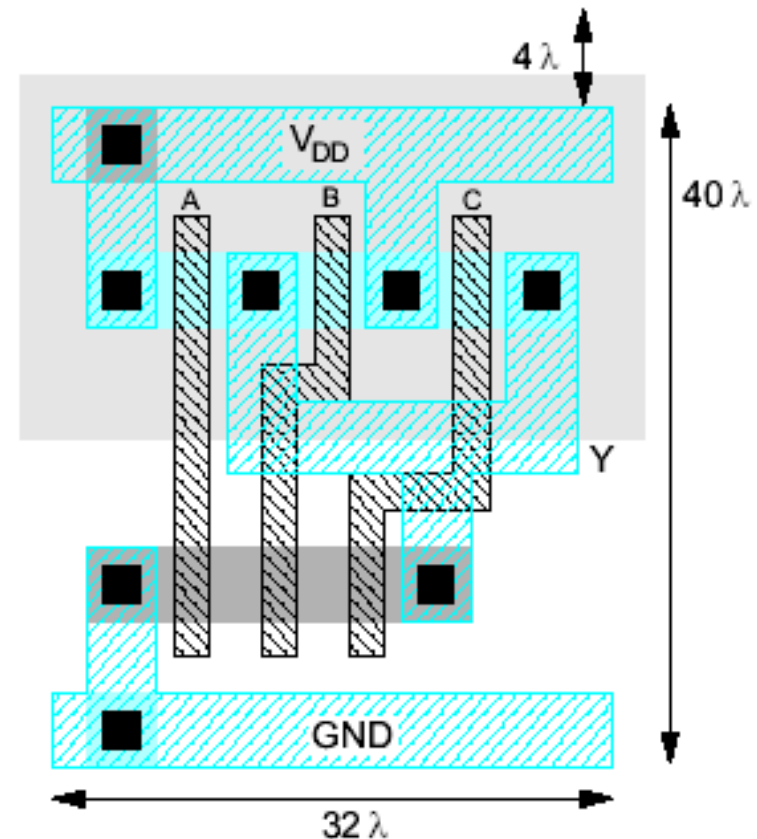
- ❑ Layout can be very time consuming
 - Design gates to fit together nicely
 - Build a library of standard cells
- ❑ Standard cell design methodology
 - V_{DD} and GND should abut (standard height)
 - Adjacent gates should satisfy design rules
 - nMOS at bottom and pMOS at top
 - All gates include well and substrate contacts

Example: Inverter



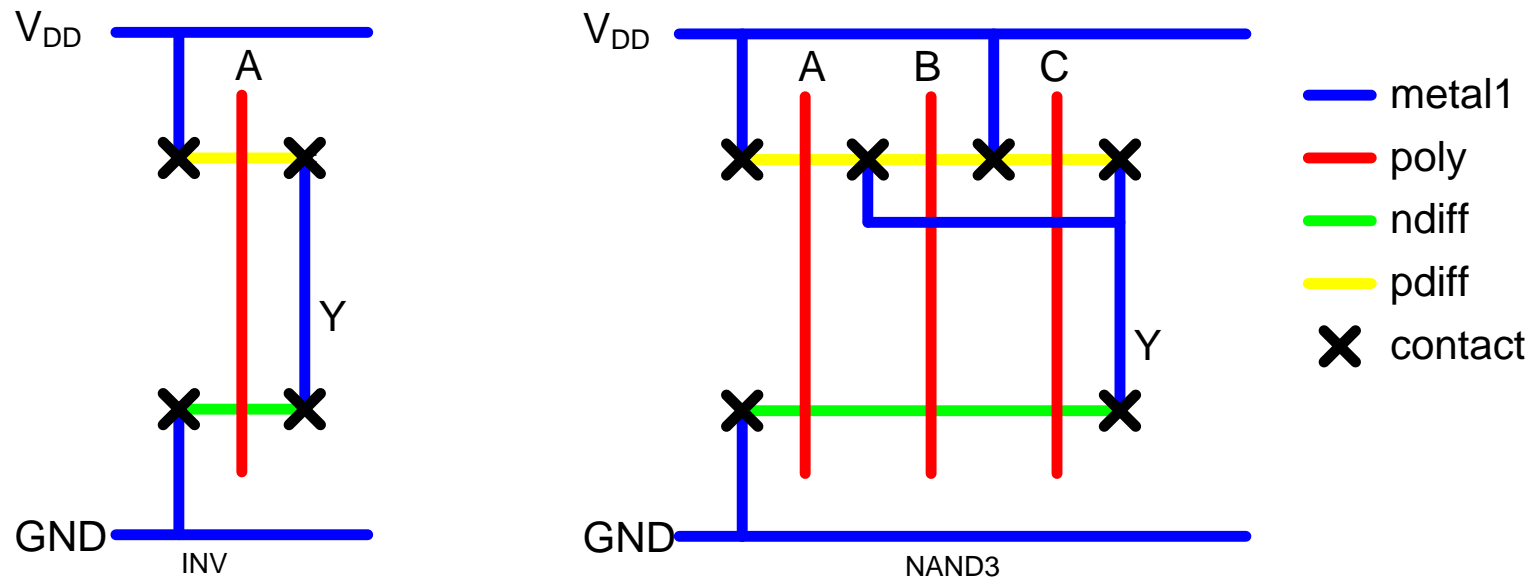
Example: NAND3

- ❑ Horizontal N-diffusion and p-diffusion strips
- ❑ Vertical polysilicon gates
- ❑ Metal1 V_{DD} rail at top
- ❑ Metal1 GND rail at bottom
- ❑ 32λ by 40λ



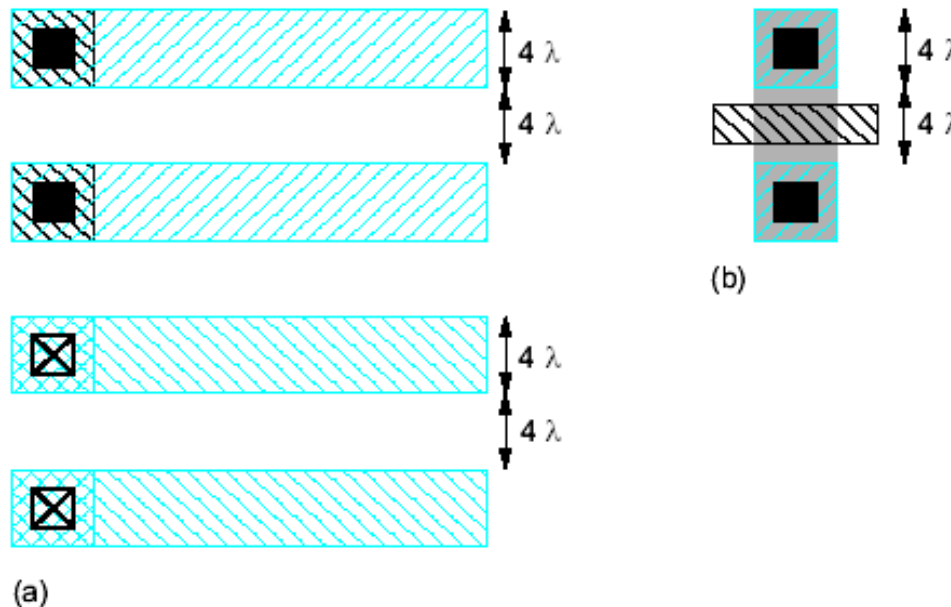
Stick Diagrams

- ❑ *Stick diagrams* help plan layout quickly
 - Need not be to scale
 - Draw with color pencils or dry-erase markers



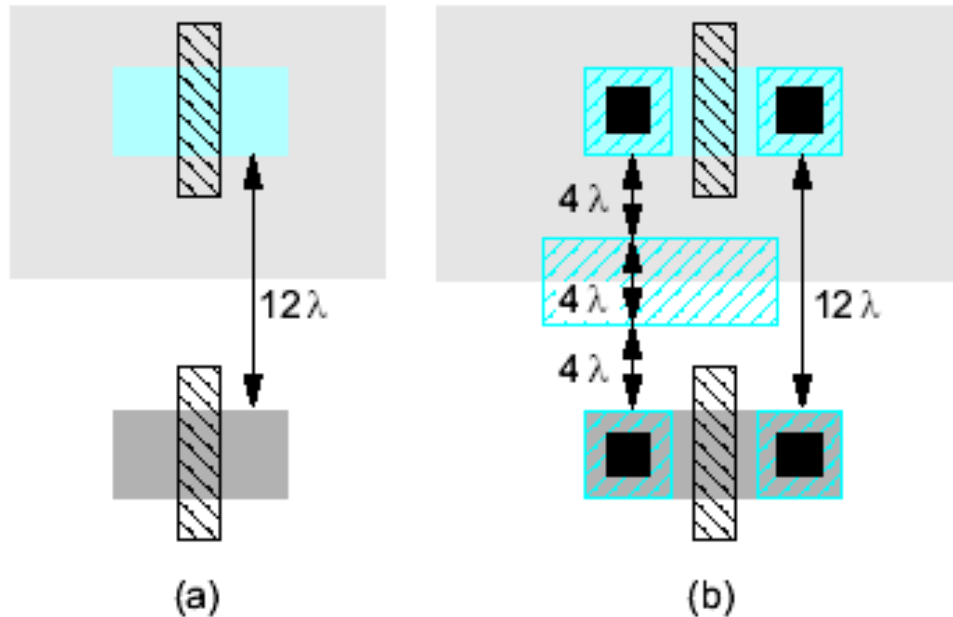
Wiring Tracks

- ❑ A *wiring track* is the space required for a wire
 - 4λ width, 4λ spacing from neighbor = 8λ pitch
- ❑ Transistors also consume one wiring track



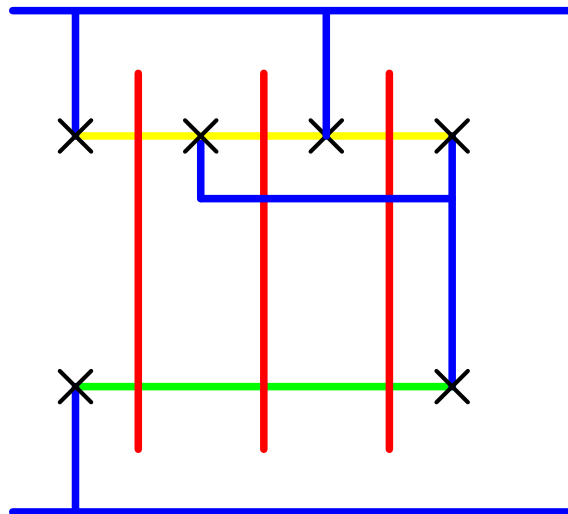
Well spacing

- ❑ Wells must surround transistors by 6λ
 - Implies 12λ between opposite transistor flavors
 - Leaves room for one wire track



Area Estimation

- ❑ Estimate area by counting wiring tracks
 - Multiply by 8 to express in λ



Example: O3AI

- Sketch a stick diagram for O3AI and estimate area

$$Y = \overline{(A + B + C)} \square D$$

