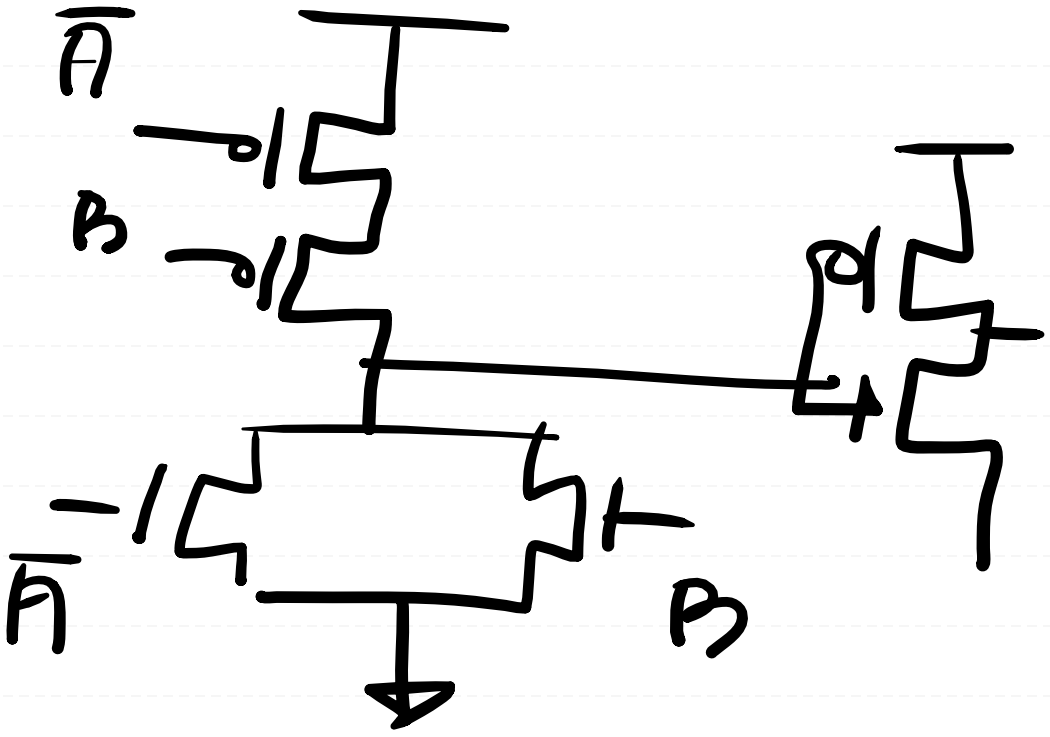
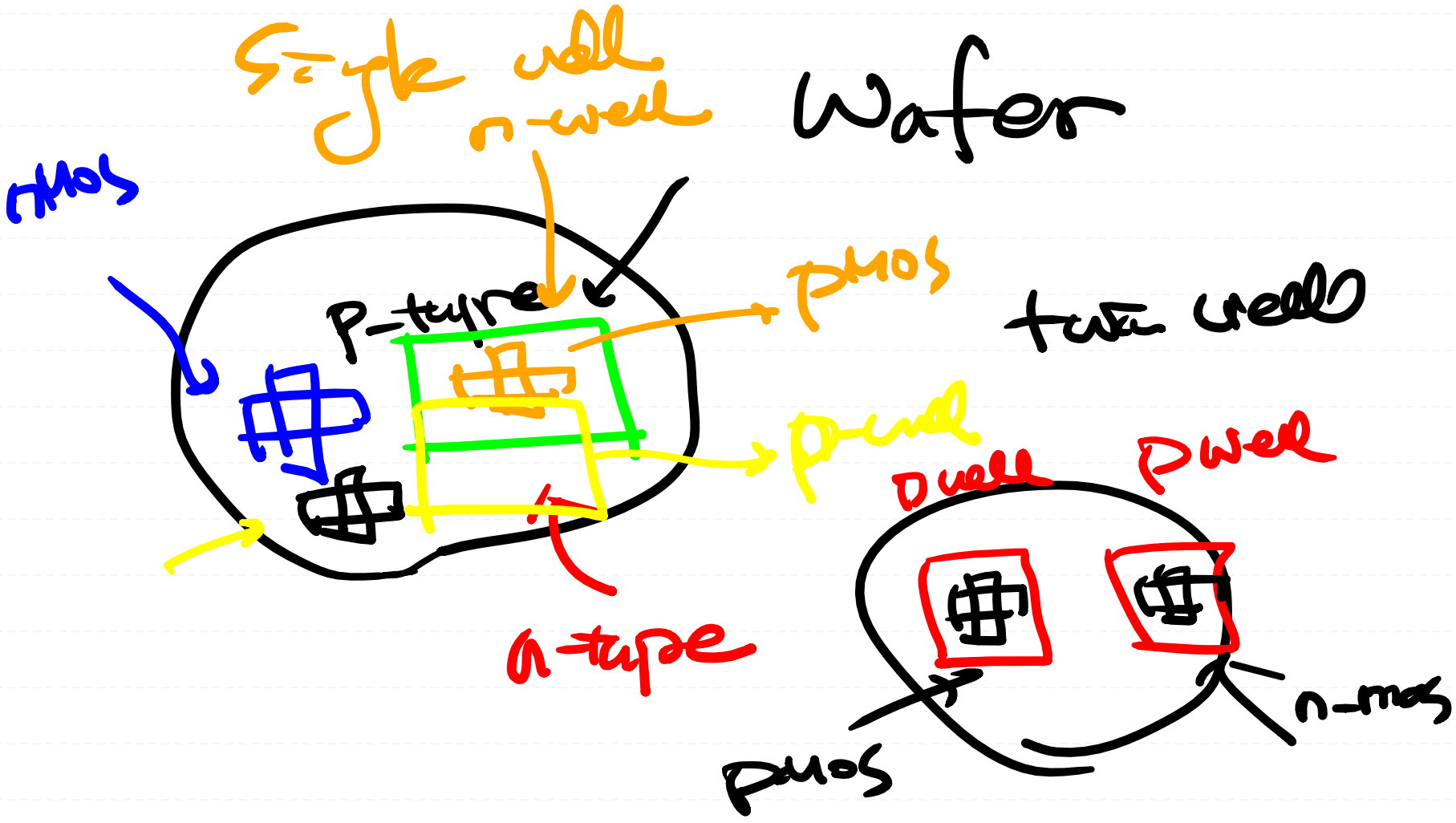
$F = \overline{\square}$ $\square$ = OR

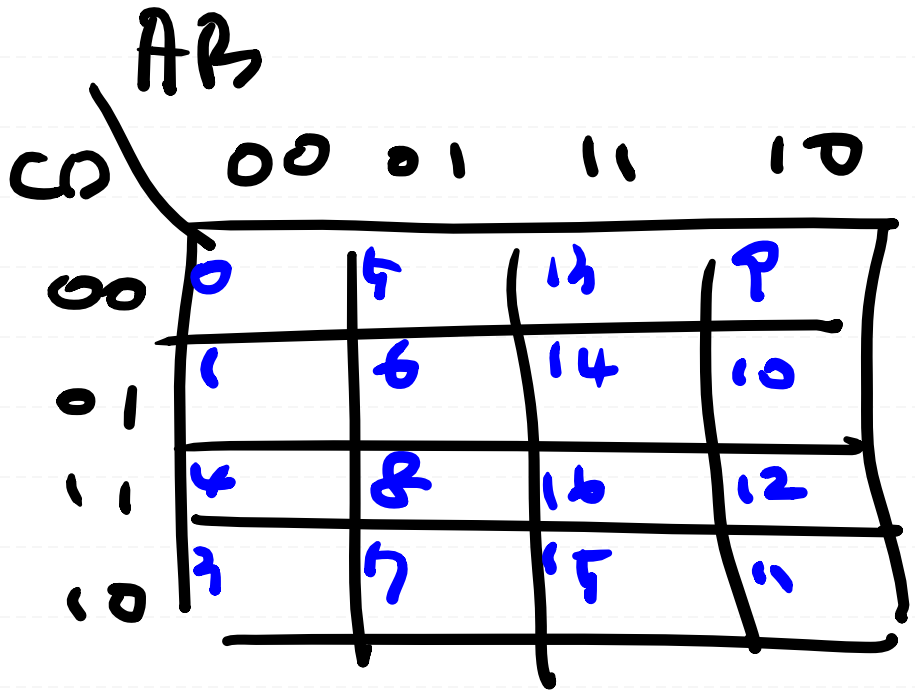
① $F = \overline{A} + B$

$= \overline{\overline{\overline{A} + B}}$




Wafer
nMOS
p-type
pMOS
n-type
pMOS
n-MOS

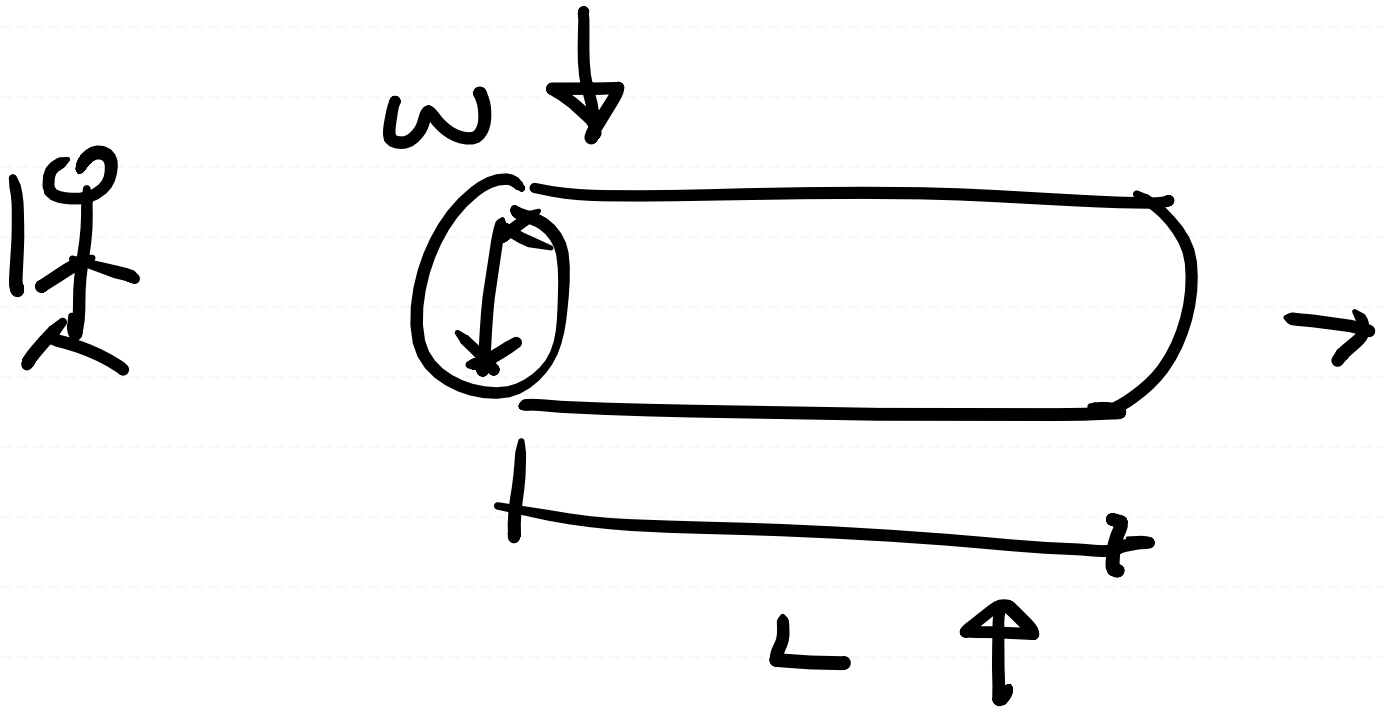
A B C D

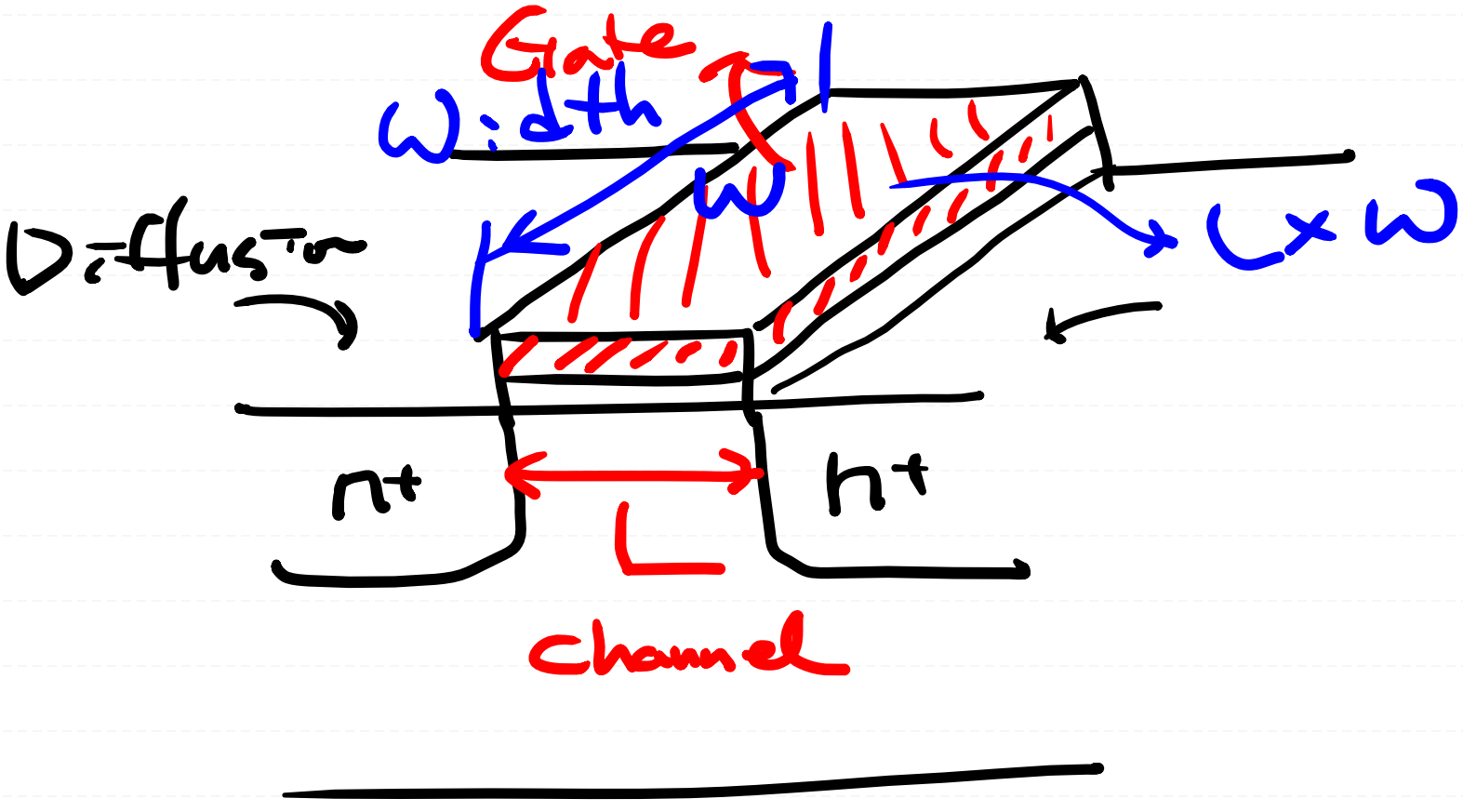


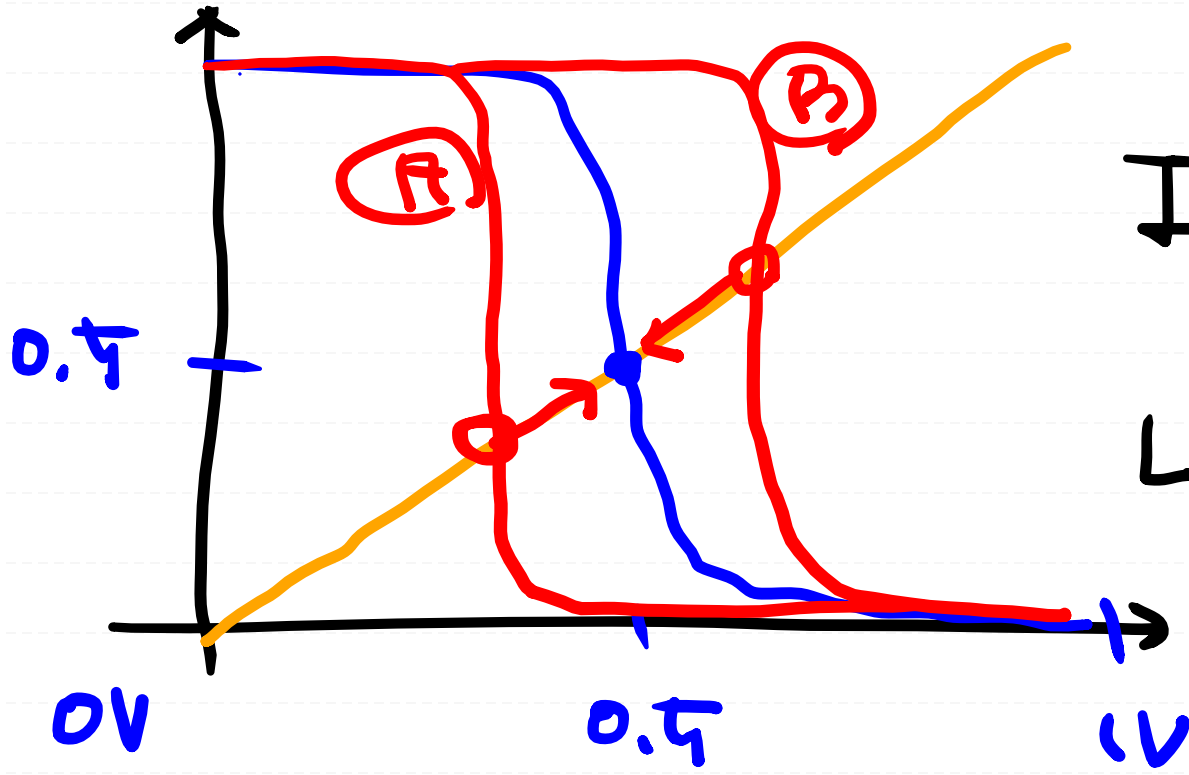
$$I_{Dsat} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$$

① ② ③ ④

$$I \propto \frac{W}{L}$$

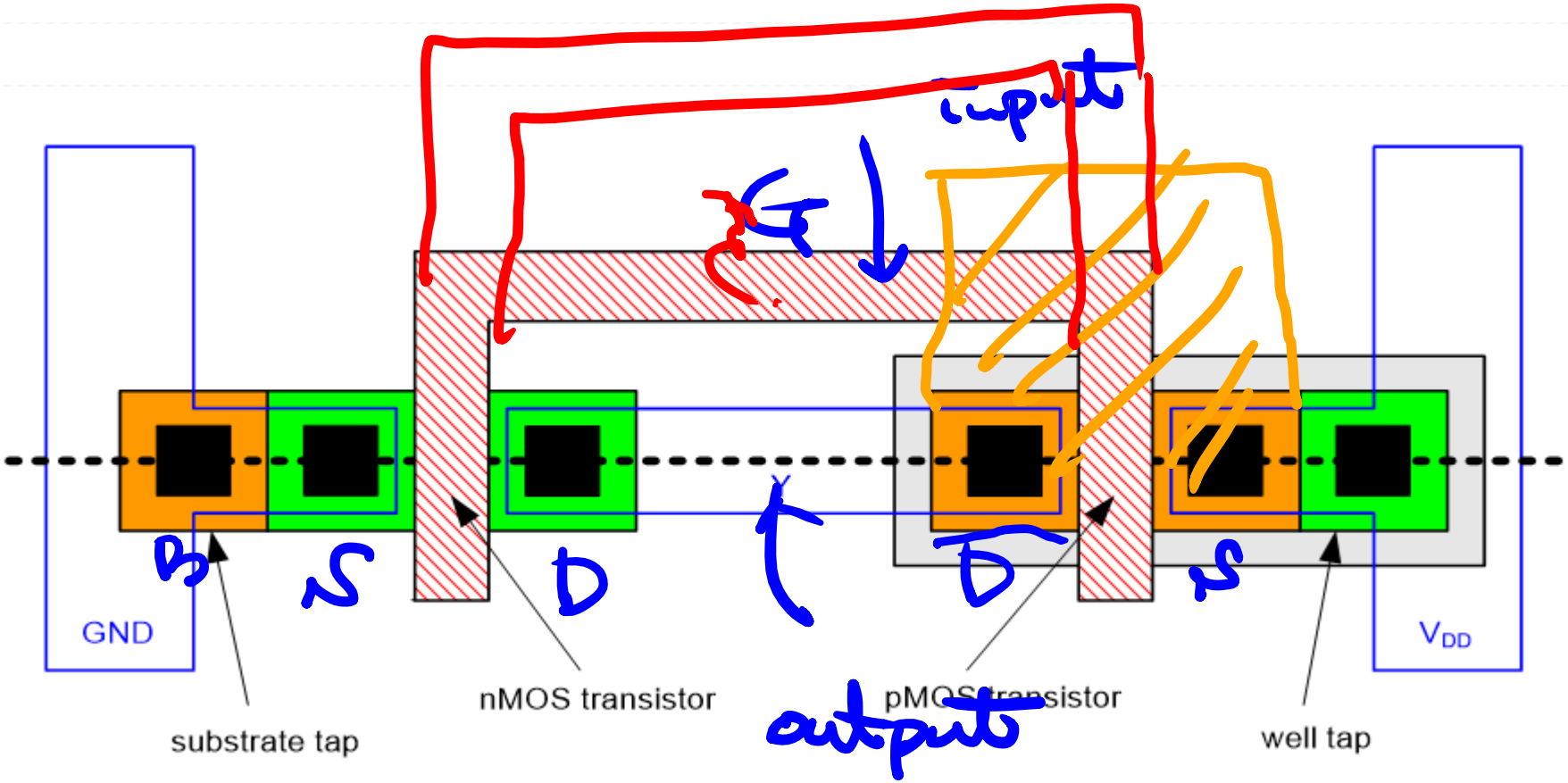

w
L

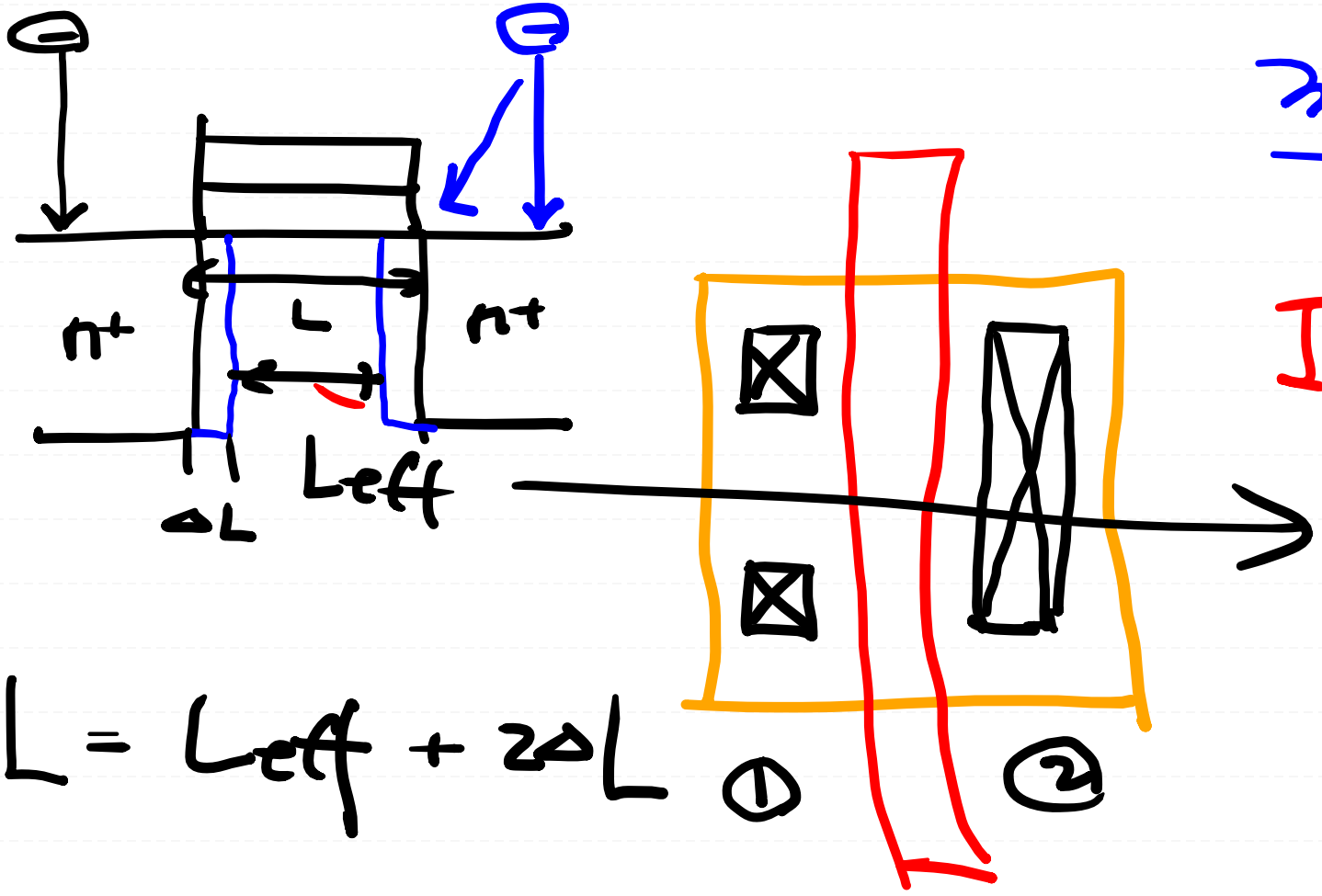

Gate
Width
W
L x W
Diffusion
n+
n+
L
Channel



$$I \propto \frac{W}{L}$$

$$L = 35nm$$


GND
V_{DD}
substrate tap
nMOS transistor
well tap

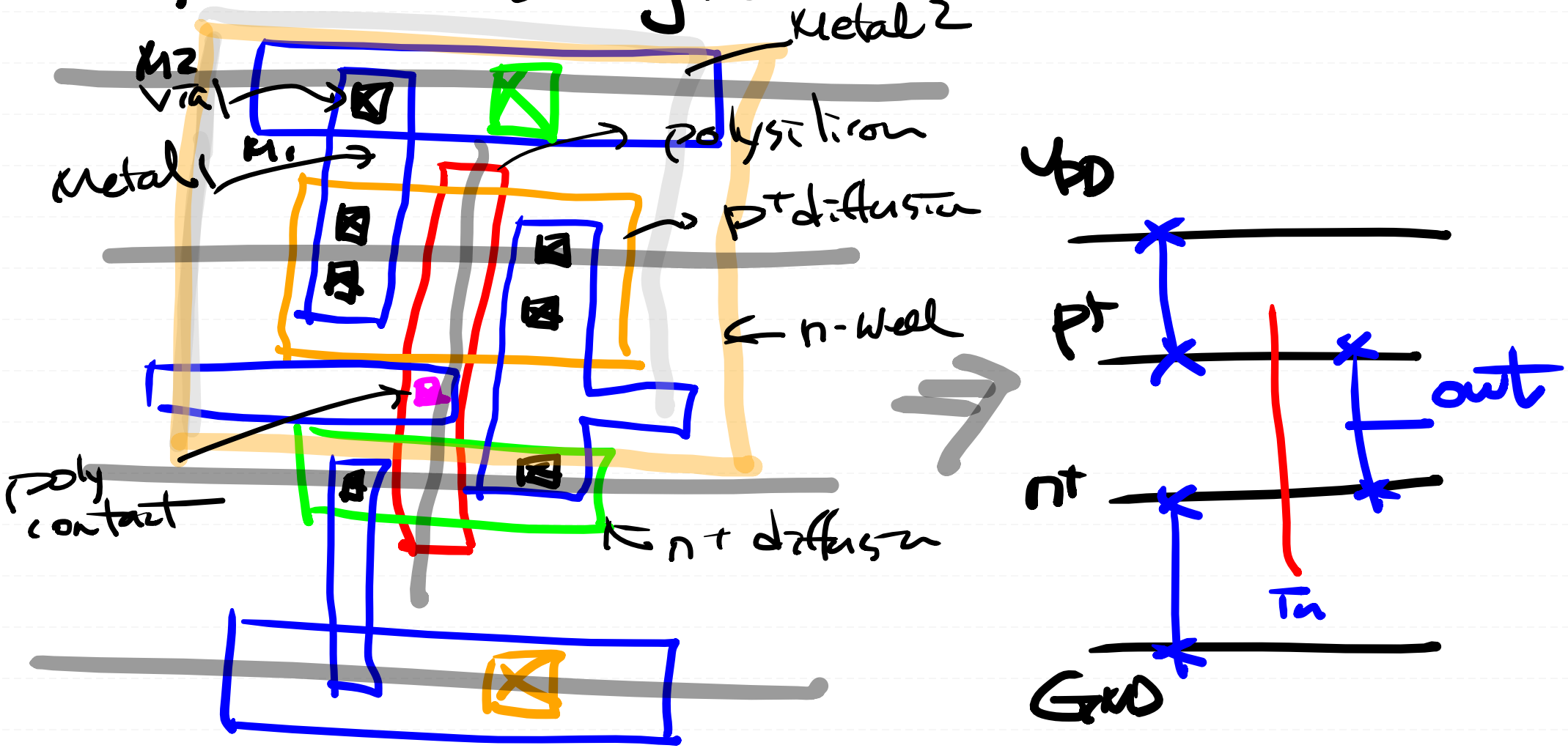


$L = L_{eff} + 2\Delta L$

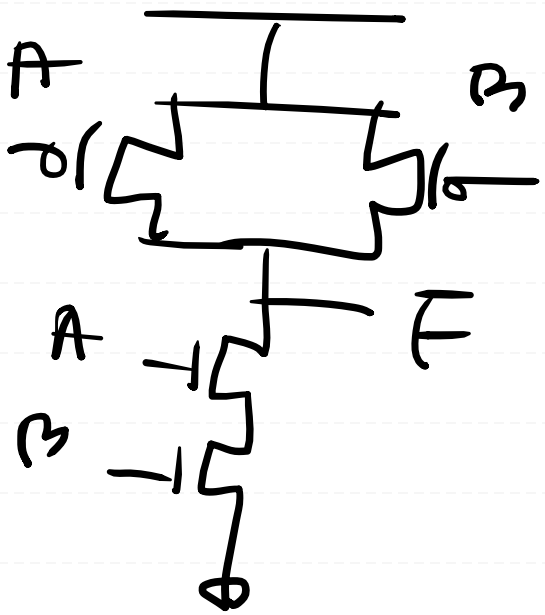
35nm ↓

$I_d \propto \frac{W}{L}$

Stick Diagram



2XNAND $F = \overline{A \cdot B}$



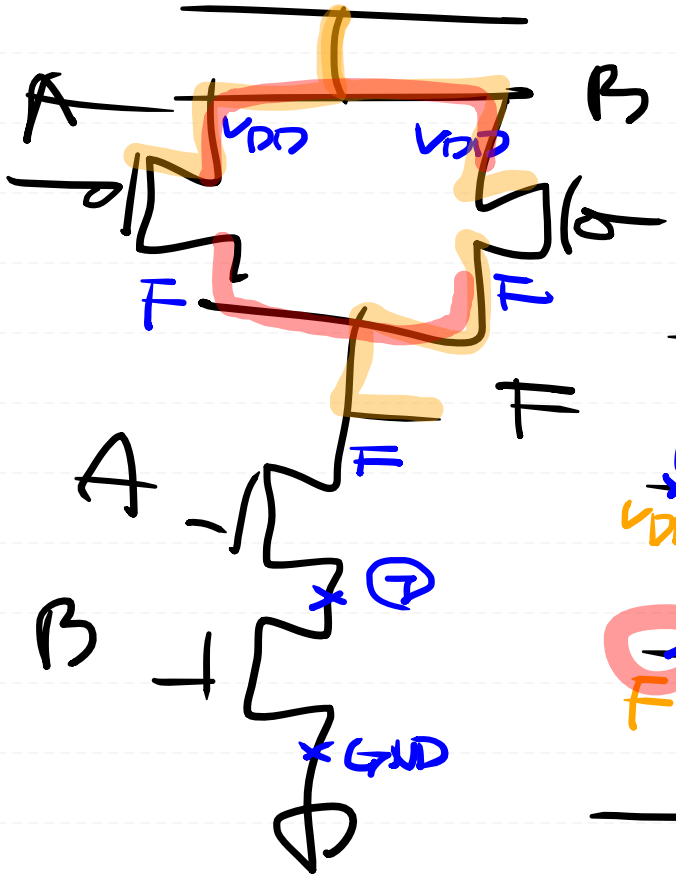
Path !!

① nMOS pMOS block 뚫린 path

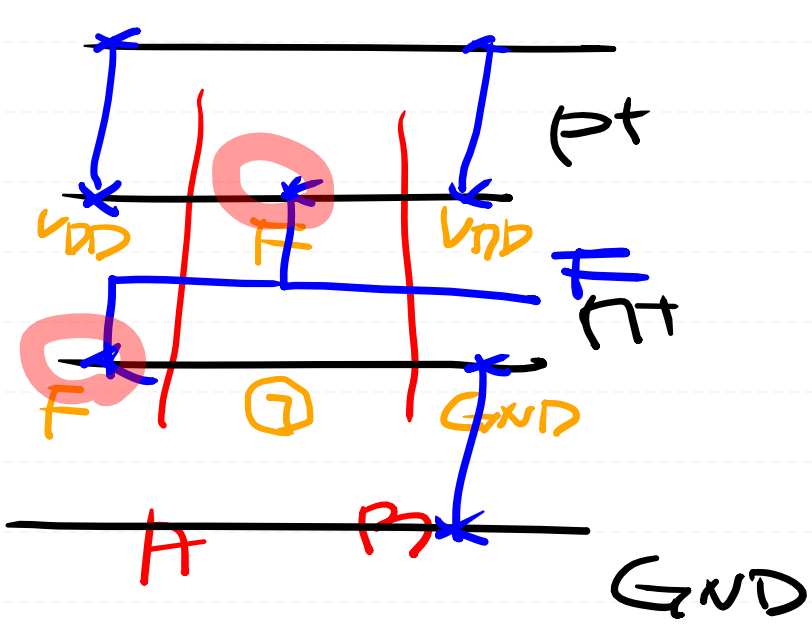
② 모든 Tr 반드시 1개씩 뚫린 경로.

Path ○ A – B

○ B – A

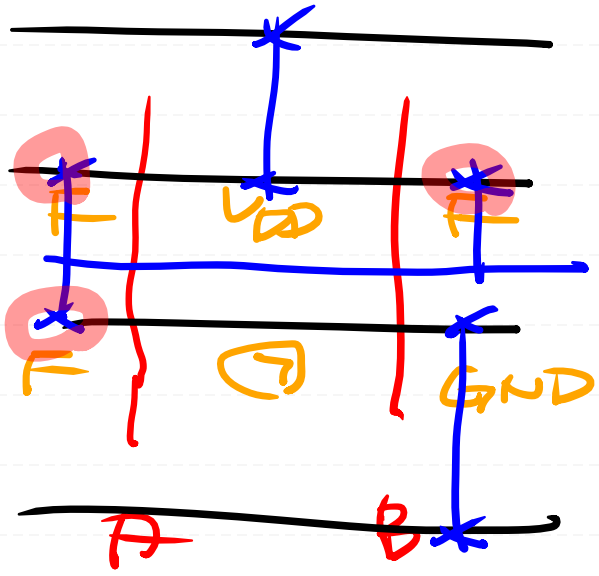


2C

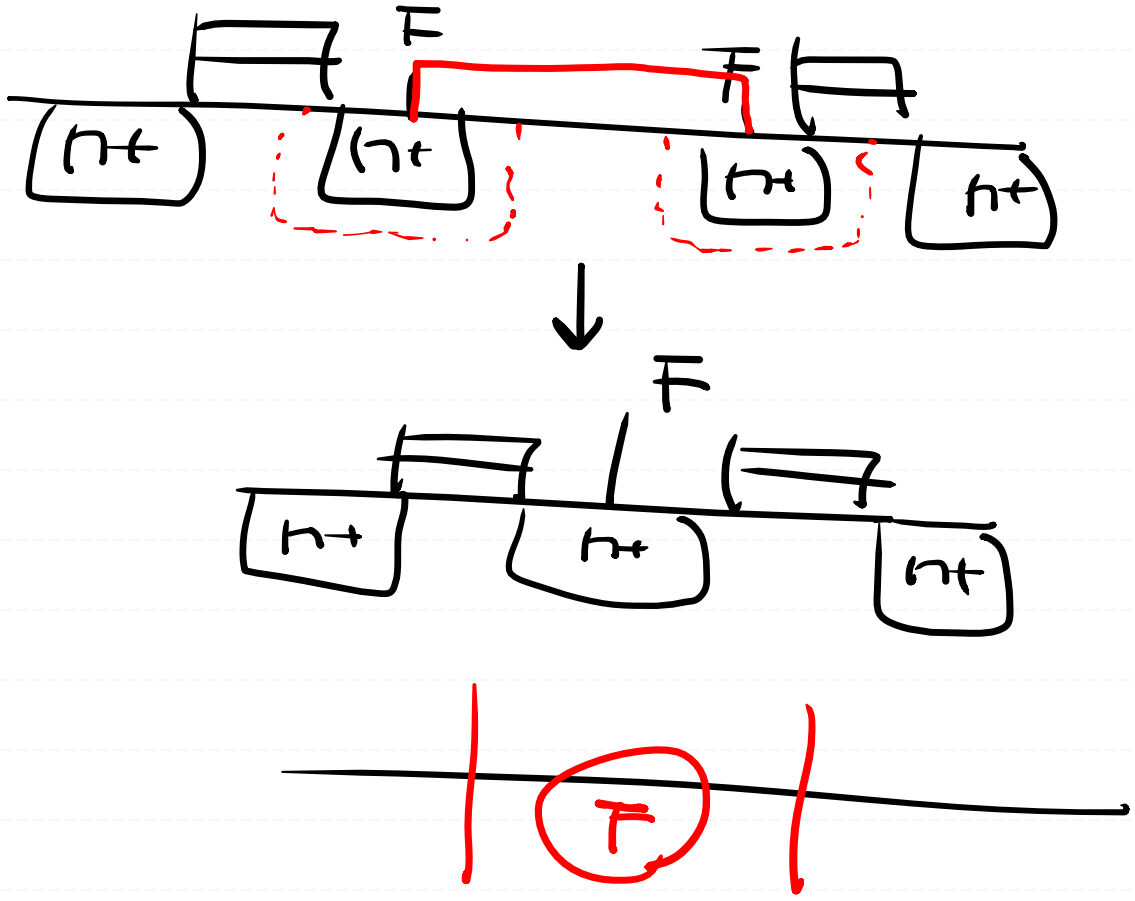


1

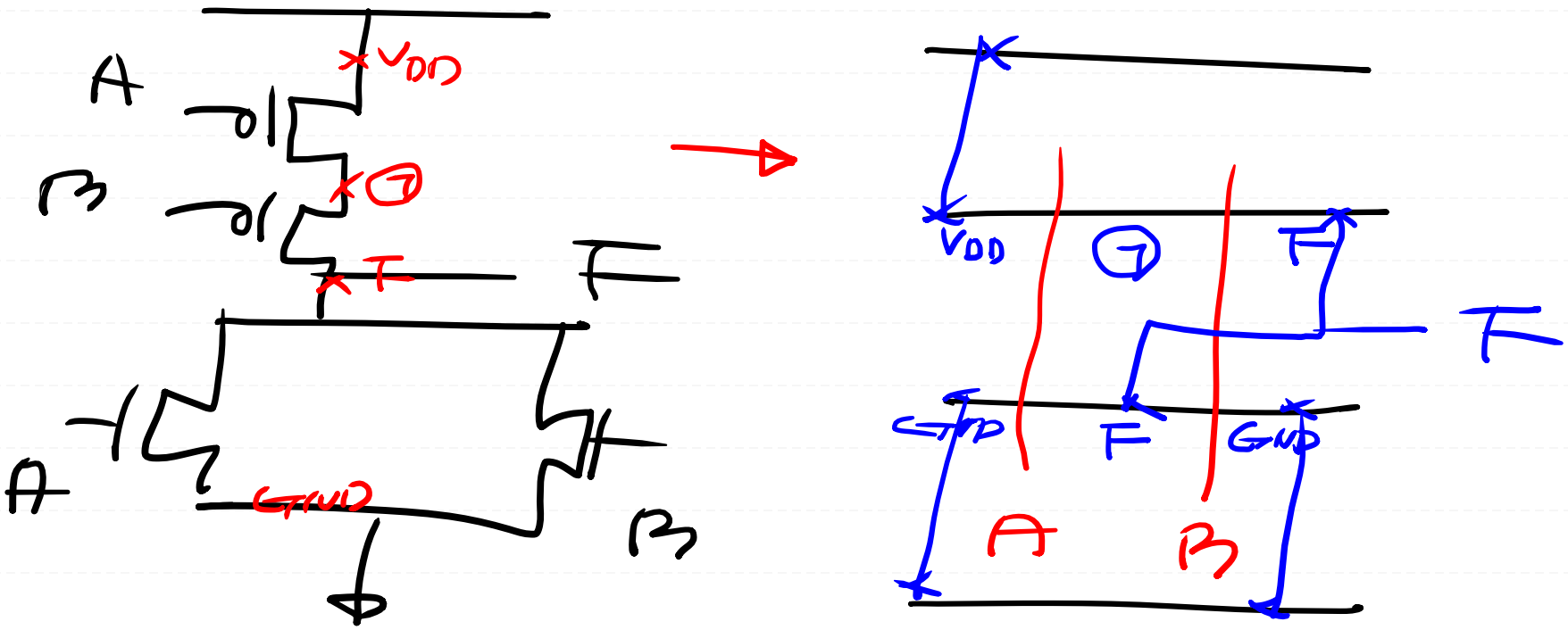
3C



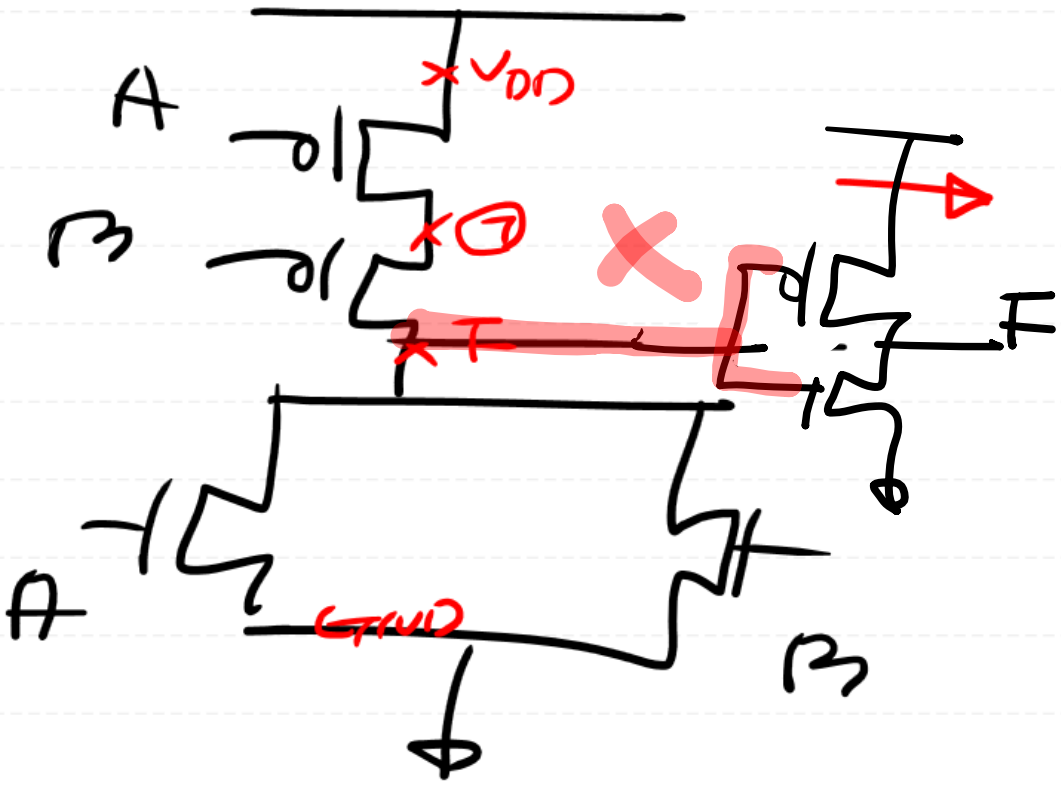
2

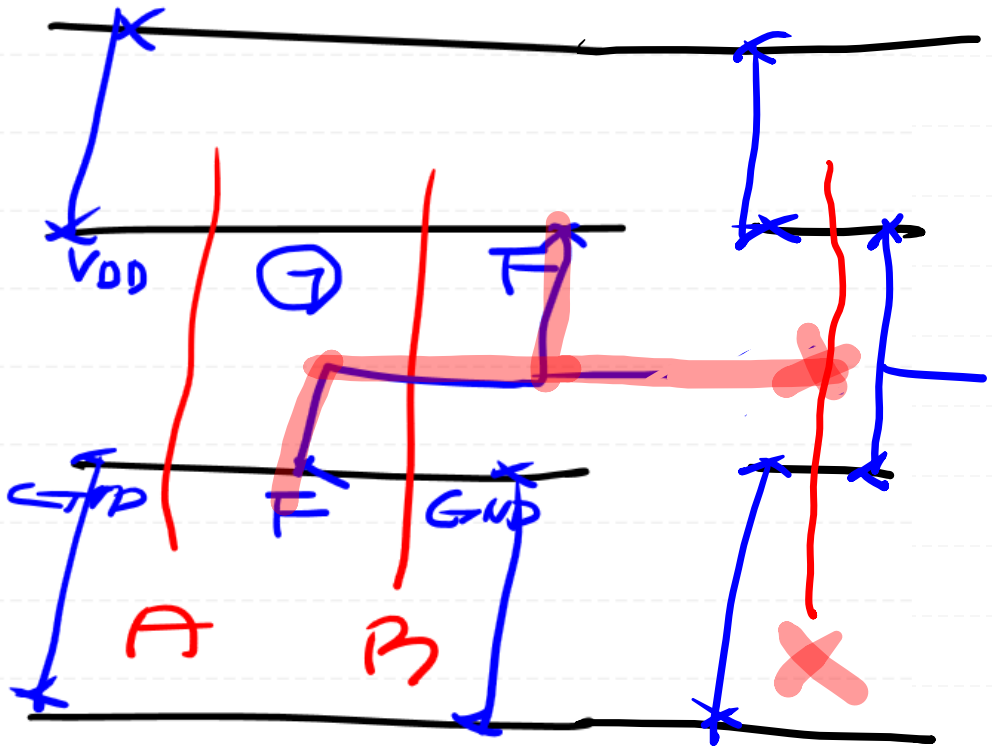

F
F
n+
n+
n+
n+
F
n+
n+
n+
F

2NOR

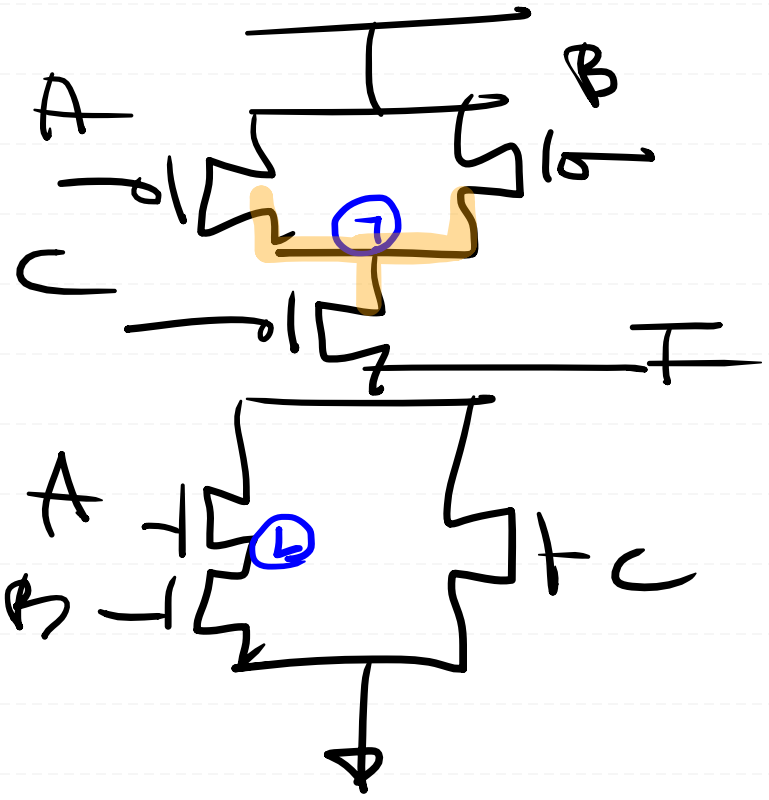


OR

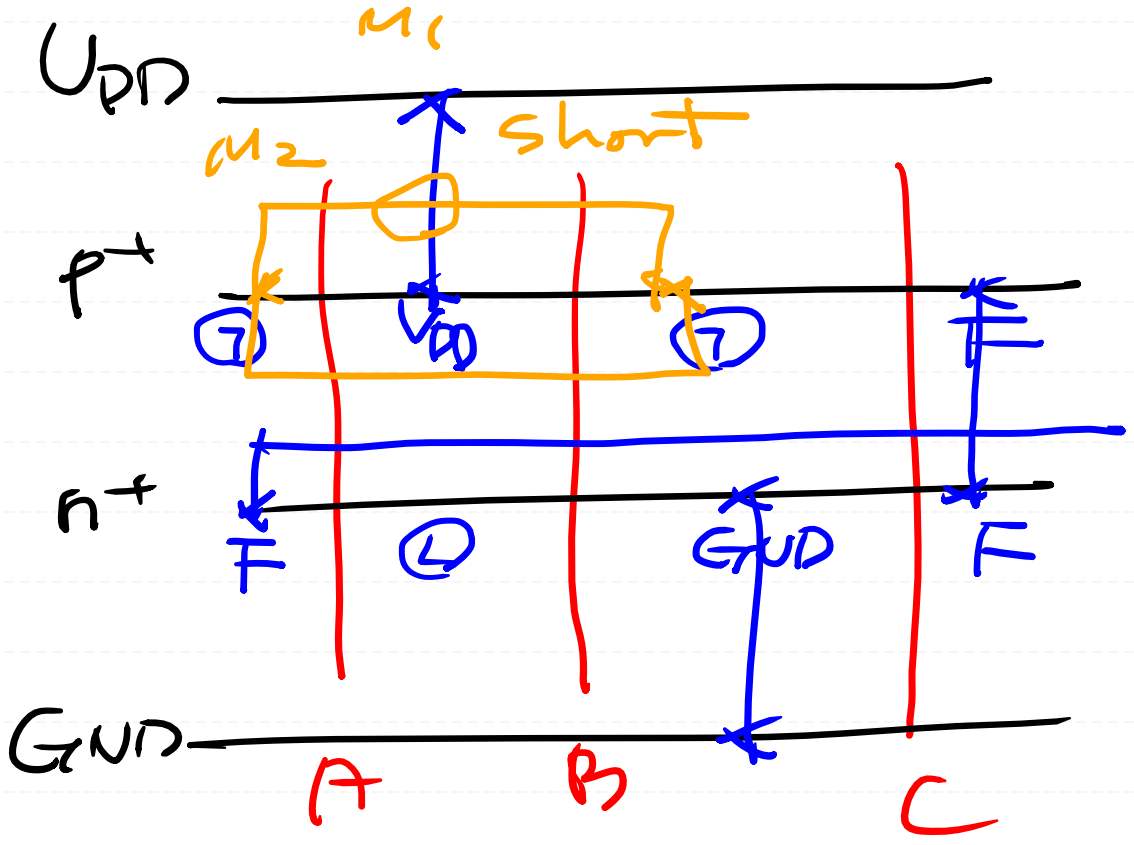




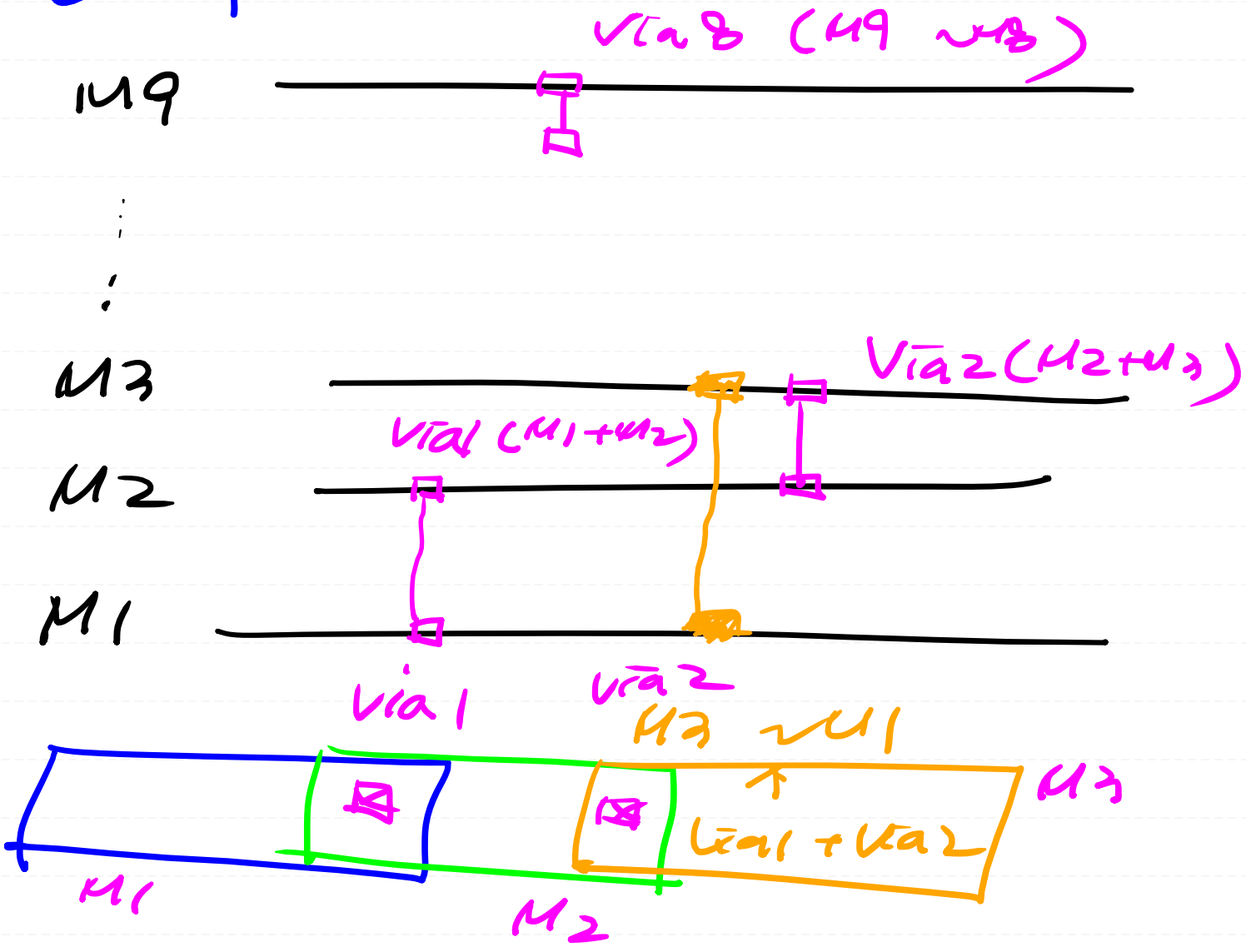
$F = \overline{A \cdot B + C}$



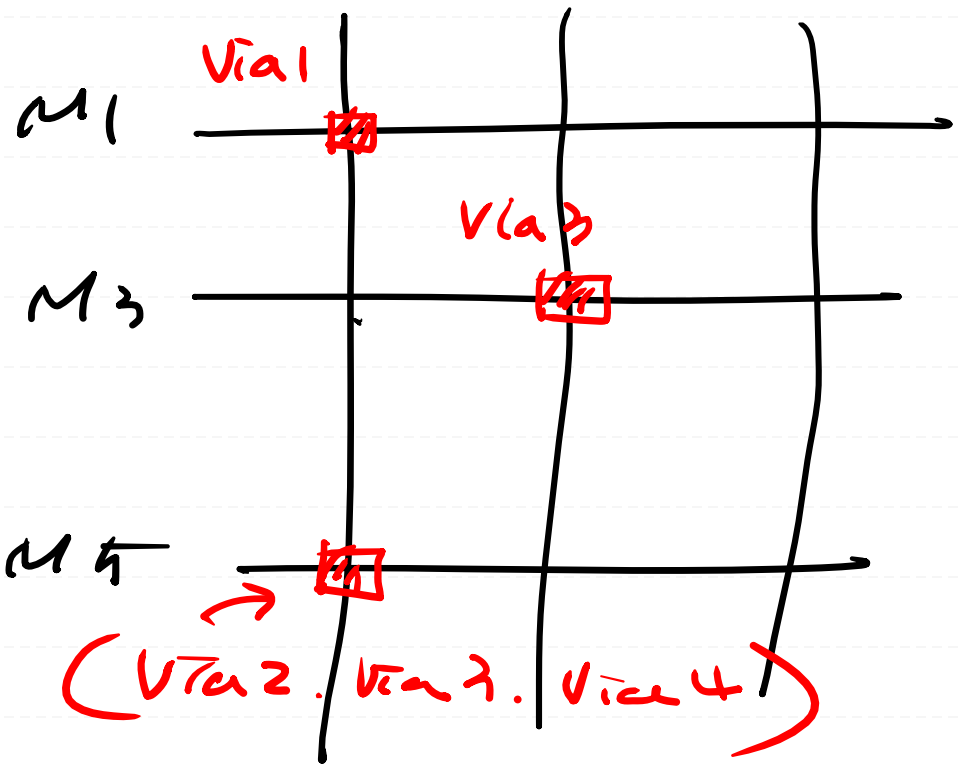
Path A-B-C



M1 ~ M9


Via8 (M9 ~M8)
M9
M3
Via2(M2+M3)
Via1 (M1+M2)
M2
M1
Via1
Via2
M3 ~M1
M3
Via1 + Via2
M1
M2

M2 M4 M6

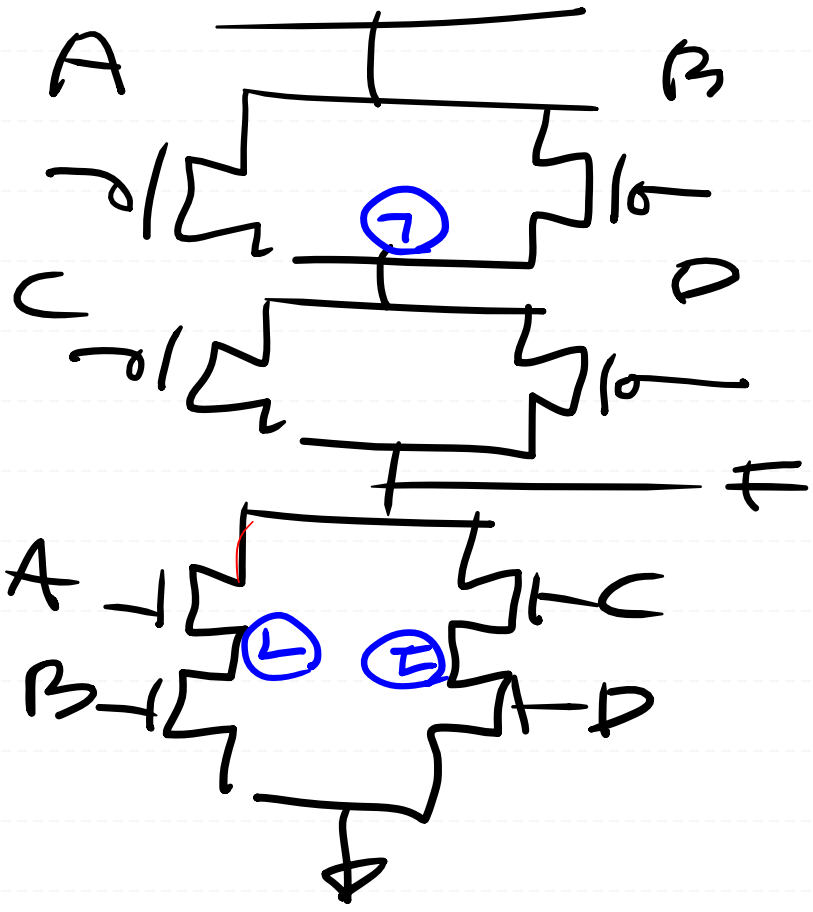


Cap

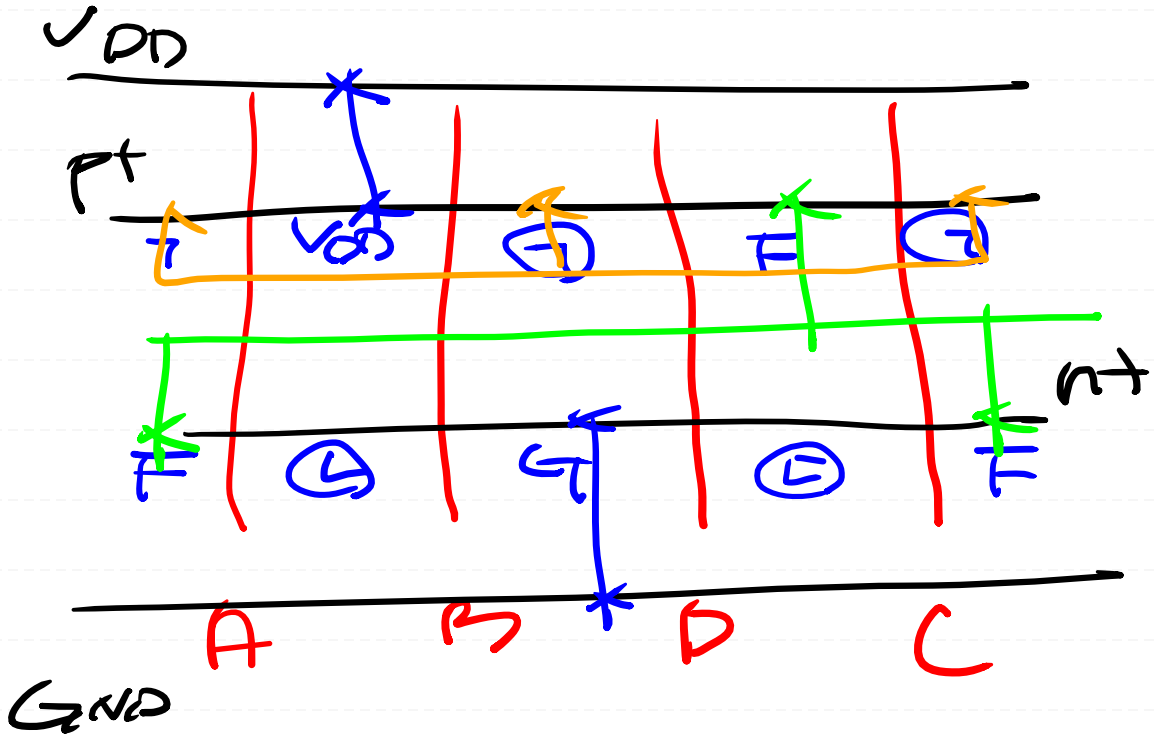
$$F = \overline{A \cdot B + C \cdot D}$$

① CMOS schematic

② stick Diagram

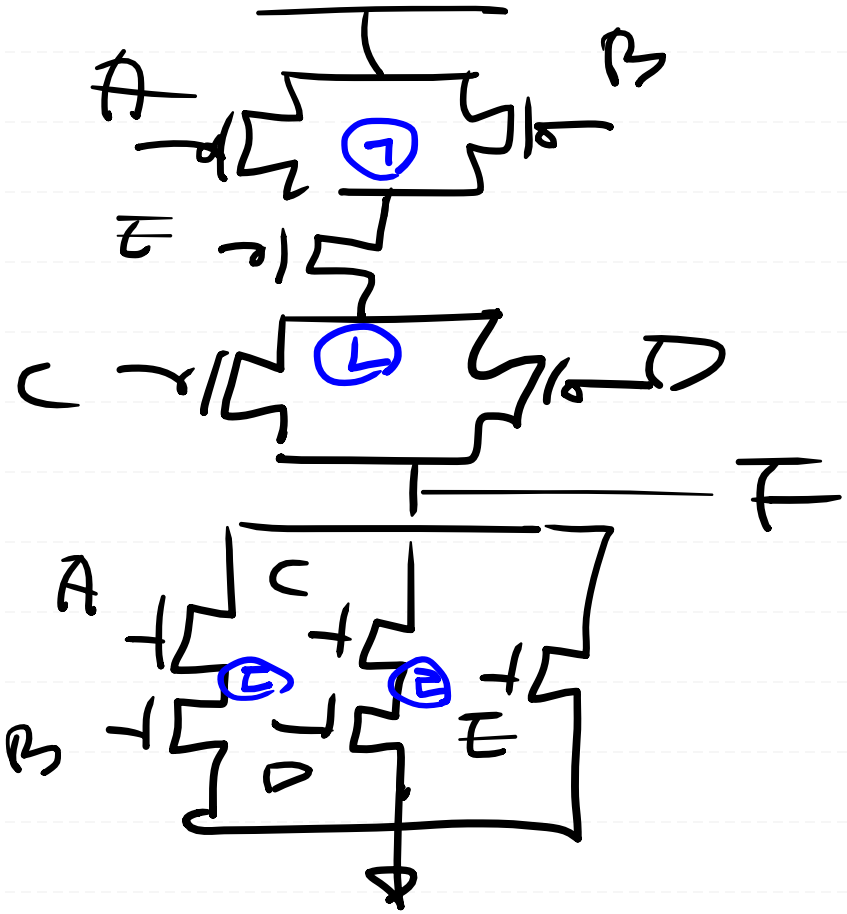


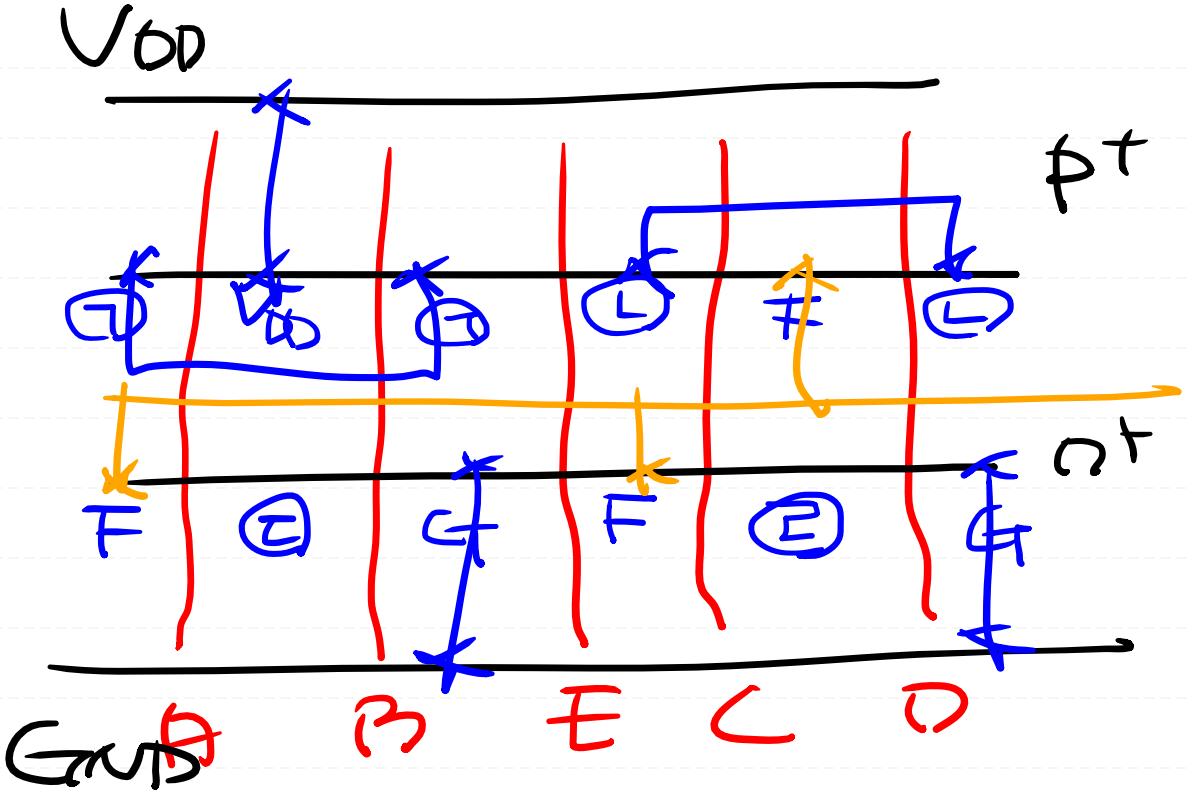
Path A B D C



$$F = \overline{A \cdot B + C \cdot D + E}$$

Path: A B E C D

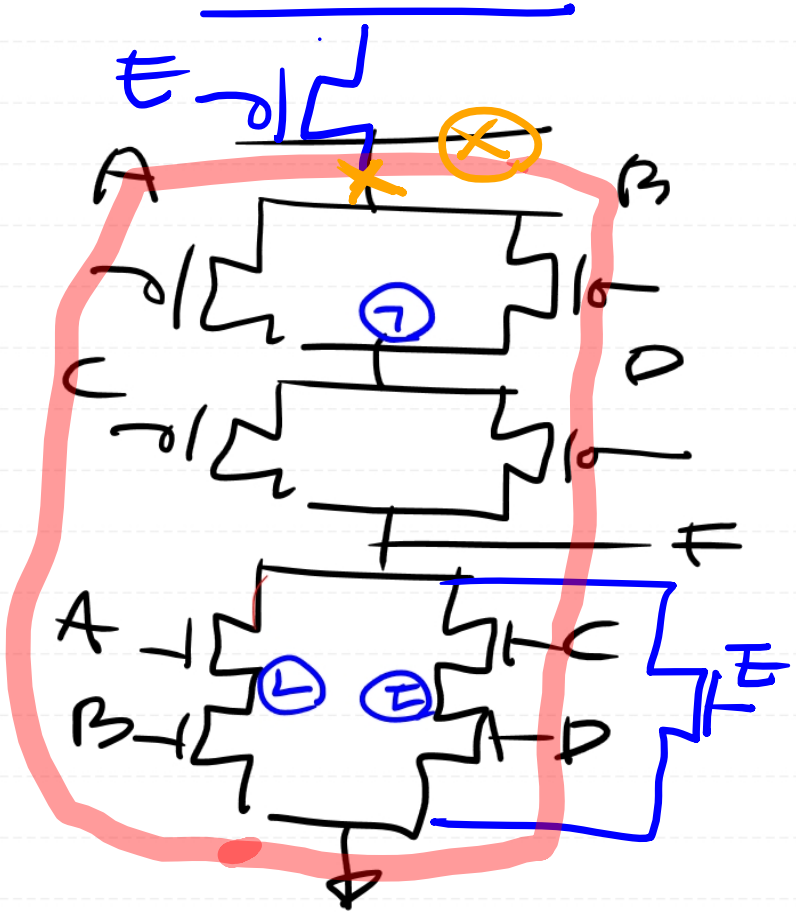




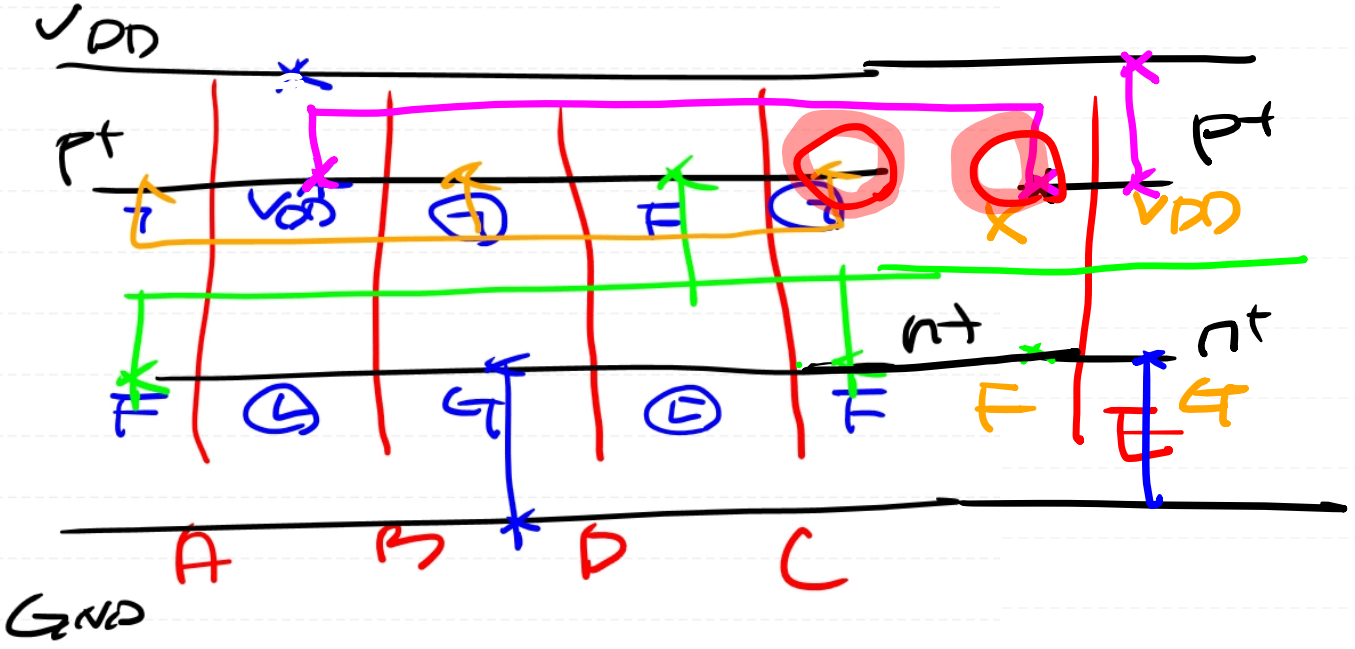
$$F = \overline{A \cdot B + C \cdot D + E}$$

① CMOS schematic

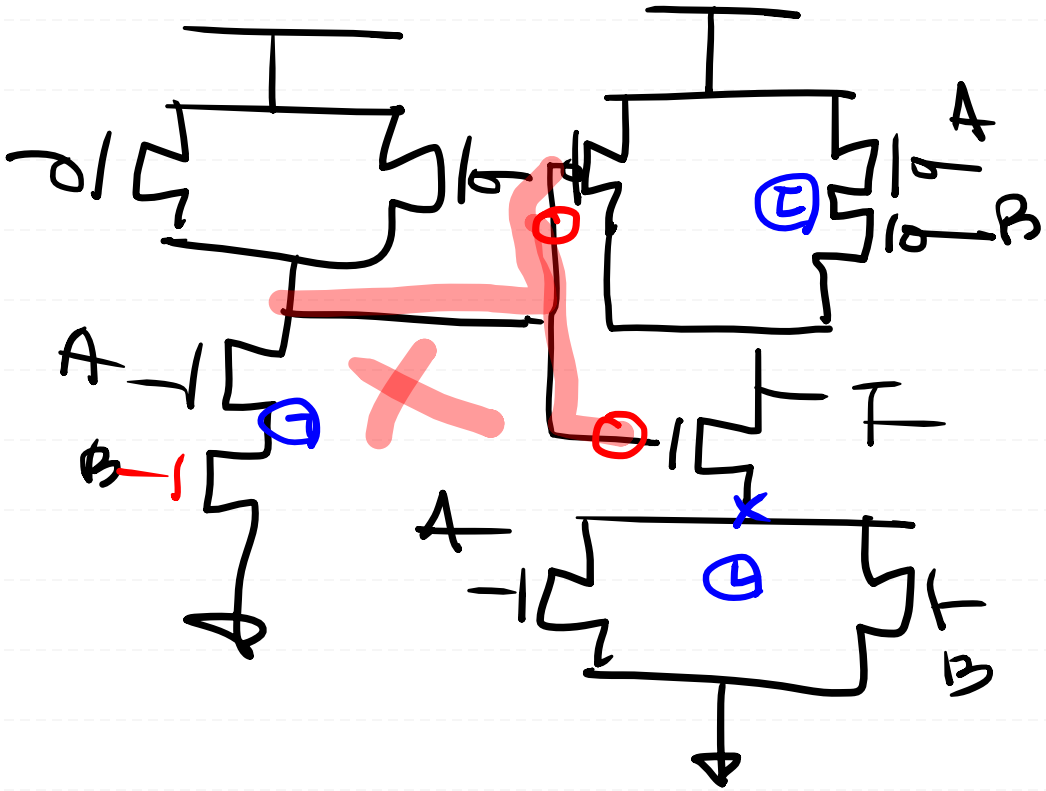
② stick Diagram

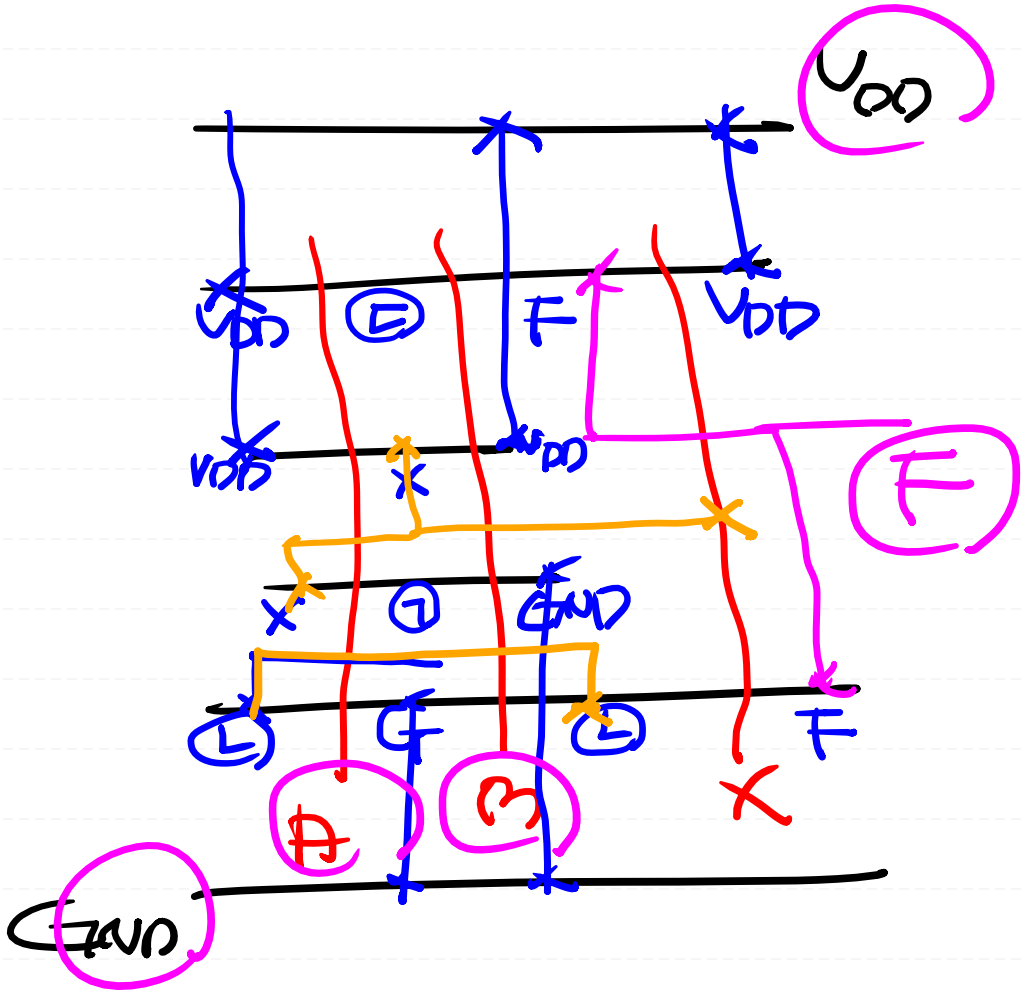


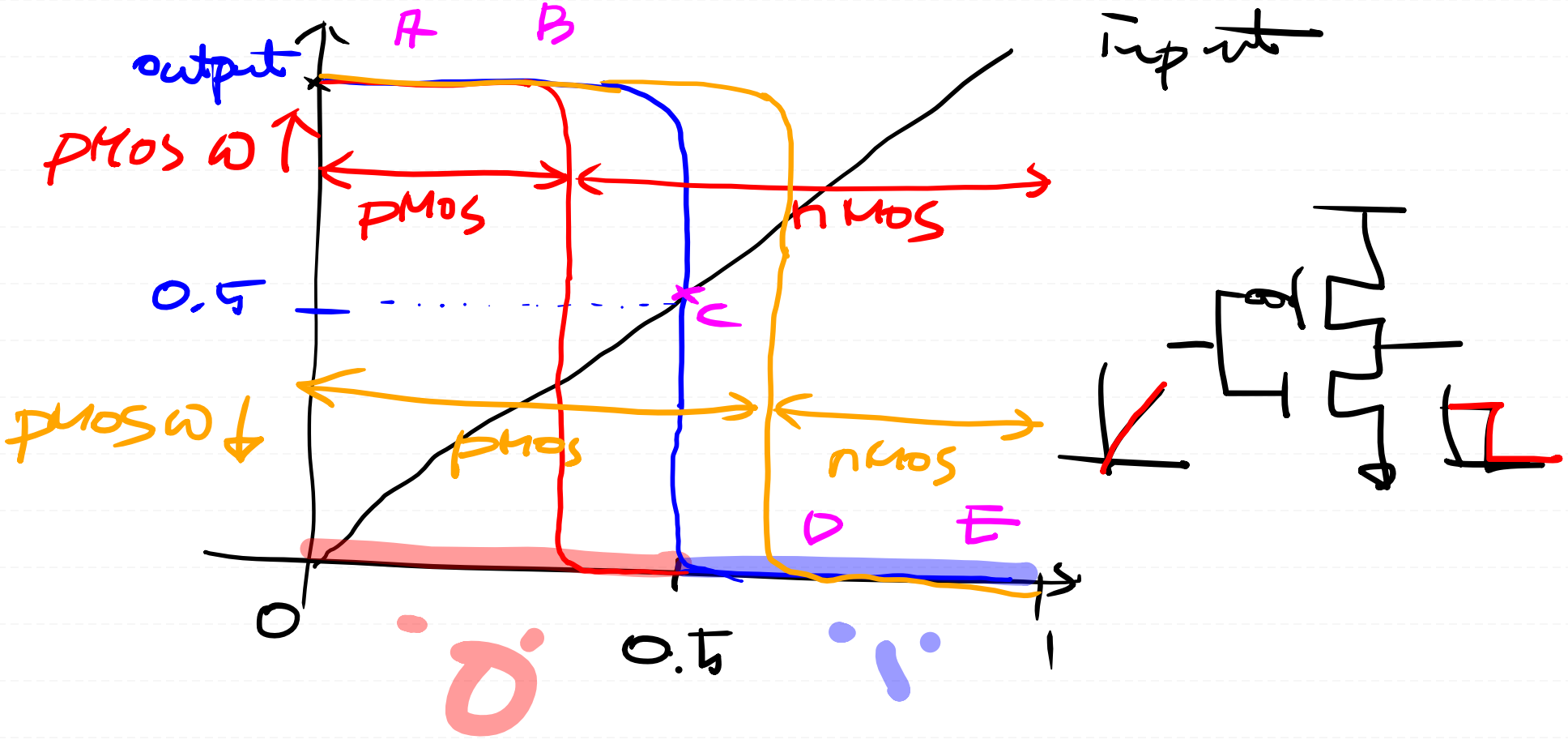
Path A B D C



$$F = \overline{A \cdot B (A+B)} = \overline{O \cdot (A+B)}$$






output
A
B
Input
pMos ω ↑
pMos
nMos
0.5
C
pMos ω ↓
pMos
nMos
D
E
0
0.5
1
0
1