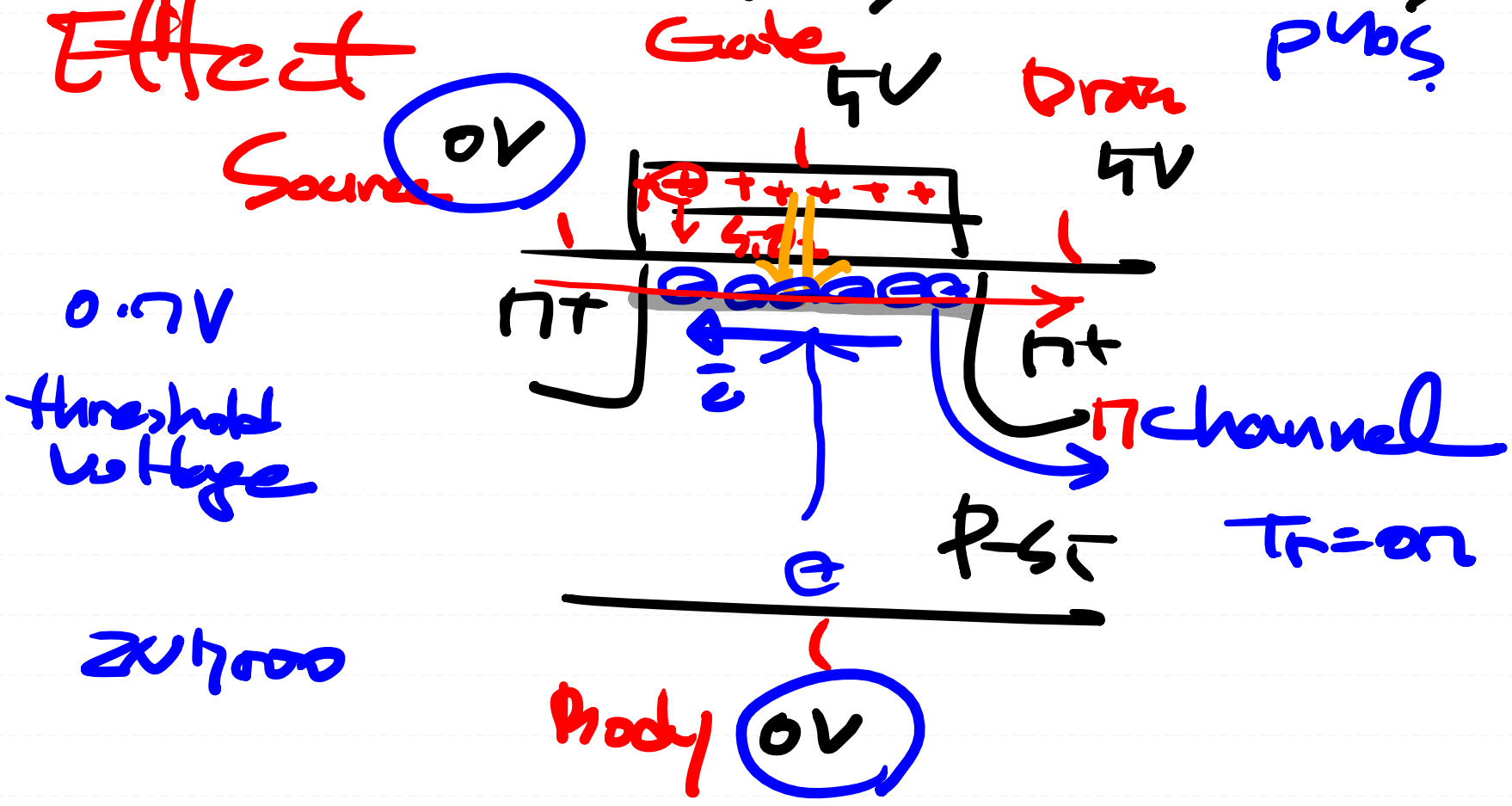
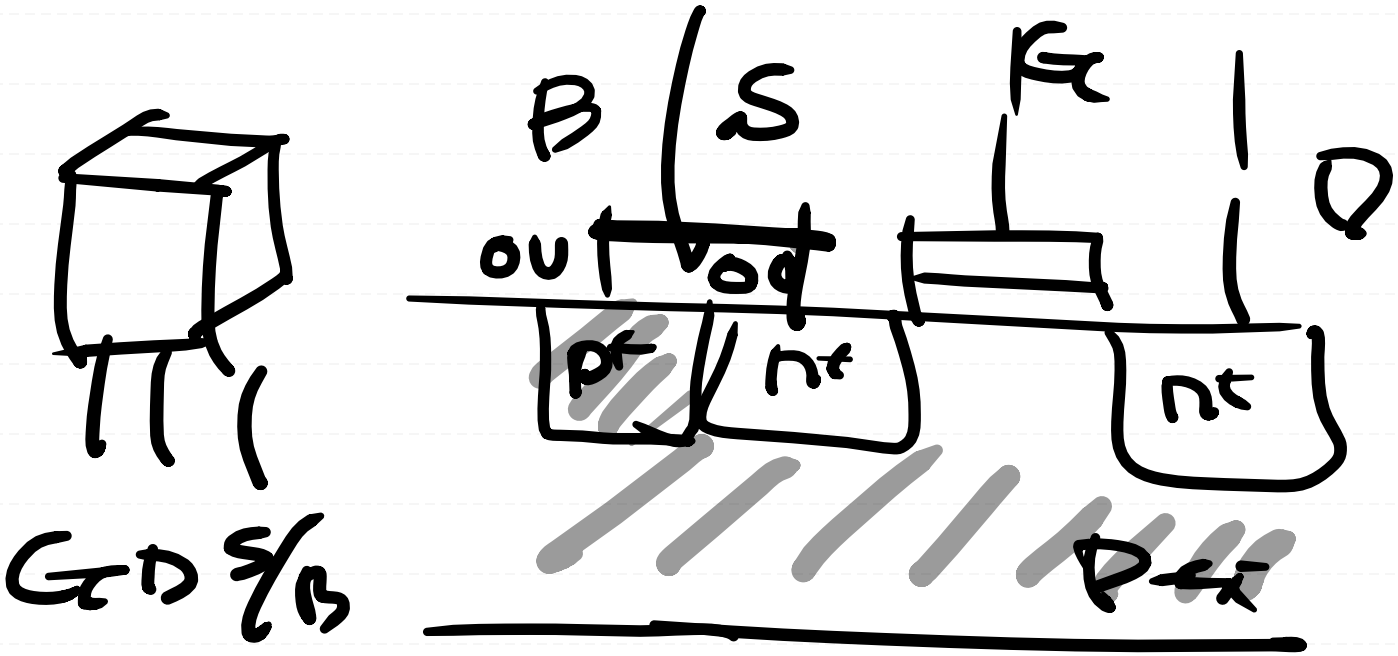
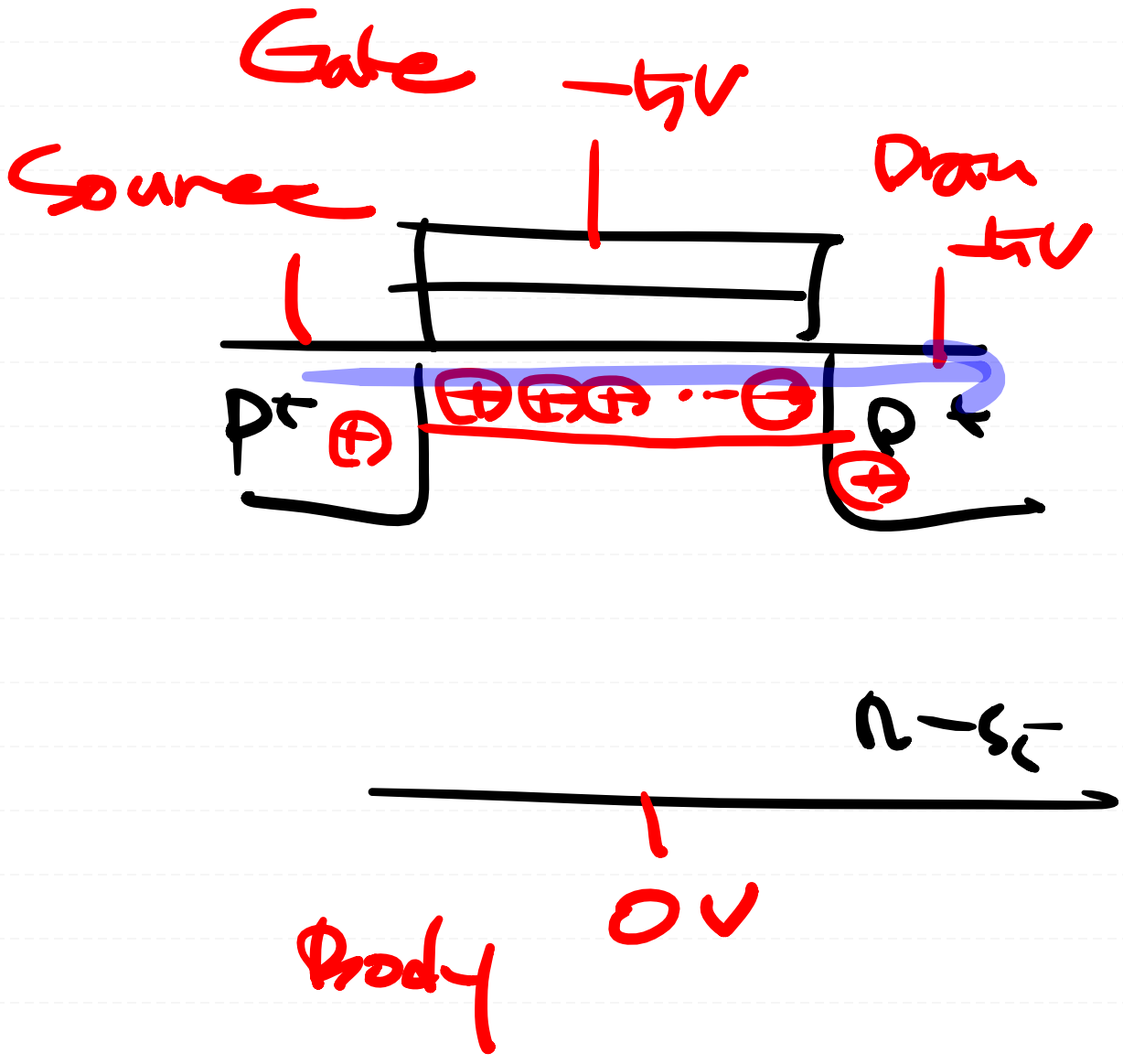
Field-effect transistor (FET)

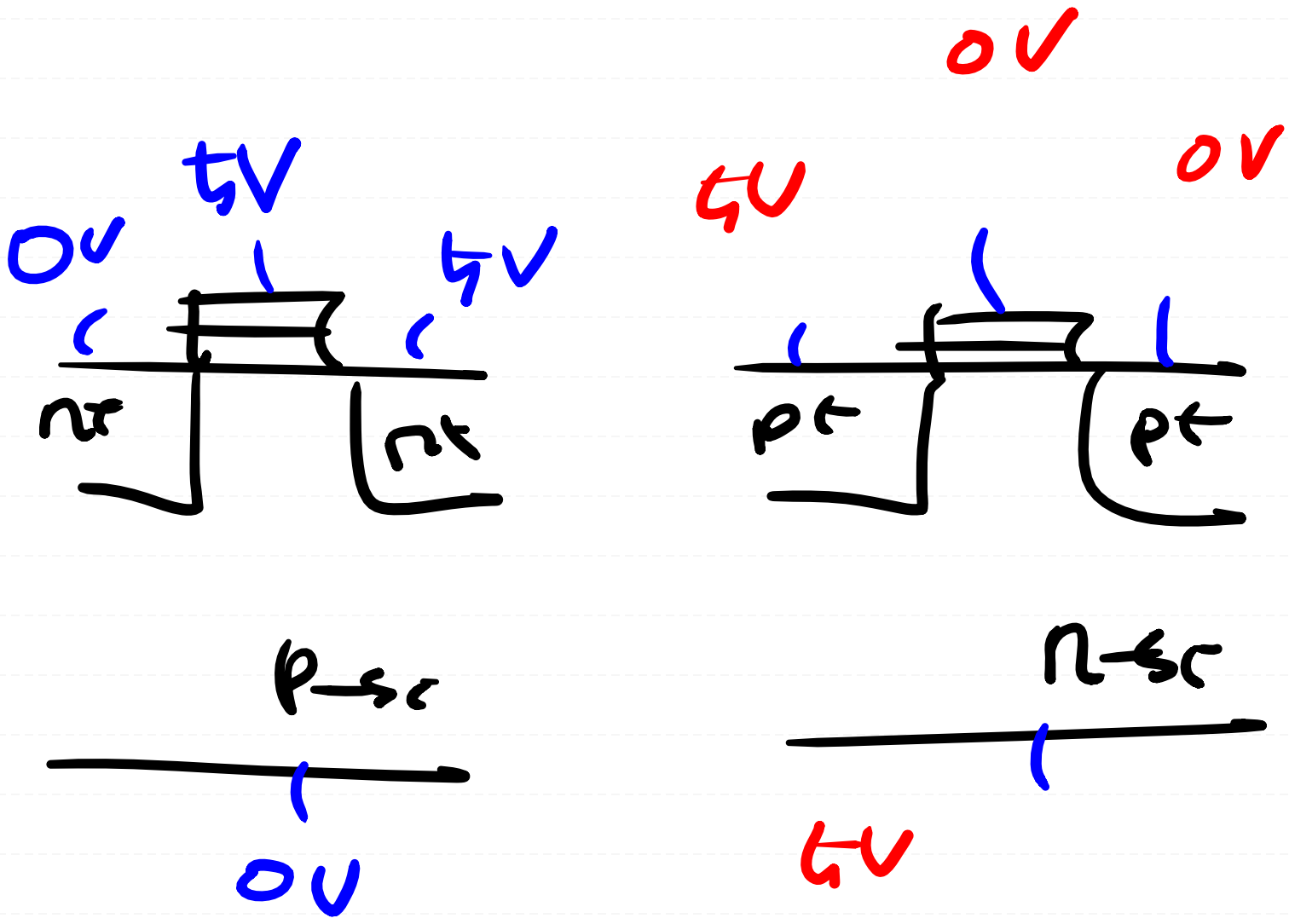
nMOS

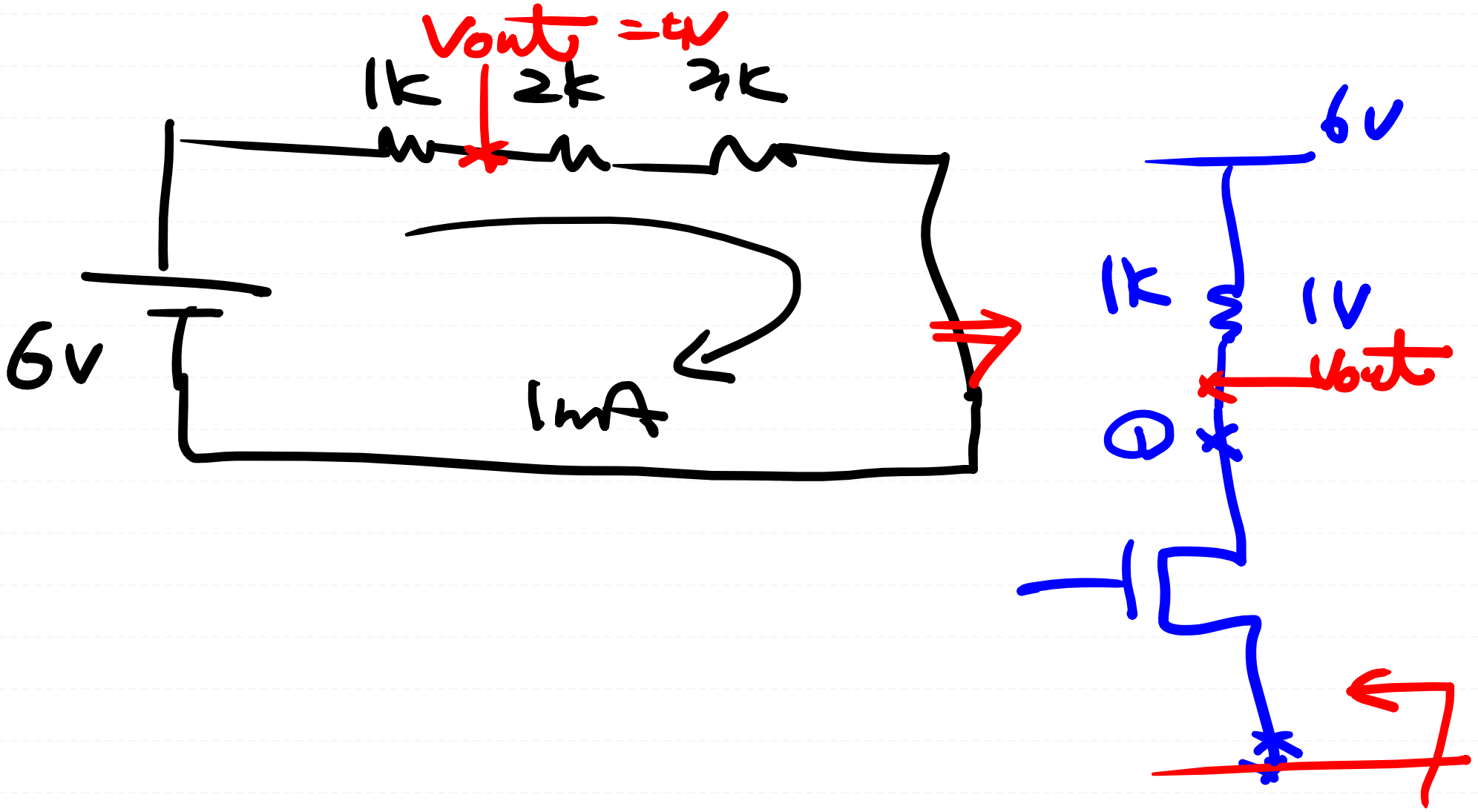
pMOS

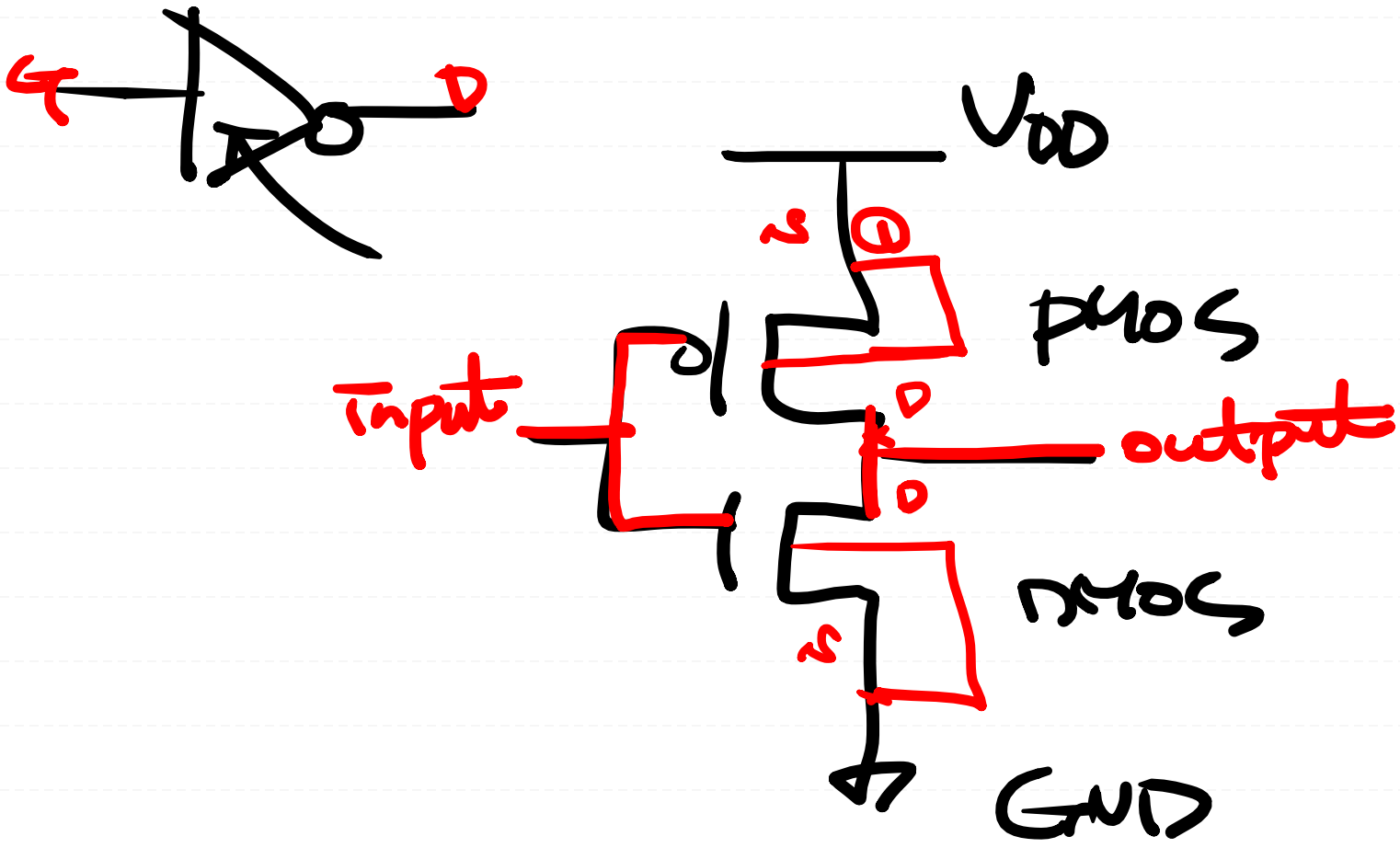


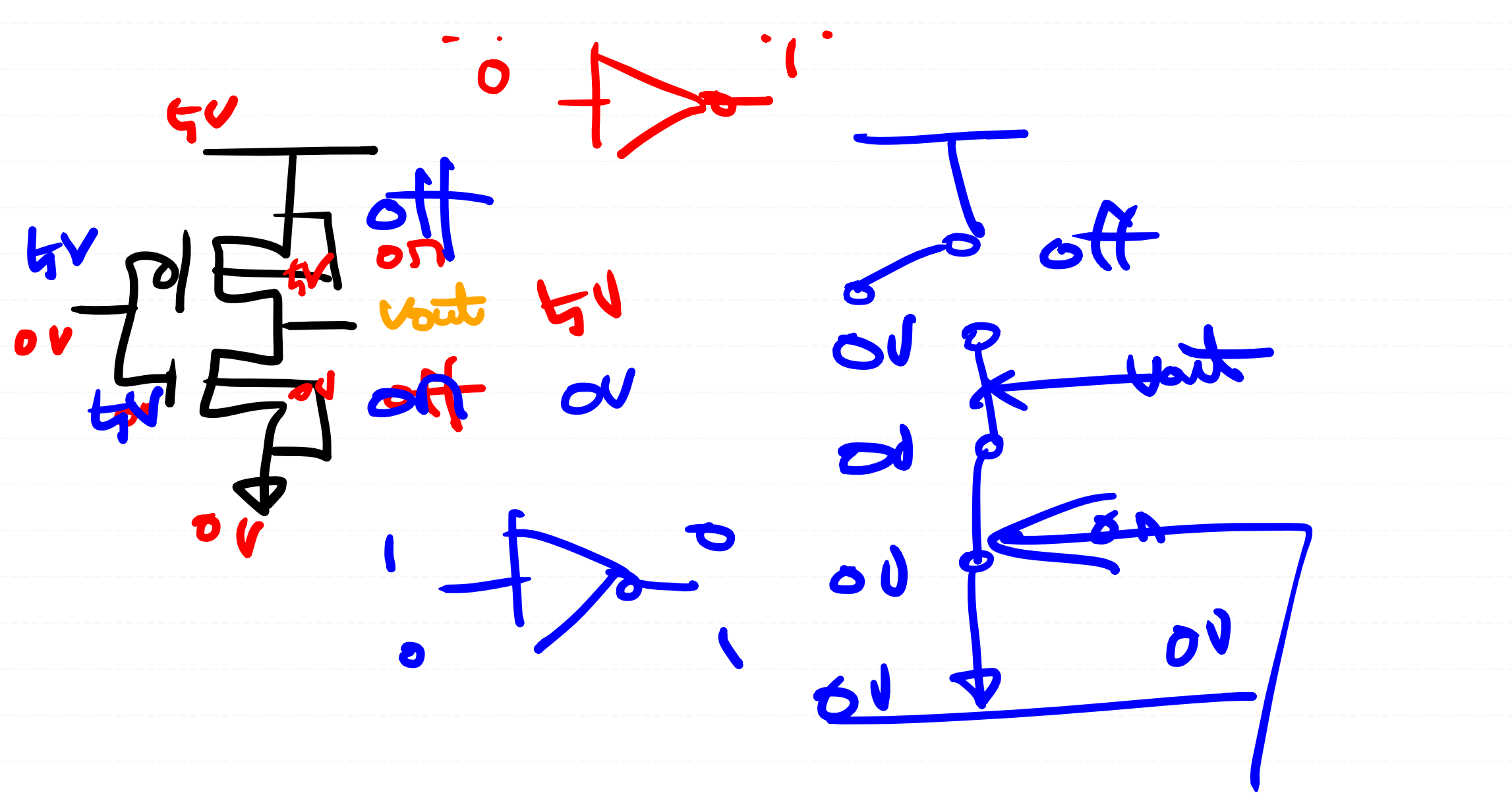

B
S
G
D
Q
out
p+
n+
n+
G D S/B
p-sub


Gate
-5V
Source
Drain
-5V
p+
p+
n-Si
0V
Body


5V
0V
5V
n+
n+
p-sc
0V
0V
5V
p+
p+
n-sc
5V


Vout = 4V
1k
2k
3k
6V
1mA
6V
1k
1V
Vout
0


G
D
VDD
S
PMOS
Input
D
output
D
NMOS
S
GND


0
1
5V
5V
5V
0V
0V
off
on
Vout
off
5V
0V
0V
1
0
0
1
5V
off
0V
Vout
0V
0V
0V

CMOS Schematic

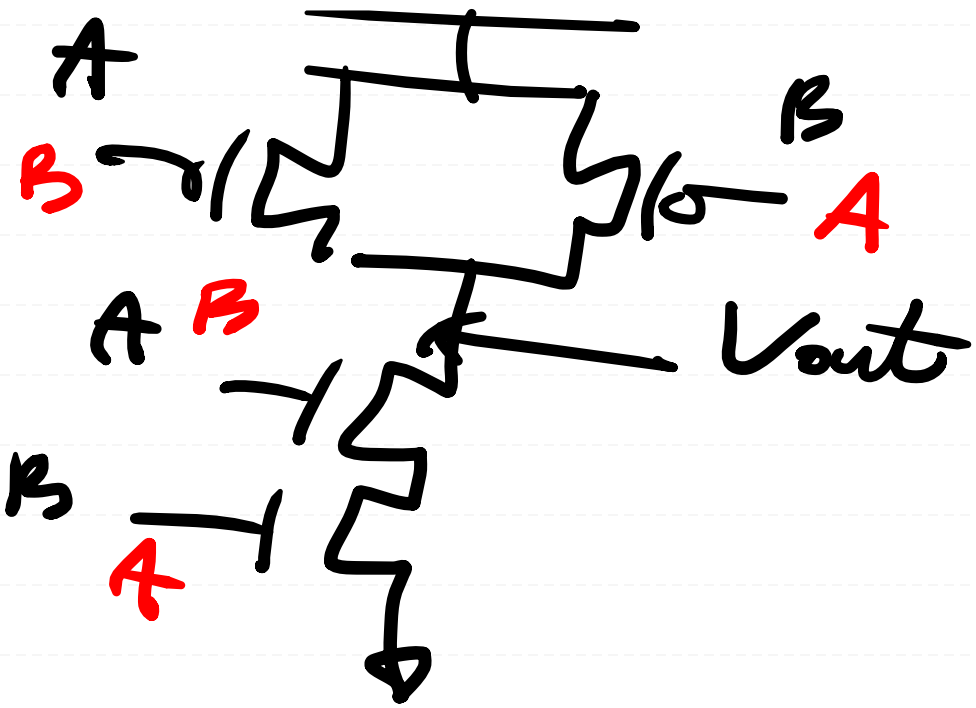
$F = \overline{A \cdot B}$

If a Is AND nMOS 직렬
pMOS 병렬

OR nMOS 병렬
pMOS 직렬

$F = \overline{A \cdot B}$

$\square = A \cdot B$ (AND)

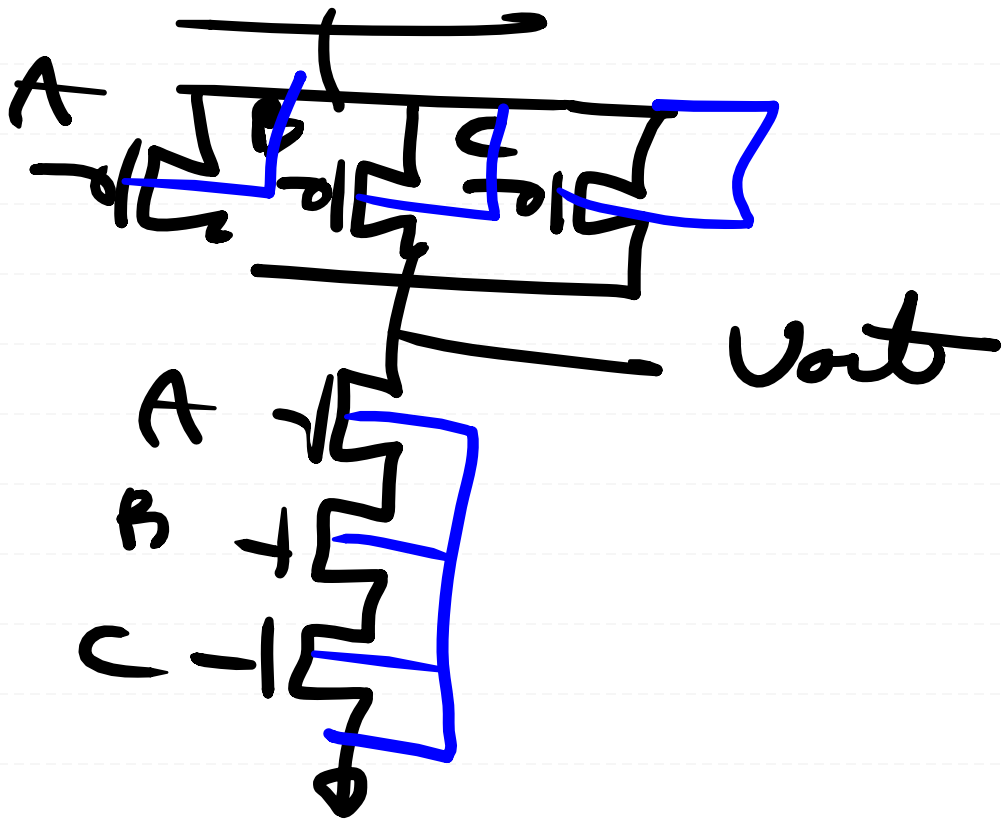


$F = \square$

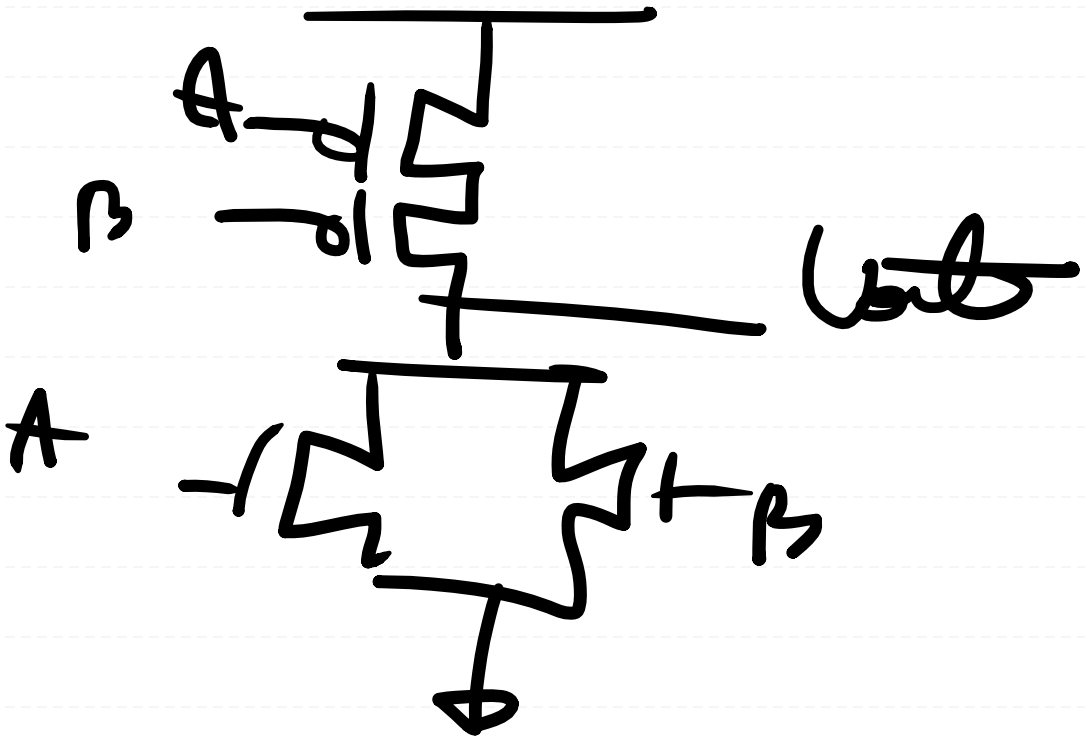
2x3

3x2

$F = \overline{A \cdot B \cdot C}$ $\square = ABC$



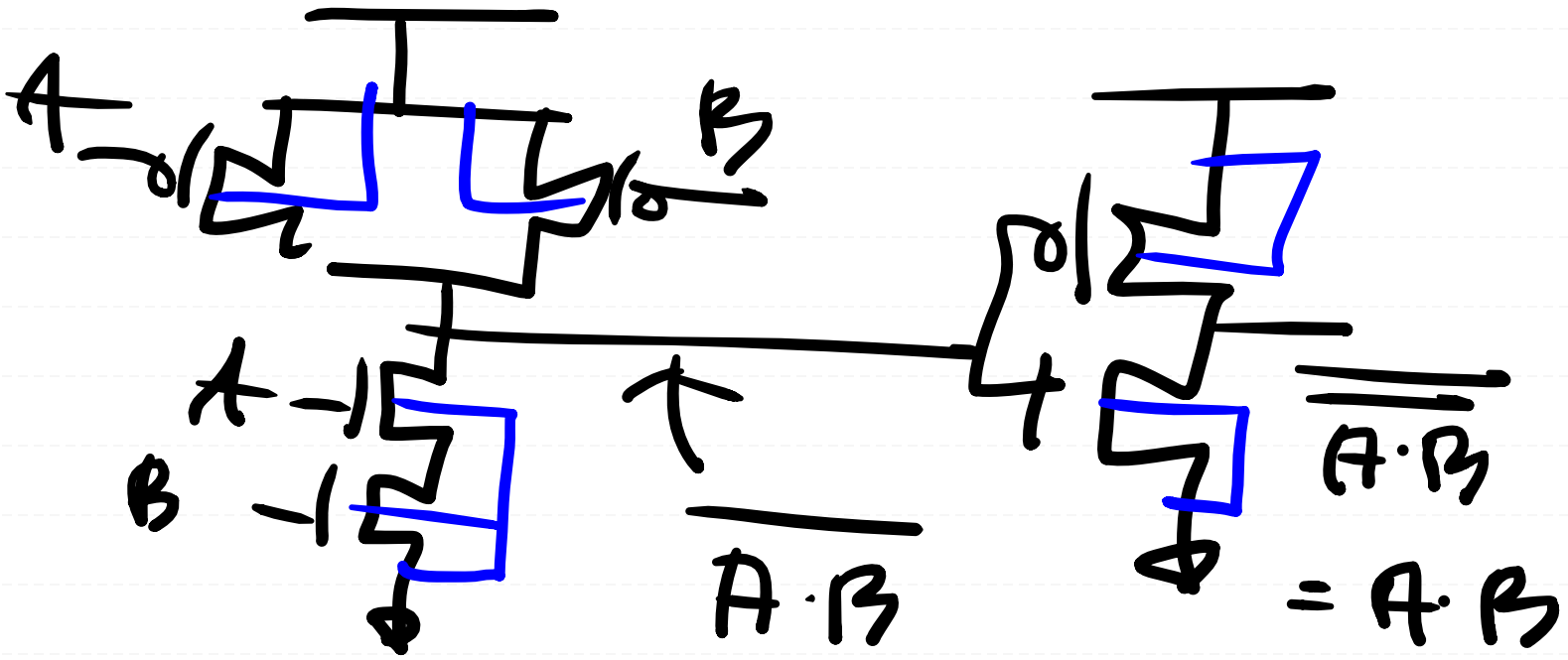
$F = \overline{A + B}$ $\square = A + B$



$F = \overline{A \cdot B}$ $\square = \overline{A \cdot B}$

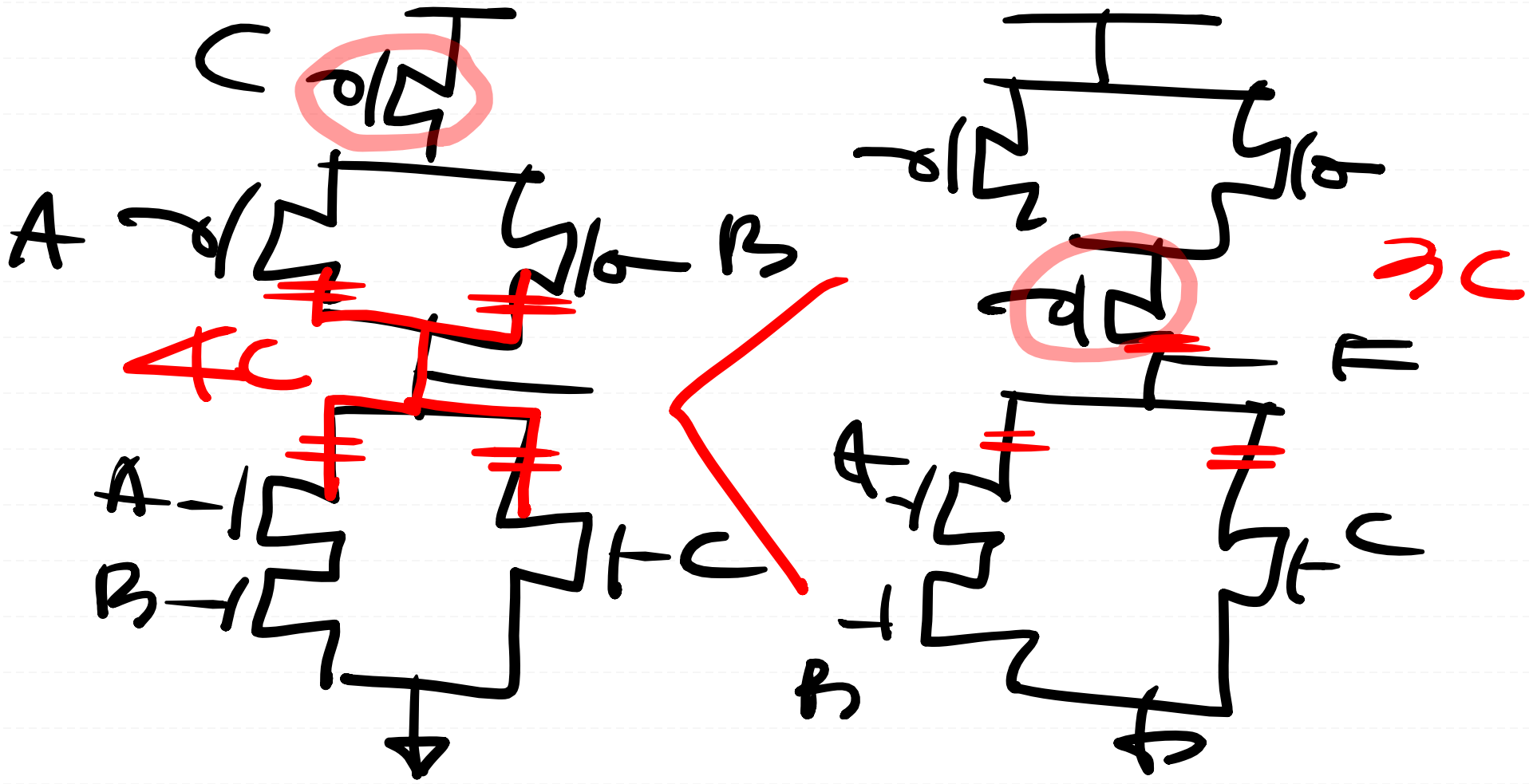
2

$= \overline{A \cdot B}$ 1

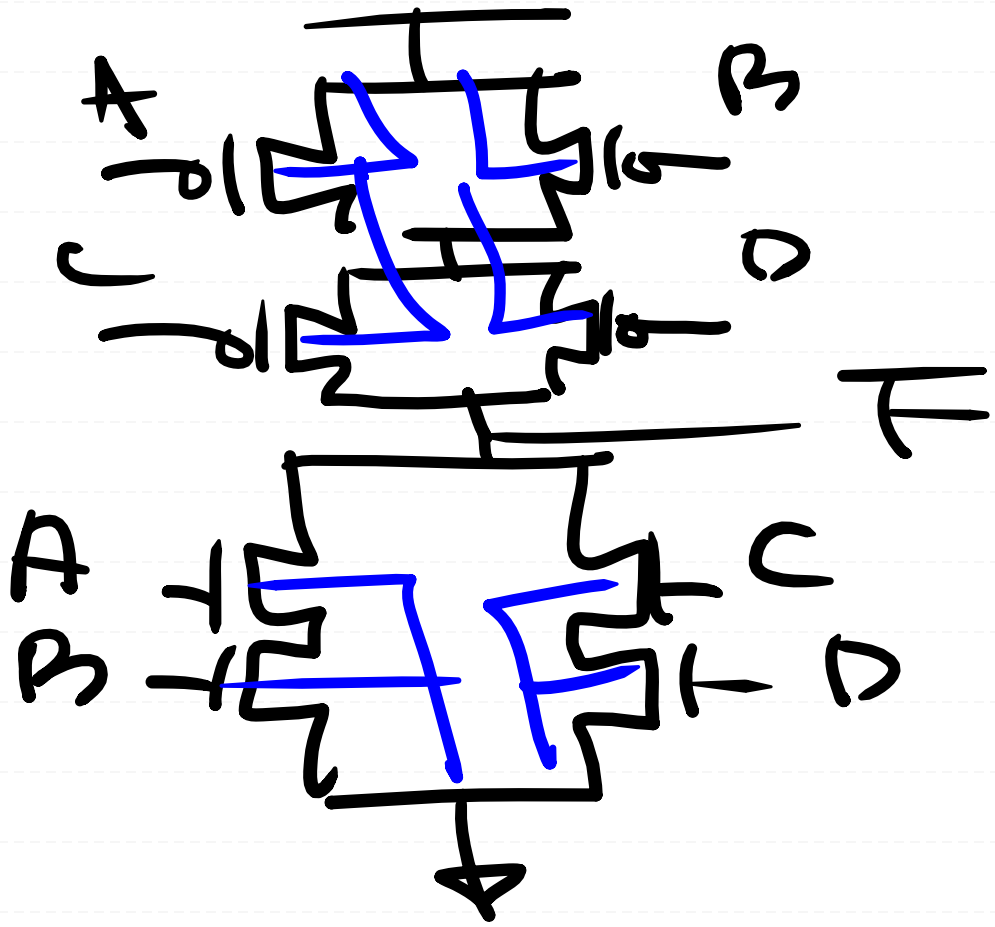


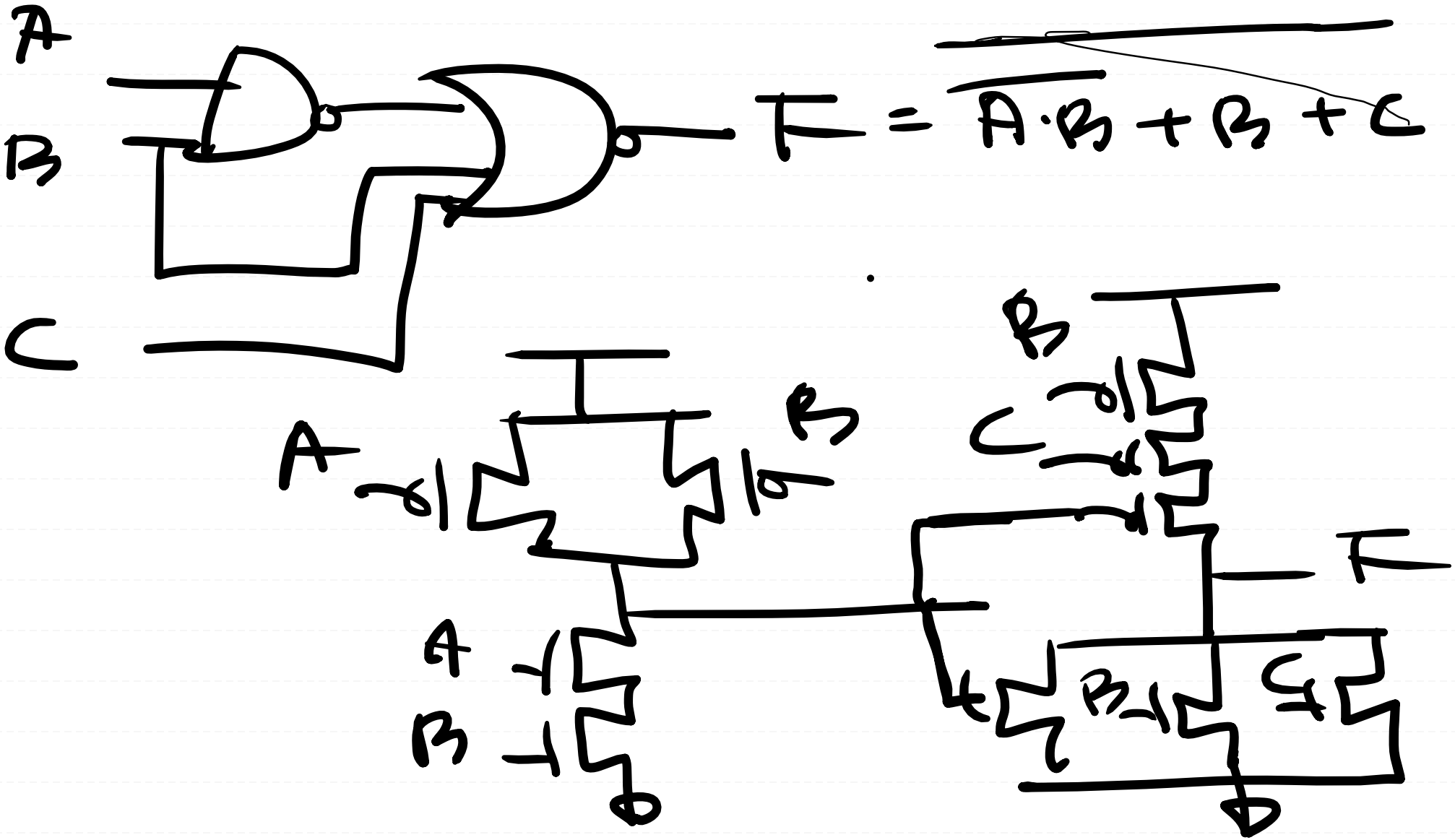
$$F = \overline{A \cdot B + C}$$

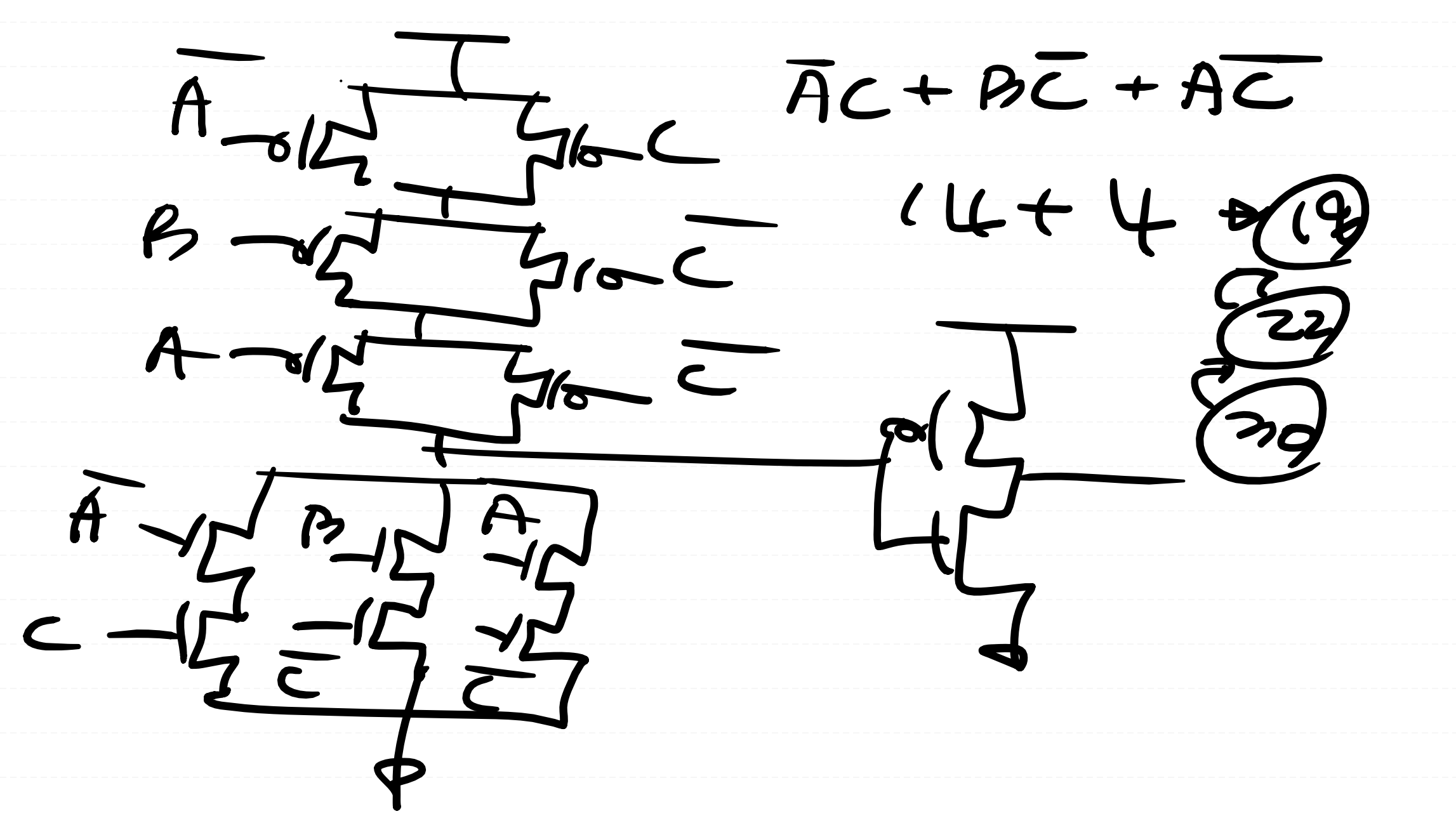
Cmos Schematic

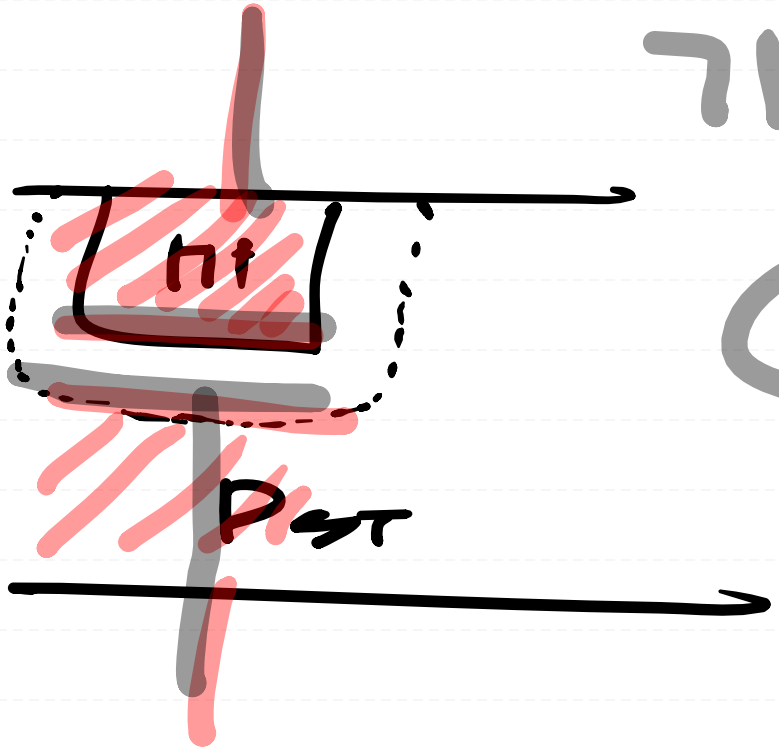


$$F = \overline{A \cdot B + C \cdot D}$$




A
B
C
F = $\overline{A \cdot B + B + C}$
A
B
B
C
F
A
B
B
C


$\bar{A}C + B\bar{C} + A\bar{C}$
A
B
A
C
C
C
A
B
A
C
C
C
(14 + 4 → (18
22
20



기생

Cap.

$\tau = R \times C$