Department of Electrical Engineering

UET, Lahore

Digital Systems Laboratory

Lab # 7(b)

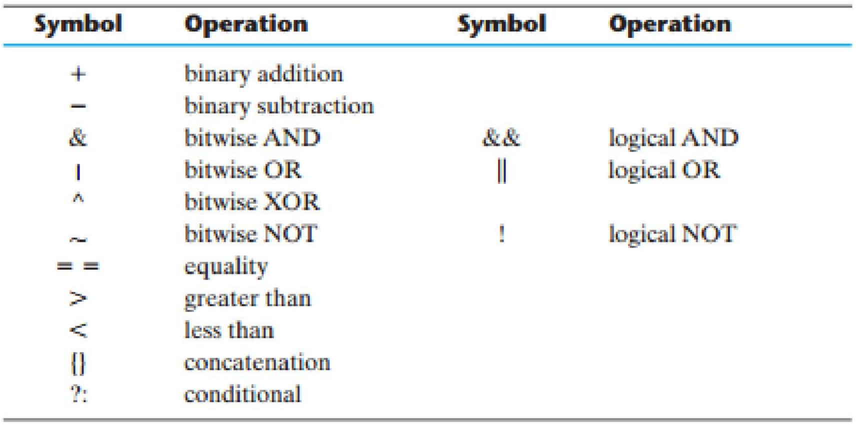
Introduction to the Dataflow Modelling in Verilog HDL

Objectives:

- To learn to program at dataflow level in Verilog HDL.

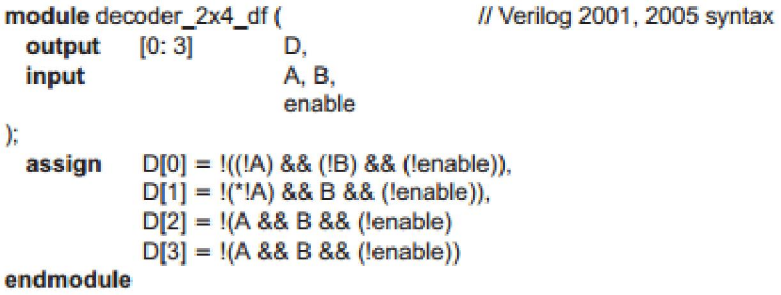
Dataflow Modelling:

Dataflow modeling of combinational logic uses a number of operators that act on binary operands to produce a binary result. Verilog HDL provides about 30 different operators. Table lists some of these operators, their symbols, and the operation that they perform. It is necessary to distinguish between arithmetic and logic operations, so different symbols are used for each.



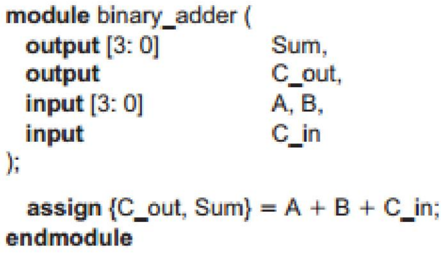
Symbol	Operation	Symbol	Operation
+	binary addition		
−	binary subtraction		
&	bitwise AND	&&	logical AND
|	bitwise OR	||	logical OR
^	bitwise XOR		
~	bitwise NOT	!	logical NOT
= =	equality		
>	greater than		
<	less than		
{}	concatenation		
?:	conditional		

Lab Task (a): Simulate behavioral model of the following Verilog HDL module [2x4 Decoder].



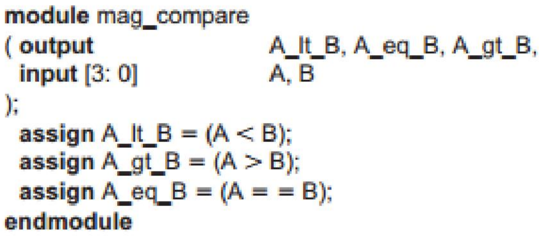
```
module decoder_2x4_df (                         // Verilog 2001, 2005 syntax
  output    [0: 3]          D,
  input                     A, B,
                            enable
);
  assign    D[0] = !((!A) && (!B) && (!enable)),
            D[1] = !(*!A) && B && (!enable)),
            D[2] = !(A && B && (!enable)
            D[3] = !(A && B && (!enable))
endmodule
```

Lab Task (b): Simulate behavioral model of the following Verilog HDL module [4-Bit Binary Adder].



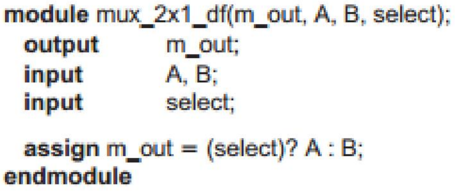
```
module binary_adder (
  output [3: 0]          Sum,
  output                 C_out,
  input [3: 0]           A, B,
  input                  C_in
);
  assign {C_out, Sum} = A + B + C_in;
endmodule
```

Lab Task (c): Simulate behavioral model of the following Verilog HDL module [4-Bit Binary Magnitude Comparator].



```
module mag_compare
( output                 A_lt_B, A_eq_B, A_gt_B,
  input [3: 0]           A, B
);
  assign A_lt_B = (A < B);
  assign A_gt_B = (A > B);
  assign A_eq_B = (A = = B);
endmodule
```

Lab Task (d): Simulate behavioral model of the following Verilog HDL module [2 to 1 line multiplexer].



```
module mux_2x1_df(m_out, A, B, select);
  output        m_out;
  input         A, B;
  input         select;
  assign m_out = (select)? A : B;
endmodule
```

Lab Instructor: ________________________

Dated: ________________________