**Department of Electrical Engineering**

**UET, Lahore**

**Digital Systems Laboratory**

# Lab # 12(a)

# Analysis and Design of Clocked Sequential Circuits

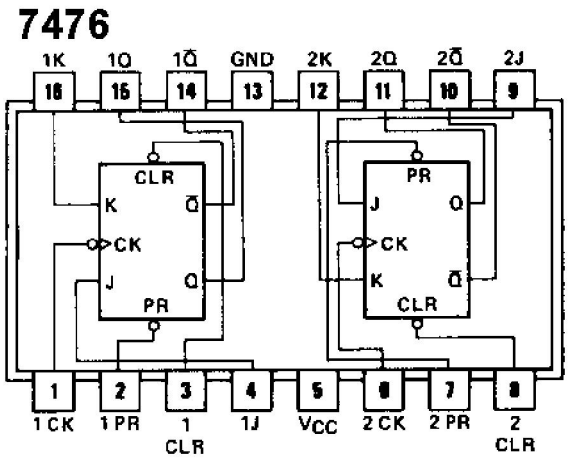
**Objective:**

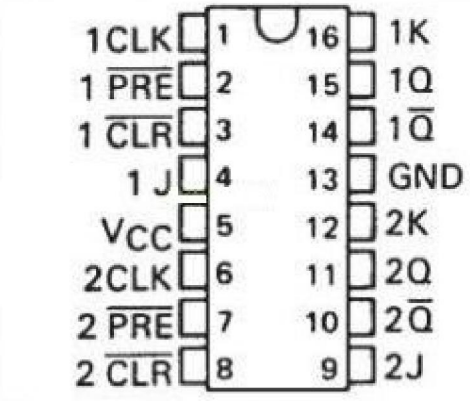
- In the first part of this lab, you will **analyze** a sequential circuit and verify its state diagram by observing the states of memory devices under clocked input.
- In the second part of this lab, you will **design** a clocked sequential circuit based on specific design requirements and verify your design by implementing it on hardware.

**Apparatus:**

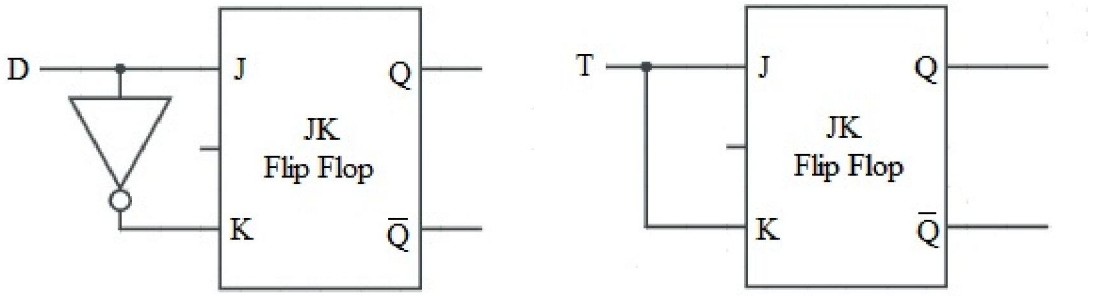
- 74LS76 Dual JK- flip flop IC
- 74LS08 AND gate IC
- 74LS86 XOR gate IC
- 74LS04 NOT gate IC
- 74LS247 BCD to IC
- 330Ω Resistors
- Common anode single 7 Segment display unit

74LS76 is a dual JK- flip flop digital IC. Its pin configuration is as follows:



You can construct a D- flip flop using a JK flip flop by adding a NOT gate between J and K inputs. Also by combining J and K terminals you can make a T-flip flop.

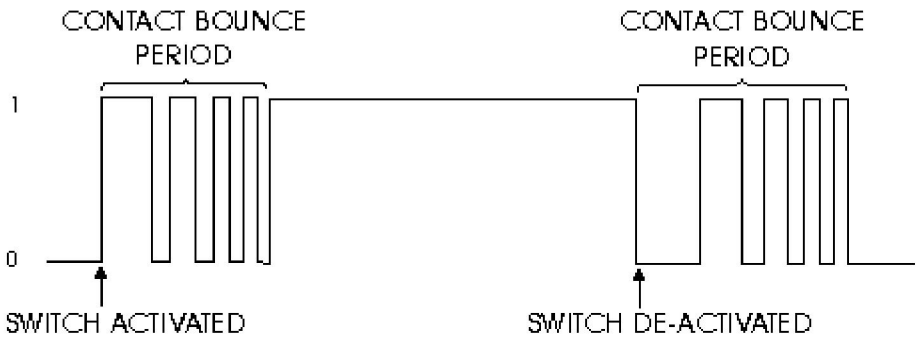



In today's lab you will observe an important issue related to the use of buttons, viz. 'Bouncing of buttons'.

**Bouncing of buttons**

Push-button switches, toggle switches, and electro-mechanical relays all have one thing in common: contacts. It's the metal contacts that make and break the circuit and carry the current in switches and relays. Because they are metal, contacts have mass. And since at least one of the contacts is on a movable strip of metal, it has springiness. Since contacts are designed to open and close quickly, there is little resistance (damping) to their movement.

Because the moving contacts have mass and springiness with low damping they will be "bouncy" as they make and break. That is, when a normally open (N.O.) pair of contacts is closed, the contacts will come together and bounce off each other several times before finally coming to rest in a closed position. The effect is called "contact bounce" or, in a switch, "switch bounce". See figure below. Note that contacts can bounce on opening as well as on closing




**The Problem**

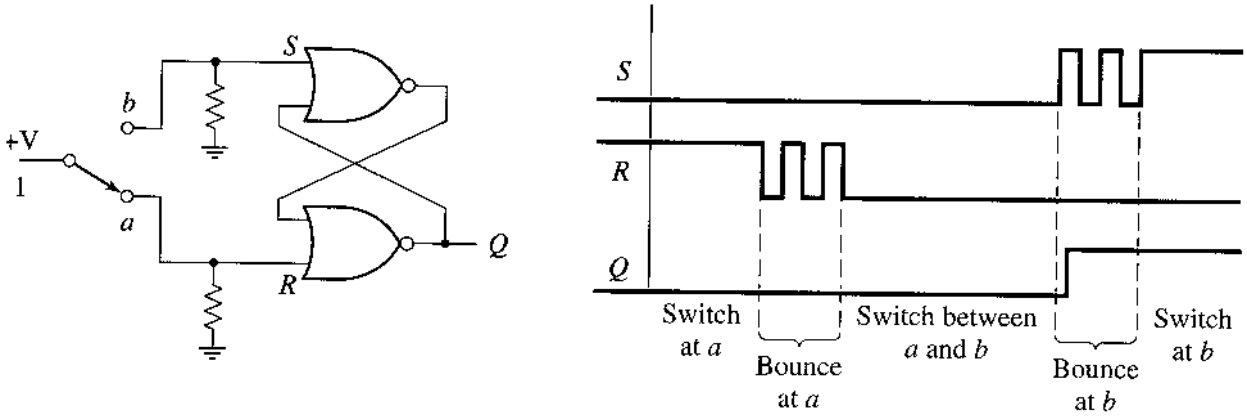
If all you want your switch or relay to do is turn on a lamp or start a fan motor, then contact bounce is not a problem. But if you are using a switch or relay as input to a digital counter, a personal computer, a digital IC, or a micro-processor based piece of equipment, then you must consider

contact bounce. The reason for concern is that the time it takes for contacts to stop bouncing is measured in milliseconds. Digital circuits can respond in microseconds/nanoseconds.

For example, in our case the response time of CLK input of 74LS76 is 16-25ns. If we apply CLK through a switch then 74LS76 will detect multiple clock edges on single change of state of the switch. As a result our sequential circuit will change multiple states when we would be expecting a single step change.

**Solution**

There are several ways to solve the problem of contact bounce (that is, to "de-bounce" the input signal). A hardware approach is shown below. It uses a cross-coupled latch made from a pair of nor gates. You can also use an SR (sometimes called an SC) flip flop. The advantage of using a latch is that you get a clean de-bounce without a delay limitation. It will respond as fast as the contacts can open and close. Note that the circuit requires both normally open and normally closed contacts. In a switch, that arrangement is called "double throw". In a relay, that arrangement is called "Form C".




**Lab Part (a): Analysis of clocked sequential circuits:**

**Theoretical Background:**

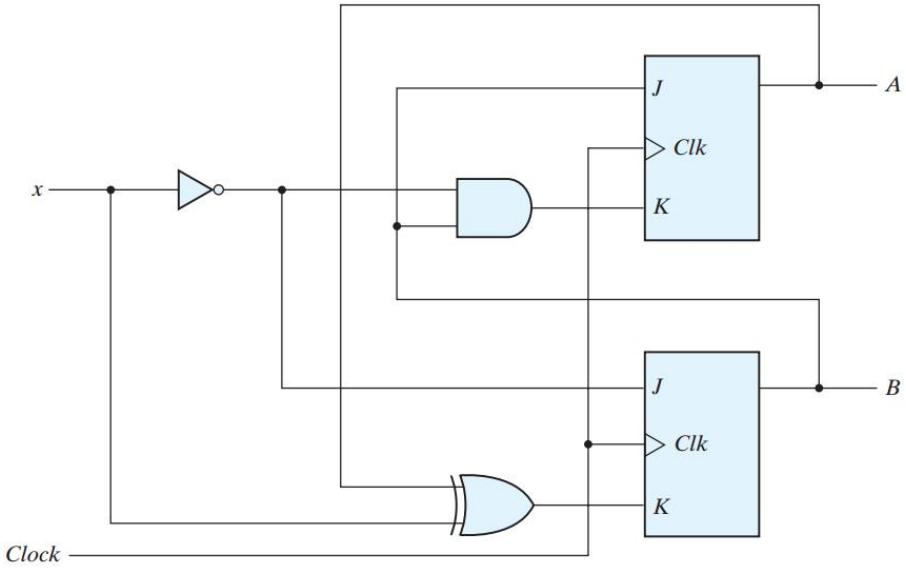
Analysis describes what a given circuit will do under certain operating conditions. The behavior of a clocked sequential circuit is determined from the inputs, the outputs, and the state of its flip-flops. The outputs and the next state are both a function of the inputs and the present state. The analysis of a sequential circuit consists of obtaining a table or a diagram for the time sequence of inputs, outputs, and internal states.

State table is made by listing next state values and outputs of sequential circuits versus present states and the inputs. The next-state values of a sequential circuit (that may use D-, JK- or T-type flip-flops) can be derived as follows:

1. Determine the flip-flop input equations in terms of the present state and input variables.
2. List the binary values of each input equation.
3. Use the corresponding flip-flop characteristic table to determine the next-state values in the state table.

**Lab Task (a):**

Analyze the following sequential circuit, i.e. obtain state table and then verify its state diagram by observing states of flip flops on the trainer board.




**Flip Flop Input Equations:**

$J_A$ = _____ $K_A$ = _____

$J_B$ = _____ $K_B$ = _____

| Present States | | Input | Next States | | Flip Flop Inputs | | | |
|---|---|---|---|---|---|---|---|---|
| A | B | X | A | B | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
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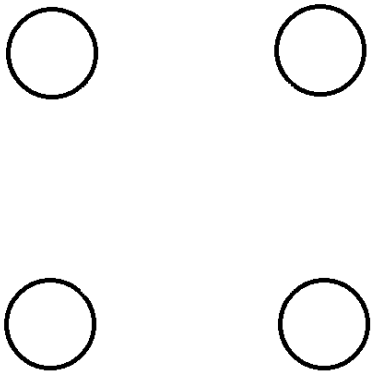
**State Diagram:**



**Observations & Comments:**

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_____

_____

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**Lab Part (b): Design of clocked sequential circuits:**

**Theoretical Background:**

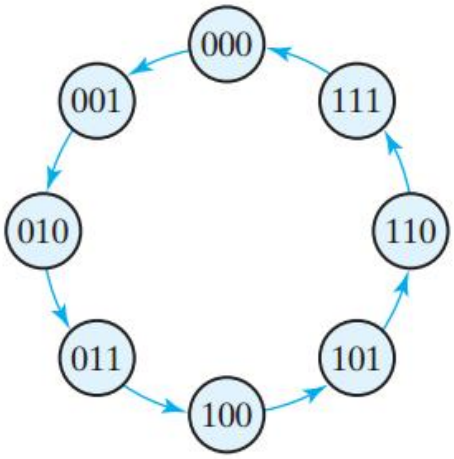
Design procedures or methodologies specify hardware that will implement a desired behavior. The design effort for small circuits may be manual, but industry relies on automated synthesis tools for designing massive integrated circuits. In our lab session, however, we'll focus on manual design procedure.

The procedure for designing synchronous sequential circuits can be summarized by a list of recommended steps:

1. From the word description and specifications of the desired operation, derive a state diagram for the circuit.
2. Reduce the number of states if necessary.
3. Assign binary values to the states.
4. Obtain the binary-coded state table.
5. Choose the type of flip-flops to be used.
6. Derive the simplified flip-flop input equations and output equations.
7. Draw the logic diagram.

**Lab Task (b):**

Design a three-bit binary counter. An n-bit binary counter consists of n flip-flops that can count in binary from 0 to $2^{n-1}$. The state diagram of a three-bit counter is shown below:




Verify the operation of your design using the trainer board. Use a BCD to 7 segment decoder IC and a 7 segment display unit to get a digital display (0-7) of the state variables.

**State Table:**

| Present States | | | Next States | | | Flip Flop Inputs | | |
|---|---|---|---|---|---|---|---|---|
| A | B | C | A | B | C | $T_A$ | $T_B$ | $T_C$ |
| | | | | | | | | |
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| Q(t) | Q(t+1) | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Use the following excitation table to obtain the Flip Flop Inputs.

Find the minimized Boolean function for the inputs of flip flops using K-map.

| | | | |
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$T_A$ =_____ $T_B$ =_____ $T_C$ =_____

**Hardware:**

**Observations & Comments:**

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_____

**Assignment:**

Design a sequential circuit that detects three consecutive 1's in an input sequence. Use D- flip flops for the design. Verify your design in lab.

**Lab Instructor:** _____

**Dated:** _____