Department of Electrical Engineering

UET, Lahore

Digital Systems Laboratory

Lab # 13

Sequential Logic: Counters

Objective:

In this lab you will learn:

- To design a binary counter using flip flops.
- To use IC for the binary counter operation.
- To cascade multiple counters in order to make custom counters.
- To implement mod N counter.

Apparatus:

- 74LS76 Dual JK- flip flop IC
- 74LS192 Presettable BCD up/down counter IC

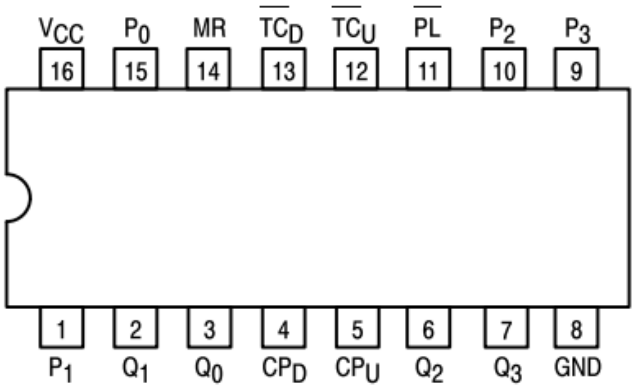
Lab Part (a): Implementation of 3-bit binary asynchronous counter using flip flops.

Lab Task (a): Design and implement a 3-bit binary asynchronous counter using T-flip flops. Display the count on a seven segment display using a BCD to 7 Segment Decoder IC.

Design:

Lab Part (b): Implementation of a cascaded counter and mod N counter.

In this part you'll use an IC for counter operation, viz. 74LS192. It is a presettable/resettable BCD up/down counter IC. Pin configuration and pin description of the 74LS192 IC is shown below:

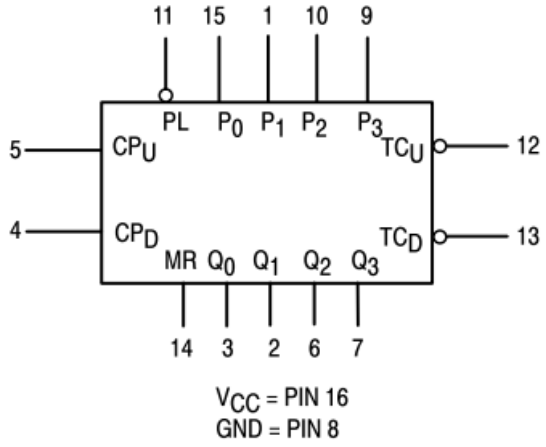


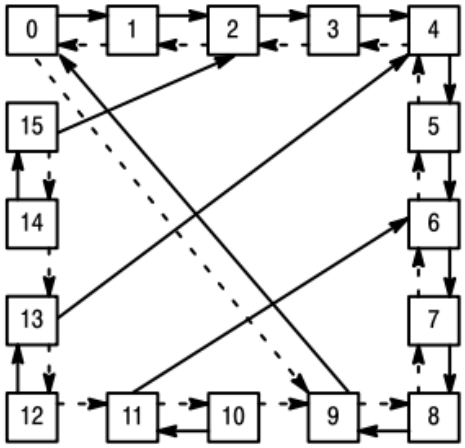
PIN NAMES

CP_U	Count Up Clock Pulse Input
CP_D	Count Down Clock Pulse Input
$\overline{MR}$	Asynchronous Master Reset (Clear) Input
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input
P_n	Parallel Data Inputs
Q_n	Flip-Flop Outputs (Note b)
$\overline{TC_D}$	Terminal Count Down (Borrow) Output (Note b)
$\overline{TC_U}$	Terminal Count Up (Carry) Output (Note b)

The logic diagram and the state diagram of the IC are presented below. The state diagram shows that 74LS192 is a BCD counter IC with the features of both up counting and down counting. Note that the unused states are also accounted for in the state diagram.

LOGIC SYMBOL





LS192

Table showing the modes of operation of 74LS192 IC are presented on the right. It shows that MR has highest priority level among all inputs. PL has highest priority after MR, which means that while IC is in parallel loading mode, count operation is ceased.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
⎍ = LOW-to-HIGH Clock Transition

Lab Task (b): Verify the following operations of 74LS192:

- Count up
- Count down
- Master reset
- Parallel Loading

Lab Task (c): Using 74LS192, design and implement a custom counter that counts from 00 to 99.

Design:

Lab Task (d): Modify the design of your last counter to make a Mod 60 counter. Implement your design.

Design:

Comments:

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Assignment:

- [Home Assignment] Implement Verilog HDL based hierarchical or behavioral model of a synchronous up/down binary counter with parallel load and asynchronous reset. [Read article 6.6 of the book: Digital Design by M. Morris Mano and Michael D. Ciletti]
- [Home Assignment] Implement Verilog HDL based hierarchical or behavioral model of a binary up/down ripple counter with parallel load and asynchronous reset. [Read article 6.6 of the book: Digital Design by M. Morris Mano and Michael D. Ciletti]

Lab Instructor: _____

Dated: _____