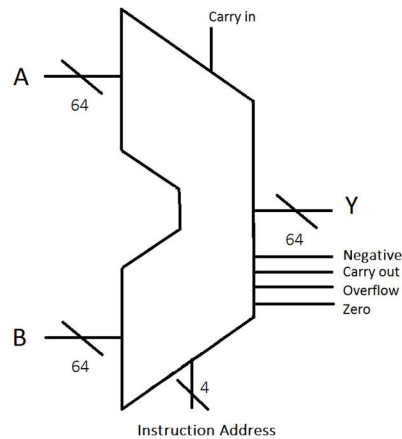


November 7, 2016

Session 2015

Design and implement a 64-bit arithmetic and logic unit (ALU) with a 4-bit address bus using Verilog HDL. The ALU should be able to perform the multiple operations on the two 64-bit input numbers against the instruction addresses shown in the table below. The ALU should accept two 64-bit numbers as its input and output a 64-bit number as the result of operation performed. The ALU should also accept a 'carry in bit' and output a 'carry out bit', an 'overflow bit', a negative bit (a bit that goes high when output goes negative) and a 'zero bit' (a bit that goes high when output is equal to zero).



| Sr. No. | Instruction address (Hex) | Operation  |
|---------|---------------------------|--|
| 1       | 0x00                      | Move A to output ( $O=A$ )   |
| 2       | 0x01                      | Move B to output ( $O=B$ )   |
| 3       | 0x02                      | Addition ( $O=A+B$ )   |
| 4       | 0x03                      | Addition with Carry ( $O=A+B+C_{in}$ )                                     |
| 5       | 0x04                      | Subtraction ( $O=A-B$ )  |
| 6       | 0x05                      | Subtraction with Carry ( $O=A-B+C_{in}$ )                                  |
| 7       | 0x06                      | Reverse Subtraction ( $O=B-A$ )  |
| 8       | 0x07                      | Reverse Subtraction with Carry ( $O=B-A+C_{in}$ )                          |
| 9       | 0x08                      | Compare ( $A-B$ : Result is not written on output, only flags are updated) |
| 10      | 0x09                      | Bitwise AND ( $O=A \& B$ )   |
| 11      | 0x0A                      | Bitwise OR ( $O=A   B$ )   |
| 12      | 0x0B                      | Bitwise EOR ( $O=A \wedge B$ )   |
| 13      | 0x0C                      | Logical Left Shift through Carry   |
| 14      | 0x0D                      | Logical Right Shift  |
| 15      | 0x0E                      | Rotate Left  |
| 16      | 0x0F                      | Rotate Right   |

The above table contains some of the basic operations from the instruction set of ARM controller.

| Sr. No. | Flag      | Logical Instruction                              | Arithmetic Instruction  |
|---------|-----------|--|---|
| 1       | Negative  | No Meaning                                       | Bit-31 of the result has been set. Indicates a negative number in signed operations               |
| 2       | Zero      | Result is all zeroes                             | Result of operation is zero   |
| 3       | Carry out | After shift operation '1' was left in carry flag | Result is greater than 32-bits  |
| 4       | Over Flow | No meaning                                       | Result is greater than 31 bits. Indicates a possible corruption of the sign bit in signed numbers |

This table of Flag operations has been taken from the datasheet of an ARM Controller.

Instructions regarding project:

- Make the project using Verilog HDL.
- You are not allowed to use gate level modelling on any level.
- Give the inputs in decimal form in the text fixture file.

Instructions regarding grading:

- Project is to be submitted by each student separately. This is an individual assignment.
- Project carries 10% marks of the lab session (1 credit hour).
- Partially running projects will be accepted as well and graded accordingly.
- Project has to be submitted in the respective lab sessions of the week starting from 14<sup>th</sup> November to 18<sup>th</sup> November.
- A one-page, hand-written report containing the algorithm has to be submitted along with the project.
- For any help you can visit me in office hours or discuss in your respective lab sessions.

Digital Systems Laboratory

