CMOS Analog IC Design

Lab 11 (Mini Project 02)

Fully-Differential Folded Cascode OTA

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PART 1: gm/ID Design Charts

Using ADT Sizing Assistant, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS to a reasonable value and L = min,1u:1u:5u.

1) VA
2) W/ID
3) fT
4) VGS

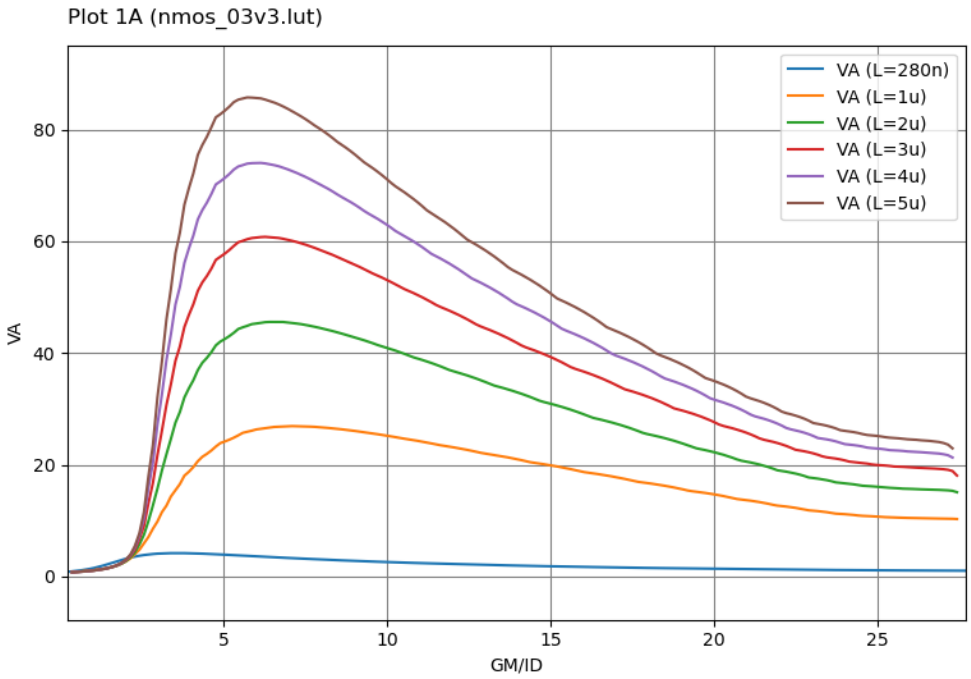


Figure 1 : :VA vs gm/id for Nmos

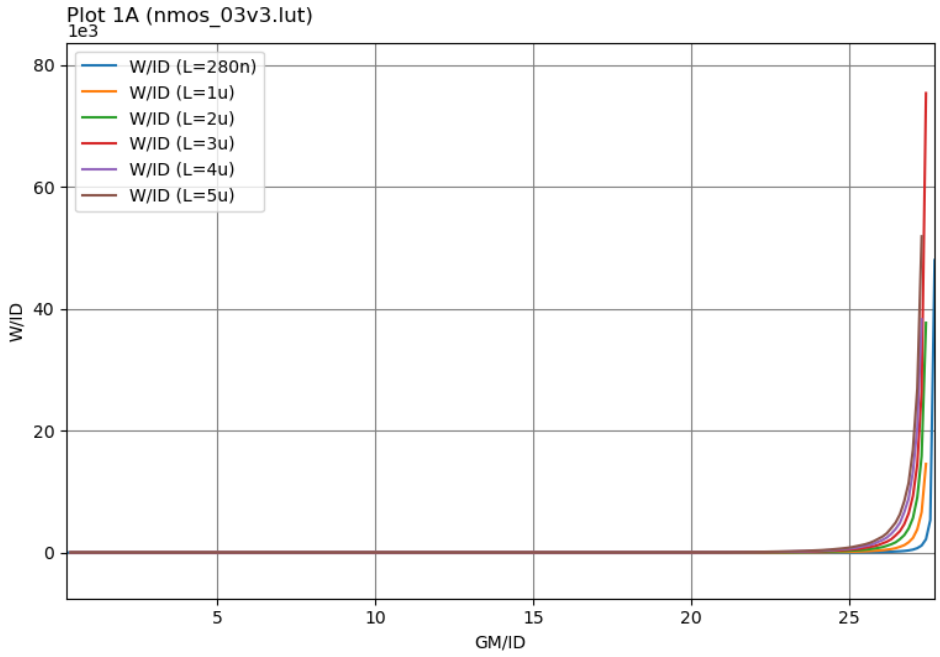


Figure 2 : : W/ID vs gm/id for Nmos

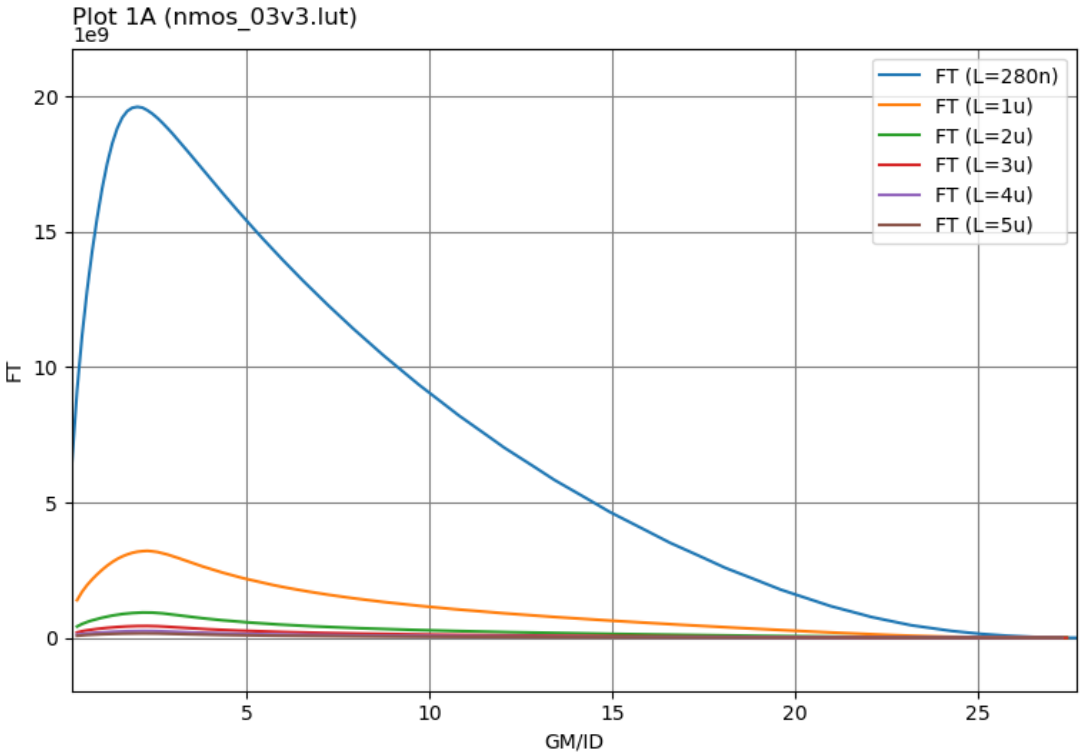


Figure 3 : FT vs gm/id for Nmos

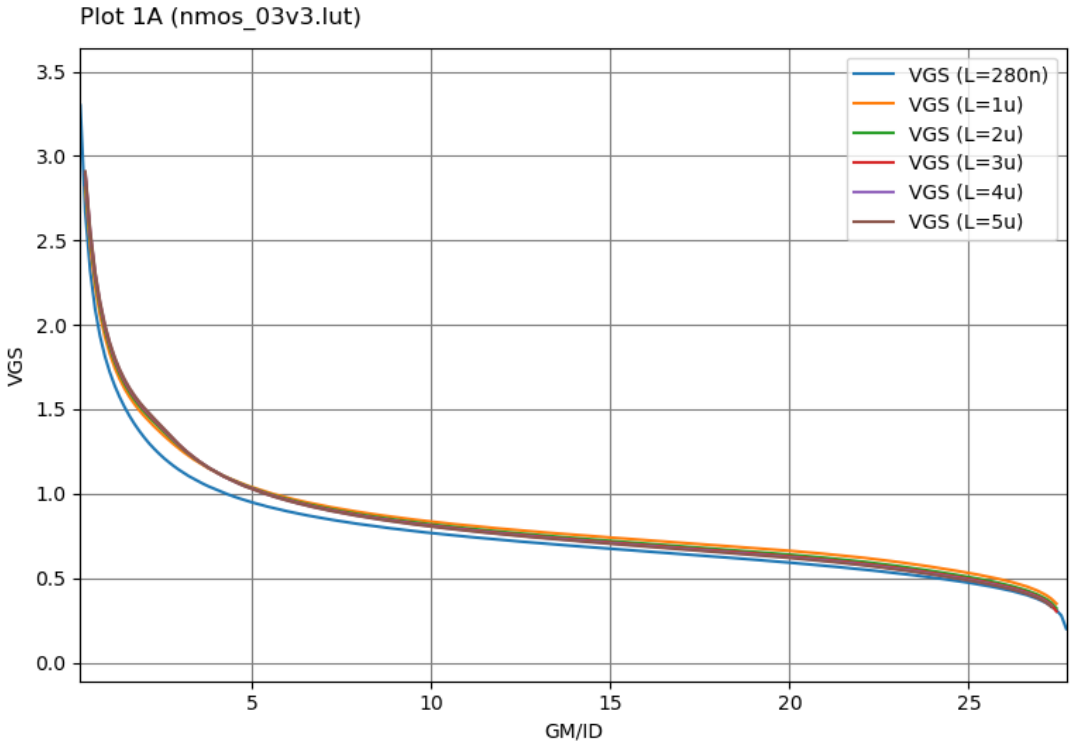


Figure 4 : : VGS vs gm/id for Nmos

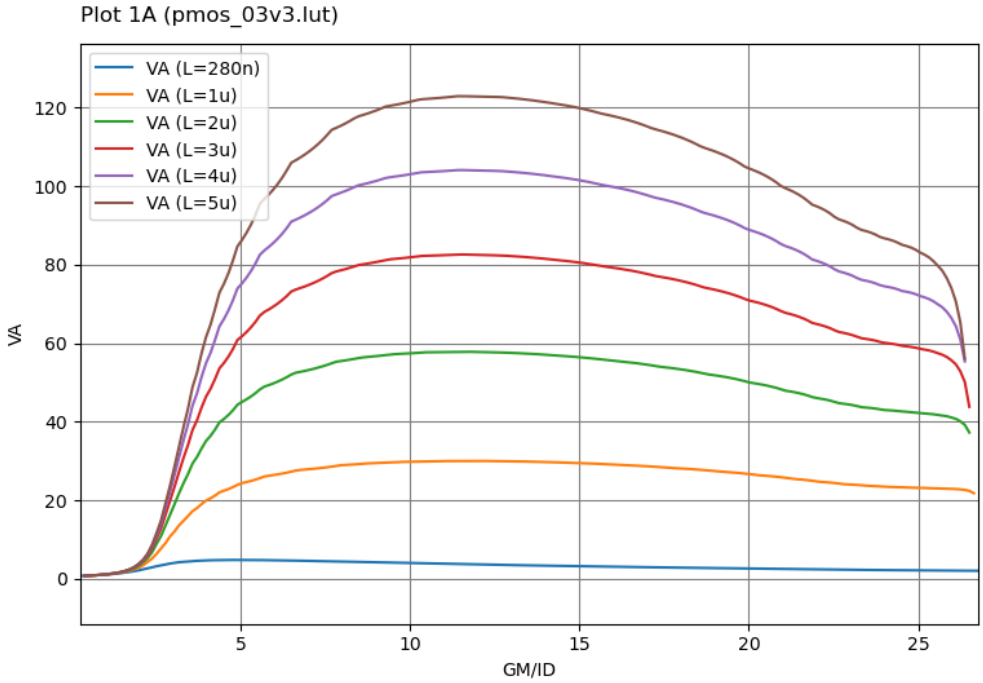


Figure 5 : VA vs gm/id for Pmos

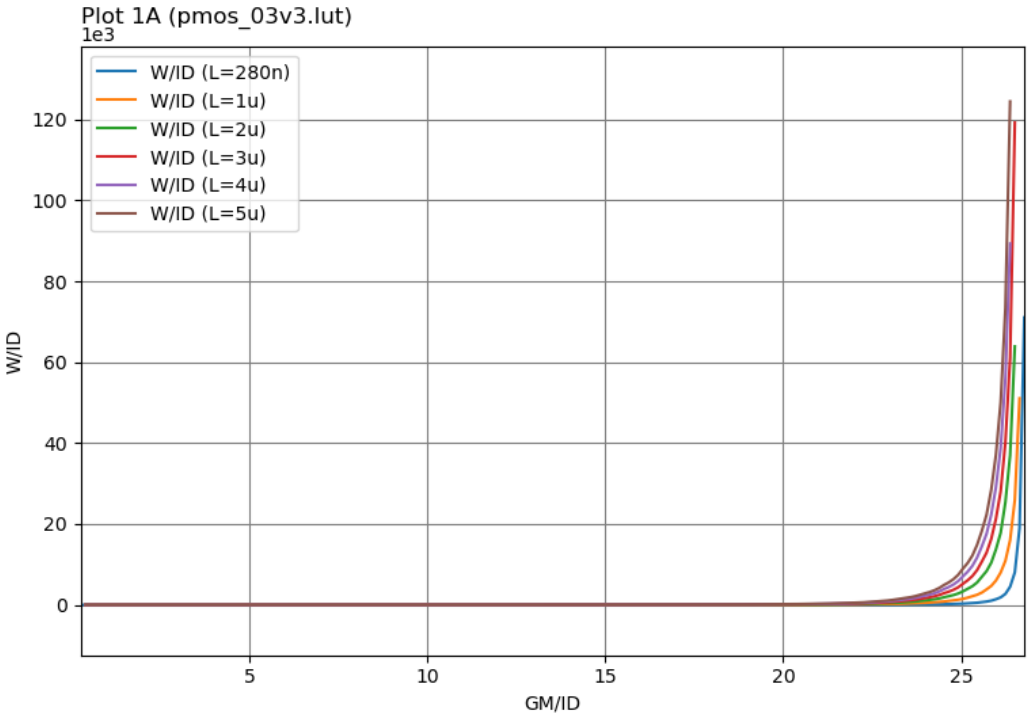


Figure 6 : W/ID vs gm/id for Pmos

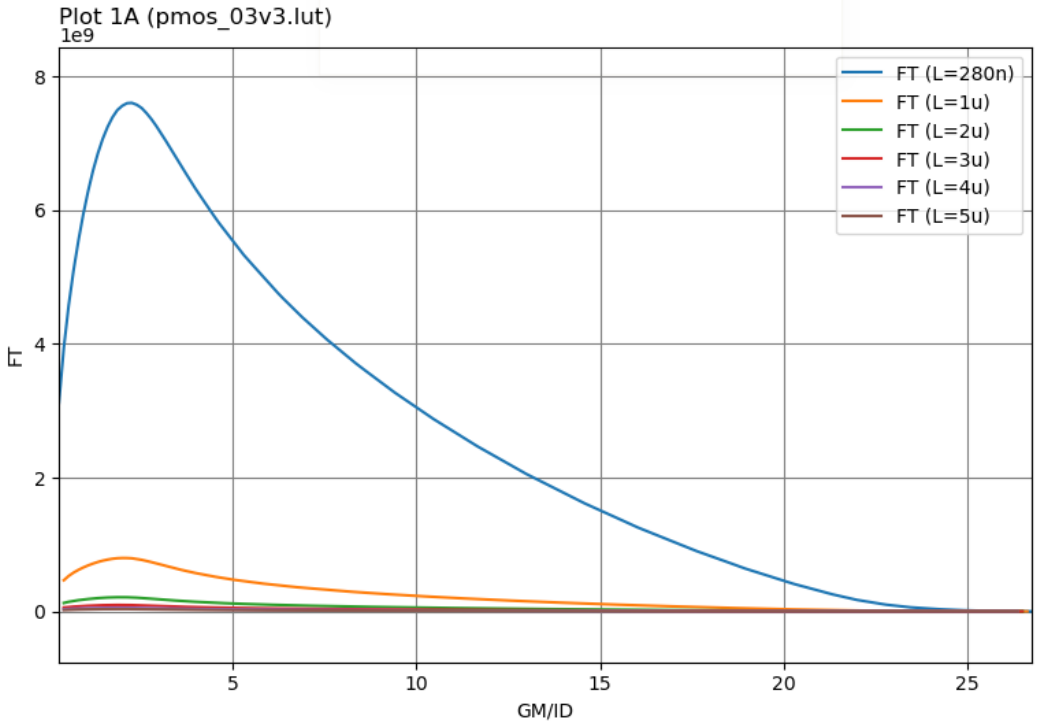


Figure 7 : FT vs gm/id for Pmos

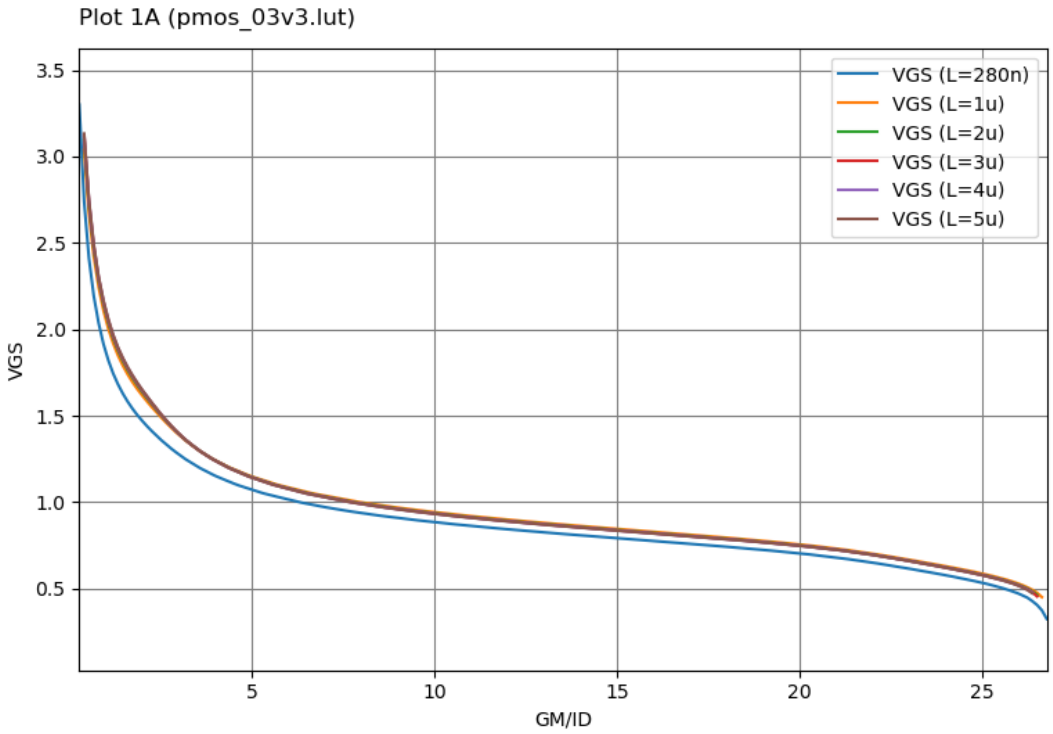


Figure 8 : VGS vs gm/id for Pmos

PART 2: OTA Design

Design a fully-differential folded cascode OTA with capacitive feedback that meets the specifications below. The current consumed in the biasing branches (current mirrors) is not included in the specifications.

Technology	GF180MCU
Supply Voltage	2.5 V
Closed-Loop Gain (ACL)	2
Phase Margin (PM)	≥70∘
CM Input Range – Low	≤ 0 V
CM Input Range – High	≥ 1 V
Differential Output Swing	1.2Vpk-to-pk
Load Capacitance (CL)	500fF
DC Loop Gain	≥ 60dB
Settling Time (1% error)	≤100ns

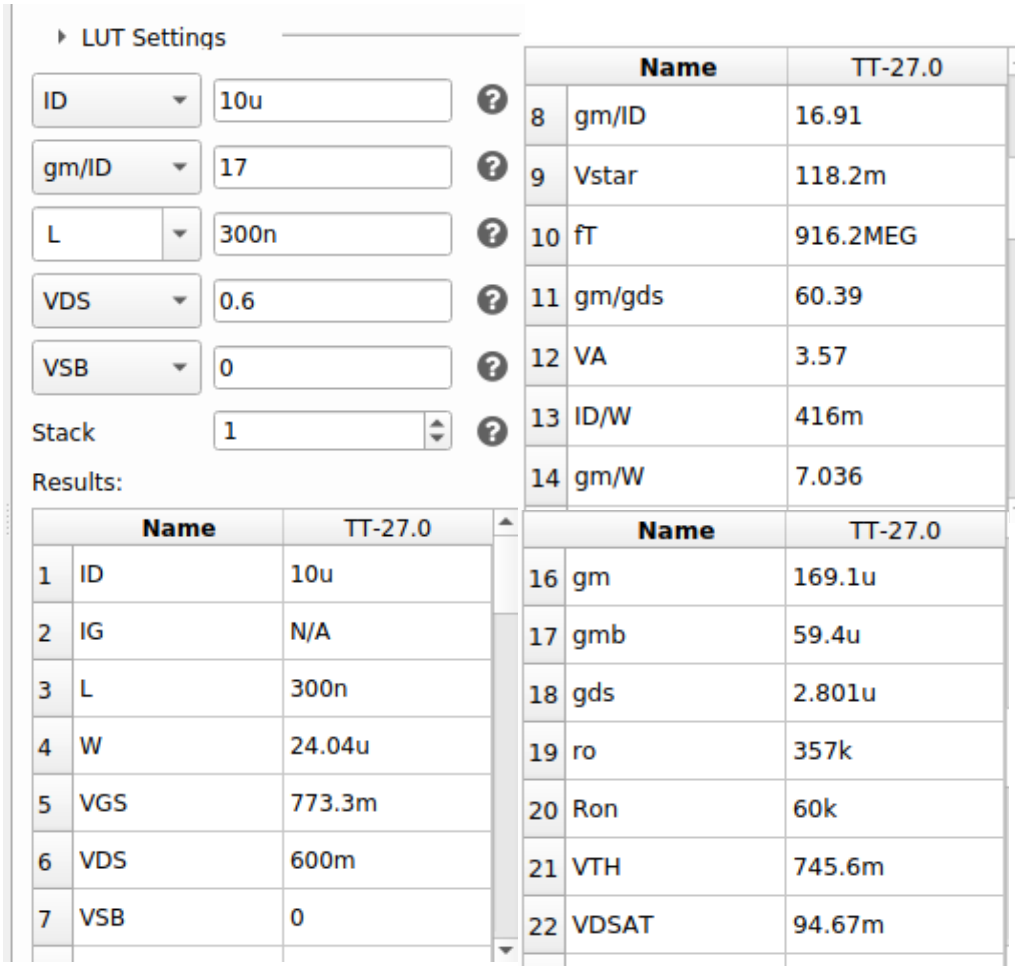
Design Procedure

- **Settling Time Specification**
  Assume a first-order system for simplicity:
  Vout = Vin (1 - e^(-t/τ))
  For 99% settling at t = 100 ns:
  0.99 = 1 (1 - e^(-100 ns/τ)) → τ = 21.7 ns
- **Closed-Loop Bandwidth**
  BWcl = 1 / (2ππ) = 7.33 MHz
- **Feedback Topology**
  Voltage–Current feedback (Shunt–Shunt) with inverting amplifier configuration.
  Feedback factor:
  β = Cf / (Cin + Cf) = 1/3
- **Loop Gain Requirement**
  Loop Gain = 1000 = β × Aol
  Aol = 3000 (with margin: Aol = 4000)
- **Gain–Bandwidth Product (GBW)**
  GBW = BWcl × Acl = 14.66 MHz
  With margin: GBW = 16 MHz

- **Transconductance Requirement**
  GBW = gm,in / (2π × Cout)
  Cout = CL + Cf = 1.5 pF
  gm = 150 µS
- **Bias Current Estimation**
  Assuming gm/Id = 15:
  Id = 10 µA
- **GBW open**
  GBW = gmin/2π*Cl → GBW = 48MHz
  Bwop = GBW/Aol >15KHz

1)input pair Pmos

gm,input >= 150 uS
Assume ID = 10uA ,gm/id = 17 ,L = 300 nm ,Vds = 0.6 ,VSB = 0



	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	300n
4	W	24.04u
5	VGS	773.3m
6	VDS	600m
7	VSB	0

	Name	TT-27.0
8	gm/ID	16.91
9	Vstar	118.2m
10	fT	916.2MEG
11	gm/gds	60.39
12	VA	3.57
13	ID/W	416m
14	gm/W	7.036

	Name	TT-27.0
16	gm	169.1u
17	gmb	59.4u
18	gds	2.801u
19	ro	357k
20	Ron	60k
21	VTH	745.6m
22	VDSAT	94.67m

2) Tail current mirror Pmos

The tail transistor will pass through it double the current of the input pair

Id = 20u ,L=1um ,gm/id = 10 , VDS = 0.6 ,VSB = 0

ID	20u
gm/ID	10
L	1u
VDS	0.6
VSB	0
Stack	1

Results:

	Name	TT-27.0
1	ID	20u
2	IG	N/A
3	L	1u
4	W	39.15u
5	VGS	943.4m
6	VDS	600m
7	VSB	0

Results:

	Name	TT-27.0
8	gm/ID	9.896
9	Vstar	202.1m
10	fT	233MEG
11	gm/gds	295
12	VA	29.81
13	ID/W	510.9m
14	gm/W	5.056

	Name	TT-27.0
16	gm	197.9u
17	gmb	93.62u
18	gds	671n
19	ro	1.49MEG
20	Ron	30k
21	VTH	783.2m
22	VDSAT	156.4m

3) Tail current mirror Nmos

The tail transistor will pass through it double the current of the input pair

Id = 20u ,L=1um ,gm/id = 10 , VDS = 0.6 ,VSB = 0

ID	20u
gm/ID	10
L	1u
VDS	0.6
VSB	0
Stack	1

Results:

	Name	TT-27.0
1	ID	20u
2	IG	N/A
3	L	1u
4	W	9.13u
5	VGS	836.3m
6	VDS	600m
7	VSB	0

Results:

	Name	TT-27.0
8	gm/ID	9.875
9	Vstar	202.5m
10	fT	1.153G
11	gm/gds	249.4
12	VA	25.26
13	ID/W	2.191
14	gm/W	21.63

	Name	TT-27.0
16	gm	197.5u
17	gmb	75.44u
18	gds	791.8n
19	ro	1.263MEG
20	Ron	30k
21	VTH	687m
22	VDSAT	172.8m

4) cascode transistors Pmos

Assume Id = 10u ,L=0.5um ,gm/id = 15 , VDS = 0.6 ,VSB = 0

ID	10u
gm/ID	15
L	0.5u
VDS	0.6
VSB	0
Stack	1

Results:

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	500n
4	W	26.63u
5	VGS	848.8m
6	VDS	600m
7	VSB	0

Results:

	Name	TT-27.0
8	gm/ID	14.94
9	Vstar	133.8m
10	fT	483.9MEG
11	gm/gds	191.2
12	VA	12.79
13	ID/W	375.5m
14	gm/W	5.612

	Name	TT-27.0
16	gm	149.4u
17	gmb	66.51u
18	gds	781.8n
19	ro	1.279MEG
20	Ron	60k
21	VTH	785.7m
22	VDSAT	107.5m

5) cascode transistors Nmos

Assume Id = 10u ,L=0.5um ,gm/id = 15 , VDS = 0.6 ,VSB = 0.3

ID	10u
gm/ID	15
L	0.5u
VDS	0.6
VSB	0.3
Stack	1

Results:

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	500n
4	W	7.59u
5	VGS	849.9m
6	VDS	600m
7	VSB	300m

Results:

	Name	TT-27.0
8	gm/ID	15
9	Vstar	133.4m
10	fT	2.207G
11	gm/gds	131.7
12	VA	8.784
13	ID/W	1.318
14	gm/W	19.76

	Name	TT-27.0
16	gm	150u
17	gmb	45.77u
18	gds	1.138u
19	ro	878.4k
20	Ron	60k
21	VTH	807.8m
22	VDSAT	110.8m

Sizing of VCASCN and VCASCP

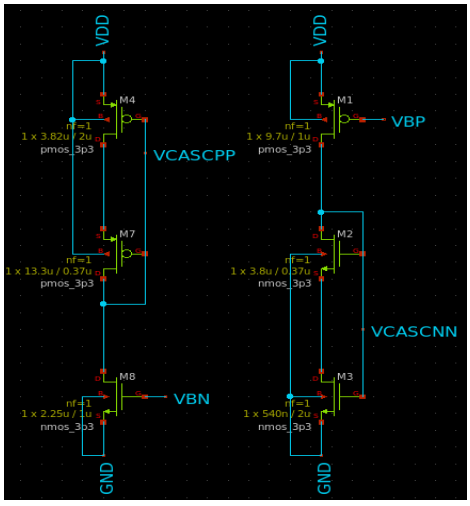


Figure 9 : Schmatic of Replica Biasing

I will use a Replica Biasing

VCASCN (NMOS cascode bias)

PMOS current mirror (reference branch)

- Choose a fixed reference current:

$$I_{D,ref} = 5\ \mu A$$

NMOS cascode device (replica)

- In a folded cascode, each NMOS cascode device carries **half of the branch current**:

$$I_{D,cascode} = \frac{I_{branch}}{2}$$

- To match this in the replica, size the cascode transistor as:

$$W_{,cascode} = \frac{W_{main}}{2}\ ,\ L_{,cascode} = L$$

NMOS tail device (in replica)

we want VGS = 1.2

assume L = 2u

Results:

	Name	TT-27.0
1	ID	5.003u
2	IG	N/A
3	L	2u
4	W	540n

VCASCP (PMOS cascode bias)

NMOS current mirror (reference branch)

- Choose a fixed reference current:

$$I_{D,ref} = 5\ \mu A$$

PMOS cascode device (replica)

- In a folded cascode, each PMOS cascode device carries **half of the branch current**:

$$I_{D,cascode} = \frac{I_{branch}}{2}$$

- To match this in the replica, size the cascode transistor as:

$$W_{,cascode} = \frac{W_{main}}{2}\ ,\ L_{,cascode} = L$$

PMOS tail device (in replica)

we want VGS = 1.2

assume L = 2u

Results:

	Name	TT-27.0
1	ID	4.996u
2	IG	N/A
3	L	2u
4	W	3.82u
5	VGS	1.2

Transistor Sizing and Operating Point Summary:

Transistor Role	W (µm)	L (nm)	gm (µS)	ID (µA)	gm/ID	Vdsat (mV)	V* (mV)	VGS
Input Pair (PMOS)	24.04	300	169.1	10	17	94.67	118.2	0.773
Tail Mirror (PMOS)	39.15	1000	197.9	20	10	156.4	202.1	0.943
Tail Mirror (NMOS)	9.13	1000	197.5	20	10	172.8	202.5	0.836
Cascode (PMOS)	26.63	370	149.4	10	15	107.5	133.8	0.848
Cascode (NMOS)	7.59	370	150	10	15	110.8	133.4	0.849

From the assumed V*, select suitable biasing for the cascode transistors (VCASCP and VCASCN).

VCASCN ≈ VGSN + V* = 0.85+0.14 = 0.99V = 1.2V with margin

VCASCP ≈ VDD - |VGSP| - V* = 2.5 - 0.85 – 0.2 = 1.45 = 1.2V with margin

Vincm,high = VDD - VGS,in – V* = 1.5249

Vincm,low = Vthp + V*,CM_nmos = 0.2025 V − 0.7456 V = -0.5431 V

Vincm,middle = 0.5V

Vout,high = VDD - V*,casc - VGS = 1.4232

Vout,min = V*,casc + V*,CM = 0.3359

Vout.middle = 0.88V

Note: I reduced the channel length of the cascode PMOS and NMOS devices from 500 nm to 370 nm in order to meet the specifications.

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.

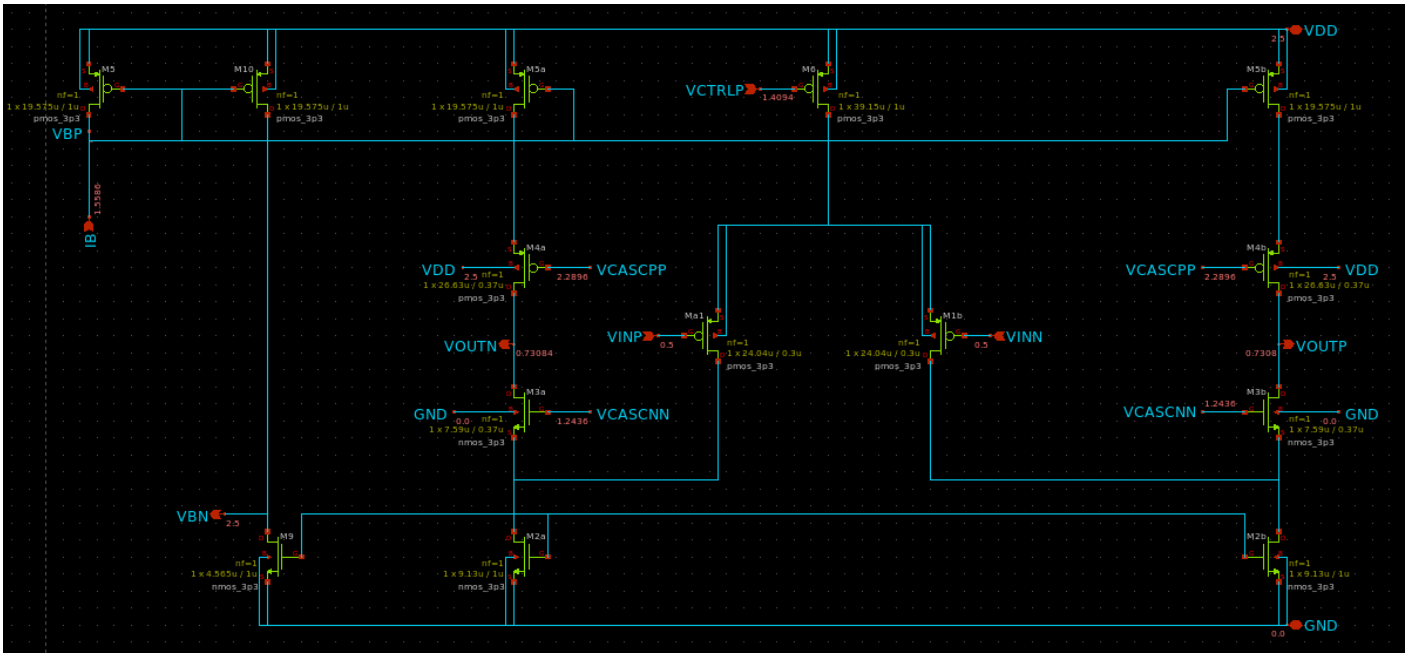


Figure 10 : Schematic of Fully-Differential Folded Cascode OTA

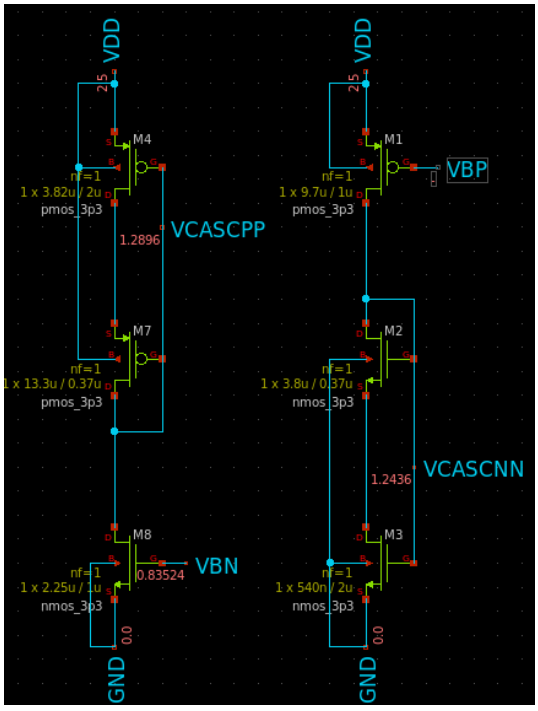


Figure 11 : Replica biasing

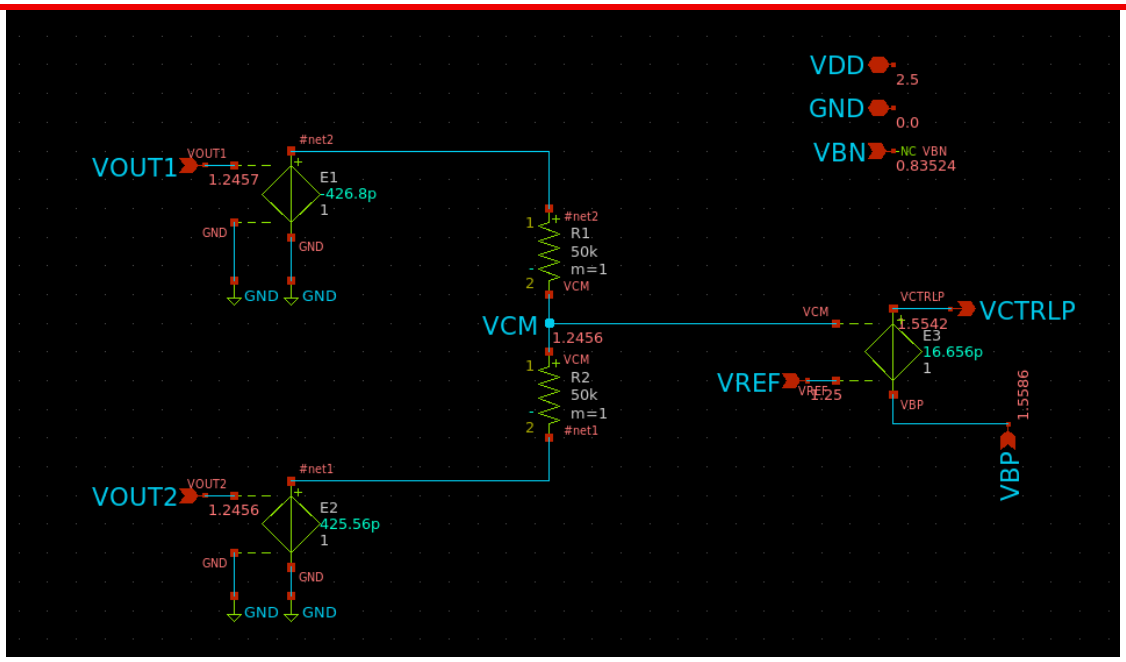


Figure 12 : Behavioral CMFB

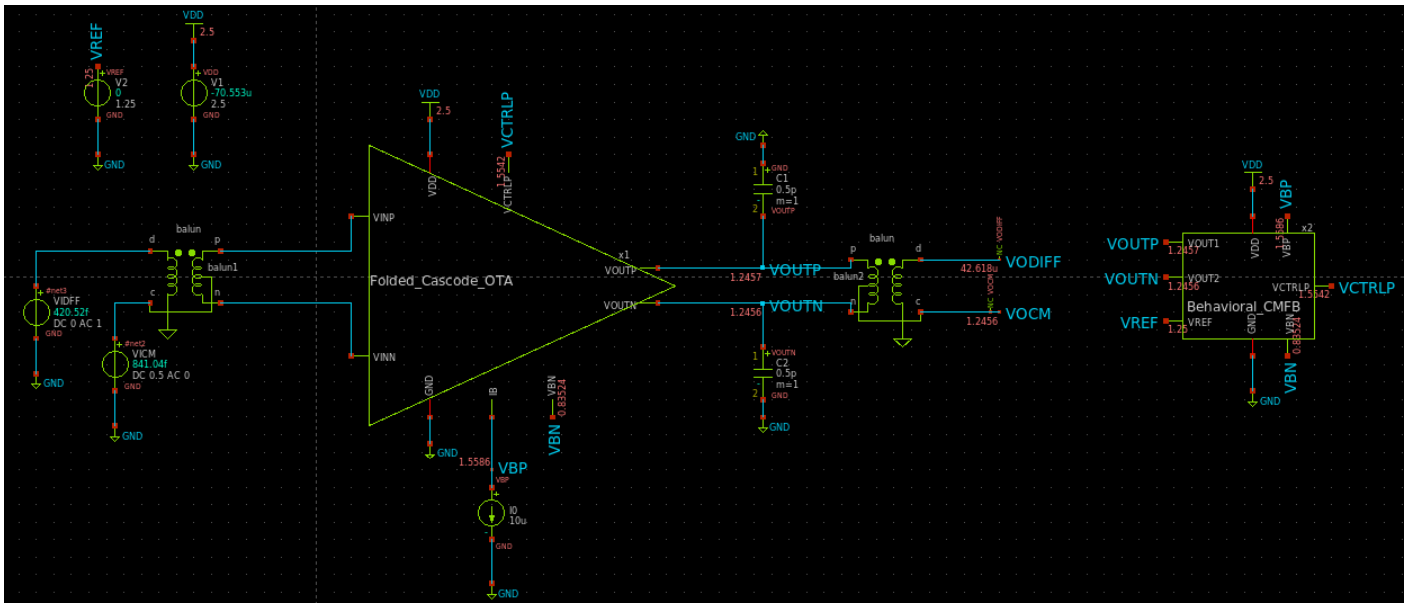


Figure 13 : open-loop testbench for simulating a folded-cascode OTA with a behavioral CMFB circuit.

DC Operating point

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm4_x1.m0	m.xm3_x1.m0	m.xm1_x1.m0
model	pmos_3p3.10	nmos_3p3.6	pmos_3p3.9
id	4.90318e-06	4.99219e-06	4.99219e-06
gm	1.85813e-05	1.41853e-05	5.04236e-05
gds	4.38492e-06	2.67182e-06	9.28769e-08
vgs	1.21039	1.24357	0.941441
vth	0.774877	0.654469	0.783923
vds	0.294425	0.427286	1.25641
vdsat	0.333805	0.473962	0.154389

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm8_x1.m0	m.xm9_x1.m0	m.xm2b_x1.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	4.90317e-06	1.01343e-05	2.02567e-05
gm	4.8363e-05	0.000100841	0.000202541
gds	1.43104e-07	3.30756e-07	1.03056e-06
vgs	0.835242	0.835242	0.835242
vth	0.685215	0.687329	0.68835
vds	1.28961	0.835239	0.424534
vdsat	0.171291	0.172088	0.172481

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm2_x1.m0	m.xm3a_x1.m0	m.xm3b_x1.m0
model	nmos_3p3.8	nmos_3p3.8	nmos_3p3.8
id	4.99219e-06	9.76045e-06	9.76045e-06
gm	8.00452e-05	0.000156219	0.000156219
gds	1.20001e-06	2.69973e-06	2.69961e-06
vgs	0.816274	0.819044	0.819044
vth	0.796201	0.799369	0.799368
vds	0.816272	0.451129	0.451186
vdsat	0.0978721	0.0980206	0.0980203

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm2a_x1.m0	m.xm5_x1.m0	m.xm10_x1.m0
model	nmos_3p3.9	pmos_3p3.13	pmos_3p3.13
id	2.02567e-05	1e-05	1.01343e-05
gm	0.000202541	0.000101062	0.000102318
gds	1.03056e-06	2.29564e-07	1.55258e-07
vgs	0.835242	0.941441	0.941441
vth	0.68835	0.783939	0.783937
vds	0.424533	0.94144	1.66475
vdsat	0.172481	0.154376	0.154377

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm5b_x1.m0	m.xm5a_x1.m0	m.xm6_x1.m0
model	pmos_3p3.13	pmos_3p3.13	pmos_3p3.13
id	9.7605e-06	9.7605e-06	2.09926e-05
gm	9.83378e-05	9.83378e-05	0.000208322
gds	9.0601e-07	9.06008e-07	3.96322e-07
vgs	0.941441	0.941441	0.945741
vth	0.783941	0.783941	0.783938
vds	0.297248	0.297248	1.22478
vdsat	0.154374	0.154374	0.157318

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xma1.m0	m.x1.xm1b.m0
model	pmos_3p3.12	pmos_3p3.12
id	1.04963e-05	1.04963e-05
gm	0.000177642	0.000177642
gds	2.69568e-06	2.69568e-06
vgs	0.775221	0.775221
vth	0.747643	0.747643
vds	0.850682	0.850681

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm7_x1.m0	m.xm4b_x1.m0	m.xm4a_x1.m0
model	pmos_3p3.12	pmos_3p3.12	pmos_3p3.12
id	4.90318e-06	9.76049e-06	9.76049e-06
gm	8.15537e-05	0.000163126	0.000163126
gds	7.25457e-07	1.31426e-06	1.31425e-06
vgs	0.915958	0.913137	0.913137
vth	0.880994	0.879986	0.879986
vds	0.915958	1.32702	1.32708

Set VICM at the middle of the CMIR

Vincm,middle = 0.5V

Select VREF to maximize the symmetrical output swing.

VREF = VDD/2 = 1.25 V

What is the CM level at the OTA output?

Vocm = 1.2457 V

What are the differential input and output voltages of the error amplifier? What is the relation between them?

ΔVidiff = Vref – Vocm = 1.25 mV – 1.2457 mV = 4.3 mV

ΔVodiff = VBP – VCTRLP = 1.558559 - 1.554193= 4.3mV

$$\frac{\Delta Vodiff}{\Delta Vidiff} = \frac{4.3\ mV}{4.3\ mV} = 1V \text{ (Buffer)}$$

2) Diff small signal ccs:

- **Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).**
- **Plot diff gain (magnitude in dB and phase) vs frequency.**

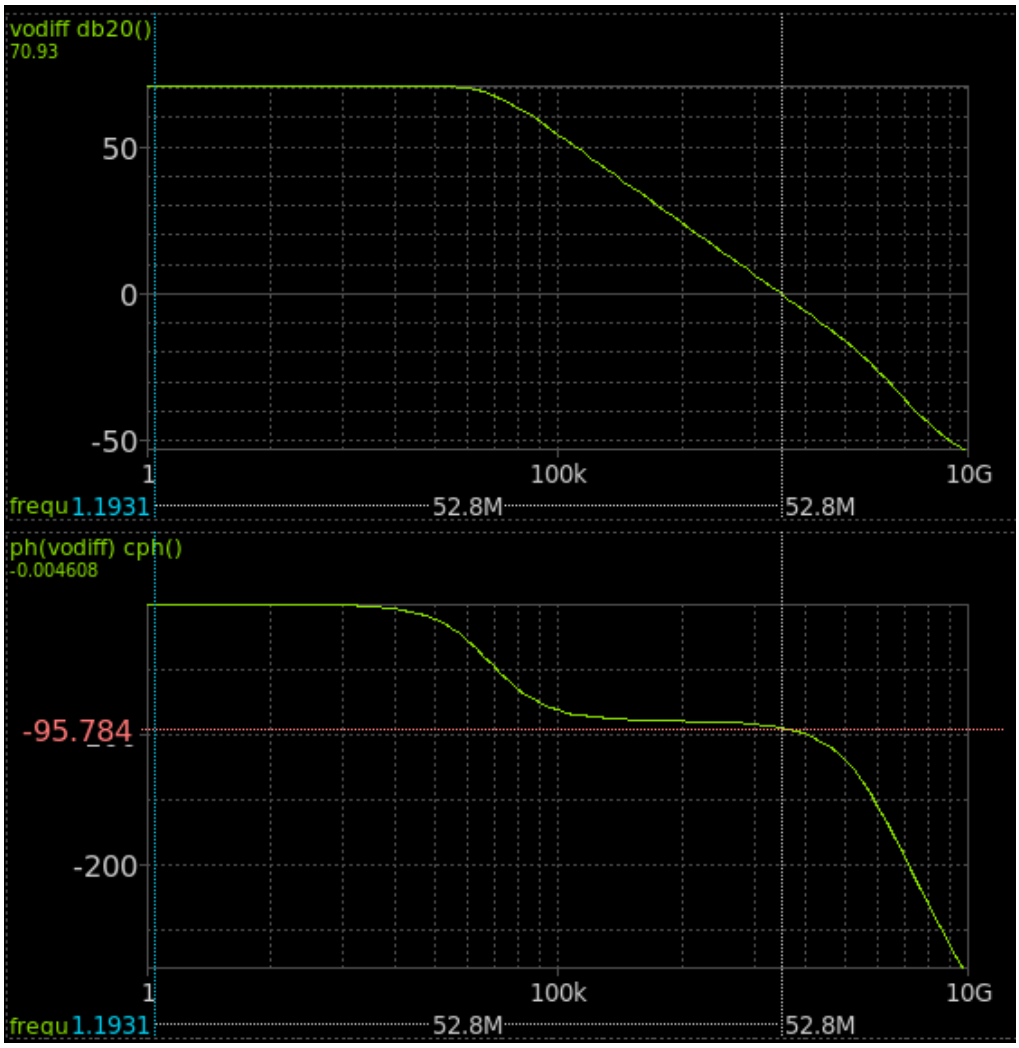


Figure 14 : diff gain (magnitude in dB and phase) vs frequency

```
gain                =   3.519799e+03 at=  1.000000e+00
bw                  =   1.494257e+04
ugf                 =   5.281160e+07
gbw = 5.259484e+07
```

Figure 15 : Open Loop Gain and BW form simulation (Behavioral CMFB)

From simulation PM = 180 + Ph(UGF) = 180 + -95.784 = 84.2°

• **Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).**

DC gain = GM Rout

Rout = Rout,up// Rout,down

Rout,up ≈ ro4(1+gm4*ro5) = 137.6 MΩ

Rout,down≈ ro3(1+gm3*(ro2//ro1)) = 15.882 MΩ

GM = gm,input = 177.642uS

DC gain = 68.06dB

Bw = $\frac{1}{2\pi * Rout * Cout}$ **→ Cout = 0.5+0.1(parasitic) = 0.6 → Bw = 18.63 KHz**

GBW = Dc gain * Bw = 51.4 MHz = UGF

$\mathrm{Wnd2} = \frac{gm,M3a}{2\pi(Css,M3a+Cdd,M2a+Cdd,Ma1a)} \rightarrow \mathrm{CDD1} = 15.49\mathrm{f}, \mathrm{CDD2} = 8.811\mathrm{f}, \mathrm{CSS} = 55.8\mathrm{f} \rightarrow \mathrm{Wp2} = 310.8\mathrm{MHz}$

PM = 90 -$Tan^{\wedge} - 1(\frac{Wp2}{Wu})$ **= 88.59°**

Parameter	Hand Analysis	Simulation Result
DC Gain	68.06 dB	70.9 dB
Bandwidth (BW)	18.63 kHz	14.9 kHz
GBW / UGF	51.4 MHz	52.8 MHz
PM	88.59°	84.2°

PART 4: Open-Loop OTA Simulation (Actual CMFB)

Sizing of Actual CMFB

Assume a reasonable CMFB current budget, e.g., 50% of the amplifier current.

Total current at CMFB = 25u

You may assume L = 1um and gm/ID = 15 for all transistors with unknown L or gm/ID for simplicity

(note that L and gm/ID for some transistors are already known, why?)

Based on topology if we use a very small current by nano amber then we will use L Max and gm/id at WI and if I design Current mirror the best case make gm/id = 10 SI and L is bigger to avoid mismatch

The sensing resistors are chosen such that the max current flowing through them (when diff signal is max) is less than the CD bias current. This avoids starving the CD when the diff output signal has its maximum excursion.

So the Current from CM Pmos assume = 5u

And the worst case if Vid = 0.6 the the Current in resistor is ir= 0.6/2R = 3u then R = 100K

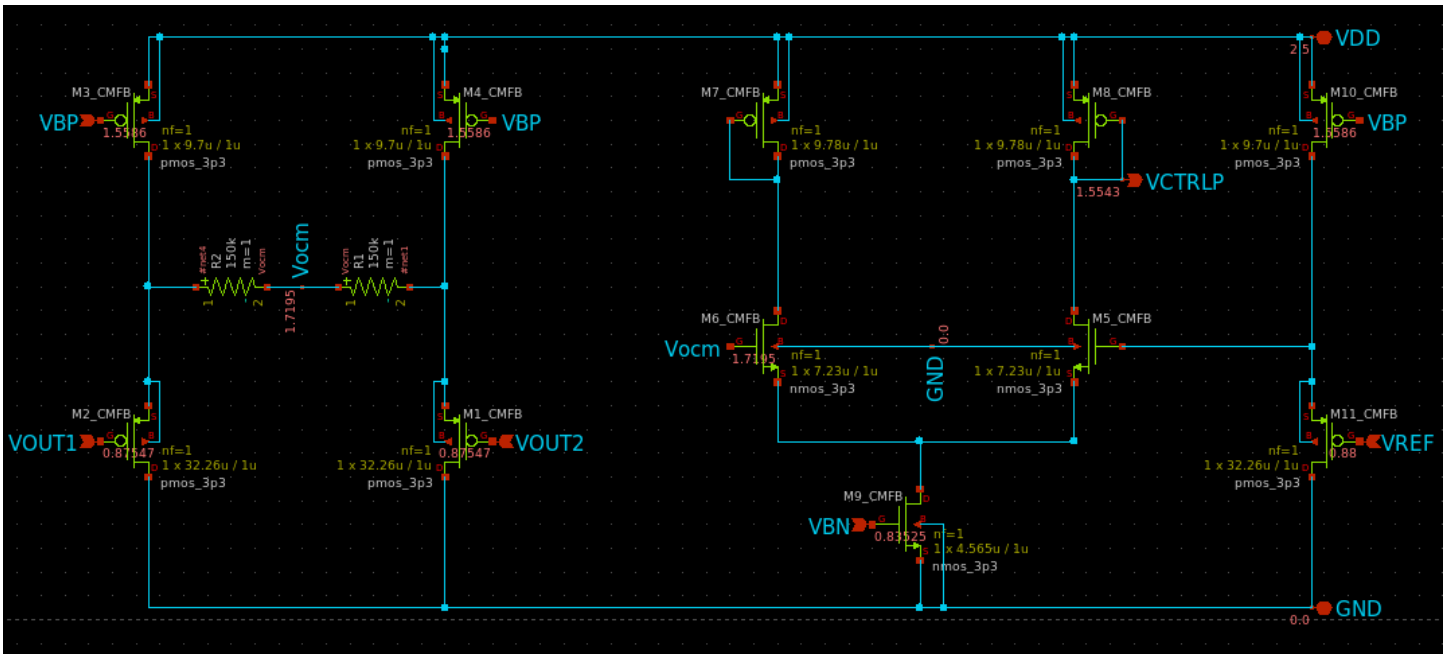


Figure 16 : Actual CMFB

Sizing of M1 ,M2 ,M11

Assume id =5u gm/id =15 , L = 1u Vds = 0.6

Results:

	Name	TT-27.0
1	ID	5u
2	IG	N/A
3	L	1u
4	W	32.26u
5	VGS	846.5m
6	VDS	600m

Sizing of M3 ,M4 ,M7 ,M8 ,M10

Will be a ratio from Tail Current mirror Pmos

Id = 5u then the W= $\frac{W,tail}{2}$=9.7 um , L=L,tail =1u

For input pair Nmos M5,M6

Assume id =5u gm/id =15 , L = 1u Vds = 0.6

Results:

	Name	TT-27.0
1	ID	5u
2	IG	N/A
3	L	1u
4	W	7.24u
5	VGS	742.4m
6	VDS	600m

Sizing of NMOS Error Amp Tail Source

Will be a ratio from Tail Current mirror Pmos

Id = 5u then the W= $\frac{W,tail}{2}$=4.565 um , L=L,tail =1u

- The branch M10 and M11 is to add the Dc shift (offset) to Vref Like Vocm

Transistor Name(s)	Role in CMFB Circuit	W (µm)	L (µm)
M1, M2 ,M11	PMOS Source Followers	32.26	1
M3 ,M4 ,M7 ,M8 ,M10	PMOS Source Follower Bias	9.7	1
M5, M6	NMOS Error Amp Input Pair	4.565	1
M9	NMOS Error Amp Tail Source	4.565	1

1) Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.

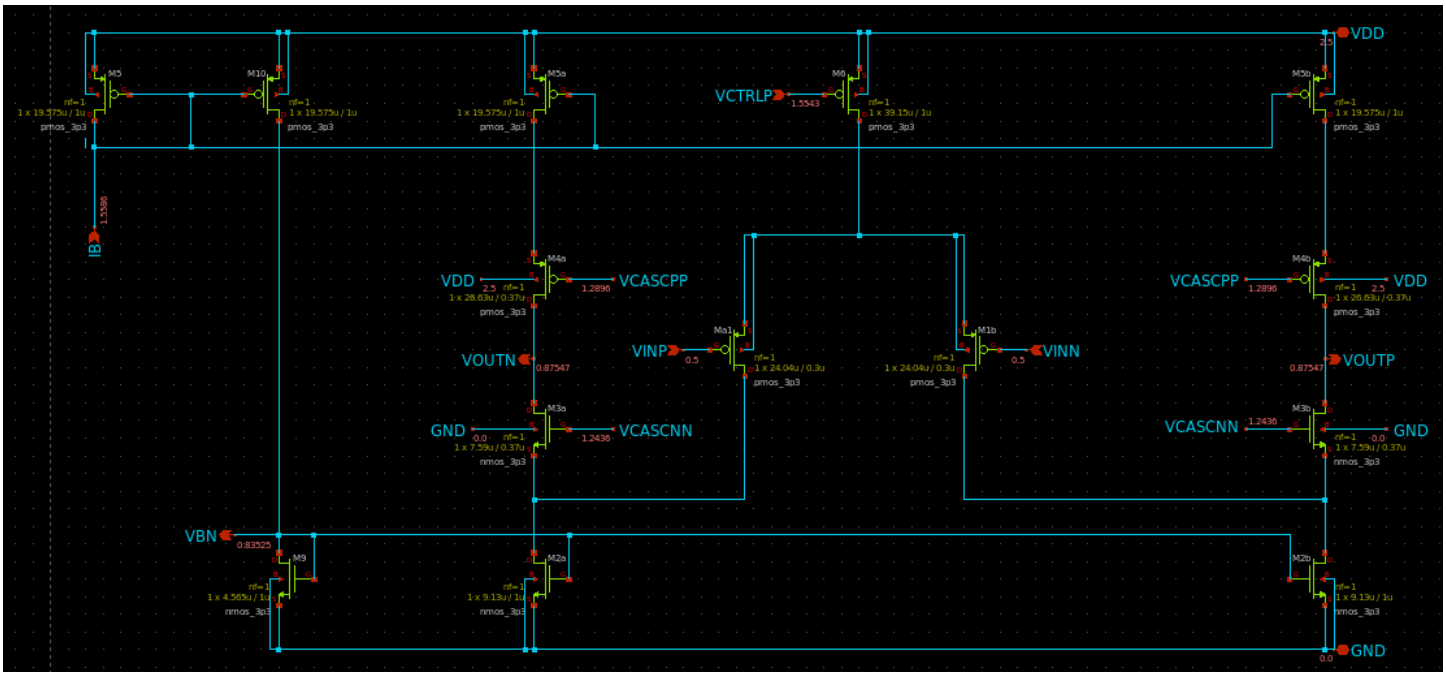


Figure 17 : : Schematic of Fully-Differential Folded Cascode OTA

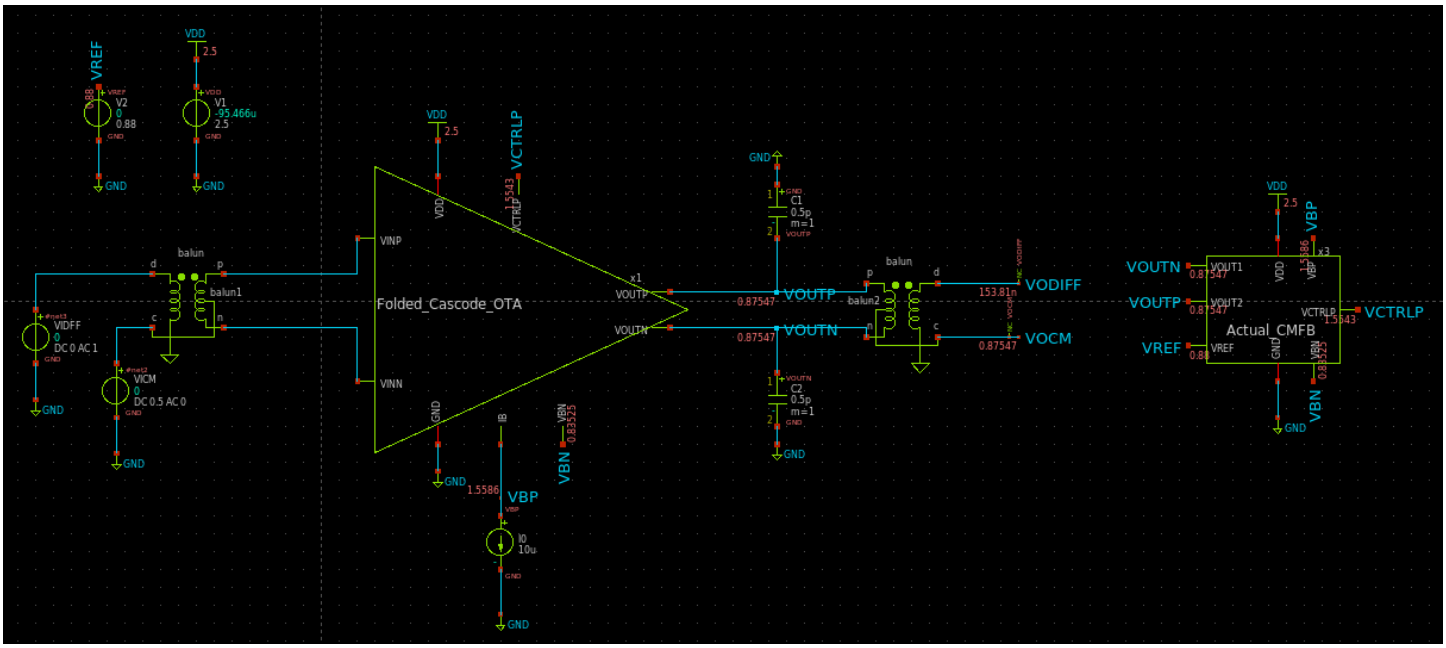


Figure 18 : open-loop testbench for simulating a folded-cascode OTA with Actual CMFB circuit

DC Operating point

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm4.m0	m.x1.xm3.m0	m.x3.xm10_cmfb.m0
model	pmos_3p3.10	nmos_3p3.6	pmos_3p3.9
id	4.90317e-06	4.99219e-06	4.93972e-06
gm	1.85813e-05	1.41853e-05	4.9917e-05
gds	4.38491e-06	2.67182e-06	1.31672e-07
vgs	1.21038	1.24357	0.941441
vth	0.774877	0.654469	0.783924
vds	0.294425	0.427286	0.775989
vdsat	0.333805	0.473963	0.154388

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm8_cmfb.m0	m.x3.xm7_cmfb.m0	m.x3.xm4_cmfb.m0
model	pmos_3p3.9	pmos_3p3.9	pmos_3p3.9
id	5.22149e-06	4.88044e-06	4.94031e-06
gm	5.18245e-05	4.98125e-05	4.9923e-05
gds	1.19302e-07	1.12395e-07	1.31084e-07
vgs	0.945741	0.939045	0.941441
vth	0.783928	0.783928	0.783924
vds	0.94574	0.939044	0.780508
vdsat	0.157326	0.152752	0.154388

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm5_cmfb.m0	m.x3.xm6_cmfb.m0	m.x1.xm8.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	5.22149e-06	4.88044e-06	4.90317e-06
gm	7.76219e-05	7.39483e-05	4.8363e-05
gds	2.06866e-07	1.96421e-07	1.43104e-07
vgs	0.984224	0.979706	0.835242
vth	0.928611	0.928611	0.685215
vds	0.814472	0.821168	1.28961
vdsat	0.115275	0.112445	0.171291

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm9.m0	m.x1.xm2b.m0	m.x1.xm2a.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	1.01343e-05	2.02568e-05	2.02568e-05
gm	0.000100841	0.000202541	0.000202541
gds	3.30756e-07	1.03057e-06	1.03057e-06
vgs	0.835242	0.835242	0.835242
vth	0.687329	0.68835	0.68835
vds	0.835239	0.42453	0.42453
vdsat	0.172088	0.172481	0.172481

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm5a.m0	m.x1.xm6.m0	m.x1.xm7.m0
model	pmos_3p3.13	pmos_3p3.13	pmos_3p3.12
id	9.7605e-06	2.09925e-05	4.90317e-06
gm	9.83378e-05	0.000208321	8.15537e-05
gds	9.06001e-07	3.9632e-07	7.25456e-07
vgs	0.941441	0.945741	0.915958
vth	0.783941	0.783938	0.880994
vds	0.297249	1.22478	0.915957
vdsat	0.154374	0.157317	0.0986095

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm4b.m0	m.x1.xm4a.m0	m.x1.xma1.m0
model	pmos_3p3.12	pmos_3p3.12	pmos_3p3.12
id	9.76051e-06	9.76051e-06	1.04963e-05
gm	0.000163126	0.000163126	0.000177642
gds	1.3142e-06	1.3142e-06	2.69567e-06
vgs	0.913135	0.913135	0.775221
vth	0.879985	0.879985	0.747643
vds	1.32728	1.32728	0.850685
vdsat	0.0975983	0.0975983	0.0942001

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm3_cmfb.m0	m.x1.xm1.m0	m.x1.xm2.m0
model	pmos_3p3.9	pmos_3p3.9	nmos_3p3.8
id	4.94031e-06	4.9922e-06	4.9922e-06
gm	4.9923e-05	5.04236e-05	8.00452e-05
gds	1.31084e-07	9.2877e-08	1.20001e-06
vgs	0.941441	0.941441	0.816274
vth	0.783924	0.783923	0.796201
vds	0.780508	1.25641	0.816272
vdsat	0.154388	0.154389	0.0978722

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm3a.m0	m.x1.xm3b.m0	m.x3.xm9_cmfb.m0
model	nmos_3p3.8	nmos_3p3.8	nmos_3p3.9
id	9.76051e-06	9.76051e-06	1.01019e-05
gm	0.000156219	0.000156219	0.000100597
gds	2.70017e-06	2.70017e-06	3.49702e-07
vgs	0.819048	0.819048	0.835242
vth	0.799369	0.799369	0.687329
vds	0.45093	0.45093	0.739779

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm11_cmfb.m0	m.x3.xm1_cmfb.m0	m.x3.xm2_cmfb.m0
model	pmos_3p3.13	pmos_3p3.13	pmos_3p3.13
id	4.93971e-06	4.94031e-06	4.94031e-06
gm	7.52933e-05	7.52993e-05	7.52993e-05
gds	8.70546e-08	8.71843e-08	8.71843e-08
vgs	0.844009	0.844022	0.844022
vth	0.783937	0.783937	0.783937
vds	1.72401	1.71949	1.71949
vdsat	0.0935863	0.0935934	0.0935934

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm5.m0	m.x1.xm10.m0	m.x1.xm5b.m0
model	pmos_3p3.13	pmos_3p3.13	pmos_3p3.13
id	1e-05	1.01343e-05	9.7605e-06
gm	0.000101062	0.000102318	9.83378e-05
gds	2.29564e-07	1.55258e-07	9.06001e-07
vgs	0.941441	0.941441	0.941441
vth	0.783939	0.783937	0.783941
vds	0.94144	1.66475	0.297249
vdsat	0.154376	0.154377	0.154374

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm1b.m0
model	pmos_3p3.12
id	1.04963e-05
gm	0.000177642
gds	2.69567e-06
vgs	0.775221
vth	0.747643
vds	0.850685
vdsat	0.0942001

What is the CM level at the OTA output? Why?

vocm = 0.875 The OTA output CM level settles at ~0.875 V because the CMFB loop forces the outputs to track the reference voltage (Vref = 0.88 V).

What are the differential input and output voltages of the error amplifier? What is the relation between them?

ΔVidiff = Vref – Vocm = 880.0 mV - 875 mV = 5 mV

ΔVodiff = VBP – VCTRLP = 1.558559 - 1.554258 = 4.3mV

$$\frac{\Delta \text{Vodiff}}{\Delta \text{Vidiff}} = \frac{4.3\ \text{mV}}{5\ \text{mV}} = 0.86\text{V}$$

They are not exactly equal because the relation between them is the gain error amplifier.

2) Diff small signal ccs:

- **Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).**
- **Plot diff gain (magnitude in dB and phase) vs frequency.**

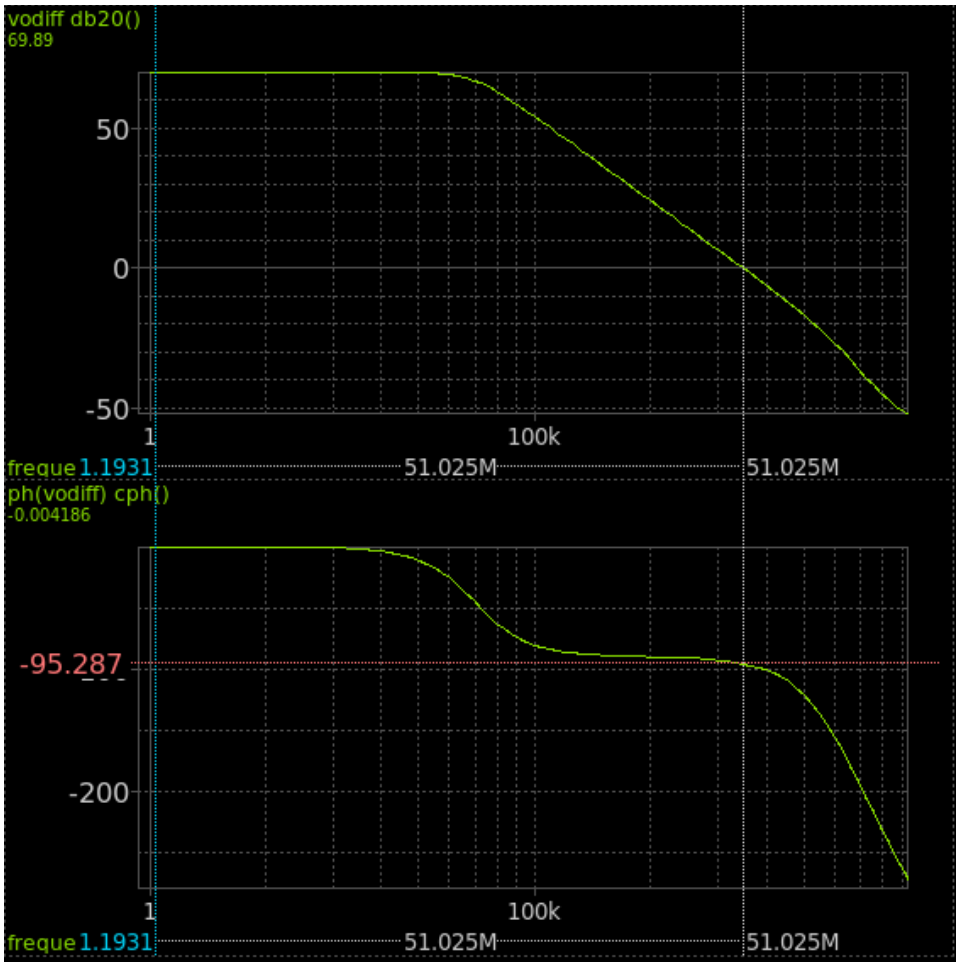


Figure 19 : diff gain (magnitude in dB and phase) vs frequency

```
gain                =   3.121452e+03 at=  1.000000e+00
bw                  =   1.644323e+04
ugf                 =   5.102532e+07
gbw = 5.132675e+07
```

Figure 20 : Open Loop Gain and BW form simulation (Actual CMFB)

From simulation PM = 180 + Ph(UGF) = 180 + -95.287 = 84.7°

• **Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).**

DC gain = GM Rout

Rout = Rout,up// Rout,down

Rout,up ≈ ro4(1+gm4*ro5) = 137.5 MΩ

Rout,down≈ ro3(1+gm3*(ro2//ro1)) = 15.88 MΩ

GM = gm,input = 177.642uS

DC gain = 68.06dB

Bw = $\frac{1}{2\pi * Rout * Cout}$ **→ Cout = 0.5+0.1(parasitic) = 0.6 → Bw = 18.63 KHz**

GBW = Dc gain * Bw = 51.4 MHz = UGF

$\mathbf{Wnd2} = \frac{gm,M3a}{2\pi(Css,M3a+Cdd,M2a+Cdd,Ma1a)} \rightarrow \mathrm{CDD1} = 15.49\mathrm{f}, \mathrm{CDD2} = 8.811\mathrm{f}, \mathrm{CSS} = 55.8\mathrm{f} \rightarrow \mathrm{Wp2} = 310.8\mathrm{MHz}$

PM = 90 - $Tan^{\wedge}(-1)(\frac{Wp2}{Wu})$ **= 88.59°**

Parameter	Hand Analysis	Simulation Result
DC Gain	68.06 dB	69.89 dB
Bandwidth (BW)	18.63 kHz	16.44 kHz
GBW / UGF	51.4 MHz	51.02 MHz
PM	88.59°	84.7°

PART 5: Closed Loop Simulation (AC and STB Analysis)

Create a new testbench with the OTA connected in closed-loop feedback configuration using capacitive feedback as shown below. Note that the CM DC level provided before the input balun is useless because it is blocked by the capacitor.

1) **Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop configuration.**

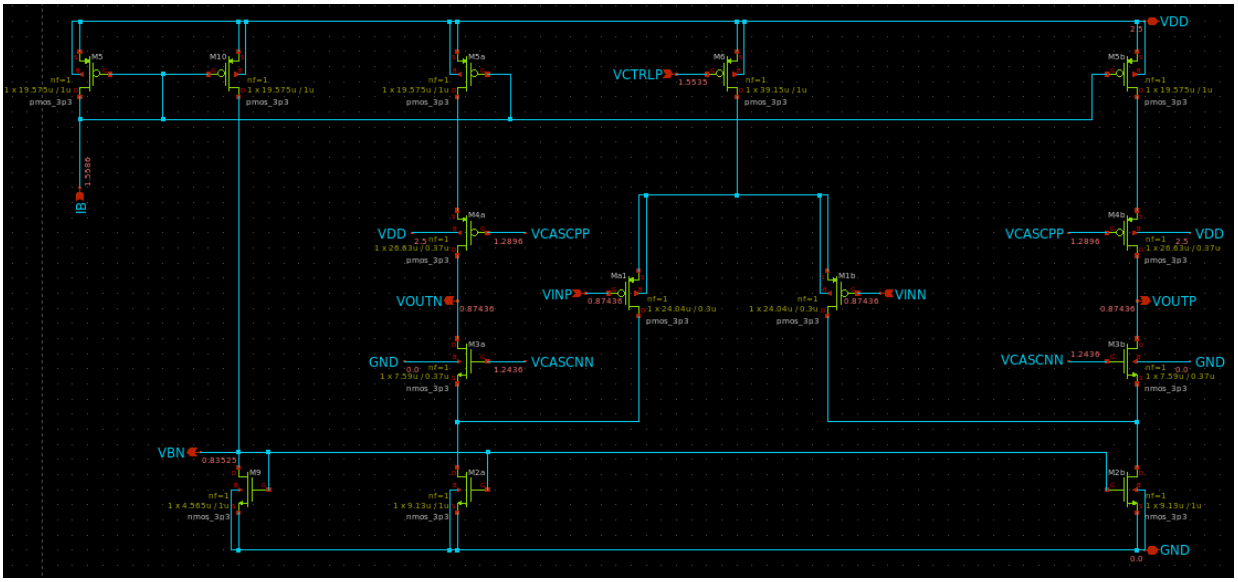


Figure 21 : Schematic of Fully-Differential Folded Cascode OTA

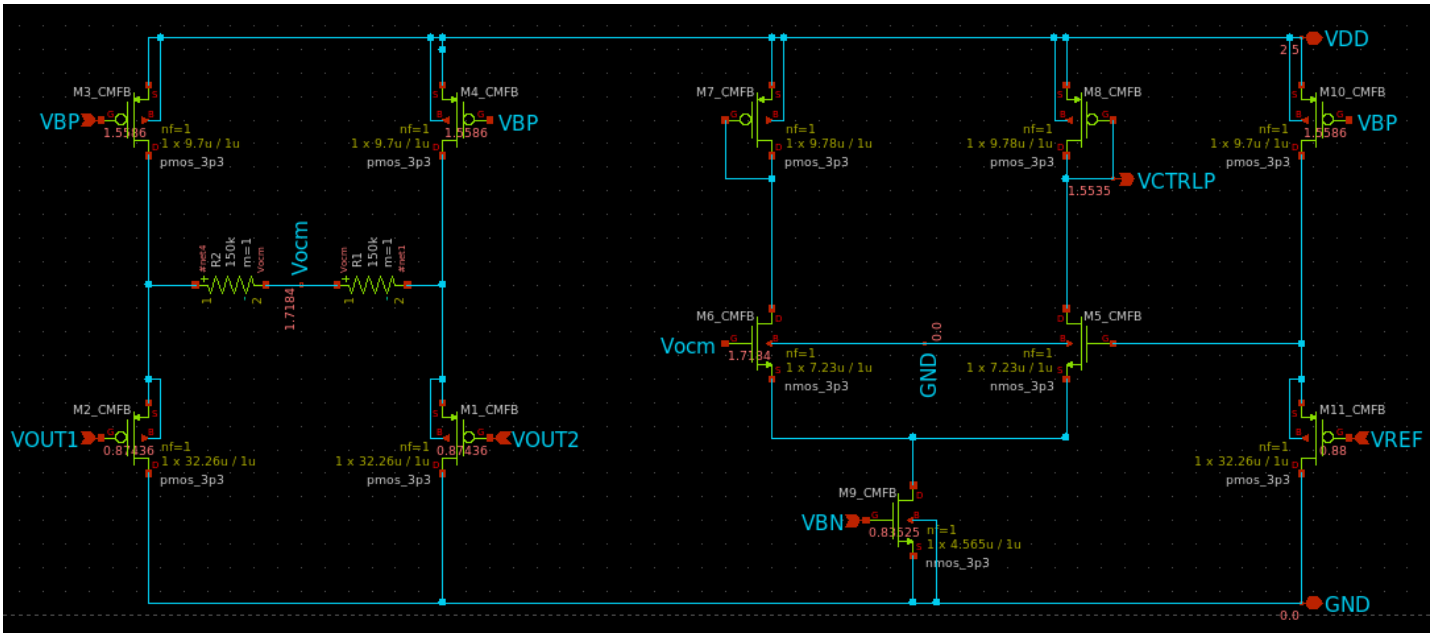


Figure 22 : Actual CMFB

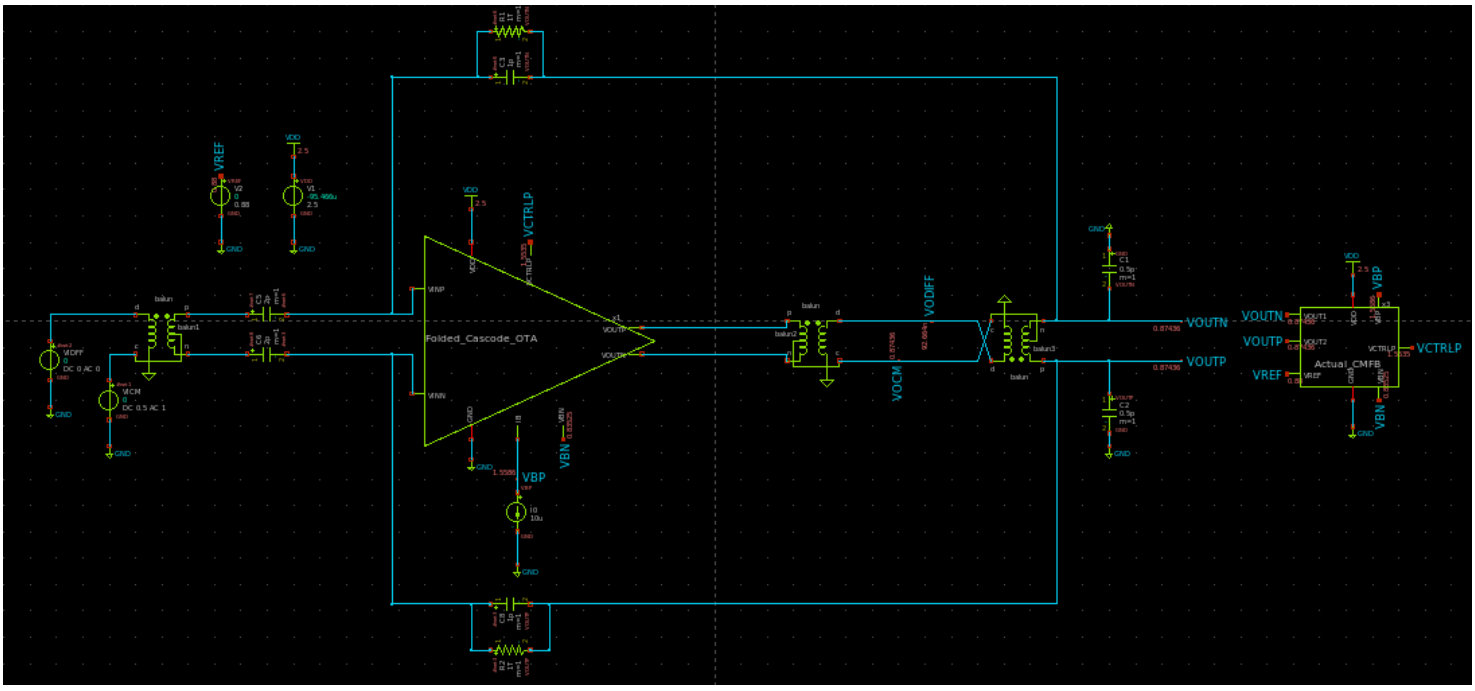


Figure 23 : Closed-loop testbench for simulating a folded-cascode OTA with a Actual CMFB circuit

DC Operating point

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm4.m0	m.x1.xm3.m0	m.x3.xm10_cmfb.m0
model	pmos_3p3.10	nmos_3p3.6	pmos_3p3.9
id	4.90317e-06	4.99219e-06	4.93972e-06
gm	1.85813e-05	1.41853e-05	4.9917e-05
gds	4.38491e-06	2.67182e-06	1.31672e-07
vgs	1.21038	1.24357	0.941441
vth	0.774877	0.654469	0.783924
vds	0.294425	0.427286	0.775989
vdsat	0.333805	0.473963	0.154388

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm3_cmfb.m0	m.x1.xm1.m0	m.x1.xm2.m0
model	pmos_3p3.9	pmos_3p3.9	nmos_3p3.8
id	4.94045e-06	4.9922e-06	4.9922e-06
gm	4.99244e-05	5.04236e-05	8.00452e-05
gds	1.30942e-07	9.2877e-08	1.20001e-06
vgs	0.941441	0.941441	0.816274
vth	0.783924	0.783923	0.796201
vds	0.781611	1.25641	0.816272
vdsat	0.154388	0.154389	0.0978722

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm8_cmfb.m0	m.x3.xm7_cmfb.m0	m.x3.xm4_cmfb.m0
model	pmos_3p3.9	pmos_3p3.9	pmos_3p3.9
id	5.26302e-06	4.83876e-06	4.94045e-06
gm	5.2064e-05	4.95608e-05	4.99244e-05
gds	1.2014e-07	1.11548e-07	1.30942e-07
vgs	0.946539	0.938208	0.941441
vth	0.783928	0.783928	0.783924
vds	0.946538	0.938207	0.781611
vdsat	0.157873	0.152183	0.154388

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm3a.m0	m.x1.xm3b.m0	m.x3.xm9_cmfb.m0
model	nmos_3p3.8	nmos_3p3.8	nmos_3p3.9
id	9.7605e-06	9.76051e-06	1.01018e-05
gm	0.000156216	0.000156217	0.000100595
gds	2.70251e-06	2.70251e-06	3.49799e-07
vgs	0.819063	0.819063	0.835242
vth	0.799374	0.799374	0.687329
vds	0.449838	0.449838	0.739363
vdsat	0.098027	0.0980271	0.172087

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm5_cmfb.m0	m.x3.xm6_cmfb.m0	m.x1.xm8.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	5.26302e-06	4.83876e-06	4.90317e-06
gm	7.80621e-05	7.34919e-05	4.8363e-05
gds	2.08111e-07	1.9512e-07	1.43104e-07
vgs	0.98464	0.979019	0.835242
vth	0.928494	0.928494	0.685215
vds	0.814091	0.822421	1.28961
vdsat	0.115611	0.112089	0.171291

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x3.xm11_cmfb.m0	m.x3.xm1_cmfb.m0	m.x3.xm2_cmfb.m0
model	pmos_3p3.13	pmos_3p3.13	pmos_3p3.13
id	4.93971e-06	4.94045e-06	4.94045e-06
gm	7.52933e-05	7.53008e-05	7.53008e-05
gds	8.70546e-08	8.7216e-08	8.72161e-08
vgs	0.844009	0.844025	0.844026
vth	0.783937	0.783937	0.783937
vds	1.72401	1.71839	1.71839
vdsat	0.0935863	0.0935951	0.0935951

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm9.m0	m.x1.xm2b.m0	m.x1.xm2a.m0
model	nmos_3p3.9	nmos_3p3.9	nmos_3p3.9
id	1.01343e-05	2.02567e-05	2.02567e-05
gm	0.000100841	0.000202541	0.000202541
gds	3.30756e-07	1.03061e-06	1.03061e-06
vgs	0.835242	0.835242	0.835242
vth	0.687329	0.68835	0.68835
vds	0.835239	0.424515	0.424515
vdsat	0.172088	0.172481	0.172481

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm5.m0	m.x1.xm10.m0	m.x1.xm5b.m0
model	pmos_3p3.13	pmos_3p3.13	pmos_3p3.13
id	1e-05	1.01343e-05	9.76051e-06
gm	0.000101062	0.000102318	9.83379e-05
gds	2.29564e-07	1.55258e-07	9.05948e-07
vgs	0.941441	0.941441	0.941441
vth	0.783939	0.783937	0.783941
vds	0.94144	1.66475	0.297256
vdsat	0.154376	0.154377	0.154374

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm5a.m0	m.x1.xm6.m0	m.x1.xm7.m0
model	pmos_3p3.13	pmos_3p3.13	pmos_3p3.12
id	9.76051e-06	2.09925e-05	4.90317e-06
gm	9.83379e-05	0.000207708	8.15537e-05
gds	9.05948e-07	5.17533e-07	7.25456e-07
vgs	0.941441	0.946539	0.915958
vth	0.783941	0.78394	0.880994
vds	0.297256	0.855792	0.915957
vdsat	0.154374	0.157864	0.0986095

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm1b.m0
model	pmos_3p3.12
id	1.04962e-05
gm	0.000178321
gds	2.50993e-06
vgs	0.769844
vth	0.744238
vds	1.21969
vdsat	0.0931265

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.xm4b.m0	m.x1.xm4a.m0	m.x1.xma1.m0
model	pmos_3p3.12	pmos_3p3.12	pmos_3p3.12
id	9.76051e-06	9.76051e-06	1.04962e-05
gm	0.000163128	0.000163128	0.000178321
gds	1.31395e-06	1.31395e-06	2.50993e-06
vgs	0.913129	0.913129	0.769845
vth	0.879982	0.879982	0.744238
vds	1.32838	1.32838	1.21969
vdsat	0.0975963	0.0975963	0.0931265

- **What is the CM level at the OTA output? Why?**

Vocm = 0.874 V The OTA output CM level settles at ~0.874 V because the CMFB loop forces the outputs to track the reference voltage (Vref = 0.88 V).

- **What is the CM level at the OTA input? Why?**

Vicm = 0.874 V ,The large feedback resistors create a DC path that forces the input common-mode level to equal the output's.

2) Differential closed-loop response:

- **Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).**
- **Plot VODIFF vs frequency**

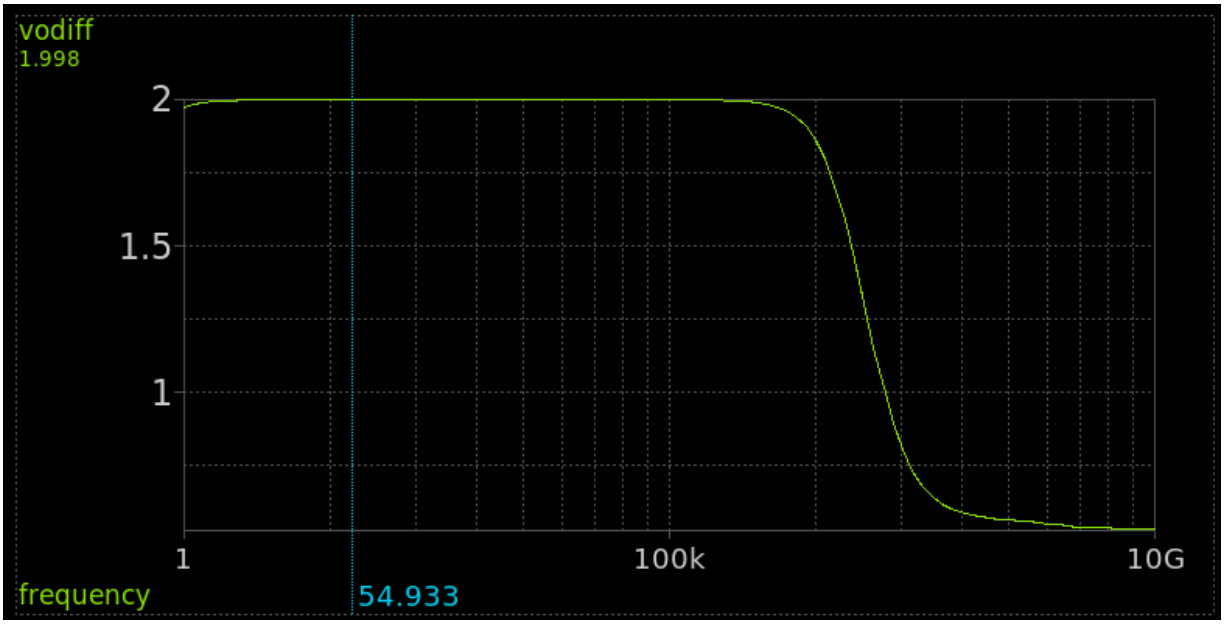


Figure 24 : VODIFF vs frequency

- **Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)**

```
gain                =   1.998060e+00 at=  1.258925e+03
bw                  =   8.472513e+06
ugf                 =   1.639110e+07
gbw = 1.692859e+07
```

Figure 25 : Closed Loop Gain and BW and UGF and GBW form simulation (Actual CMFB)

3) Differential and CMFB loops stability (STB analysis):

- **Run STB analysis (in addition to AC analysis 1Hz:10Gz, logarithmic, 10 points/decade) two times: first using the 0V source in the diff path, and second using the 0V source in the CM path.**

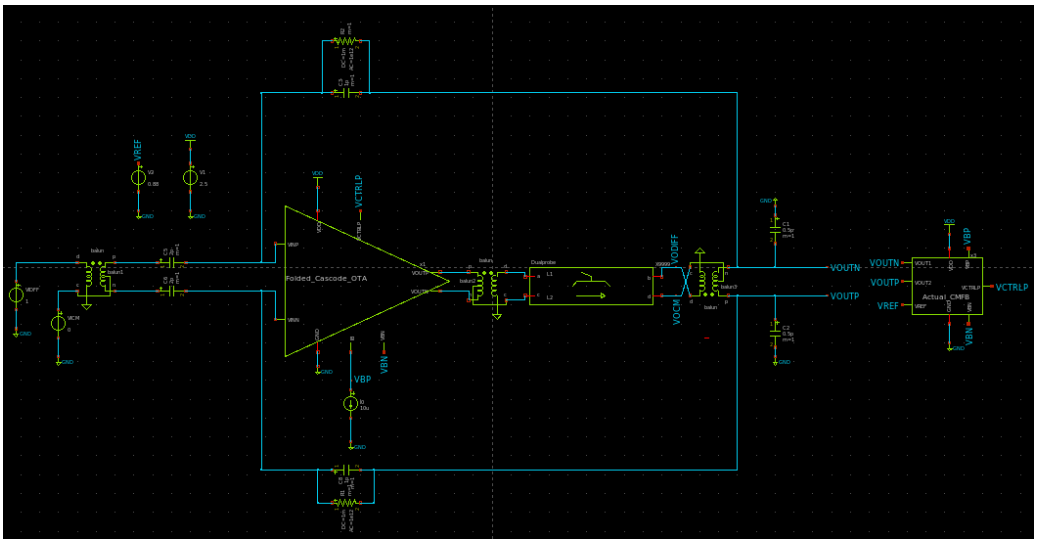


Figure 26 : A closed-loop testbench for simulating the AC response and stability of the OTA with capacitive feedback.

- **Plot loop gain in dB and phase vs frequency for the two simulations overlaid.**

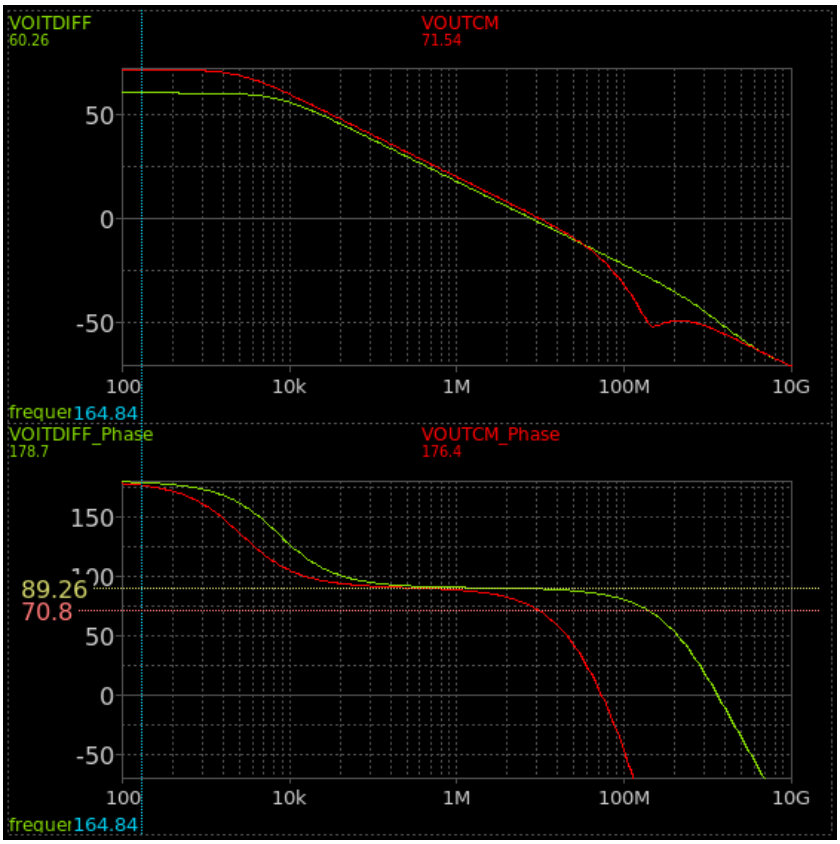


Figure 27 : loop gain in dB and phase vs frequency for diff path and CM path overlaid

```
diff1_lg = 6.025642e+01
diff1_gx = 7.584074e+06
diff1_pm = 8.926434e+01
-------------------------------
cm1_lg = 7.155297e+01
cm1_gx = 9.558142e+06
cm1_pm = 7.083427e+01
```

Figure 28 : PM for diff path and CM path.

- **Compare GBW and PM of diff and CM loops. Comment.**

Parameter	diff path	CM path
DC Gain	60.26 dB	71.45 dB
GBW / UGF	7.58 MHz	9.56 MHz
PM	89.26°	70.08°

Comment :

The design successfully makes the common-mode loop faster than the differential loop, which is a key requirement for high-performance fully-differential amplifiers, while ensuring both loops are independently stable with ample phase margin.

- **Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation.**

Parameter	Loop Gain (LG)	Open loop
DC Gain	60.26 dB	69.88 dB
GBW	7.58 MHz	51.03 MHz

Comment :

LG decreased due to beta effect ($\simeq 1/3$) so GBW and DC Gain decreased
The DC gain difference is expected due to the feedback factor, while the lower closed-loop GBW accurately reflects the extra capacitive loading from the feedback network itself.

PART 6: Closed Loop Simulation (Transient Analysis)

1) Differential and CMFB loops stability (transient analysis) + CL settling time: Differential input pulse

• Apply a differential input pulse (initial value = 0, pulse value = 100mV, delay = 1us, period = 2us, pulse width = 1us, rise = fall = 10ns). → PULSE(0 100m 1u 10n 10n 1u 2u)

• Run transient analysis for 3us with 10ns max step.

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

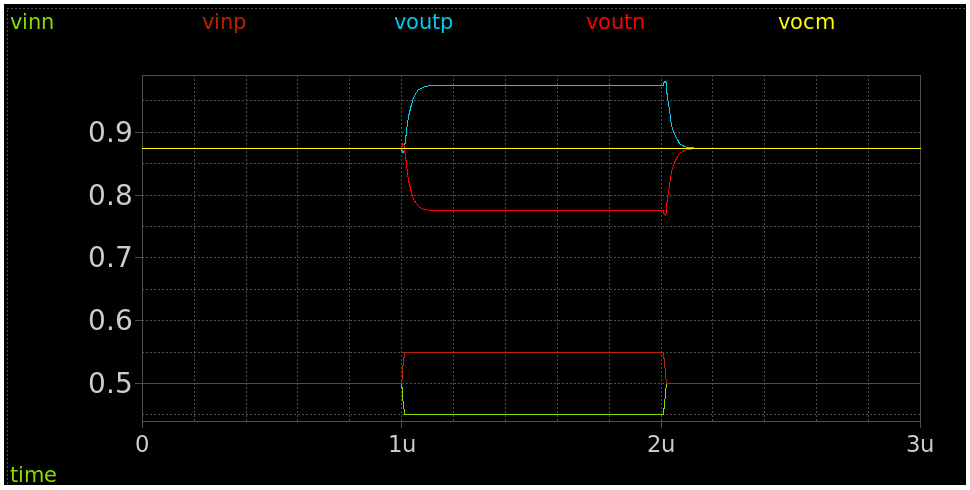


Figure 29 : VINP, VINN, VOUTP, VOUTN, and VOCM overlaid for DIFF input pulse

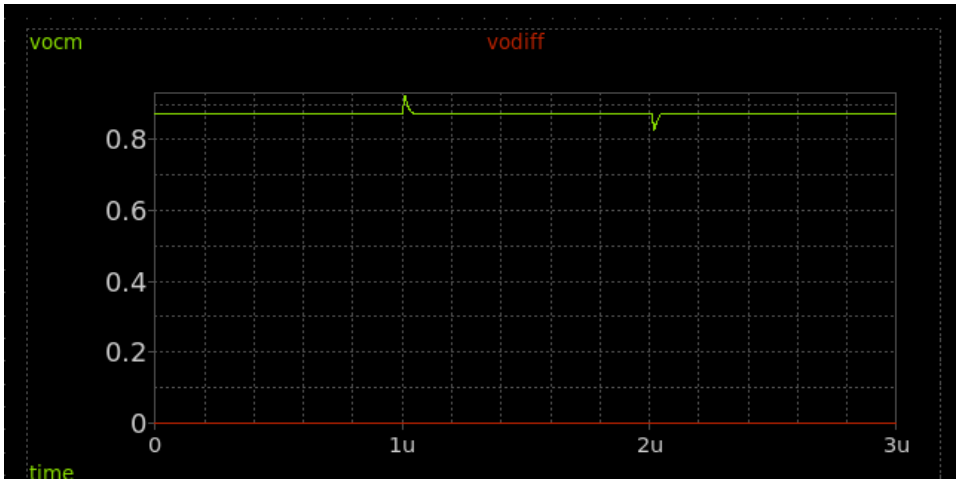


Figure 30 : Vocm and Vodiff overlaid for DIFF input pulse

• Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

No there is no ringing in both loops differential/CM , yes the both are stable cause the PM>70

But there an small **(glitch)** overshot at Vocm case the PM_CM = 70.8 is less than 76

• Calculate the 1% settling time and compare it to the required specification. If the specification is not satisfied, what design changes could be a possible solution?

```
settling                =   9.65624e-08
```

The simulated 1% settling time is 96.56 ns. This value successfully meets the required design specification of ≤ 100 ns.

If not satisfied you can increase GBW → increase gm or decrease CL

2) Differential and CMFB loops stability (transient analysis): CM input pulse

• Set differential input to zero and apply the same previous pulse at the balun CM input.

• Run transient analysis for 3us to test the fully differential capacitive amplifier stability.

• Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

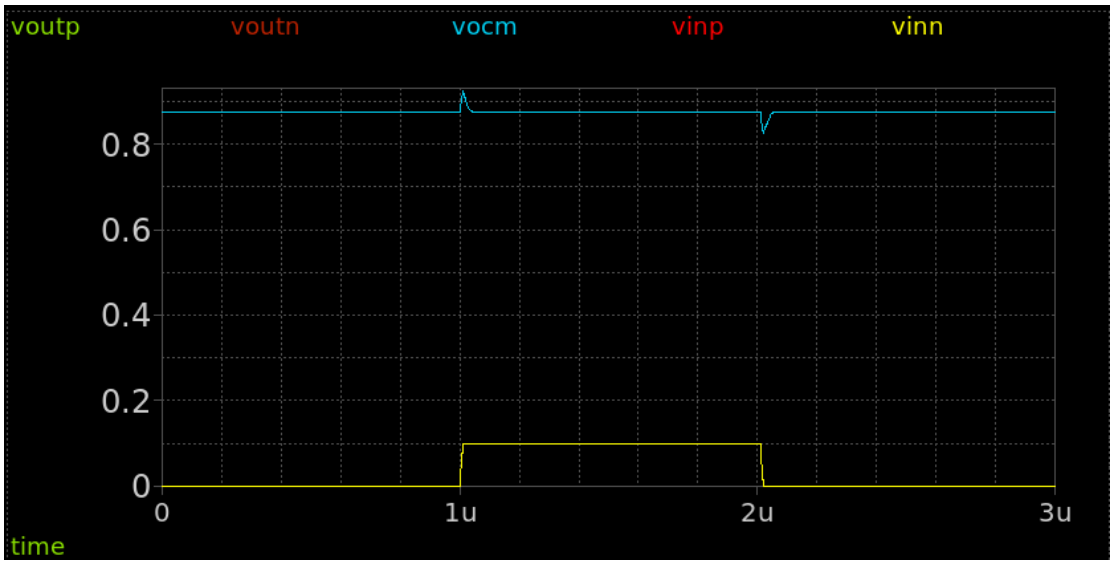


Figure 31 : VINP, VINN, VOUTP, VOUTN, and VOCM overlaid for CM input pulse

• Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

No there is no ringing in both loops differential/CM , yes the both are stable cause the PM>70

But there an small **(glitch)** overshot at Vocm case the PM_CM = 70.8 is less than 76

3) Output swing:

- **Apply a differential sinusoidal input with freq = 100kHz and amplitude = 150mV.**
- **Run transient analysis for three periods (30us) with 0.1us max time step.**
- **Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.**

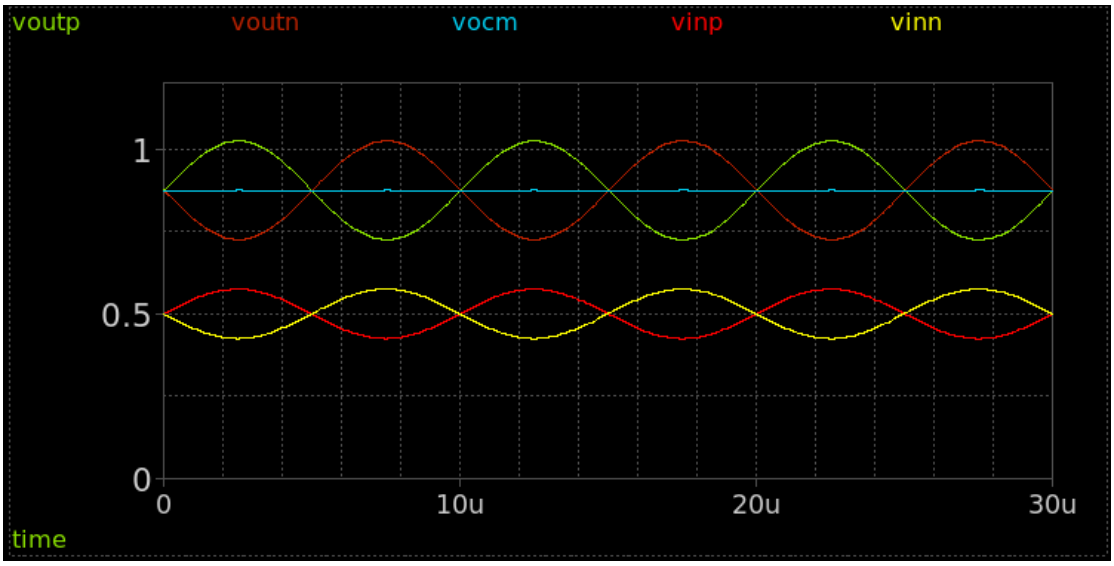


Figure 32 : VINP, VINN, VOUTP, VOUTN, and VOCM overlaid for differential sinusoidal input

- **Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.**

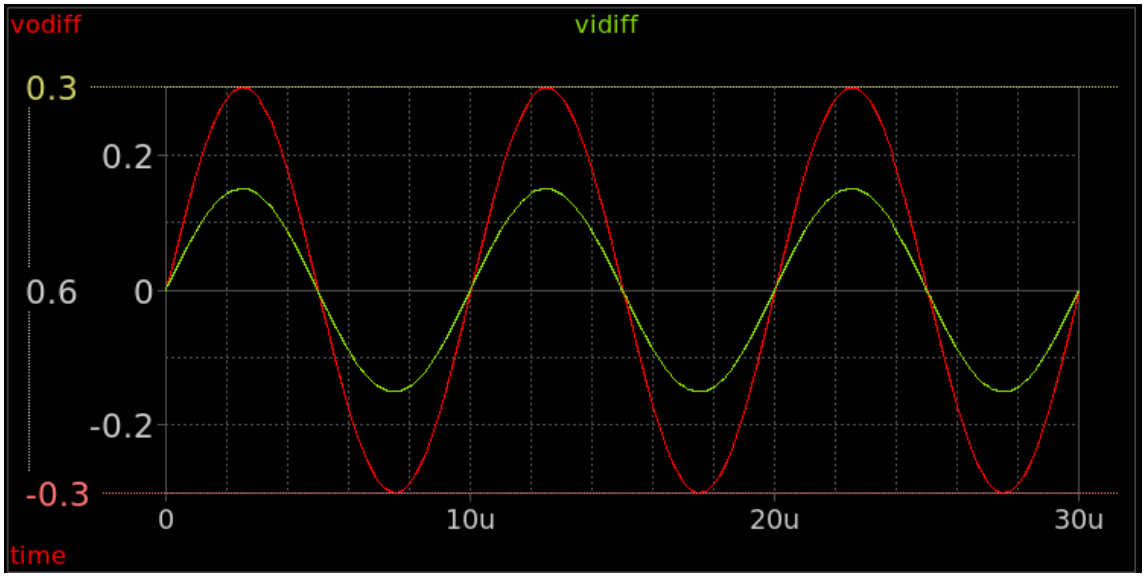


Figure 33 : VIDIFF and VODIFF overlaid for differential sinusoidal input

- **Calculate the diff input and output peak-to-peak swings and the closed loop gain.**

Peak-to-peak = 0.3 - -0.3 = 0.6 V

Aocl = $\frac{0.6\ V}{0.3\ V}$ = 2

Final Summary Folded-Cascode OTA Performance Verification :

Parameter	Specification	Simulated Result	Status
Closed-Loop Gain	2	1.998	✅
DC Loop Gain	≥ 60 dB	60.26 dB	✅
Phase Margin (PM)	≥ 70°	89.26°	✅
Settling Time (1% error)	≤ 100 ns	96.56 ns	✅
Differential Output Swing	1.2 Vpk-pk	> 1.9 V (Available)	✅
CM Input Range – Low	≤ 0 V	-0.54 V	✅
CM Input Range – High	≥ 1 V	1.52 V	✅

Appendix

OP_code

```
.control
save all
op
show m : id : gm : gds : vgs : vth : vds : vdsat
print allv
write lab11_OP.raw
.endc
```

Diff_small_signal

```
.control
save all
op
ac dec 10 1 10G
meas ac Gain MAX vmag(VOUT) FROM=1 TO=10G
let ff2=Gain*0.707
meas ac BW WHEN vmag(VOUT)=ff2 FALL =1
save v(VOUT)
remzerovec
write lab11_ac.raw
.endc
```

Loop gain"

```
.func tian_loop_1() {1/(1-1/(2*(ac1.I(v.X9999.Vi)*ac2.V(X9999.x)-
ac1.V(X9999.x)*ac2.I(v.X9999.Vi))+ac1.V(X9999.x)+ac2.I(v.X9999.Vi)))}
.func tian_loop_2() {1/(1-1/(2*(ac3.I(v.X9999.Vi1)*ac4.V(X9999.y)-
ac3.V(X9999.y)*ac4.I(v.X9999.Vi1))+ac3.V(X9999.y)+ac4.I(v.X9999.Vi1)))}
*--------------------------------------------------------
* Probes
*--------------------------------------------------------
.save V(X9999.x) I(v.X9999.Vi)
.save V(X9999.y) I(v.X9999.Vi1)
*--------------------------------------------------------
* CONTROL BLOCK
*--------------------------------------------------------
.control

  set filetype=ascii
  set num_threads=8
  set color0=white
  set color1=black
  set xbrushwidth  =3
  unset askquit
```

```
optran 0 0 0 100n 4u 0
op
write stb.raw
set appendwrite
*--------------------------------------------------------
* First Loop STB analysis
*--------------------------------------------------------
* Set voltage AC to 1
alter i.X9999.Ii1 acmag=0
alter v.X9999.Vi1 acmag=0
alter v.X9999.Vi acmag=1
ac dec 50 100 10G
* Set Current to 1
alter i.X9999.Ii acmag=1
alter v.X9999.Vi acmag=0
ac dec 50 100 10G
*--------------------------------------------------------
* Second Loop STB analysis
*--------------------------------------------------------
* Set voltage AC to 1
alter i.X9999.Ii acmag=0
alter v.X9999.Vi acmag=0
alter v.X9999.Vi1 acmag=1
print loop1_LG
ac dec 50 100 10G
* Set Current to 1
alter i.X9999.Ii1 acmag=1
alter v.X9999.Vi1 acmag=0
ac dec 50 100 10G
let tian_signal_1 = tian_loop_1()
let loop_L1_gain_db = db(tian_signal_1)
let loop_L1_gain_ph = 180*cph(tian_signal_1)/pi
*plot loop_L1_gain_db
*plot loop_L1_gain_ph
save tian_signal_1
meas ac Gain_1 MAX vmag(tian_signal_1) FROM=1 TO=10G
let LG_L1 = 20*log10(Gain_1)
meas ac L1_GAIN_CROSSOVER_FREQ WHEN loop_L1_gain_db=0
meas ac L1_phaseatzerogain FIND loop_L1_gain_ph AT=L1_GAIN_CROSSOVER_FREQ
*let L1_PM = abs(180 - L1_phaseatzerogain)
*print L1_PM
let loop1_LG = LG_L1
let loop1_GX = L1_GAIN_CROSSOVER_FREQ
let loop1_PM = L1_phaseatzerogain
save loop1_LG
save loop1_GX
save loop1_PM
```

```
   let tian_signal_2 = tian_loop_2()
   let loop_L2_gain_db = db(tian_signal_2)
   let loop_L2_gain_ph = 180*cph(tian_signal_2)/pi
   *plot loop_L2_gain_db
   *plot loop_L2_gain_ph
   save tian_signal_2
   meas ac Gain_2 MAX vmag(tian_signal_2) FROM=1 TO=10G
   let LG_L2 = 20*log10(Gain_2)
   meas ac L2_GAIN_CROSSOVER_FREQ WHEN loop_L2_gain_db=0
   meas ac L2_phaseatzerogain FIND loop_L2_gain_ph AT=L2_GAIN_CROSSOVER_FREQ
   *let L2_PM = abs(180 - L2_phaseatzerogain)
   *print L2_PM
   let loop2_LG = LG_L2
   let loop2_GX = L2_GAIN_CROSSOVER_FREQ
   let loop2_PM = L2_phaseatzerogain
   save loop2_LG
   save loop2_GX
   save loop2_PM
let DIFF1_LG = loop1_LG
let DIFF1_GX = loop1_GX
let DIFF1_PM = loop1_PM
let CM1_LG = loop2_LG
let CM1_GX = loop2_GX
let CM1_PM = loop2_PM
   echo ----------------------------------------------------
   print DIFF1_LG DIFF1_GX DIFF1_PM
   echo      ----------------------------
   print CM1_LG CM1_GX CM1_PM
   echo ----------------------------------------------------
   write Dstb.raw tian_signal_1 tian_signal_2
   .meas ac CMGain MAX vmag(VODIFF) FROM=1 TO=1k
   let ff2=Gain*0.707
   .meas ac BW WHEN vmag(VODIFF)=ff2 FALL =1
let GBW            = Gain*BW
print GBW
.endc"
```

Settling time:

```
".control
save all
tran 10n 3u

let v_initial = x.
let v_final = x + margin
let v_swing = v_final - v_initial

let v_1_percent = v_initial + 0.01 * v_swing
let v_99_percent = v_initial + 0.99 * v_swing

meas tran t_ Settling TRIG v(VOUT) VAL=v_10_percent RISE=1 TARG v(VOUT) VAL=v_99_percent RISE=1

print t_ Settling

write Settling.raw
.endc"
```