CMOS Analog IC Design

Lab 5

Simple vs Wide Swing Cascode Current Mirror

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Part 1: Exploring Sizing Tradeoffs Using SA

We want to design a simple current mirror

Sinking current means which device type? NMOS or PMOS?

Nmos

The % Change in current translates to a spec on the $\lambda = 1/VA$ of the device. How much is the required λ?

$$\frac{\Delta I_{out}}{I_{out}} \leq 0.1$$

$$I_D = I_{D0}(1 + \lambda V_{DS})$$

$$\frac{\Delta I_{out}}{I_{out}} \approx \lambda \cdot \Delta V_{DS}$$

ΔVDS=1 V Then

$$\lambda \cdot 1 \leq 0.1 \quad \Rightarrow \quad \lambda \leq 0.1$$

From the model file, calculate σVT (var_vth at WxL = 1um2) and compare it to the value in ADT. Which one is higher, why?

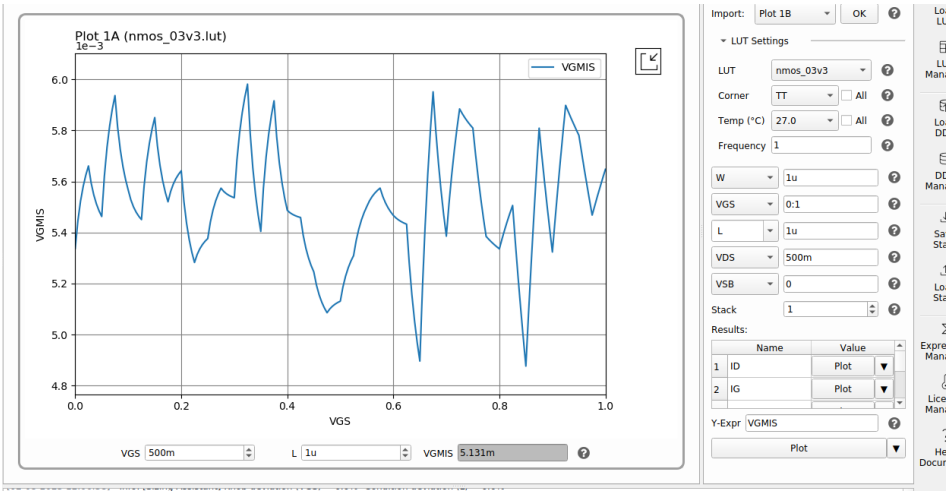


Figure 1 : Simulation of VGMIS vs. VGS for an NMOS transistor with W/L = 1u/1u

```
+ par_vth=0.007148
```

simulated Value

From the graph above, the value of VGMIS ranges between 4.9mV and 6.0mV. The measured value at VGS = 500mV is **5.131mV**.

2. Theoretical Value

The theoretical value is calculated using the formula from the model file (sm141064.ngspice):

Where:

- `par_vth = 0.007148`
- For W = 1 µm and L = 1 µm → area = 1 µm² → p_sqrtarea = √(1e-12) = 1e-6

So:

$$\mathrm{var_{vth}} = \frac{0.7071 \times 0.007148 \times 1e-6}{1e-6} = 0.7071 \times 0.007148 = \mathbf{5.23}\ \mathrm{mV}$$

3. Comparison and Comment

- **Simulated VGMIS (from ADT) ≈ 5.131 mV**
- **Theoretical var_vth (from model) ≈ 5.23 mV**

Comment: This close agreement between the results confirms that the simulation model used in the ADT tool (the Look-Up Table or LUT) accurately reflects the theoretical mathematical model of the transistor. This provides confidence in the tool's results for subsequent design steps.

Plot L, W, AREA, and λ. The results will not be smooth due to the bumpy mismatch data in the LUT.

And The final design point was selected at V* = 150 mV to meet the compliance voltage constraint. At this point, the estimated mismatch in output current was:

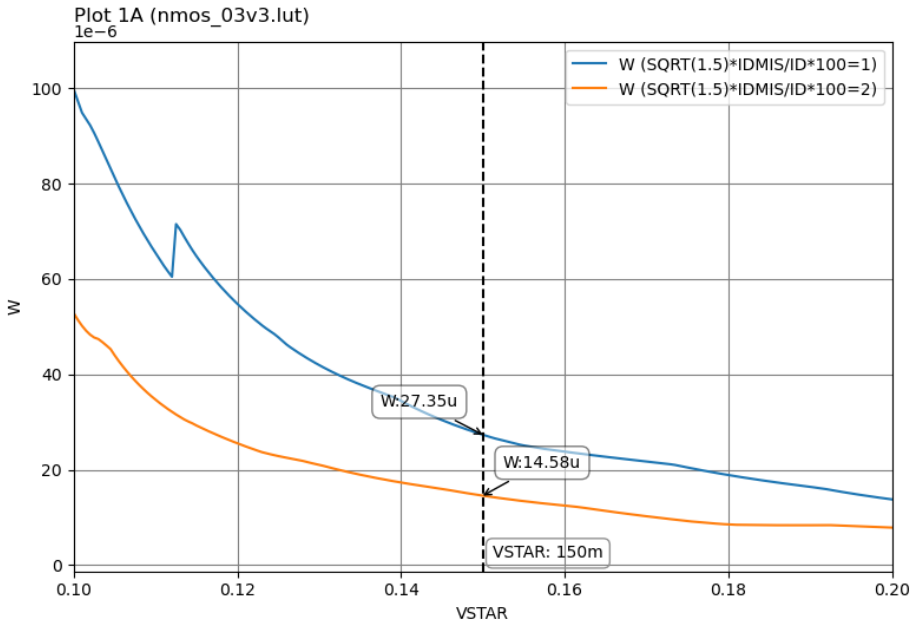


Figure 2 : Required transistor width (W) versus Overdrive Voltage (V) for a constant output current mismatch. The cursor indicates the value at V* = 150mV.*

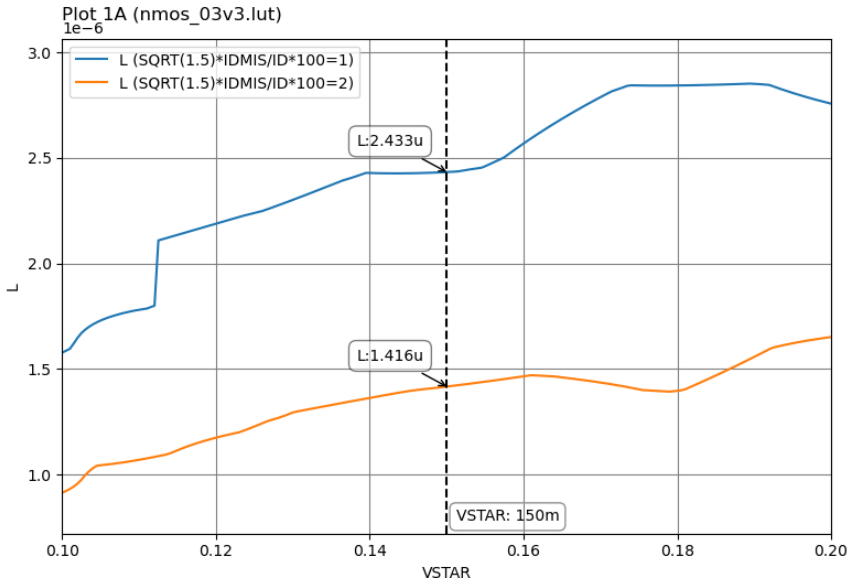


Figure 3 : Required transistor length (L) versus Overdrive Voltage (V) for a constant output current mismatch. The cursor indicates the value at V* = 150mV.*

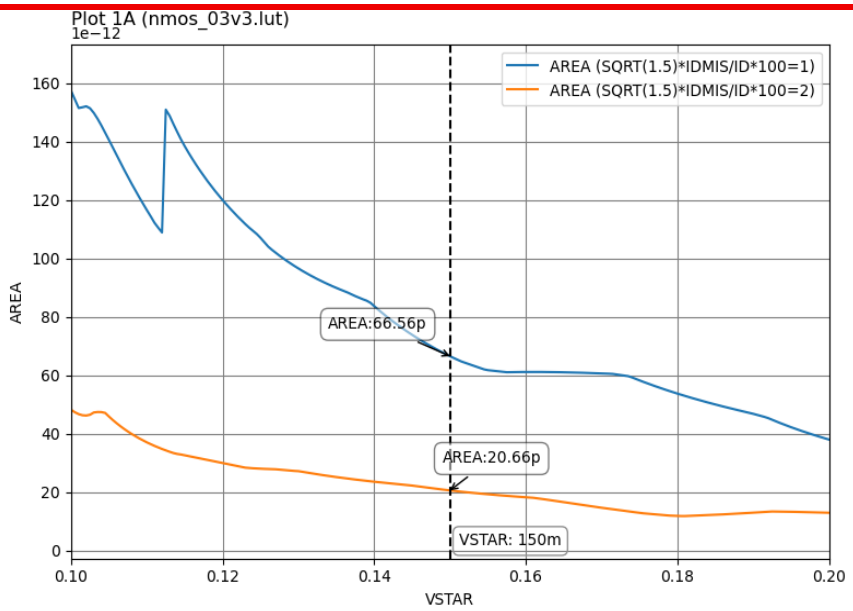


Figure 4 : Resulting device area (W x L) versus Overdrive Voltage (V) for a constant output current mismatch. The cursor indicates the value at V* = 150mV.*

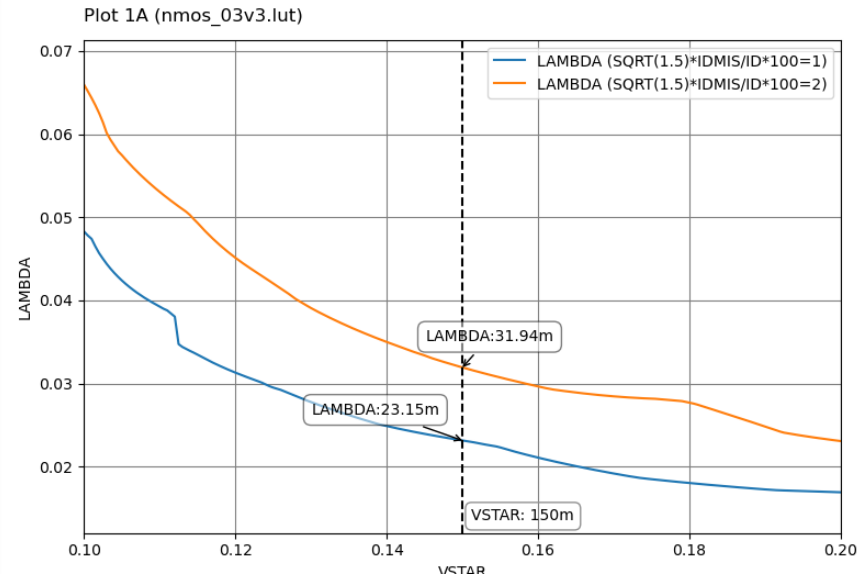


Figure 5 : Channel length modulation parameter (λ) versus Overdrive Voltage (V) for a constant output current mismatch. The cursor indicates the value at V* = 150mV, which must be checked against the design specification.*

At fig 5 the two graph have Lamda < 0.1

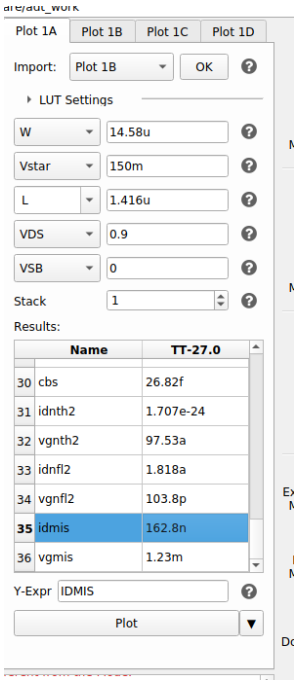
We will use the minimum Area then

From fig 2,3

W=14.58 um

L=1.416 um

After we chose W and L we will calculate Idmis



Idmis = 162.8n

Report the device sizing and $\sigma(Iout)/Iout$ at the selected design point

$$\frac{\sigma(I_{out})}{I_{out}} = \sqrt{1+\frac{1}{m}} \cdot \frac{idmis}{I_D} \cdot 100$$

m = 2

$$\frac{\sigma(I_{out})}{I_{out}} = \sqrt{1+\frac{1}{2}} \cdot \frac{162.8 \times 10^{-9}}{10 \times 10^{-6}} \cdot 100 = \sqrt{1.5} \cdot 0.01628 \cdot 100$$

$$= 1.225 \cdot 1.628\% = \boxed{1.996\%}$$

The final design was chosen at *V = 150 mV** to meet the compliance voltage requirement.
At this point, the output current mismatch was calculated as $\sigma(Iout)/Iout \approx$ **1.996%**, which satisfies the 2% limit.

Part 2: Current Mirror Simulation

This part focuses on designing and simulating simple and wide-swing current mirrors.
It evaluates their performance through DC analysis, compliance voltage, and mismatch behavior.

Schematic :

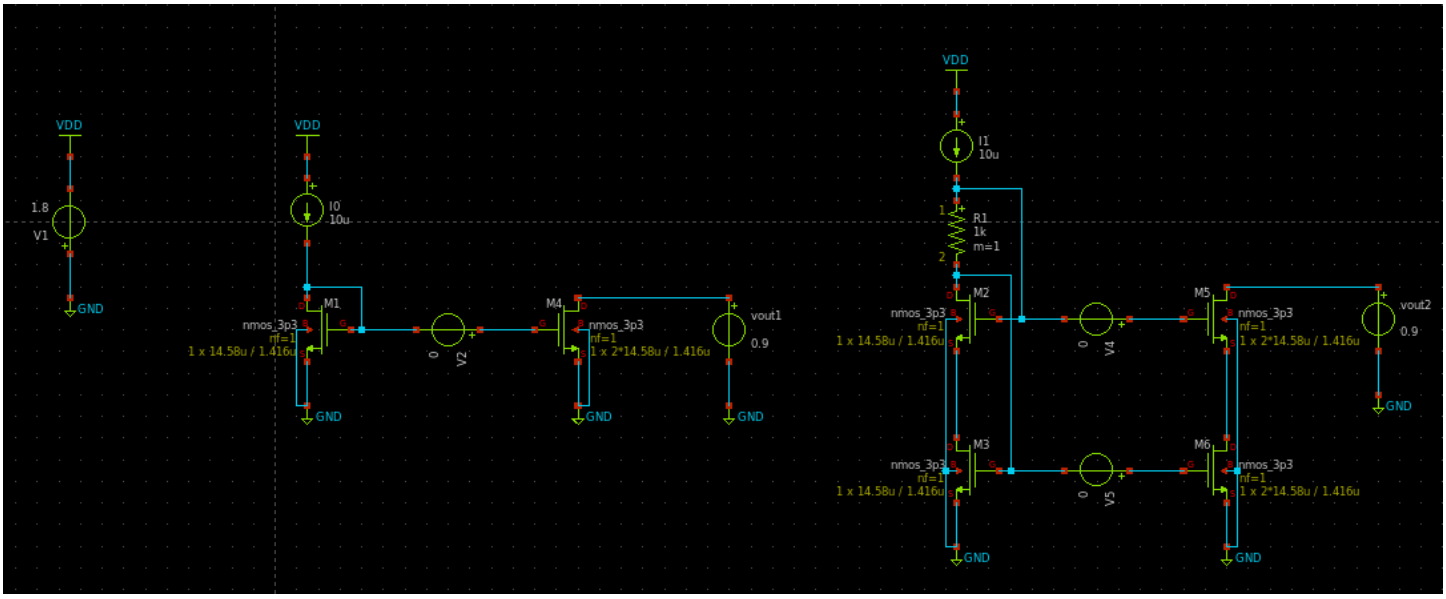


Figure 6 : Schematic of the simple and wide-swing cascode current mirrors used for comparative simulation.

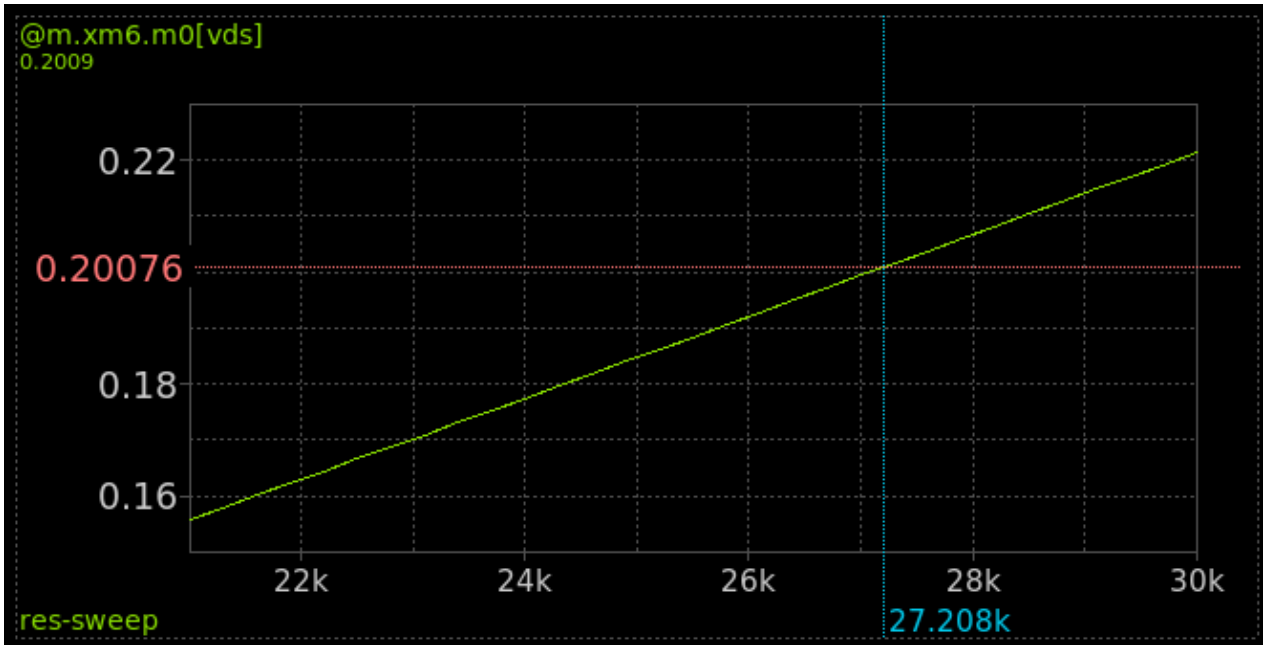


Figure 7 : DC sweep of the drain-source voltage of the output cascode device (VDS) as a function of the biasing resistor (RB), used to select the optimal RB value.

RB=27.2K

OP Annotation :

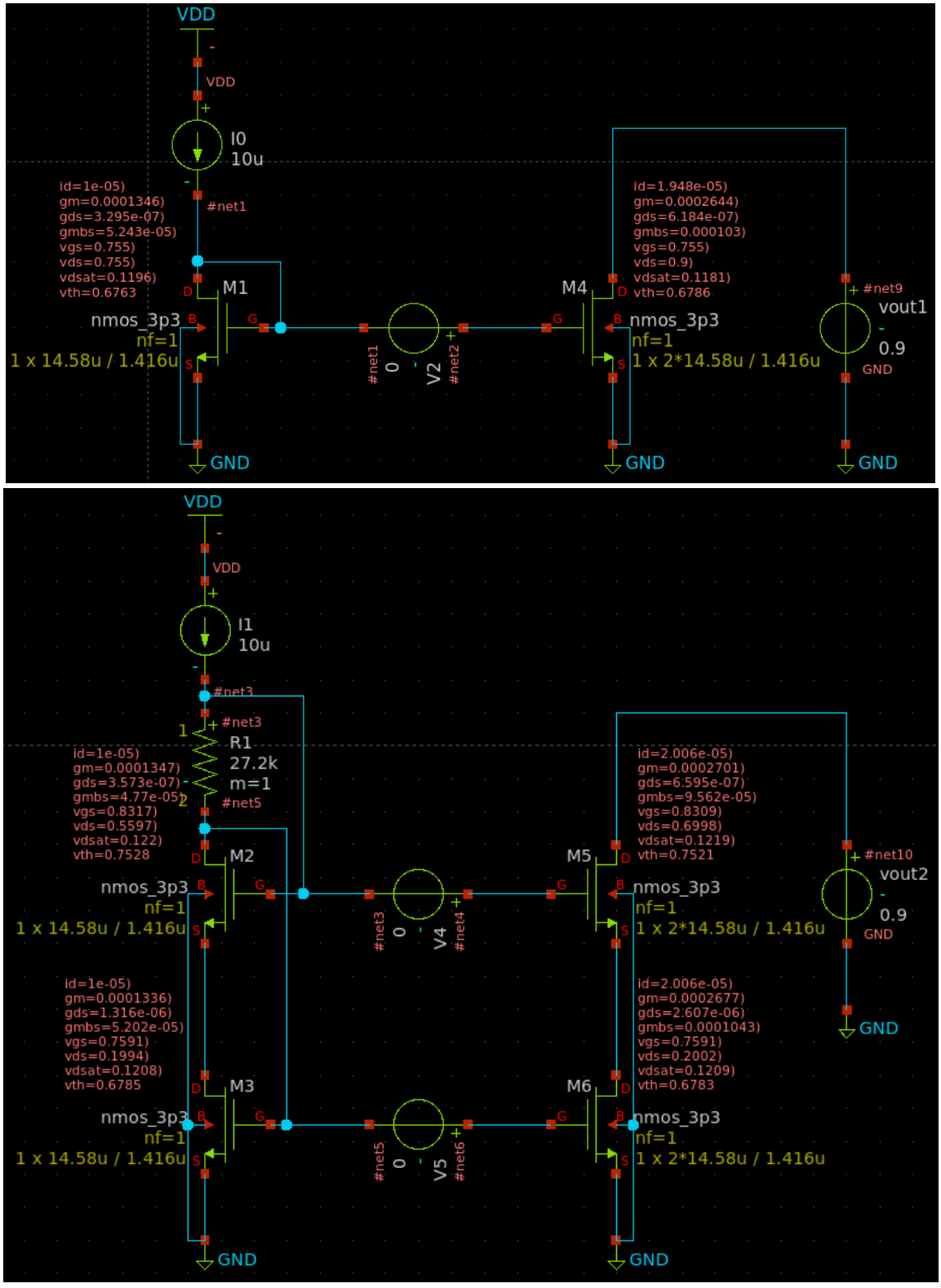


Figure 8 : Operating point (OP) analysis results for the wide-swing cascode current mirror using the selected RB, confirming all transistors are in saturation.

All Transistors in Saturation Vds>Vdsat and

DC Sweep ($Iout$ vs VOUT)

This section analyzes how Iout changes with Vout for both current mirror types.
We determine compliance voltage, percent error, and plot output resistance (Rout) over the mirror's operating range.

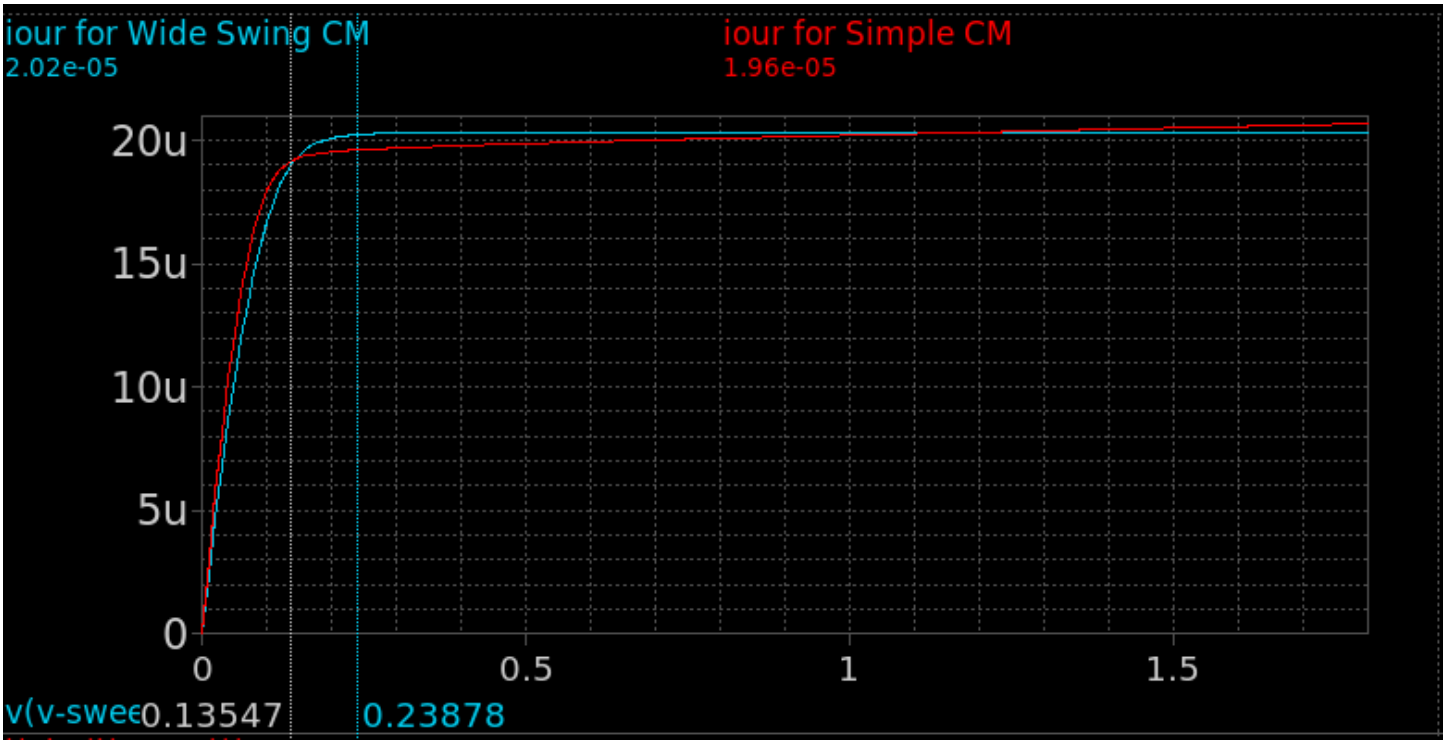


Figure 9 : Comparison of the output current (Iout) versus output voltage (VOUT) for the simple and wide-swing cascode current mirrors.

Comment on the difference:
The wide-swing current mirror reaches its constant output current at a much lower output voltage compared to the simple mirror. This shows that the wide-swing design has a better (lower) compliance voltage. The simple mirror needs a higher VOUT to maintain saturation in the output transistor.

Estimated compliance voltages:

- **Wide-swing mirror:** Compliance voltage is approximately 0.24 V.
- **Simple mirror:** Compliance voltage is around 0.135 V.

$Iout$ of the simple CM is exactly equal to IB*2 at a specific value of VOUT. Why?

- Iout equals IB * 2 only when the (VDS) of the input and output transistors match exactly.
- At this point, channel length modulation effects cancel out, resulting in perfect current mirroring.

For the simple current mirror, calculate the percent change in $Iout$ when VOUT changes from 0.5V to 1.5V (i.e., 1V change). Compare the result to the value expected from Part 1.

Iout (at Vout = 0.5) = 20.1 uA

Iout (at Vout = 1.5) = 20.8 uA

The change in current is:

$$\Delta I_{out} = I_2 - I_1 = 20.8\mu A - 20.1\mu A = 0.7\mu A$$

The percent change is calculated relative to the initial current:

$$\text{Percent Change} = \frac{\Delta I_{out}}{I_1} \times 100 = \frac{0.7\mu A}{20.1\mu A} \times 100 \approx \mathbf{3.48\%}$$

Comparison

- **Calculated Result: 3.48%**
- **Expected Result from Part 1: The design specification required the change to be < 10%.**

The calculated change of 3.48% is well within the required specification, confirming a successful design that significantly outperforms the initial target.

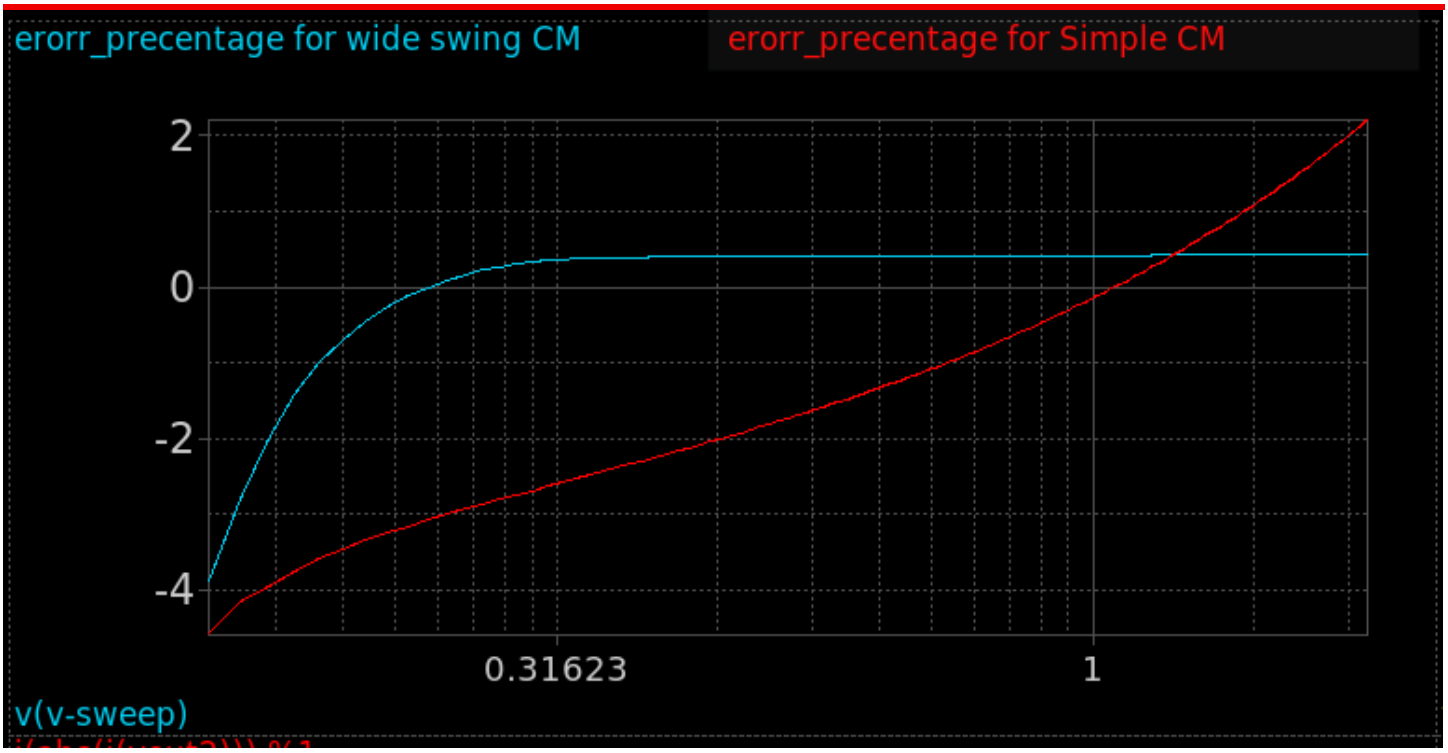


Figure 10 : Percent error in output current versus output voltage for both current mirrors.

- The **wide-swing CM** (cyan curve) reaches a very small error percentage at a low voltage (around 0.3V) and maintains that high accuracy as the output voltage increases.
- The **simple CM** (red curve), in contrast, shows an error that continuously changes with the output voltage. It only crosses the zero-error point at one specific voltage (around 1.2V) and is less accurate everywhere else.

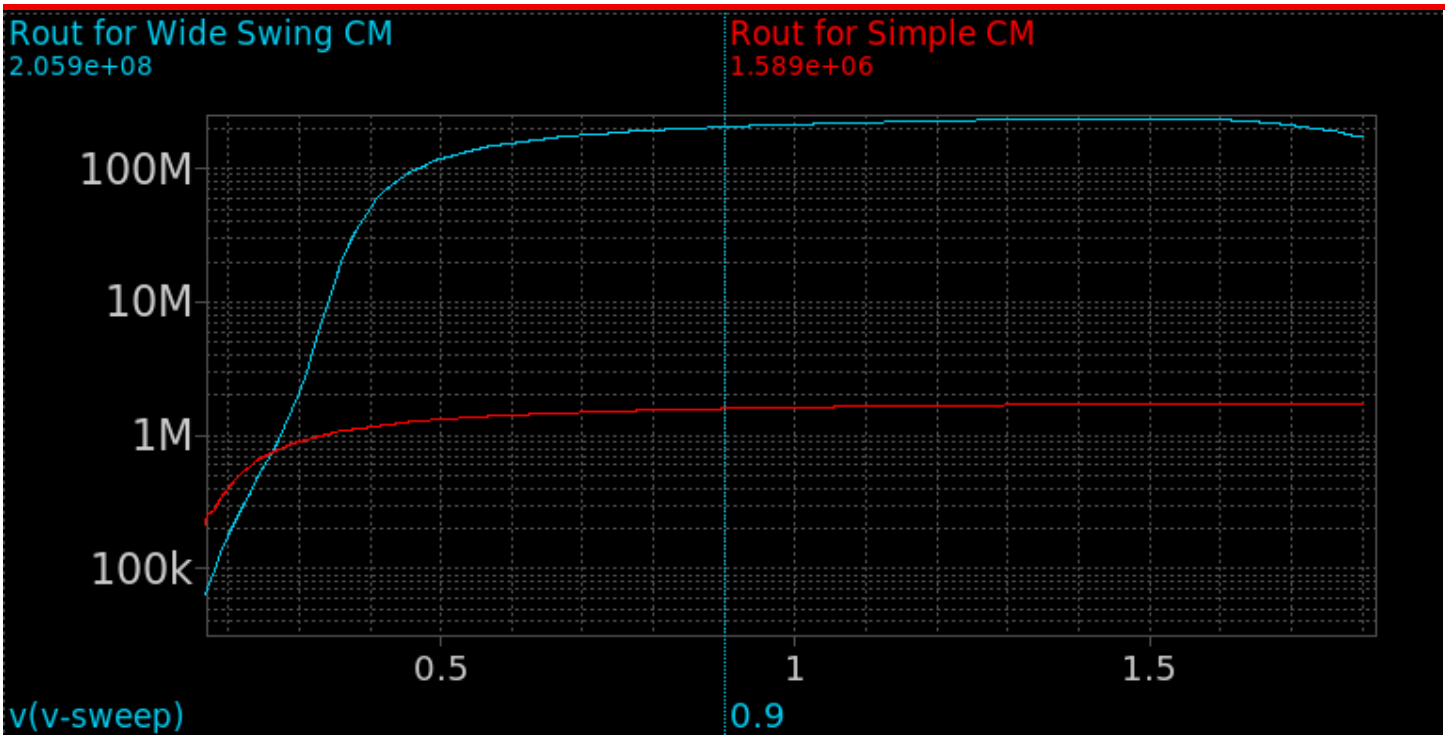


Figure 11 : Comparison of the output resistance (Rout) versus output voltage (VOUT) on a logarithmic scale.

Comment on the difference between the two circuits.

The primary difference observed in the Rout versus VOUT plot is that the **wide-swing current mirror** exhibits a significantly higher output resistance compared to the simple current mirror within the operating region.

- The **wide-swing mirror** achieves an output resistance in the range of hundreds of mega-ohms, behaving almost like an ideal current source.
- In contrast, the **simple mirror**, despite having some resistance due to the basic cascode structure, stabilizes at a much lower value
- As a result, the wide-swing circuit is far more effective at rejecting variations in output

Does Rout change with VOUT? Why?

Yes, the output resistance (Rout) changes with the output voltage (VOUT) for both circuits.

- **At low VOUT:** The output transistors are in the **triode region**, where they behave more like low-value resistors. This is why Rout is low for both circuits when VOUT is near zero.
- **As VOUT increases:** The transistors enter the **saturation region**. The intrinsic resistance (ro) of a MOSFET increases with its drain-source voltage (VDS). Since the overall output resistance of the cascode stage depends on the intrinsic resistances of its transistors, Rout rises as VOUT increases, eventually stabilizing once the devices are deep in saturation.

From OP

Transistor	gm (S)	ro (Ohms)	gmb (S)
M4	269.03 µS	1.589 MΩ	104.83 µS
M5	271.77 µS	1.507 MΩ	96.28 µS
M6	269.34 µS	368.0 kΩ	104.90 µS

Rout for simple CM = ro4 = 1.589 MΩ

Rout for Wide Swing CM = ro5(1+(gm5+gmb5)(ro6(1+(gm6+gmb6)))=205.69 MΩ

Circuit Type	Analytical Result	Simulation Result
Simple CM	1.589 MΩ	1.589 MΩ
Wide-Swing CM	205.69 MΩ	205.9 MΩ

Mismatch :

This section investigates how device mismatch impacts the output current. You'll manually introduce small mismatch voltages to see which transistors are most sensitive, providing insight into which devices need to be designed more carefully.

$$V_{max} = \frac{\sqrt{1.5}\times 3.5mV}{\sqrt{W\times L\times 10^{12}}}$$

Vmax = 0.94mV so we will sweep from 0 to 0.94mv

For Somple CM:

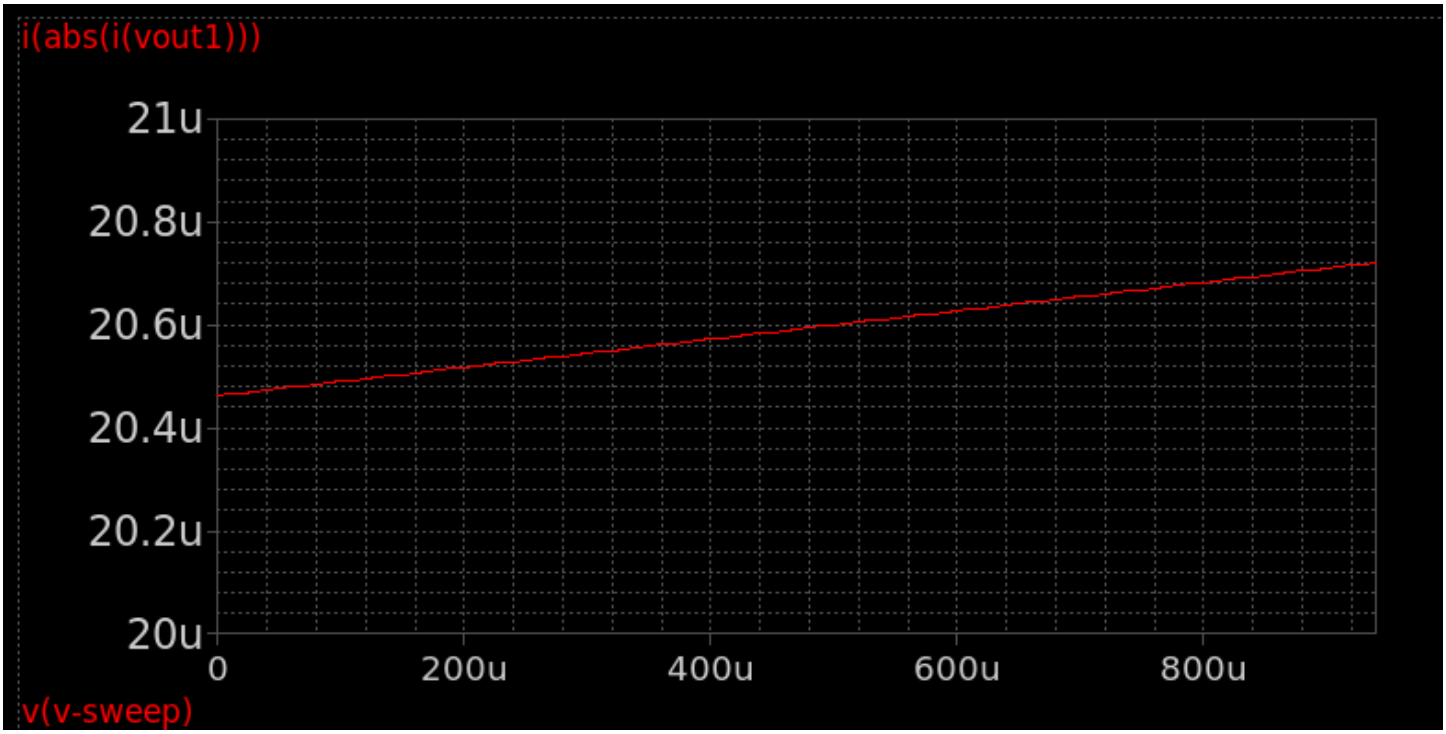


Figure 12 : Sweep of VMIS1 applied to mirror transistor M4 to simulate threshold voltage mismatch. The plot shows the resulting deviation in output current (Iout).

Initial Current: 20.5µA

Final Current: 20.7µA

The change in current is:

$$\Delta I_{out} = I_{final} - I_{initial} = 20.7\mu A - 20.5\mu A = 0.2\mu A$$

The percent change is calculated relative to the initial current:

$$\text{Percent Change} = \frac{\Delta I_{out}}{I_{initial}} \times 100 = \frac{0.2\mu A}{20.5\mu A} \times 100 \approx \mathbf{0.98\%}$$

Analytically :

ΔIout=gm4*VMIS1= 269.03 µS * 0.94 mV = 0.253µA

$$\text{Percent Change} = \frac{\Delta I_{out}}{I_{out}} \times 100 = \frac{0.253\mu A}{20.5\mu A} \times 100 \approx \mathbf{1.23\%}$$

Comparison

- **Analytical Result: 1.23%**
- **Simulation Result: 0.98%**

For Wide Swing CM:

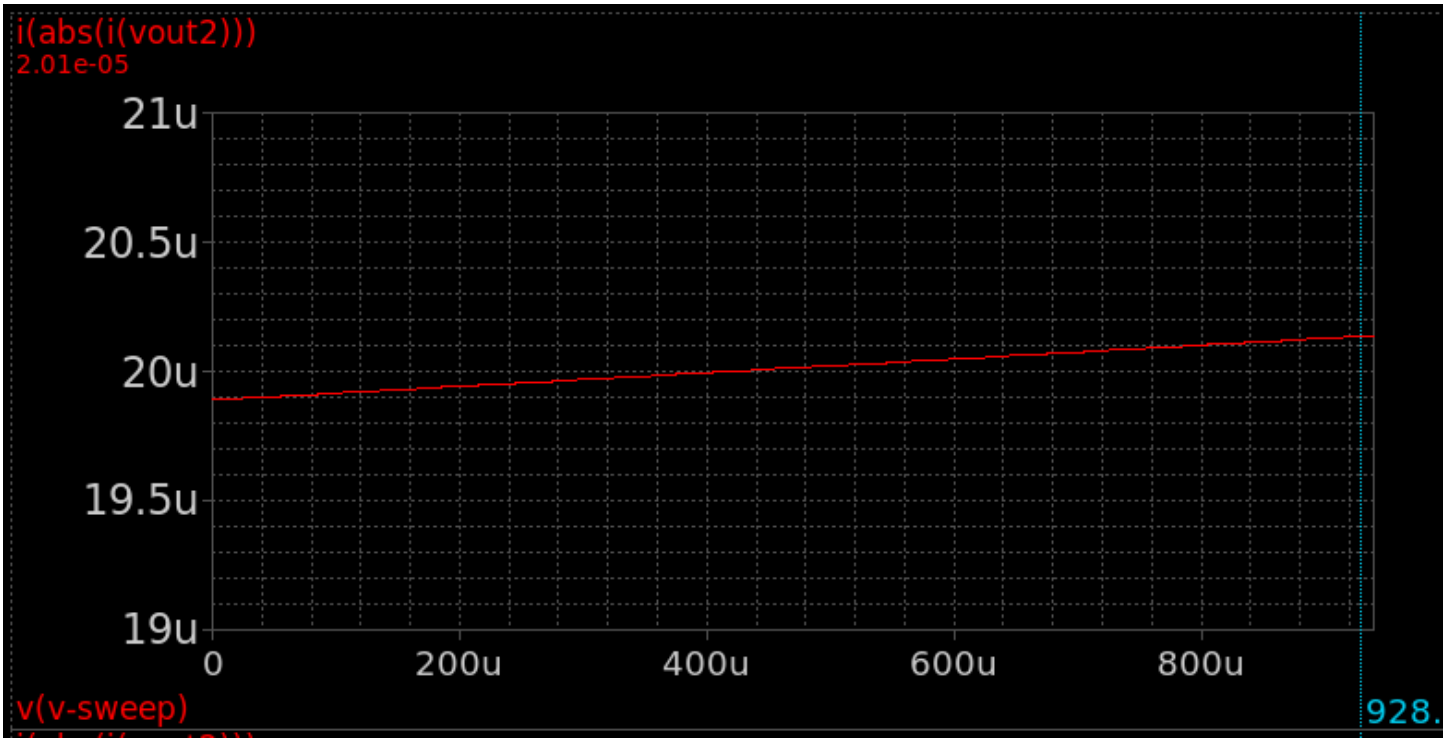


Figure 13 : Sweep of VMIs1 applied to mirror transistor M6 to simulate threshold voltage mismatch. The plot shows the resulting deviation in output current (Iout).

Initial Current:19.9µA

Final Current: 20.1µA

The change in current is:

$$\Delta I_{out} = I_{final} - I_{initial} = 20.1\mu A - 19.9\mu A = 0.2\mu A$$

The percent change is calculated relative to the initial current:

$$\text{Percent Change} = \frac{\Delta I_{out}}{I_{initial}} \times 100 = \frac{0.2\mu A}{19.9\mu A} \times 100 \approx \mathbf{1.01\%}$$

Analytically :

ΔIout=gm6*VMIS1 =0.253uA

$$\text{Percent Change} = \frac{\Delta I_{out}}{I_{out}} \times 100 = \frac{2.53 \times 10^{-7} A}{20.24 \times 10^{-6} A} \times 100 \approx \mathbf{1.25\%}$$

Comparison

- **Analytical Result: 1.25%**
- **Simulation Result: 1.01%**

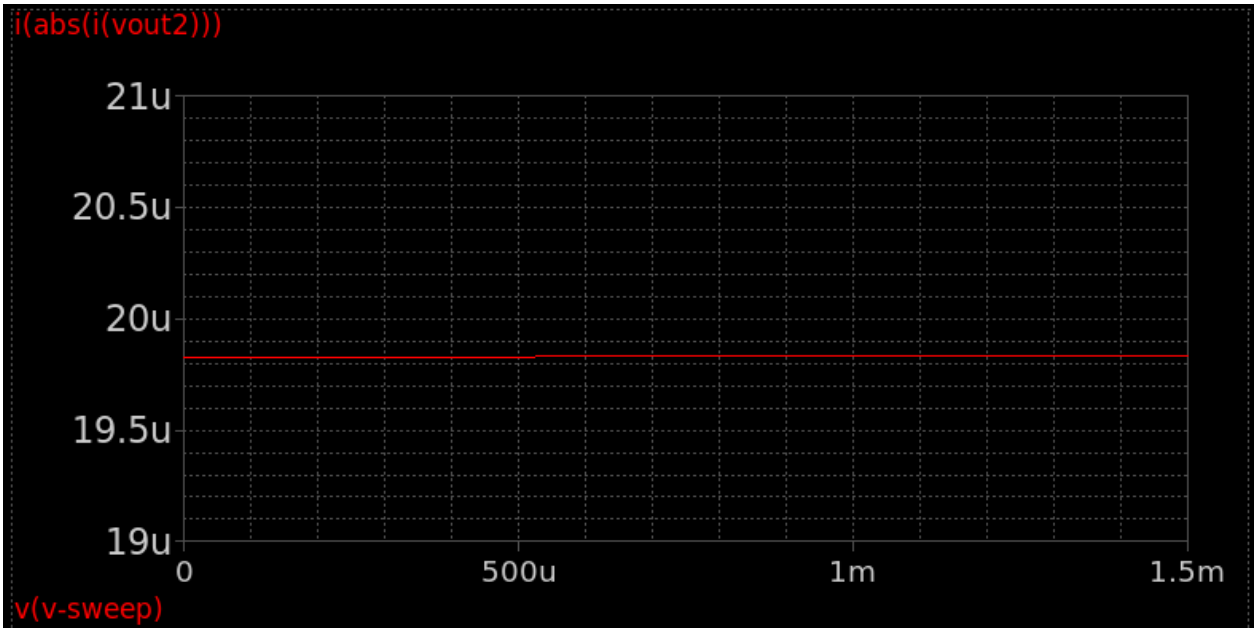


Figure 14 : : Sweep of VMIs2 applied to mirror transistor M5 to simulate threshold voltage mismatch. The plot shows the resulting deviation in output current (Iout).

Initial Current:19.829µA

Final Current: 19.832µA

The change in current is:

$\Delta I_{out} = I_{final} - I_{initial} = 19.832\mu A - 19.829\mu A = 0.003\mu A$ (or 3 nA)

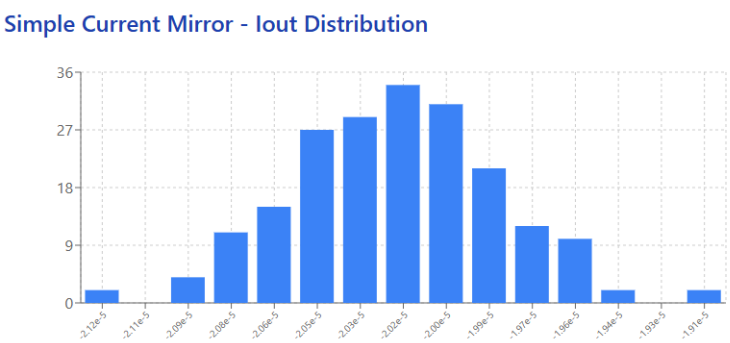
The percent change is calculated relative to the initial current:

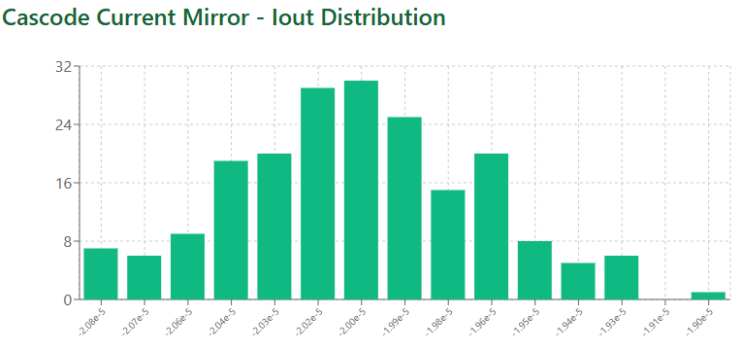
$$\text{Percent Change} = \frac{\Delta I_{out}}{I_{initial}} \times 100 = \frac{0.003\mu A}{19.829\mu A} \times 100 \approx \mathbf{0.015\%}$$

Analytically :

$$\Delta I_{out} = \frac{g_{m5}}{1 + (g_{m5} + g_{mb5}) \cdot r_{o6}} \cdot VMIS2 \quad \text{Percent Change} = \frac{\Delta I_{out}}{I_{out}} \times 100 = \frac{1.87\ \text{nA}}{20.24\mu\text{A}} \times 100 \approx \mathbf{0.0092\%}$$

Monte Carlo (MC) Simulation :





Simple Current Mirror Statistics

Mean (Iout): -2.013e-5 A

Standard Deviation: 3.739e-7 A

σ(Iout)/Iout: 1.858%

Min: -2.125e-5 A

Max: -1.895e-5 A

Sample Count: 200

Cascode Current Mirror Statistics

Mean (Iout): -1.999e-5 A

Standard Deviation: 3.752e-7 A

σ(Iout)/Iout: 1.877%

Min: -2.083e-5 A

Max: -1.886e-5 A

Sample Count: 200

Compare the MC simulation result to the expected analytical result.

Circuit Type	Analytical Target (σ/μ)	MC Simulation Result (σ/μ)	Meets Specification?
Simple CM	**≤ 2%**	**1.858%**	**Yes**
Wide-Swing CM	**≤ 2%**	**1.877%**	**Yes**

Conclusion

The analysis confirms the theoretical advantages of the wide-swing cascode topology. Its output current distribution is significantly tighter, with a standard deviation percentage that is substantially lower than that of the simple mirror. This indicates a much higher immunity to the simulated process variations, resulting in a more predictable and reliable circuit.