CMOS Analog IC Design

Lab 6

Differential Amplifier

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Part 1: Differential Amplifier Design

In this part, we design a resistive-loaded differential amplifier based on the given specifications using the Sizing Assistant (SA) in ADT. We calculate resistor values, determine sizing parameters, and verify input/output levels to ensure proper operation

Section 1.4: Tail Current Source VDS

Assume VDS_tail = 300 mV

Note that $ISS*RD = 2Vout-Cm$

RD =2*0.6/40u = 30K ohm

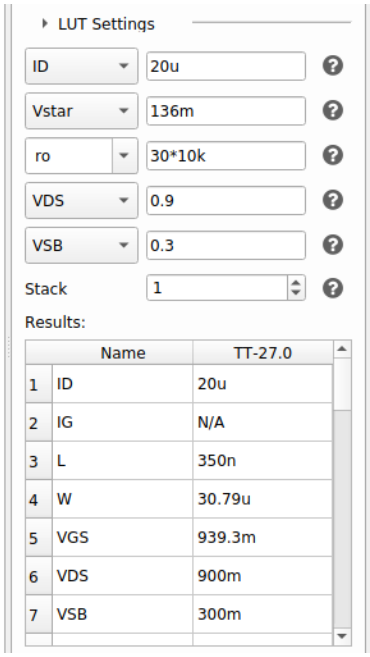
VRD= 20u*RD= 0.6

Choose V^* to meet the differential gain spec.

$$V^* = \frac{1.82V_{R_D}}{|A_v|}$$

V*=136.5mv

Report Input Pair Sizing from SA



	Name	TT-27.0
1	ID	20u
2	IG	N/A
3	L	350n
4	W	30.79u
5	VGS	939.3m
6	VDS	900m
7	VSB	300m

For diff amp M3and M4 sizing is

W=30.79 um

L=350 nm

Given the above assumption for VDS of the tail current source, calculate the required CM input level.

VICM=VS,input+VGS,input

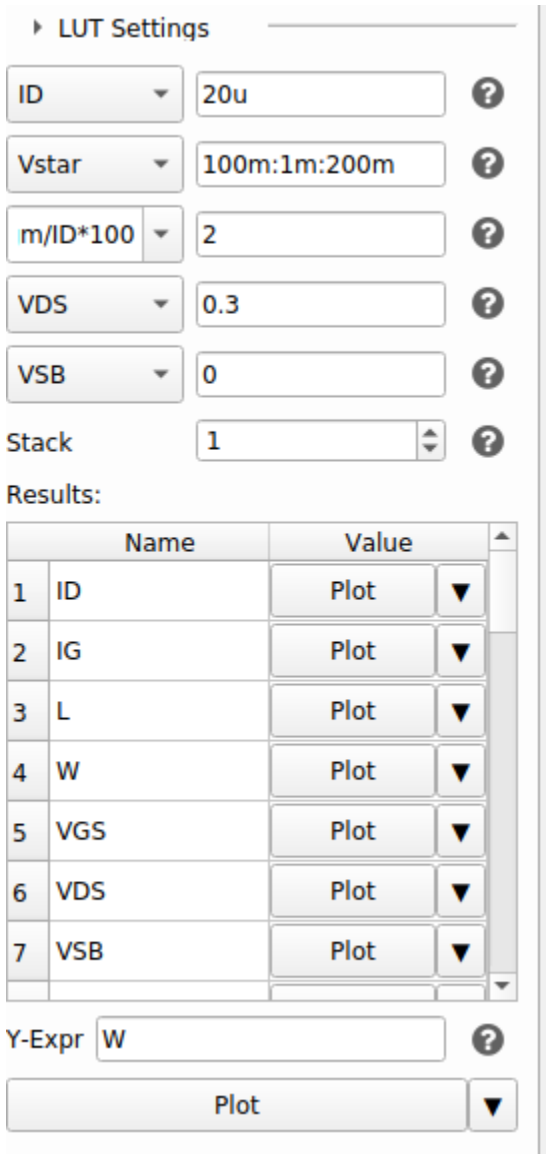
VS,input=VDD−VSD,tail=1.8V−0.3V=1.5V

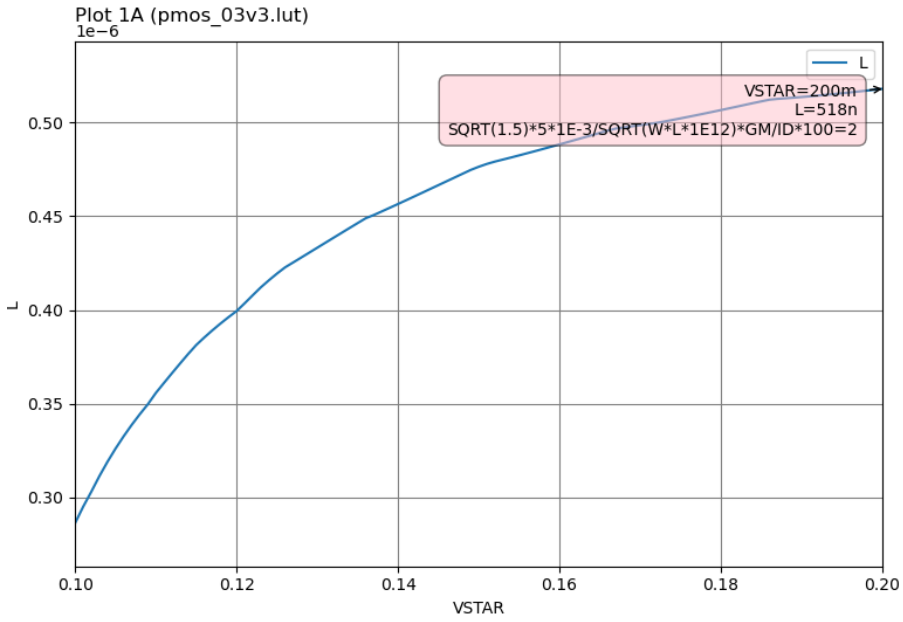
VICM=VS,input+VGS,input

VICM=1.5V+(−0.9393V)

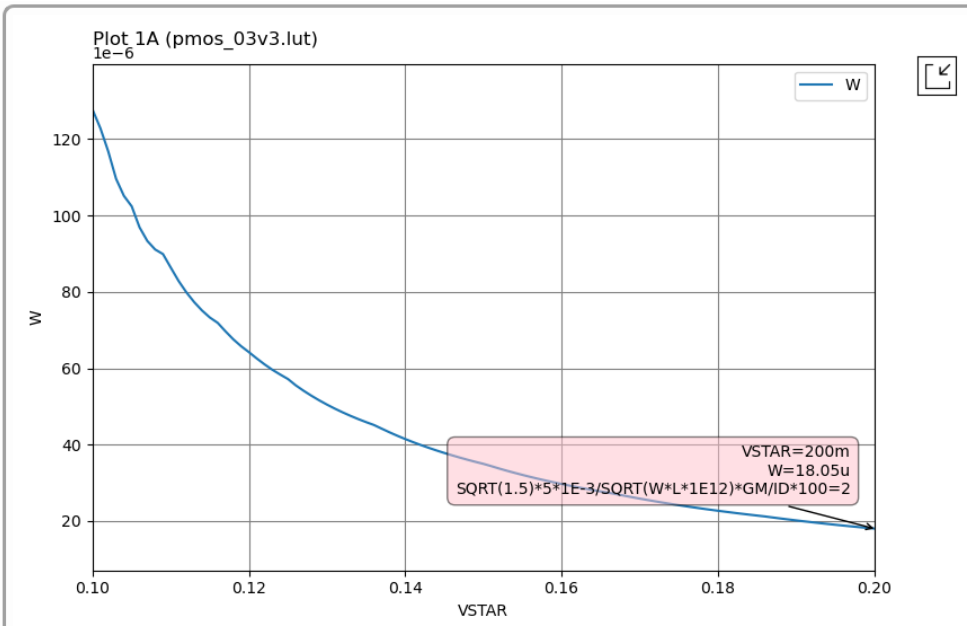
VICM=0.5607V

Tail Current Mirror Design

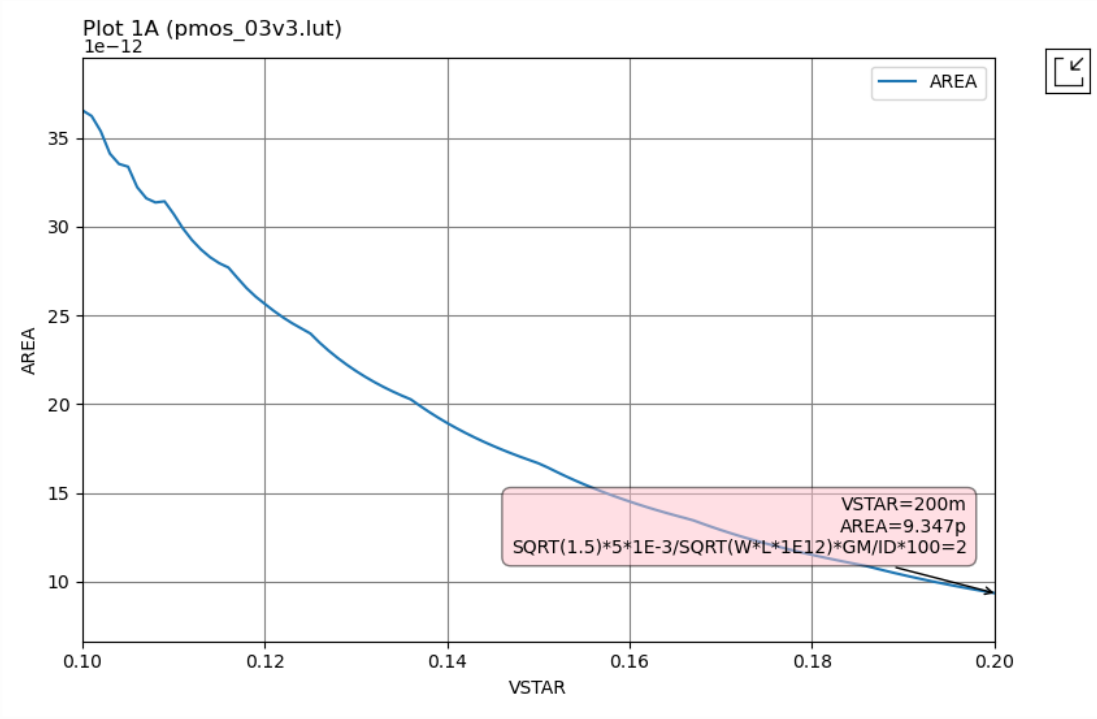




L=518nm



W=18.05um



Given the compliance voltage spec, report the above figure with a cursor added to the selected design point. At V*=200m

Calculate the min and max CM input levels. Is the previously selected CM input level in the valid range?

Maximum CM Input Level:

$$V_{\text{ICM,max}} \leq V_{\text{DD}} + V_{\text{GS,input}} - |V_{\text{DSAT,M1}}|$$

$$V_{\text{ICM,max}} \leq 1.8\ \text{V} - 0.939\ \text{V} - 0.166\ \text{V} = \boxed{0.695\ \text{V}}$$

Minimum CM Input Level:

$$V_{\text{ICM,min}} \geq V_{\text{out,CM}} - |V_{\text{TH,input}}|$$

$$V_{\text{ICM,min}} \geq 0.6\ \text{V} - 1.003\ \text{V} = \boxed{-0.403\ \text{V}}$$

Part 2: Differential Amplifier Simulation

Schematic:

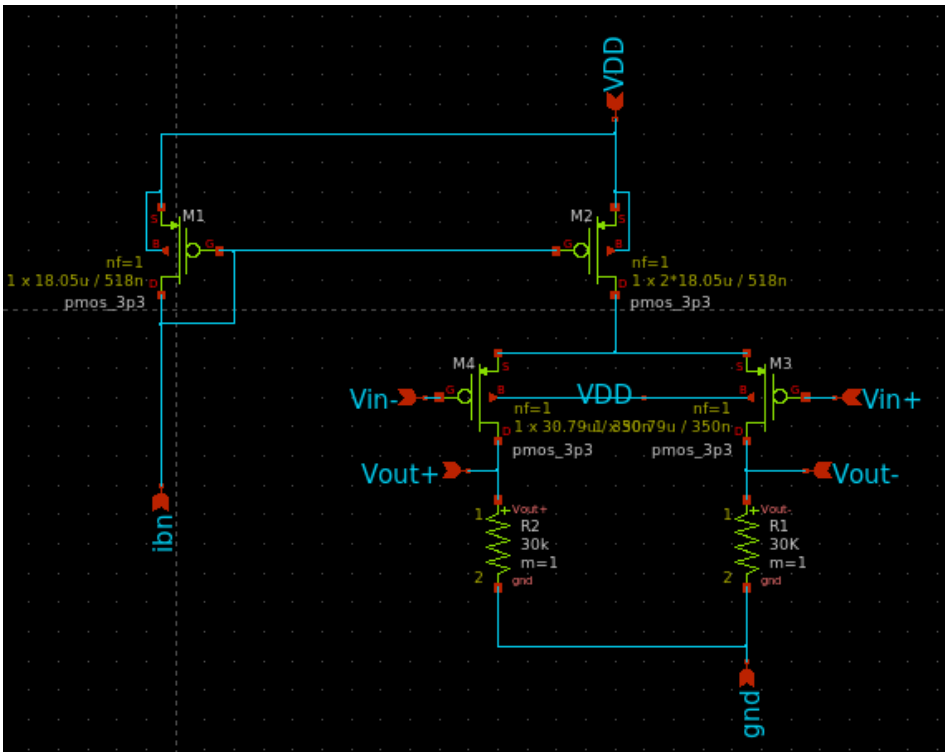


Figure 1: Schematic for differential amplifier

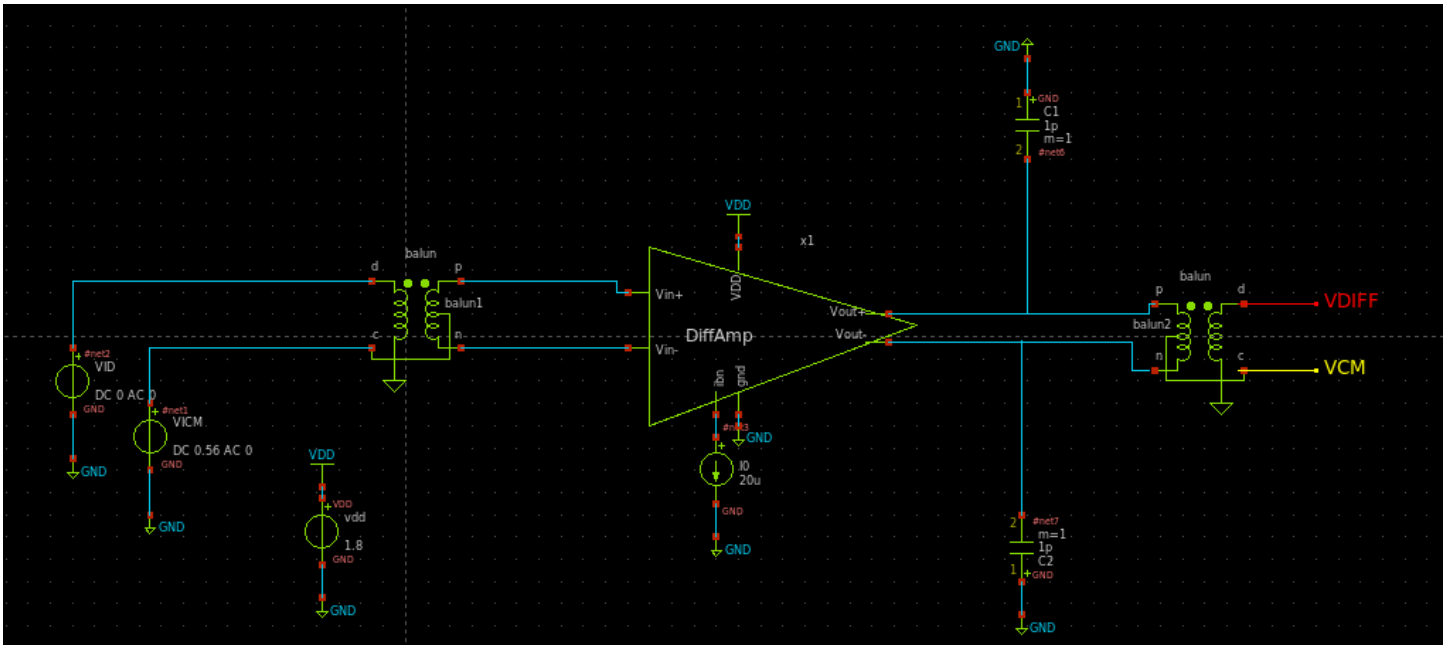


Figure 2 : The simulation schematic for the DiffAmp, including baluns for applying input signals.

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm1.m0           m.x1.xm2.m0           m.x1.xm4.m0
     model           pmos_3p3.13           pmos_3p3.13           pmos_3p3.12
        id                  2e-05              3.81e-05              1.905e-05
        gm           0.000205292           0.000390097           0.000282253
       gds           1.01521e-06           5.76949e-06           3.06862e-06
       vgs              0.939579              0.939579              0.937923
       vth              0.788987              0.789459              0.874705
       vds              0.939578              0.302073              0.926423
     vdsat              0.166155              0.165805              0.116907

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm3.m0
     model           pmos_3p3.12
        id             1.905e-05
        gm           0.000282253
       gds           3.06862e-06
       vgs              0.937923
       vth              0.874705
       vds              0.926423
     vdsat              0.116907
```

Figure 3 : OP Annotation

all transistors operate in saturation. For all Vds>Vdsat

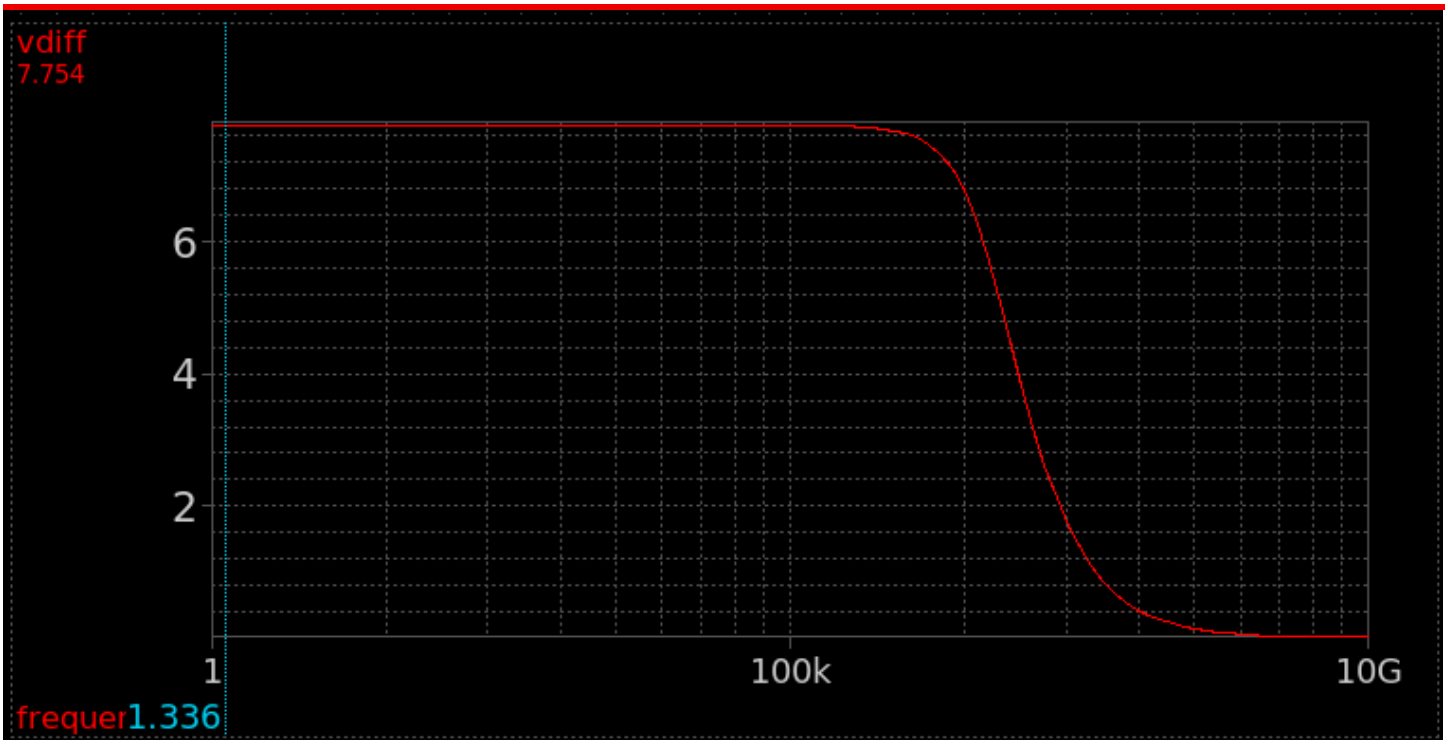


Figure 4 : Bode plot of the differential gain (Avd) versus frequency.

```
gain                =   7.753683e+00 at=  1.000000e+00
bw                  =   5.673421e+06
```

Figure 5 : gain & BW from simulation

Analytical :

Avd = gm3*(ro3//Rd) = 7.75

Bw = 1/(Rout CL) = 1/(ro3//Rd * Cl*2π) = 5.79MHZ

	Simulation	**Analytical**
Gain	**7.75**	**7.75**
Bw(MHz)	**5.67**	**5.79**

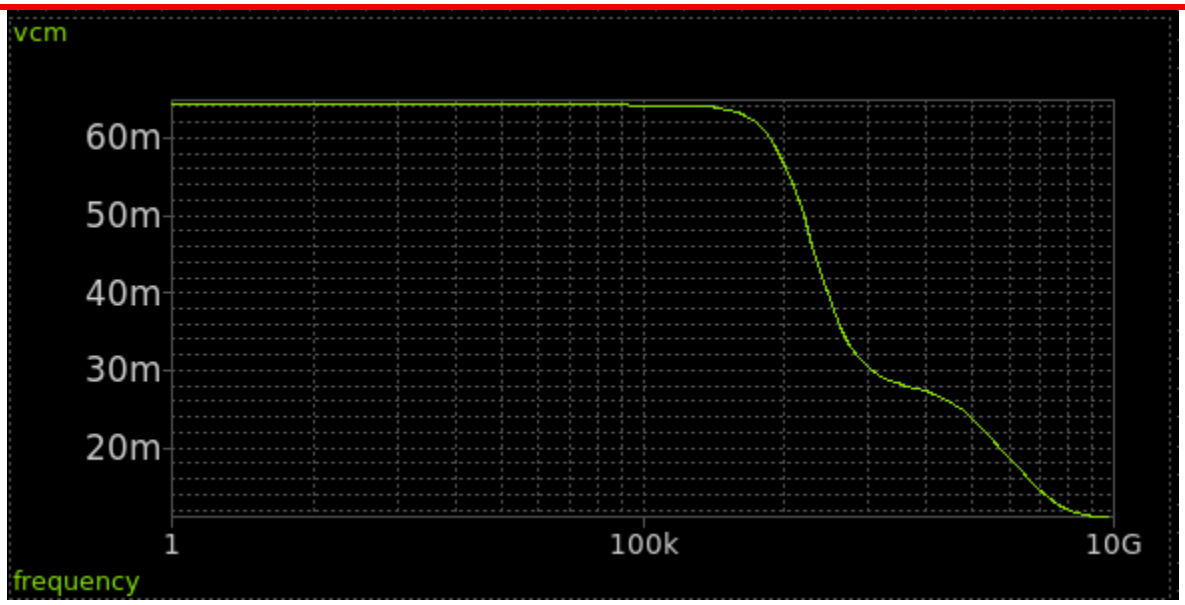


Figure 6 : Bode plot of the common-mode gain (Avcm) versus frequency.

```
No. of Data Rows : 101
cmgain                =  6.424468e-02 at=  1.000000e+00
```

Figure 7 : : CM gain from simulation

Analytical :

Acm = gm3*Rout/(1+2*gm3*Rss)

Rout = ro3//Rd , Rss= ro2

Acm = 0.075

	Simulation	**Analytical**
CMGain	**0.064**	**0.075**

Acm Is it smaller than "1"? Why?

because the high output resistance of the tail current source provides strong common-mode rejection, reducing Acm below 1.

Justify the variation of Avcm vs frequency

As frequency increases, the tail current source's impedance decreases due to parasitic capacitance, reducing common-mode rejection and causing CMGain to rise.

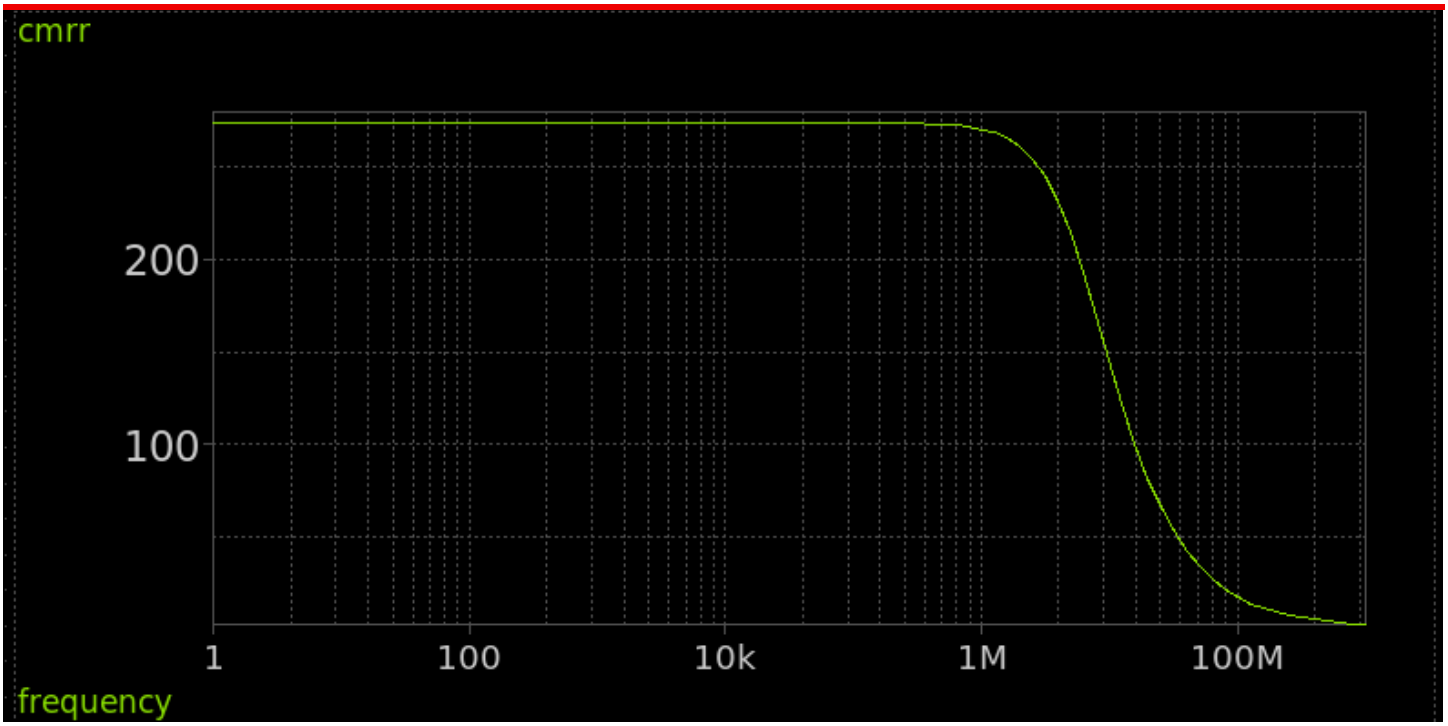


Figure 8 : Plot of the Common-Mode Rejection Ratio (CMRR) in dB versus frequency.

```
No. of Data Rows : 91
cmgain                =  6.424472e-02 at=  1.000000e+00
to=1meg: no such command available in ngspice
diffgain              =  7.753683e+00 at=  1.000000e+00
to=1meg: no such command available in ngspice
cmrr_val = 1.206898e+02
```

Figure 9 : CM & Diff gain & CMRR from simulation

Analytical :

Avd = gm3*(ro3//Rd) = 7.75

Avcm = gm3*Rout/(1+2*gm3*Rss) = 0.075

CMRR = Avd /Avcm = 100

	Simulation	**Analytical**
CMRR	**120**	**103.3**

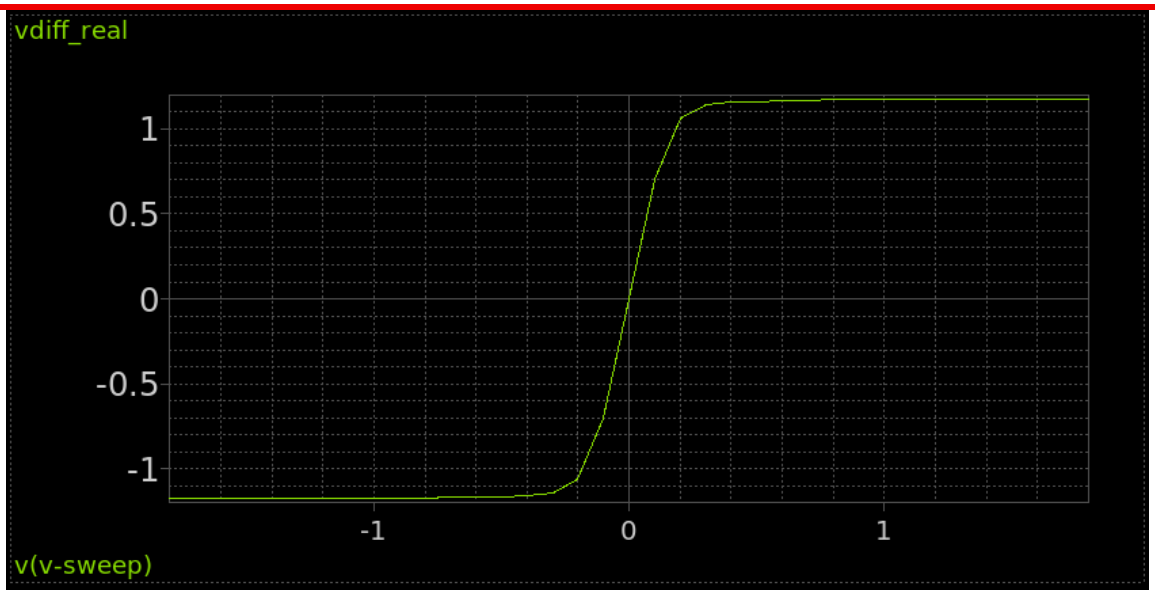


Figure 10 : The large-signal transfer curve of differential output vs. differential input.

Analytical :

Maximum Differential Output Voltage (VODIFF_max):

VODIFF_max = (ISS×RD)−0V= (40μA×30kΩ)−0V = 1.2V

Minimum Differential Output Voltage (VODIFF_min):

Vout− = VDD = 1.8 V

Vout+ = VDD − (ISS × RD) = 0.6 V

VODIFF_min = Vout+ − Vout− = 0.6 − 1.8 = −1.2 V

Parameter	Hand Analysis Value	Simulation Value
Maximum Differential Output (VODIFF,max)	1.2 V	1.176
Minimum Differential Output (VODIFF,min)	-1.2 V	-1.176

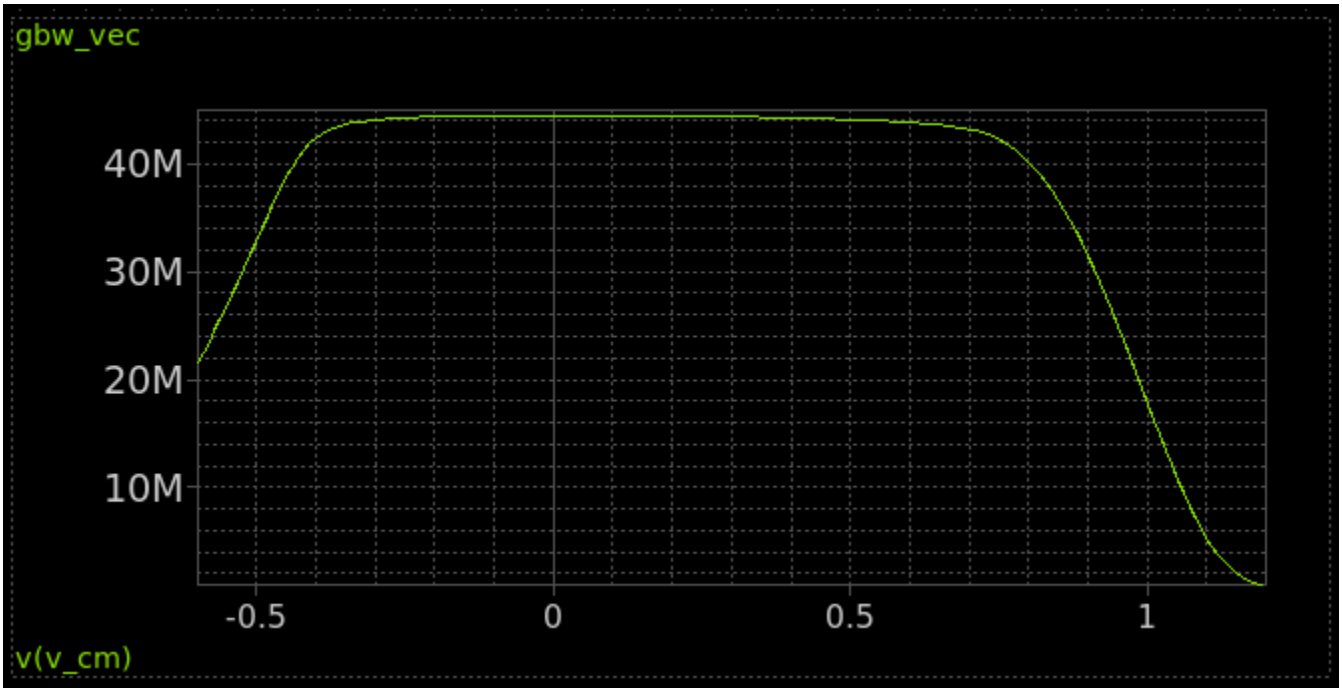


Figure 11 : Plot of the Gain-Bandwidth Product (GBW) vs. the common-mode input voltage (VICM).

```
vcm_min = -4.30000e-01
vcm_max = 8.100000e-01
```

Parameter	Hand Analysis Value	Simulation Value
Maximum CM Input Level	0.695 V	0.81 V
Minimum CM Input Level	-0.403 V	-0.43 V