CMOS Analog IC Design

Lab 1

LPF Simulation and MOSFET Characteristics

Supervised by: Dr. Hesham Omran

PART 1: Low Pass Filter Simulation (LPF)

Schematic :

Design a first order low pass filter that has R = 1$k\Omega$ and 1ns time constant .

T=RC then C=1pf

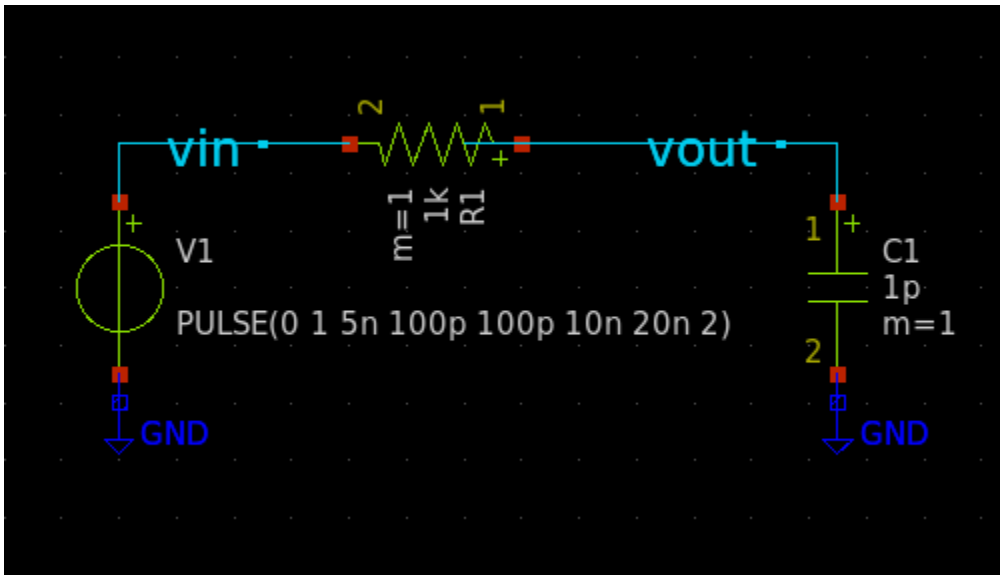

Figure 1 : first order low pass filter

Transient Analysis :

Report transient analysis results for two periods

Code:

```
.control
save all
tran 100p 40n
write rc_ckt.raw
.endc
```

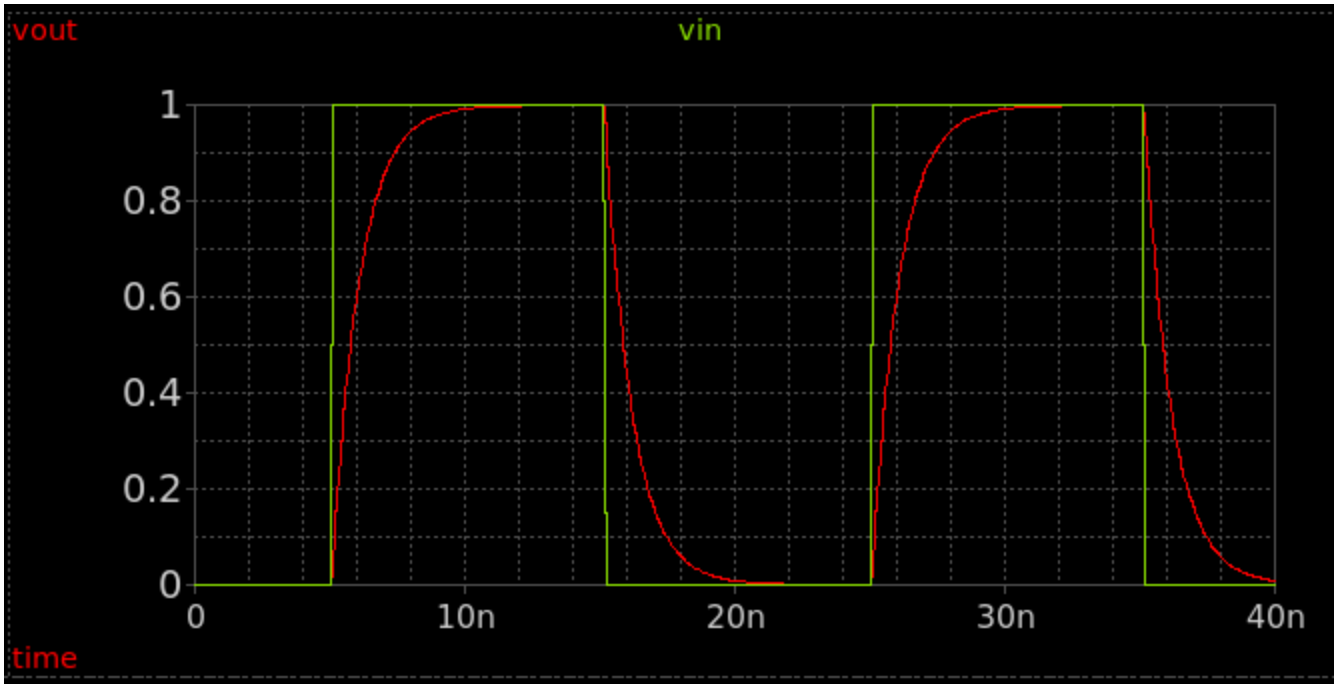

Figure 2 : Vin Vs Voot

Calculate rise and fall time (10% to 90%) using measure command. Export the results to an output text file.

Code:

```
"
.tran 100p 40n
.control
run
meas tran t_rise TRIG v(vout) VAL=0.1 RISE=1 TARG v(vout) VAL=0.9 RISE=1
meas tran t_fall TRIG v(vout) VAL=0.9 FALL=1 TARG v(vout) VAL=0.1 FALL=1
print t_rise > tran_result.txt
print t_fall >> tran_result.txt
.endc
.end
"
```

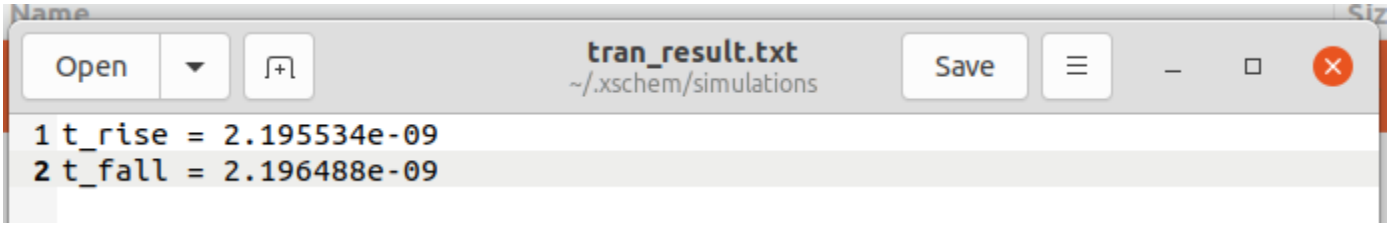

Figure 3 : T Rise & Fall From the text file

Derive an analytical expression for the rise and fall times as a function of the RC time constant. Compare simulation with analytical results in a table.

Analysis :

Capacitor Calculation:

C = $\frac{Time\ Constant}{R}$

C = $\frac{(1 * 10^{-9})}{1000} = 1\ \text{pF}$

Rise/Fall Time (10%-90%) Calculation:

t_rise = t_fall = ln(9) * Time Constant

t_rise = t_fall = 2.197 * 1 ns

t_rise = t_fall = 2.197ns

	Simulation	Analytical
Rise Time (ns)	**2.195**	**2.197**
Fall Time (ns)	**2.196**	**2.197**

Do parametric sweep for R = 1:1:5$k\Omega$

Code:

```
.control
save all
let R_val = 1000
let R_stop = 5000
let R_step = 1000
while R_val le R_stop
alter R1 R_val
tran 100p 40n
meas tran t_rise TRIG v(vout) VAL=0.1 RISE=1 TARG v(vout) VAL=0.9 RISE=1
meas tran t_fall TRIG v(vout) VAL=0.9 FALL=1 TARG v(vout) VAL=0.1 FALL=1
print R_val t_rise >> tran_result.txt
print R_val t_fall >> tran_result.txt
write rc_ckt.raw
set appendwrite
let R_val = R_val + R_step
end
.endc
```

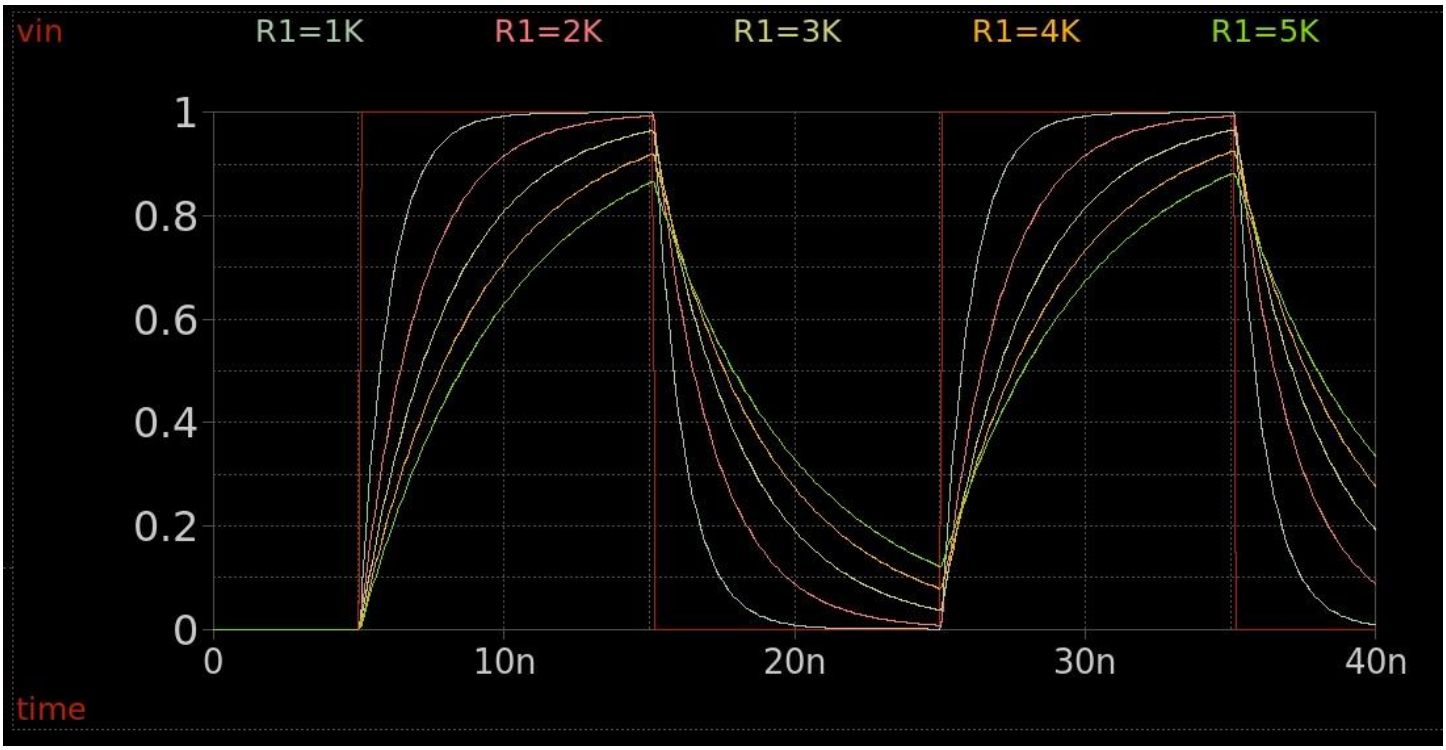

Figure 4 : Overlaid transient response from the parametric sweep for R = 1kΩ to 5kΩ

Comment :

- As the resistance R increases from 1 kΩ to 5 kΩ, the theoretical time constant τ increases proportionally from 1 ns to 5 ns.
- The simulated rise time and fall time also increase approximately linearly, maintaining the same trend.

AC Analysis :

Schematic :

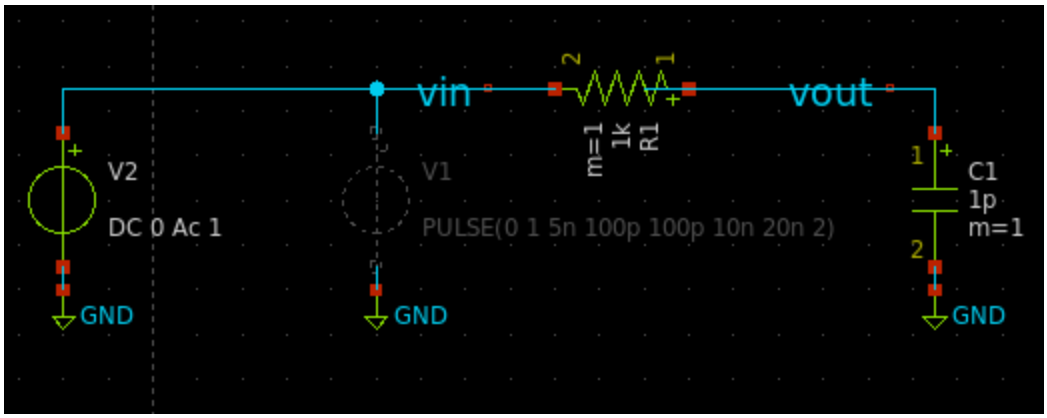

Figure 5 : Modify your testbench to perform ac analysis

Bode Plot (magnitude and phase) for the LPF

Code:

```
.control
save all
ac dec 10 1 10g
write rc_ckt.raw
meas ac MAX_GAIN MAX vmag(vout) FROM=1 TO=10G
meas ac BW WHEN vmag(vout)=0.707 FALL=1
print MAX_GAIN BW >> ac_result.txt
.endc
```

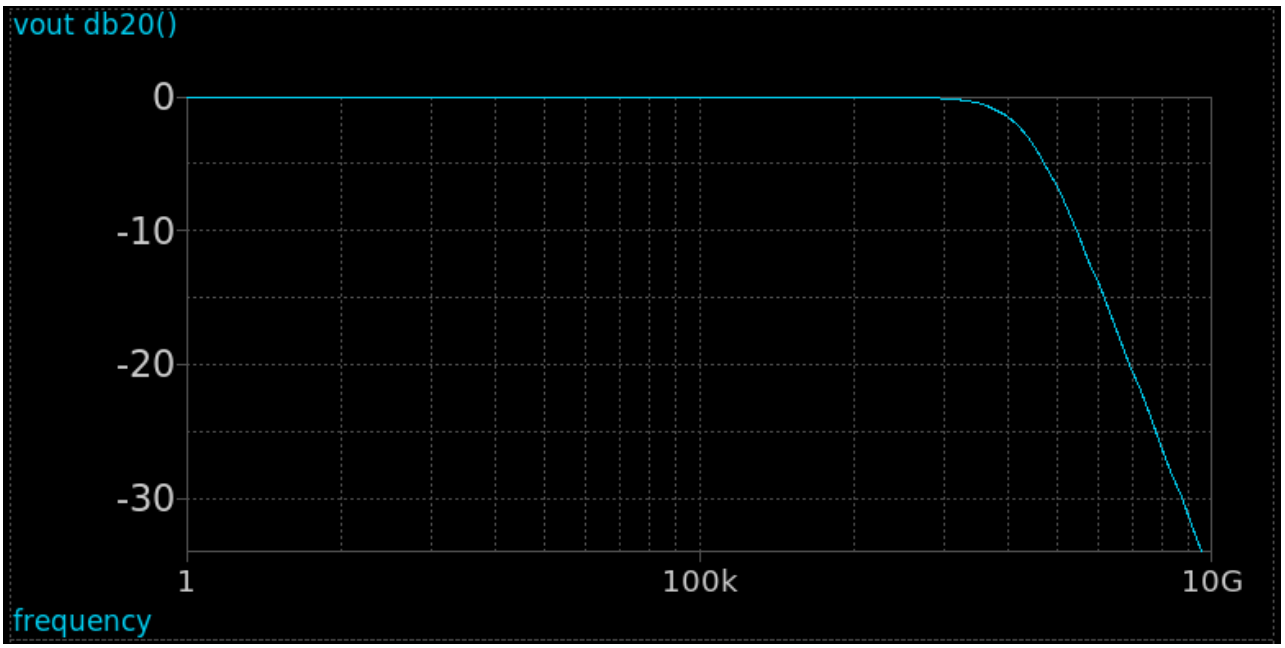

Figure 6 : Bode Plot magnitude for LPF

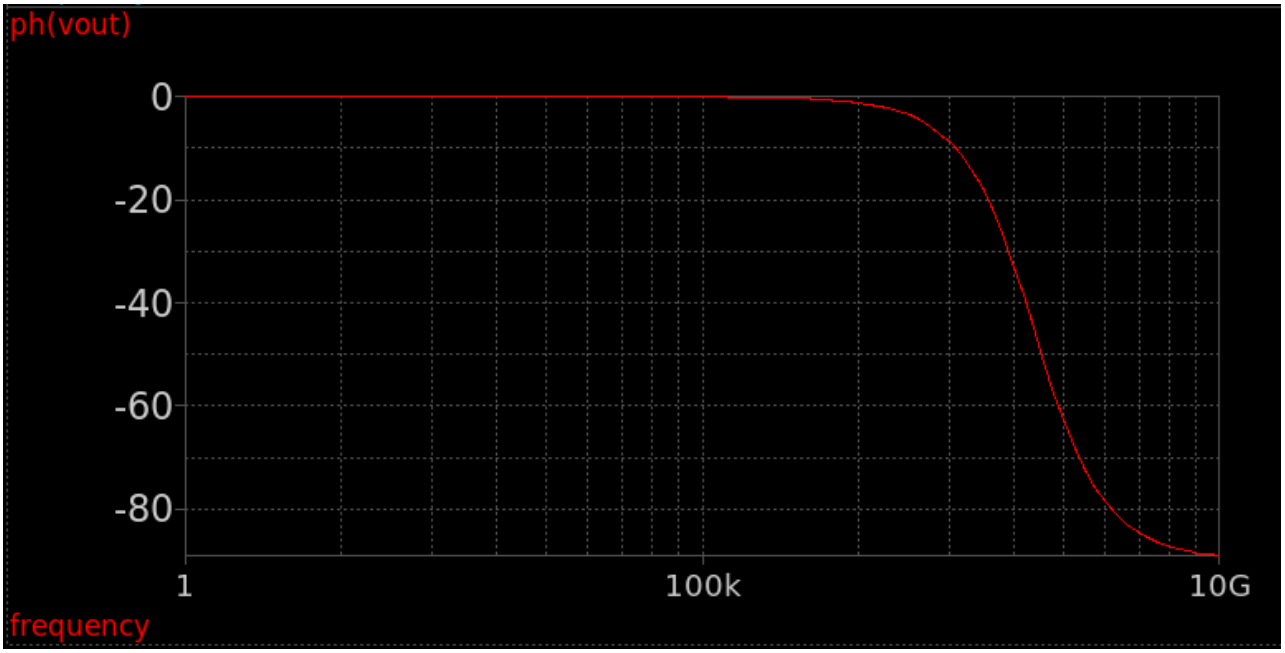

Figure 7 : Bode Plot phase for LPF

Calculating DC gain and 3dB bandwidth and Export the results form text file .

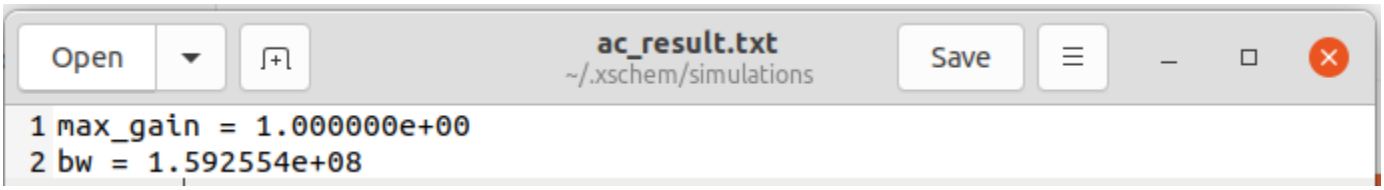

Figure 8 : DC gain and 3dB bandwidth from text file

Derive an analytical expression (equation) for the bandwidth. Compare simulation with analytical results in a table.

Analysis :

$\mathrm{BW} = f_{3dB} = \frac{1}{(2\pi RC)}$

	Simulation	Analytical
DC Gain (dB)	**0**	**0**
3dB Bandwidth (MHz)	**159.25**	**159.15**

Do parametric sweep for R = 1,10,100,1000$k\Omega$. Report overlaid results. Comment on the results

Code:

```
.control

save all
let R_val = 1k
let R_stop = 1meg
let R_mult = 10
while R_val le R_stop
alter R1 R_val
ac dec 10 1 10g
write rc_ckt.raw
set appendwrite
meas ac MAX_GAIN MAX vmag(vout) FROM=1 TO=10G
meas ac BW WHEN vmag(vout)=0.707 FALL=1
print R_val MAX_GAIN BW >> ac_result.txt
let R_val = R_val * R_mult
end
.endc
```

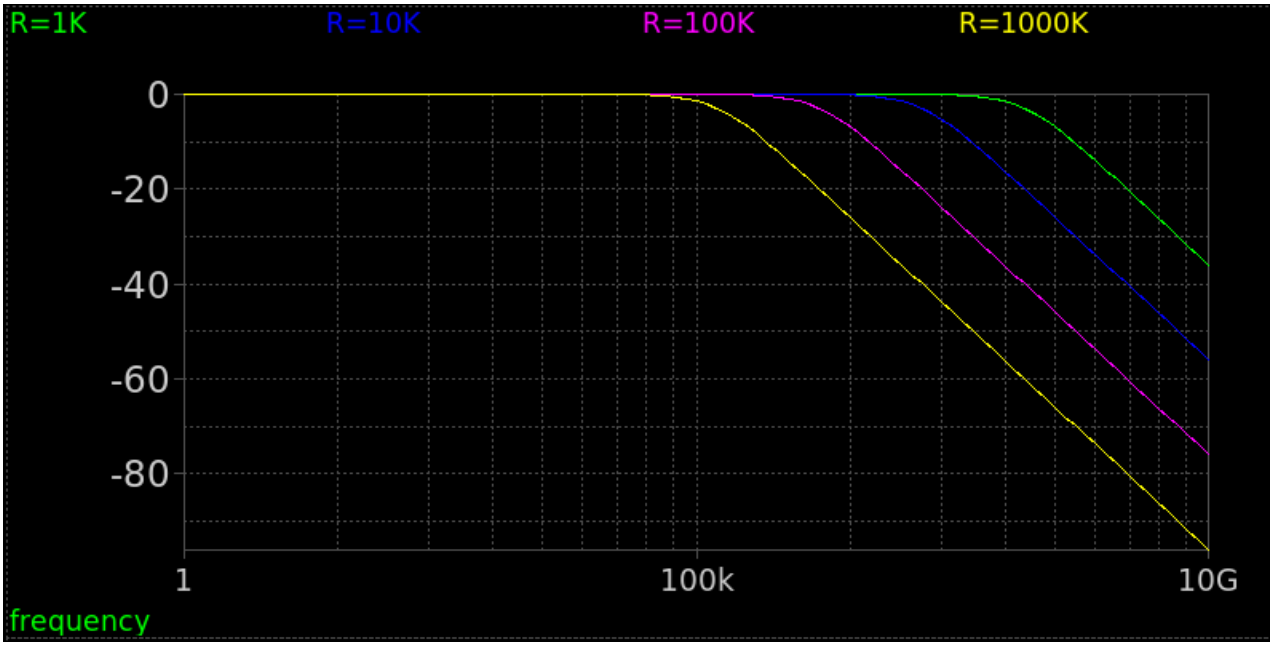

Figure 9 : Bode plot of the LPF showing the effect of sweeping the resistance

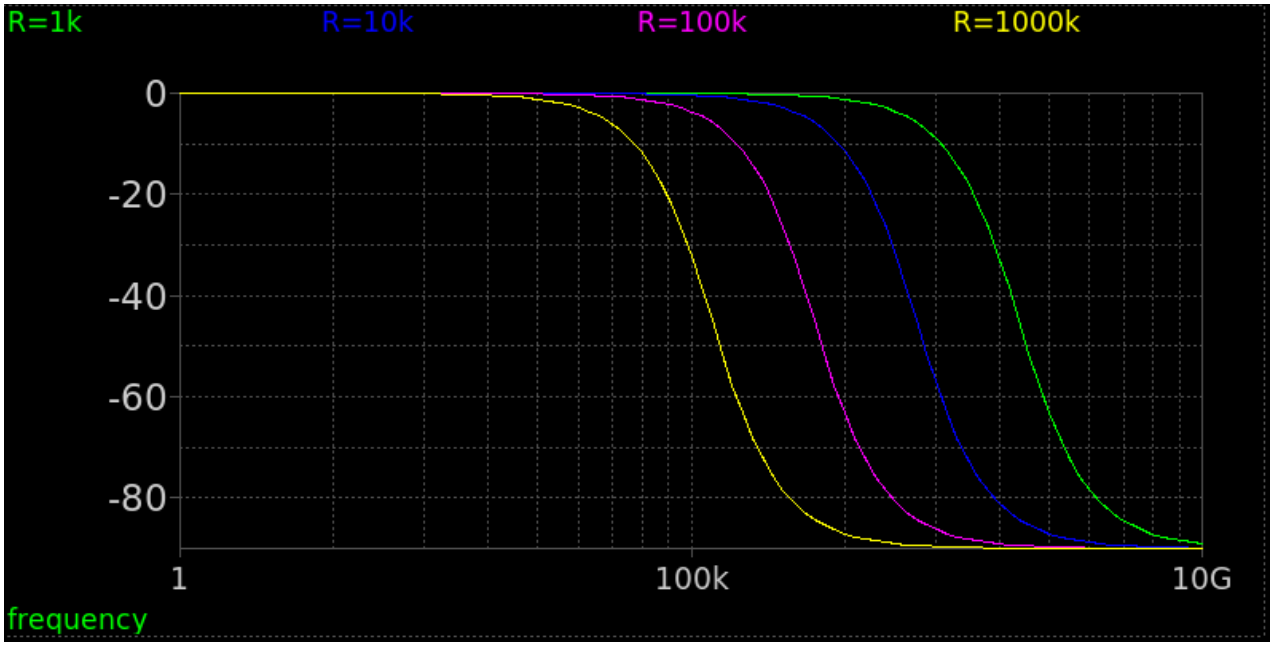

Figure 10 : phase of LPF showing the effect of sweeping the resistance

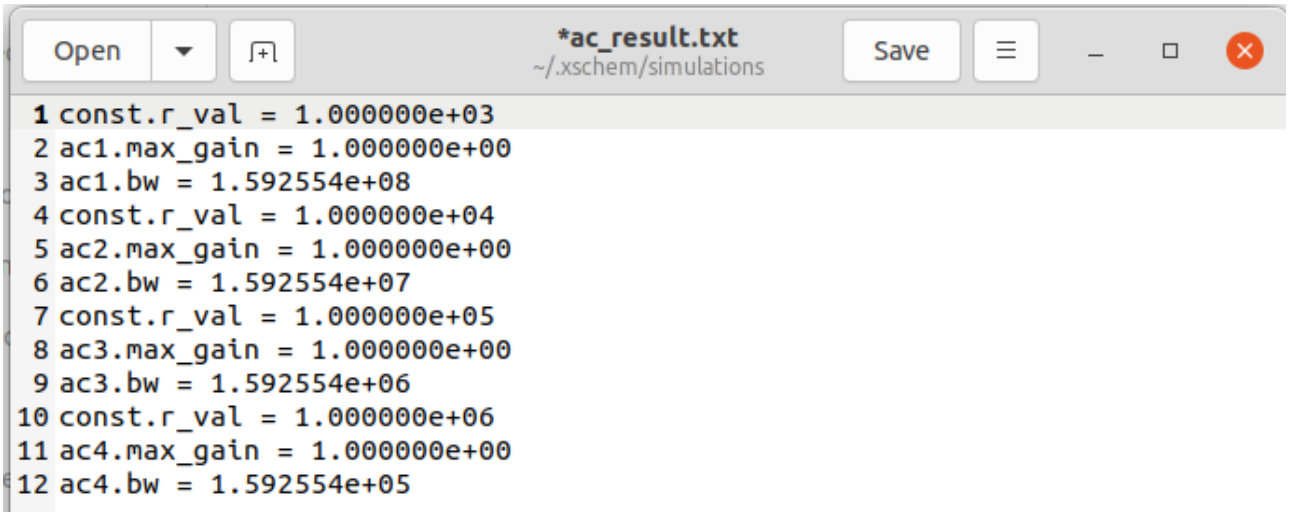

Figure 11 : Sweep Results: Resistance vs DC Gain & Bandwidth (from text file)

Comment :

- As the resistance **R** increases, the filter's **cutoff frequency decreases**, meaning it starts blocking signals at lower frequencies.
- This relationship is inversely proportional: the data shows that when the resistance increases by a factor of 10, the bandwidth decreases by the same factor, while the passband gain remains constant at 0 dB.

PART 2: MOSFET Characteristics

Schematic :

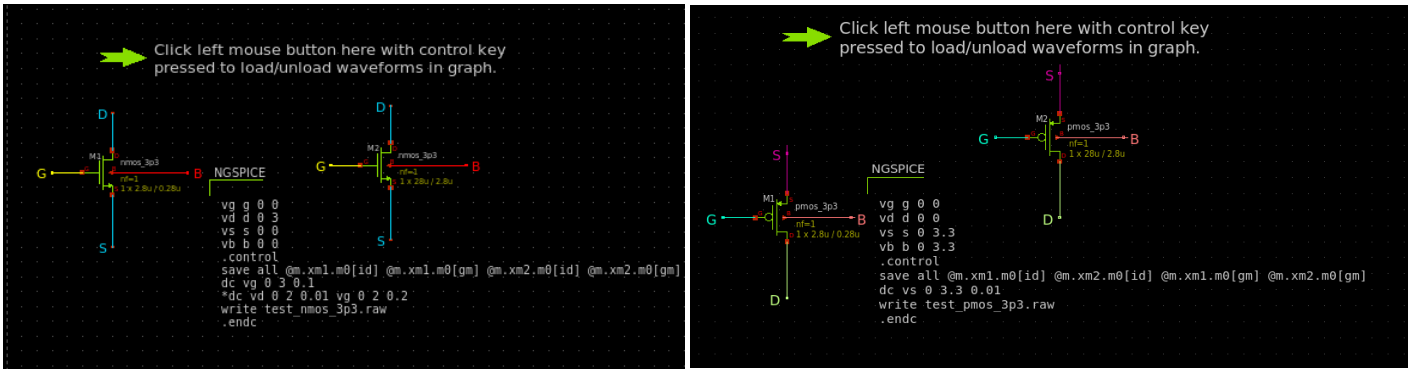

Figure 12 : Schematic & Code for NMOS and PMOS

For Short channel : W = 2.8u & L = 280n
For Long channel : W = 28u & L = 2.8u
Aspect ratio W/L = 10 in both

$ID - VGS$ characteristics for NMOS device :

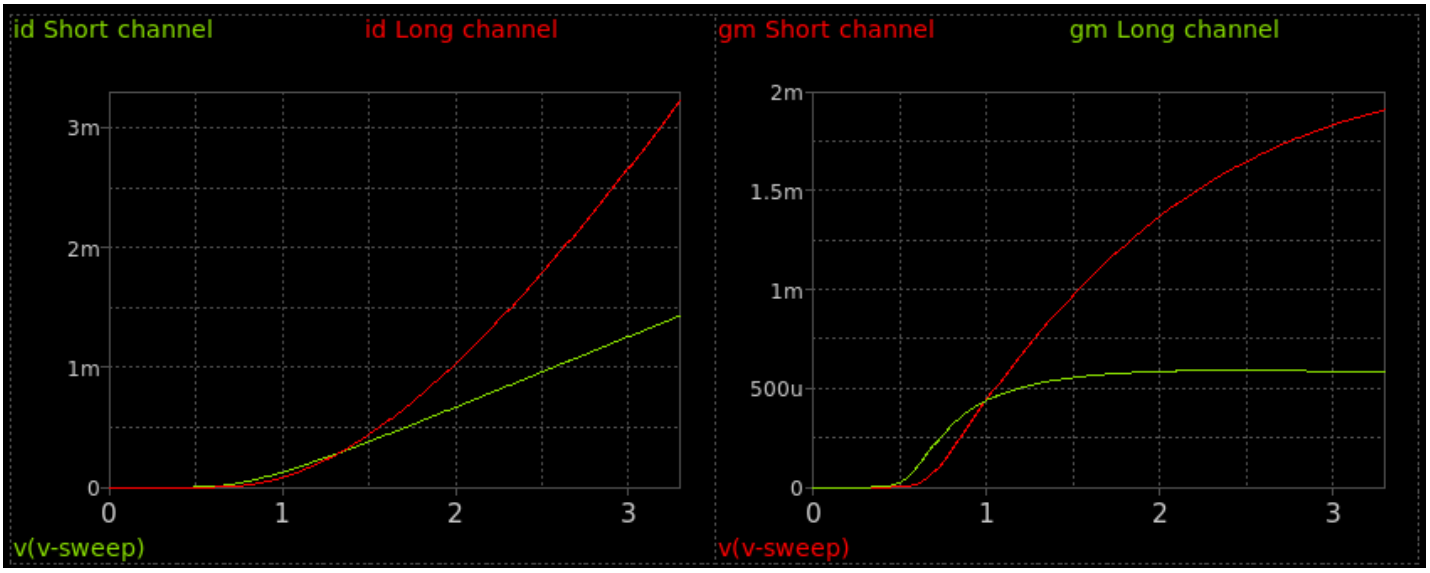

Figure 13 : NMOS ID vs VGS & gm vs VGS for short and long channel.

$ID - VGS$ characteristics for PMOS device :

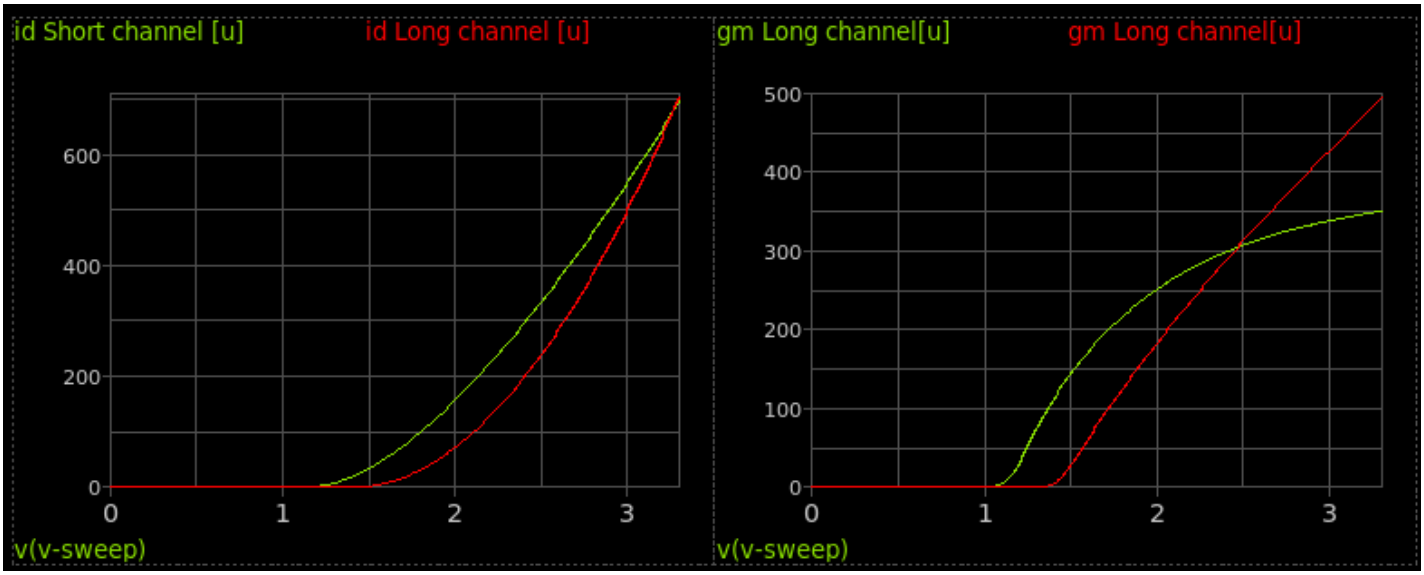

Figure 14 : PMOS ID vs VGS & gm vs VGS for short and long channel.

Comment on the differences between short channel and long channel results.

- Which one has higher current? Why?

In Nmos Long channel have a higher current and **in Pmos Short channel have a higher current** why ?
For NMOS, short-channel devices show lower current despite shorter L due to velocity saturation and mobility degradation. Long-channel follows the quadratic square-law, while short-channel exhibits a linear relation as secondary effects dominate .
For PMOS, short-channel devices have higher current despite velocity saturation and mobility degradation, because the reduced channel length dominates and short-channel effects are less severe compared to NMOS**.**

- Is the relation linear or quadratic? Why?

For **long-channel**, the relation is **quadratic** due to the square-law behavior of MOSFETs in saturation. For **short-channel**, it becomes **more linear** because high electric fields cause velocity saturation, breaking the square-law dependence.

ID for NMOS & PMOS devices at VGS = VDD

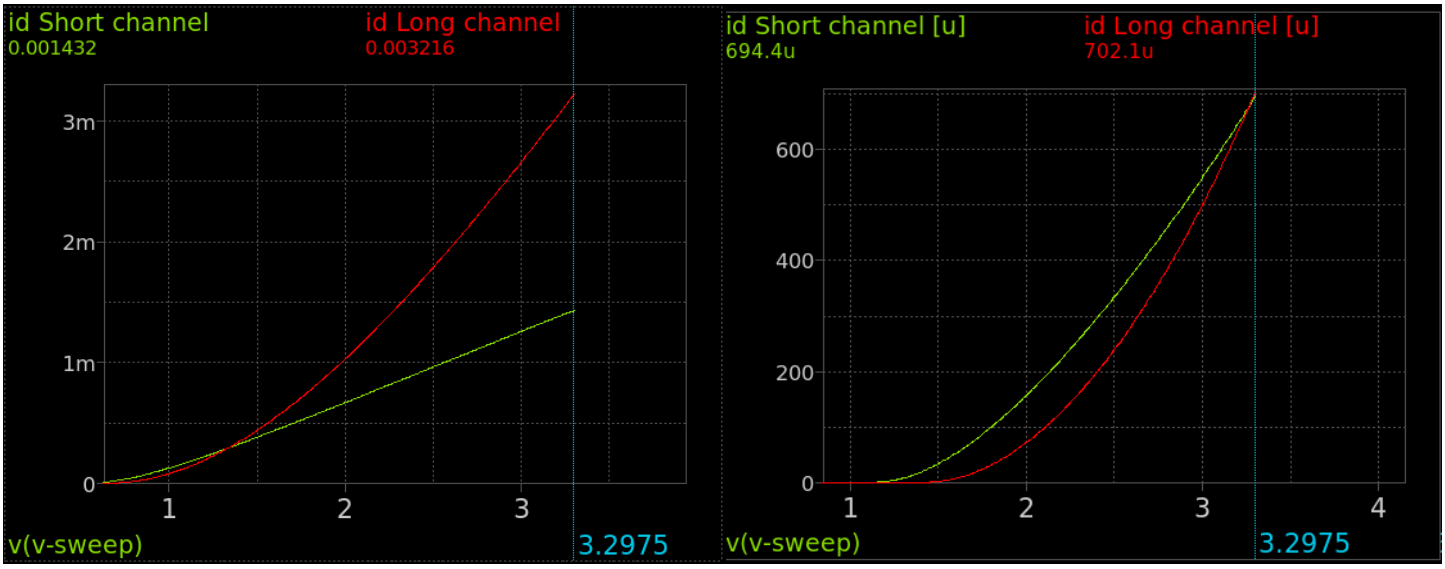

Figure 15 : ID For NMOS & PMOS at VGS = VDD

For NMOS :

Id Short channel = 1.432 mA
Id Long channel = 3.216 mA
For PMOS :
Id Short channel = 0.6944 mA
Id Long channel = 0.7021 mA

Comment on the differences between NMOS and PMOS.

- Which one has higher current? Why?

The NMOS transistor has a higher current. This is because the mobility of its charge carriers (electrons, μn) is significantly higher than the mobility of the PMOS charge carriers (holes, μp).

- What is the ratio between NMOS and PMOS currents at VGS = VDD?

For Short channel: Id NMOS/Id PMOS = 4.6

For Long channel: Id NMOS/Id PMOS = 2.1

- Which one is more affected by short channel effects?

NMOS is more affected by short-channel effects than PMOS because electrons have higher mobility, making NMOS more prone to velocity saturation and mobility degradation.

gm vs VGS using ADT :

For Short channel : W = 2.8u & L = 280n
For Long channel : W = 28u & L = 2.8u
Aspect ratio W/L = 10 in both

For NMOS device : VDS = VDD = 3.3V & VGS = 0 : 3.3 & VSB = 0

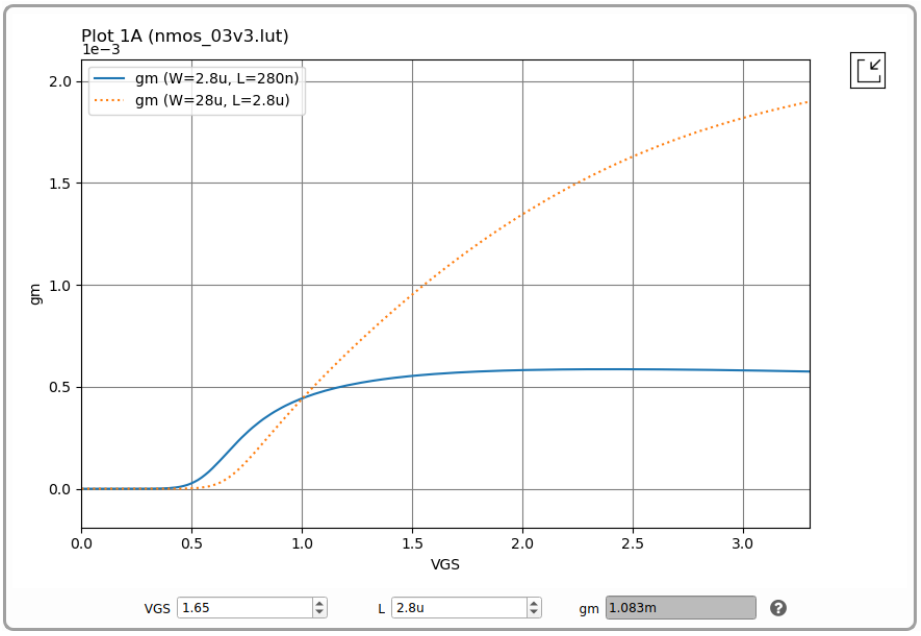

Figure 16 : gm vs Vgs in ADT

Comment on the differences between short channel and long channel results.

- Does gm increase linearly? Why?

No, not perfectly. For the long-channel device, the increase is close to linear. For the short-channel device, the gm begins to saturate at higher VGS values. This is because gm is the slope of the ID-VGS curve, and effects like velocity saturation limit the current increase in short-channel devices.

- Does gm saturate? Why?

Yes, the gm of the short-channel device clearly saturates. This is a direct result of velocity saturation. When the charge carriers reach their maximum possible velocity, increasing VGS further does not yield a proportional increase in current. As a result, the transconductance flattens out.

ID vs VDS (use ADT)

For NMOS device : VDS = 0:3.3 & VGS = 1:1:3 & VSB = 0

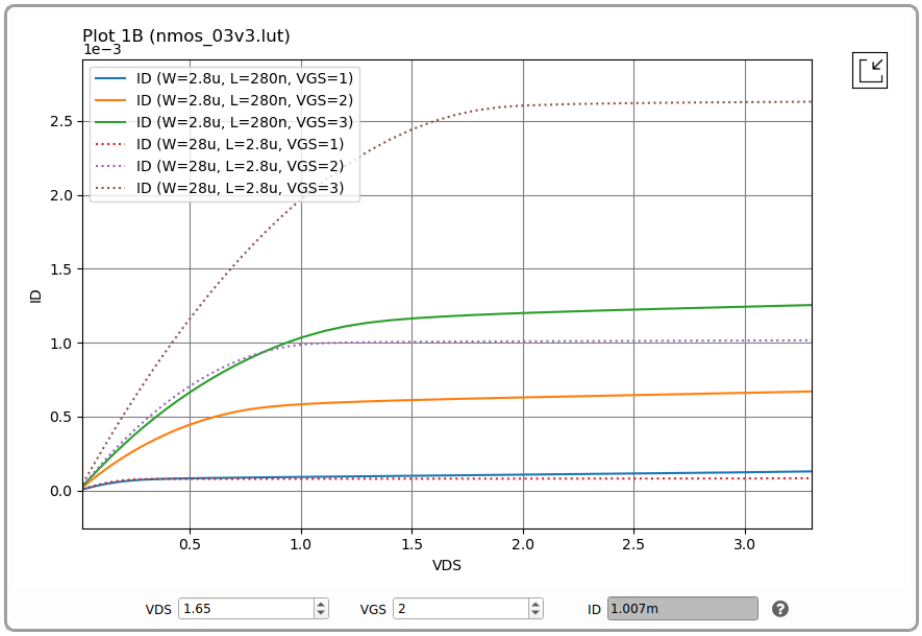

Figure 17 : ID VS VDS in ADT

Comment on the differences between short channel and long channel results.

- Which one has higher current? Why?

In Nmos Long channel has a higher current because short-channel devices show lower current despite shorter L due to velocity saturation and mobility degradation. Long-channel follows the quadratic square-law, while short-channel exhibits a linear relation as secondary effects dominate

- Which one has higher slope in the saturation region? Why?

Short-channel devices have a **higher slope** in the saturation region because they have a **lower output resistance ro** due to stronger **channel length modulation** and **DIBL**, which degrade current saturation.

gm and ro in Triode and Saturation (use ADT)

For NMOS device : VDS = 0:3.3 & VGS = Vth+0.5 & VSB = 0

And Vth = 662mV from ADT then VGS = 1.162 V

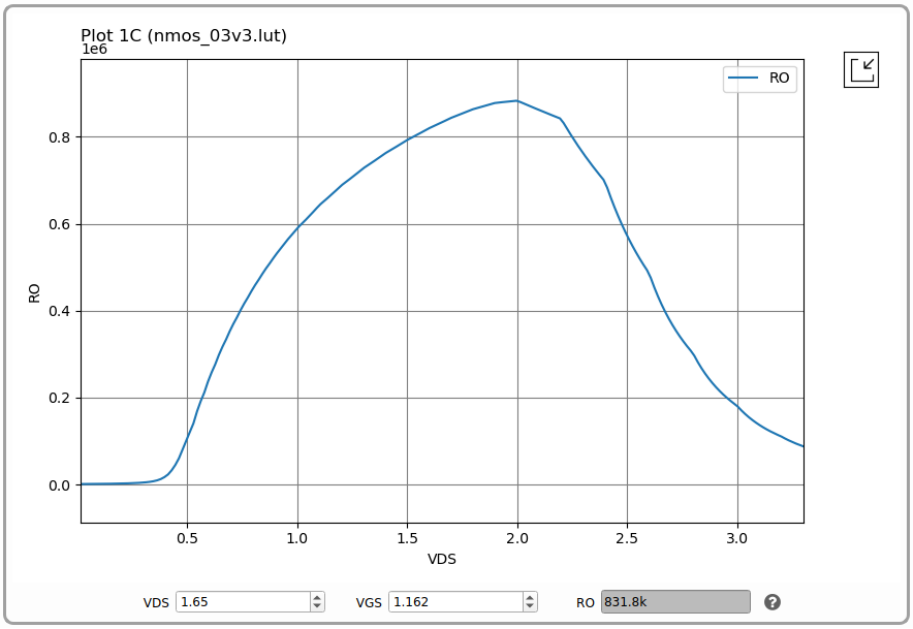

Figure 18 : ro VS VDS in ADT

Comment

- In **short-channel MOSFETs**, as **VDS increases into deep saturation**, **DIBL (Drain-Induced Barrier Lowering)** reduces the **threshold voltage VTH**, causing the **drain current** to rise more sharply. This increases the **slope of the ID VS VDS curve**, thereby reducing the **output resistance (ro)**. So while **ro initially increases** in saturation, it **eventually decreases at high VDS due to DIBL**.

Gm VS VDS

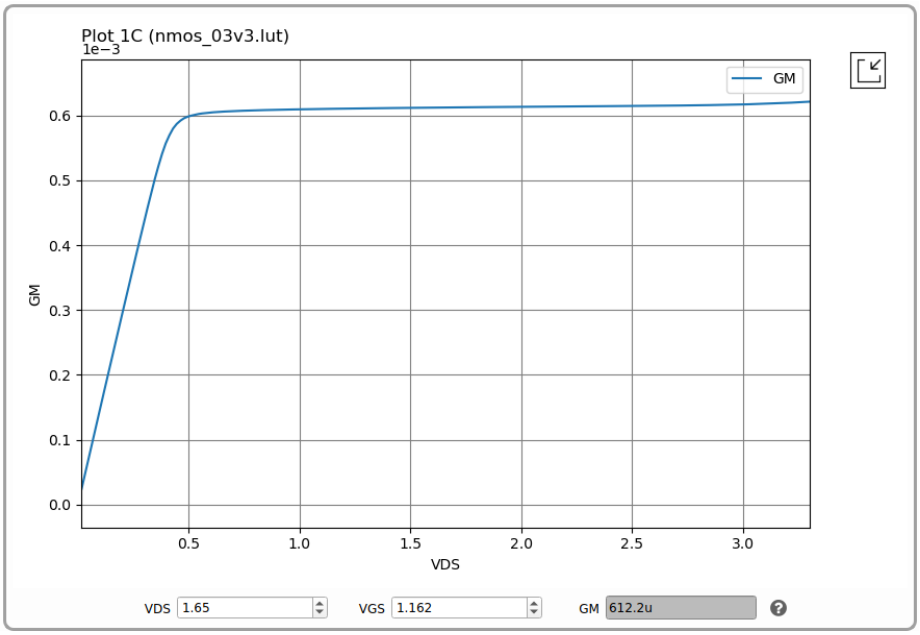

Figure 19 : Gm VS VDS in ADT

Comment

- gm increases **linearly** in the **triode region** and becomes **constant** in **saturation**. This indicates that the **saturation region** provides a **stable** and **high transconductance**, which is **essential for analog amplifier design**