CMOS Analog IC Design

Lab 4

Common Drain Frequency Response

Supervised by: Dr. Hesham Omran

Part 1: Device Sizing Using SA

We used ADT's Sizing Assistant to determine the required PMOS width (W) by setting gm/ID = 10 and selecting L = 1u. The tool estimated W to achieve V* = 200 mV, ensuring good speed-power trade-off and saturation operation.

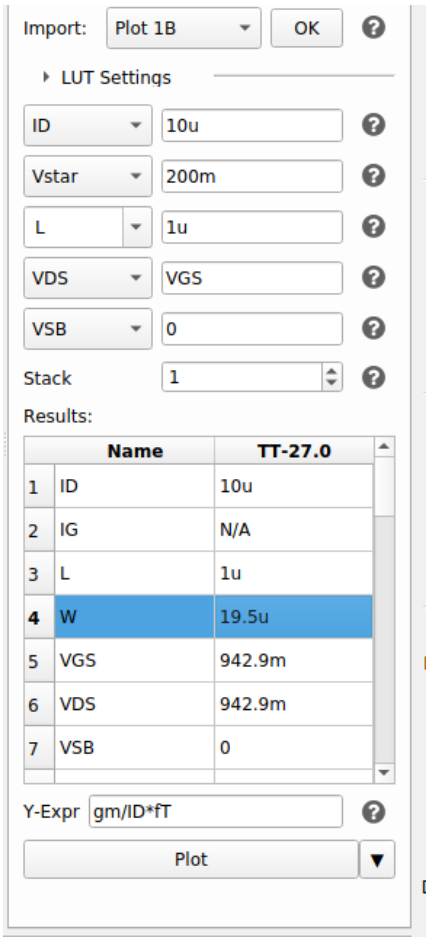

Figure 1 : Screenshot from the Sizing Assistant tool showing the chosen gm/ID, L, and the extracted W for the PMOS transistor (V = 200 mV).*

Then W=19.5 um

Part 2 : CD Amplifier

The CD amplifier was built in Xschem using the sized PMOS and a current source of 10 µA. We then verified the transistor is in saturation by checking OP results like VDS > VDSAT and gm > 0.

Schematic :

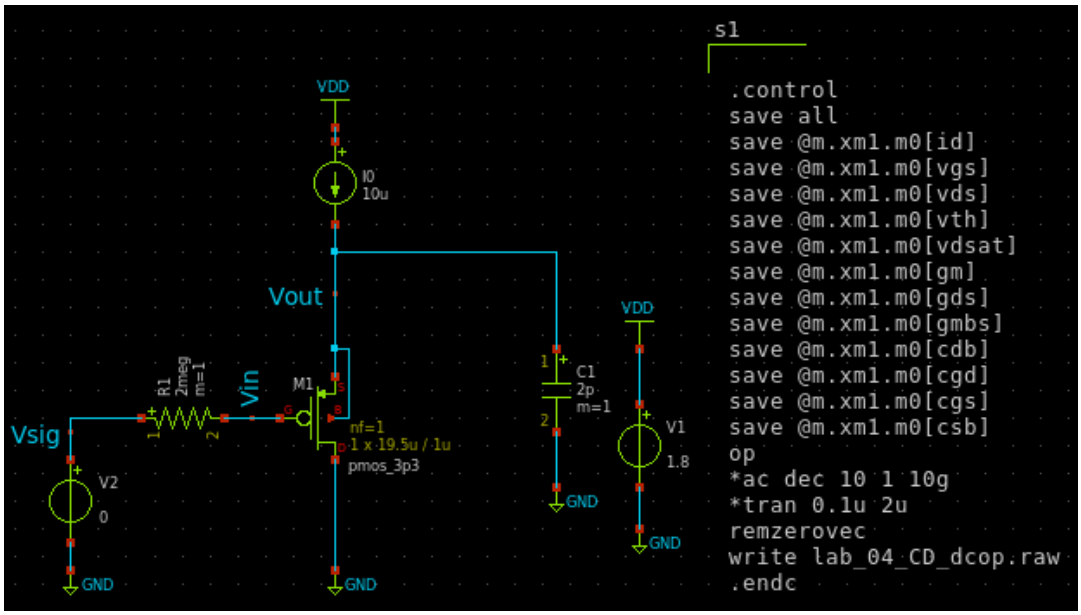

Figure 2 : Common-Drain (CD) amplifier schematic using PMOS input

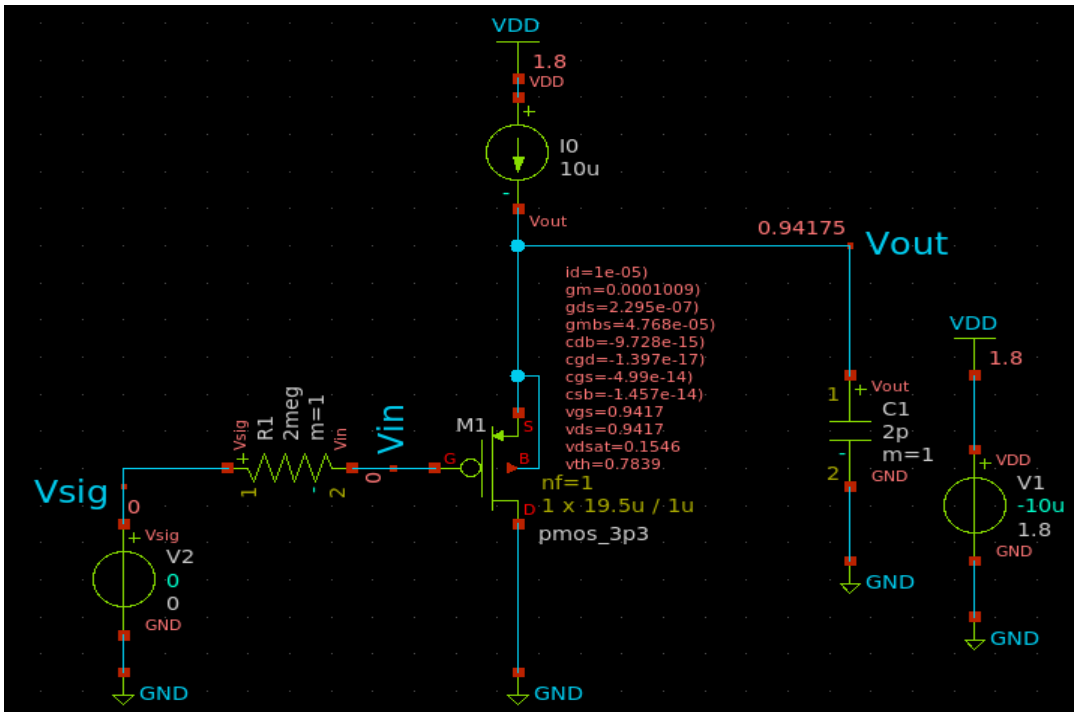

Figure 3 : Operating point analysis results showing transistor parameters confirming saturation operation

Check that the transistor operates in saturation?

VDS > VDSAT

0.94 > 0.15

AC Analysis :

An AC analysis was performed to evaluate the amplifier's gain across frequency. We studied the effect of varying CL and Rsig on the gain curve, especially the peaking behavior which indicates resonance at certain conditions.

I change the Vsource value to "dc 0 ac 1"

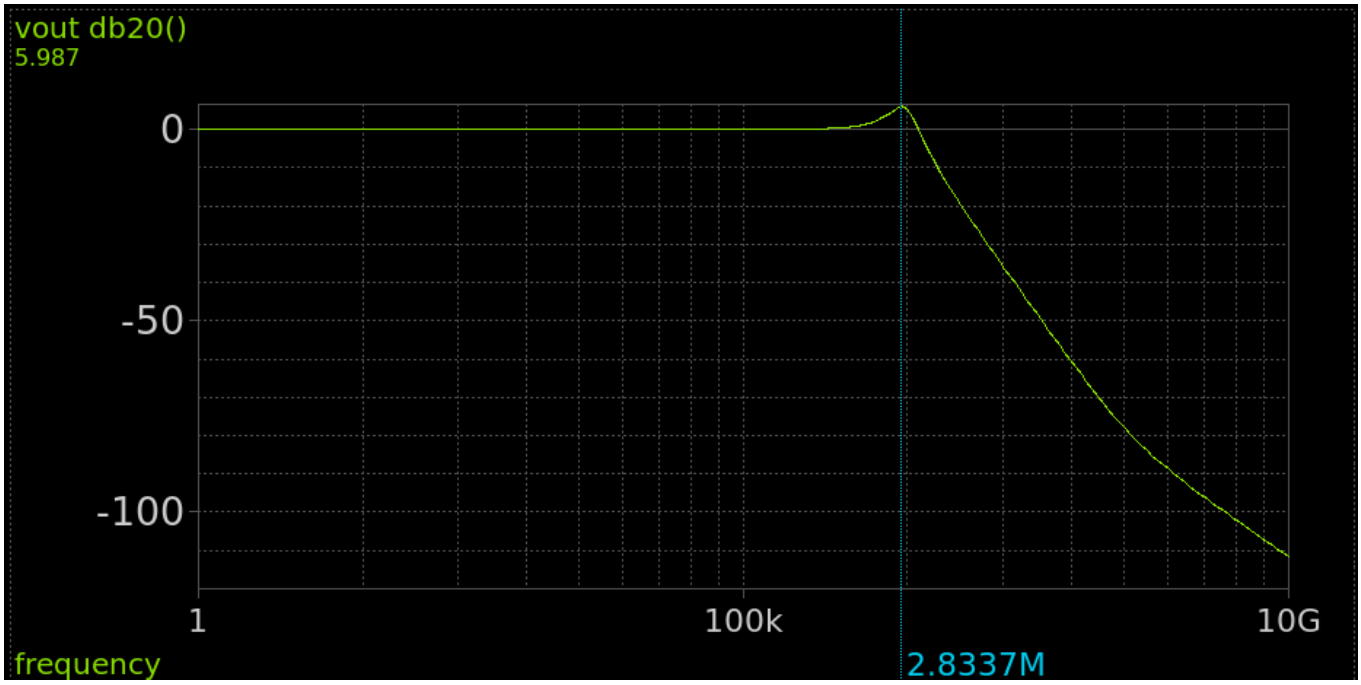

Figure 4 : AC magnitude response showing the frequency-dependent gain of the CD amplifier

Do you notice frequency domain peaking? How much is the peaking?

Yes, the simulation results clearly show frequency domain peaking.

The peaking is **1.999** (which is equivalent to a +6 dB increase in gain). This means the output signal's amplitude at the peak frequency is nearly double its value at low frequencies. This peak occurs at a frequency of **2.82 MHz**.

```
peaking                =  1.999437e+00 at=  2.818383e+06
```

Analytically calculate the quality factor (use approximate expressions). Is the system underdamped or overdamped?

Using this formula

$$Q = \frac{\sqrt{b_2}}{b_1} \approx \sqrt{\frac{g_m(C_{gs} + C_{gd})R_{sig}}{C_L}}$$

decreases $Q \rightarrow$ ( ) becomes dom

Gm= 2*id/v* = 100 Su or from simulation gm = 0.000109 S

And Cgs = 49.9 fF , Cgd = 0.014 fF , Rsig = 2 M ohm , Cl = 2 pF

Q = 2.24

underdamped

Now we will use parametric sweep: CL = 2p, 4p, 8p.

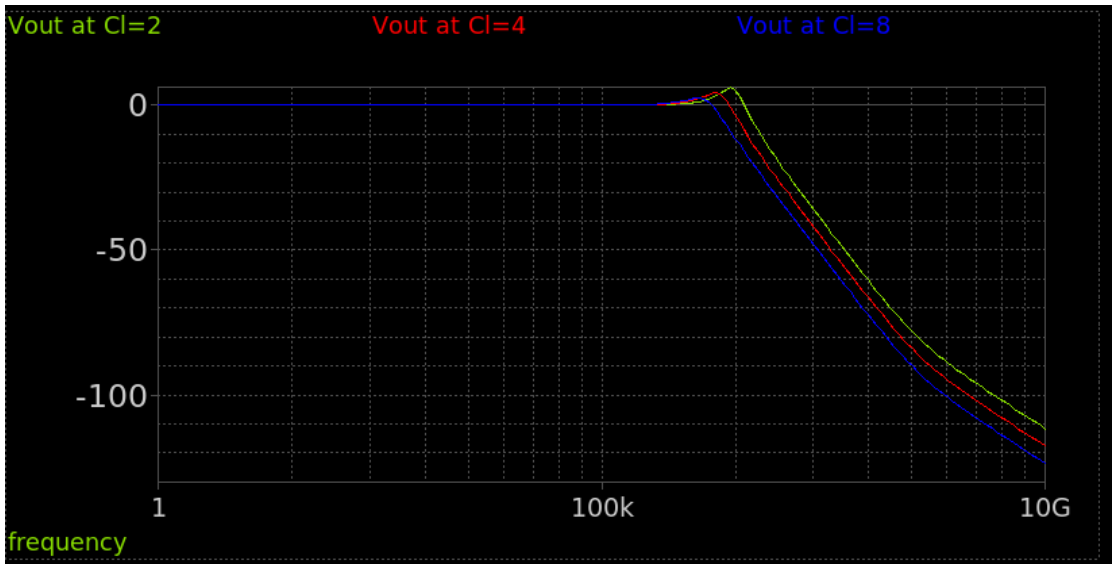

Figure 5 : AC response overlay showing the effect of load capacitance CL on peaking behavior.

Peaking vs. CL & Q-Factor Results

Load Capacitor (CL)	Q-Factor	Peaking (Linear Magnitude)	Peaking (dB)
2 pF	2.24	1.999	+6.02 dB
4 pF	1.58	1.652	+4.36 dB
8 pF	1.12	1.32	+2.41 dB

Comment:

An increase in capacitance results in a lower quality factor, which consequently diminishes the amplitude of the resonance peak.

Now we will do parametric sweep: Rsig = 20k, 200k, 2M.

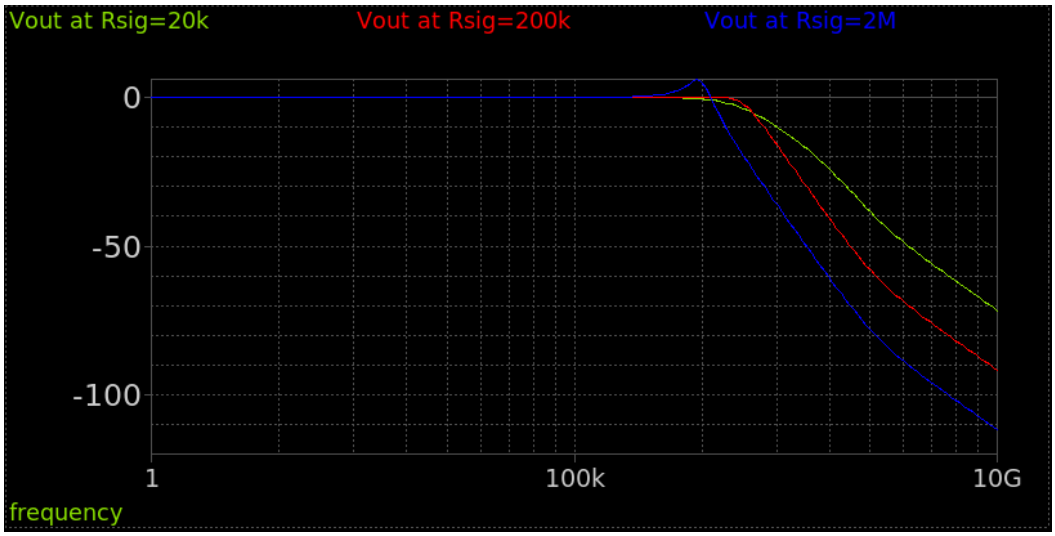

Figure 6 : AC response overlay showing the effect of Rsig on frequency-domain peaking.

Peaking vs. Rsig & Q-Factor Results

Source Resistance (Rsig)	Q-Factor	Peaking (Linear Magnitude)	Peaking (dB)
20 kΩ	0.223	0.998	-0.02 dB
200 kΩ	0.707	1.015	+0.13 dB
2 MΩ	2.234	1.999	+6.02 dB

Comment:

Increasing the resistance leads to a higher quality factor, which causes the peaking in the frequency response to increase accordingly.

Transient Analysis :

Using a pulse input, we simulated the amplifier's time-domain response. The output showed ringing and overshoot, especially for large CL and Rsig. We quantified overshoot and linked it to Q and peaking.

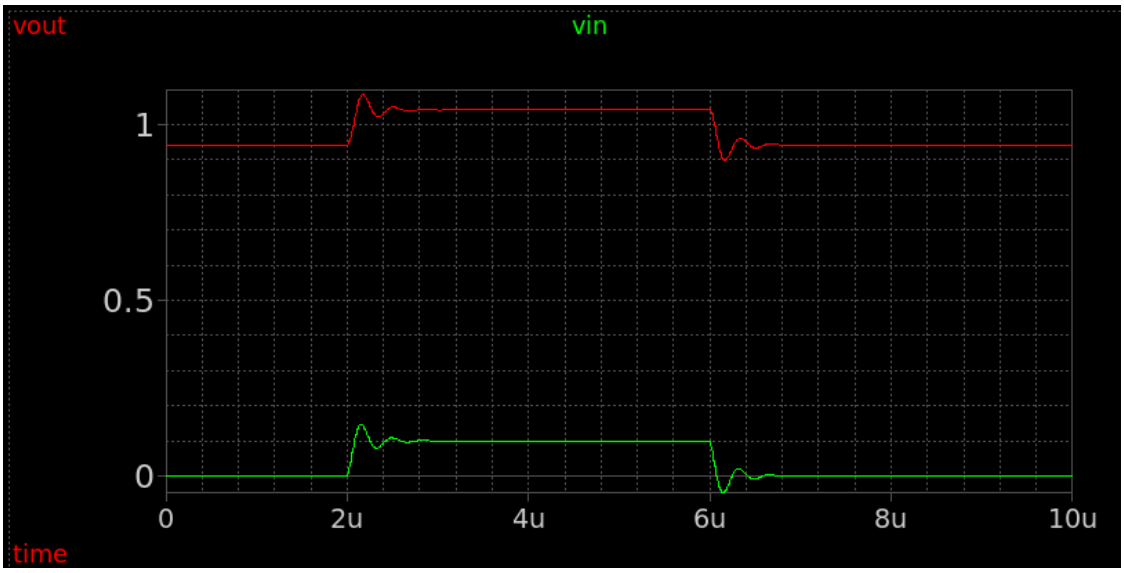

Figure 7 : Time-domain response showing Vin and Vout with ringing and DC shift.

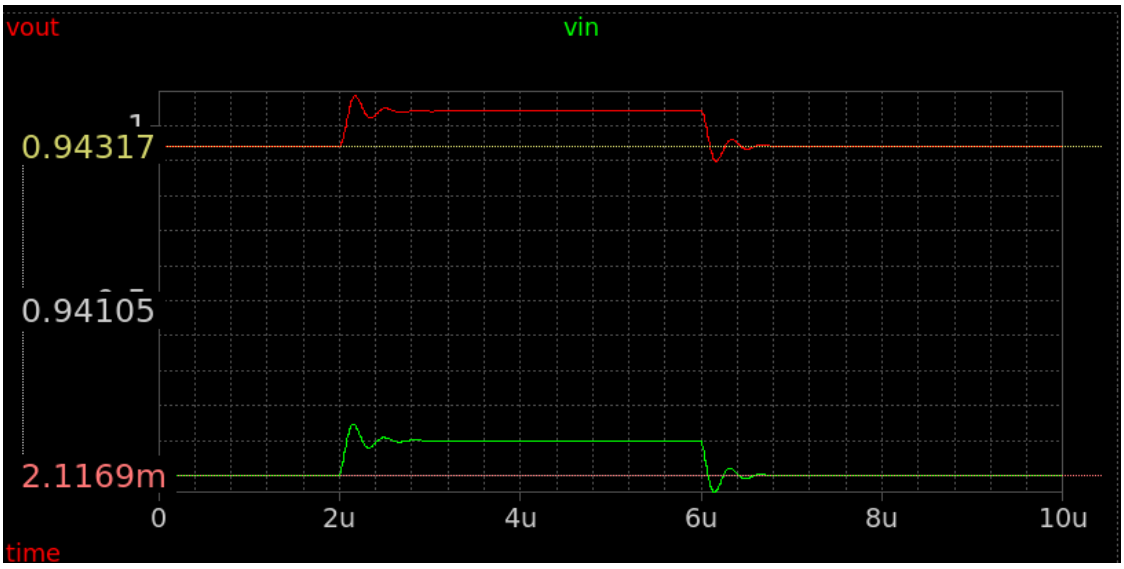

Figure 8 : Time-domain response showing Vin and Vout with ringing and DC shift with cursor

DC voltage difference (DC shift) between Vin and Vout = Vout – Vin = 0.94

What is the relation between the DC shift and VGS of the transistor

The DC shift between Vin and Vout is ≈ to the transistor's Vgs (here:VGS≈0.9417)

How to shift the signal down instead of shifting it up?

Use an **NMOS** source follower instead of a **PMOS**.

Do you notice time domain ringing? How much is the overshoot?

Yes, time-domain ringing is observed in the output waveform following the rising and falling edges of the input pulse.

The overshoot can be calculated as:

Vpeak from graph = **1.086V**

Vfinal = **1.043V**

Vout = **0.943V**

Overshoot (%) = (Vpeak−Vfinal/Vfinal−Vinitial)*100 = 44%

Now we will use parametric sweep: CL = 2p, 4p, 8p.

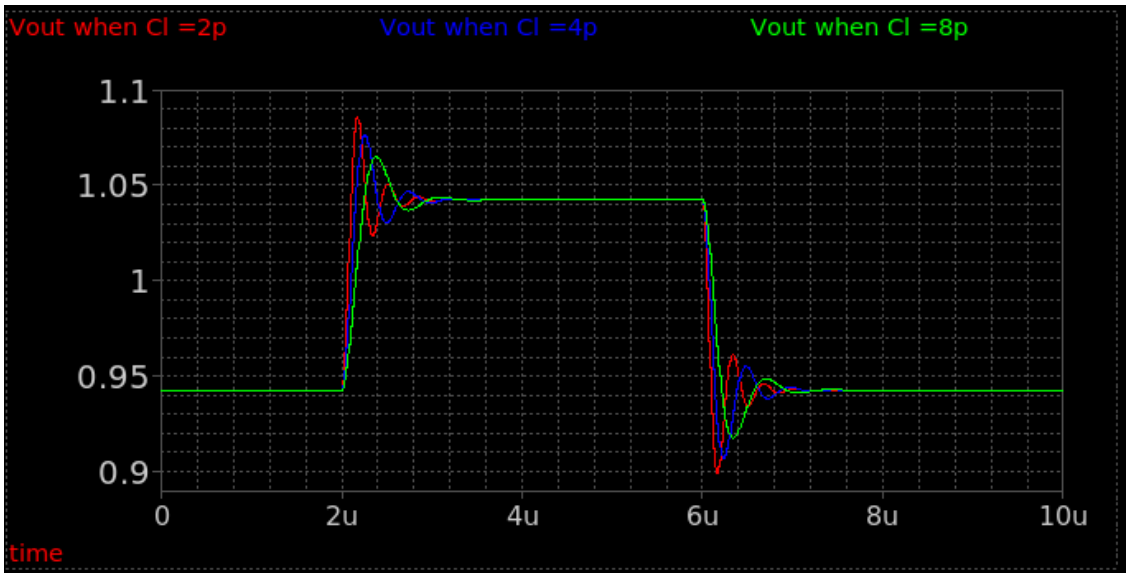

Figure 9 : Output overshoot as a function of load capacitance CL

Overshoot vs. Load Capacitance.

Load Capacitor (CL)	Initial Voltage (Vinitial)	Final Voltage (Vfinal)	Peak Voltage (Vpeak)	Overshoot (%)
2 pF	**0.943V**	**1.043V**	**1.086V**	**44.00%**
4 pF	**0.943V**	**1.042V**	**1.077V**	**36.20%**
8 pF	**0.943V**	**1.044V**	**1.066V**	**21.80%**

Comment :

The results show that as the load capacitance increases, the percent overshoot decreases. This is because a larger capacitor lowers the circuit's Q-factor, making the system more stable and less underdamped, which directly results in less ringing in the transient response.

Now we will do parametric sweep: Rsig = 20k, 200k, 2M.

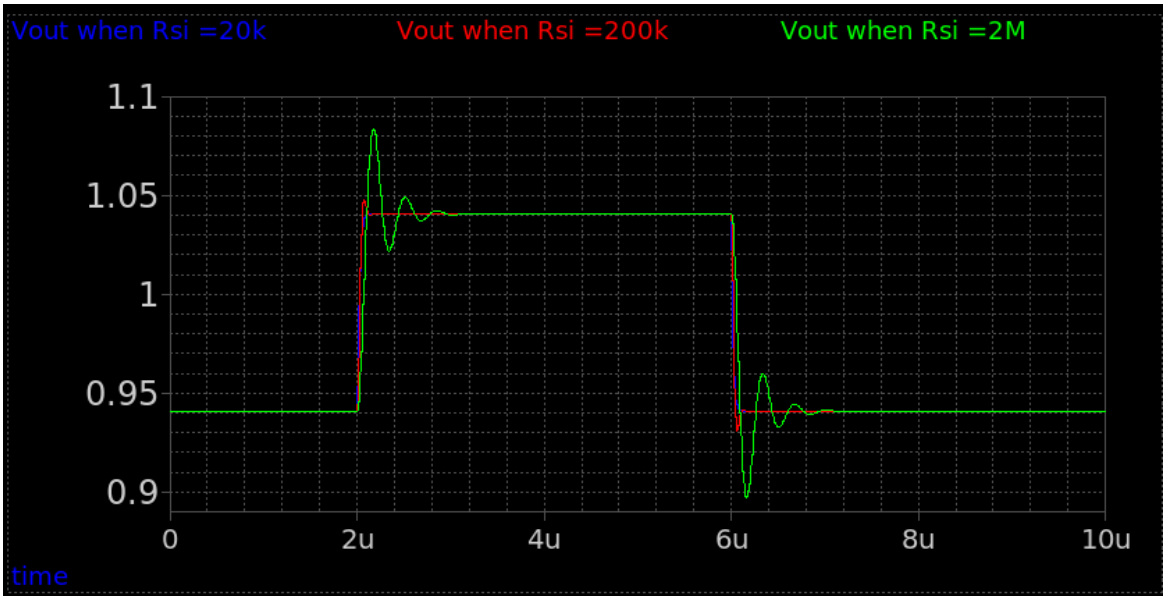

Figure 10 : Output overshoot as a function of load capacitance Rsig

Overshoot vs Rsig .

Source Resistance Rsig	Initial Voltage (Vinitial)	Final Voltage (Vfinal)	Peak Voltage (Vpeak)	Overshoot (%)
20 kΩ	**0.941V**	**1.041V**	**1.041V**	**0%**
200 kΩ	**0.941V**	**1.041V**	**1.047V**	**6.70%**
2 MΩ	**0.941V**	**1.040V**	**1.084V**	**44.00%**

Comment :

The data clearly shows that increasing the source resistance **Rsig** significantly increases the percent **overshoot**. This happens because a higher **Rsig** increases the circuit's quality factor (**Q**), making the system more **underdamped**. As a result, the transient response exhibits greater **overshoot** and more noticeable **ringing**.

At **Rsig = 20kΩ**, the calculated **Q = 0.223 < 0.707**, indicating an **overdamped** system with **no overshoot** observed.

$Zout$ (Inductive Rise) :

We simulated Zout using an AC analysis with the test voltage method. The results showed that Zout exhibits inductive behavior at mid frequencies. We compared the simulated Zout with theoretical estimates.

Schematic :

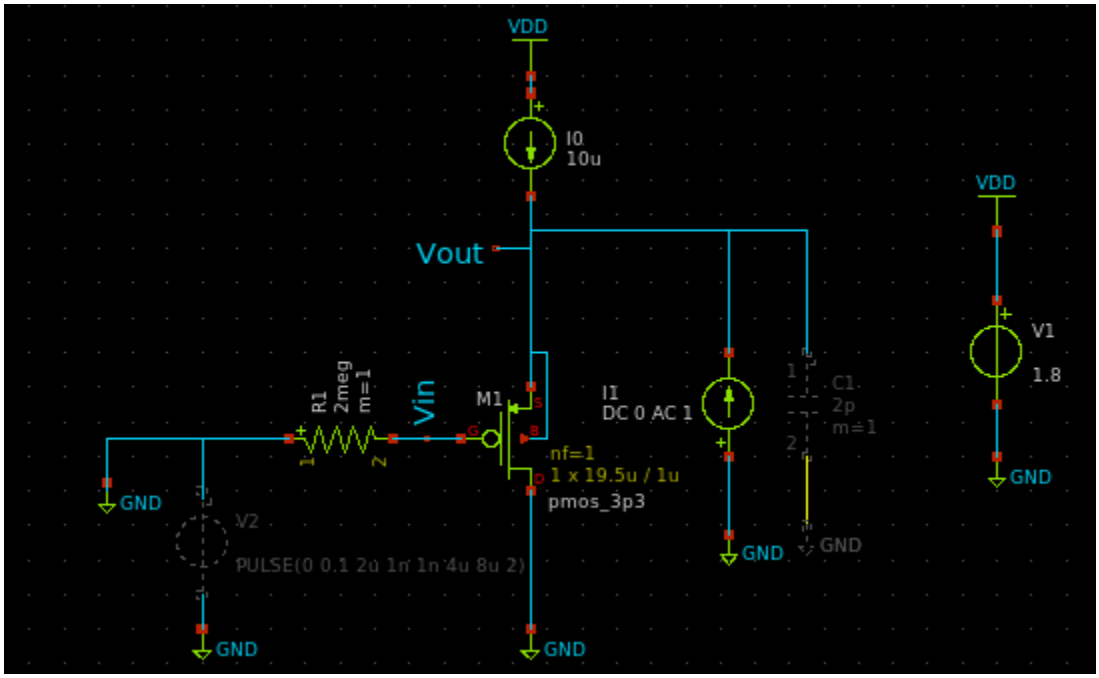

Figure 11 : Zout Testbench – AC current source at output, Vin removed

Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade)

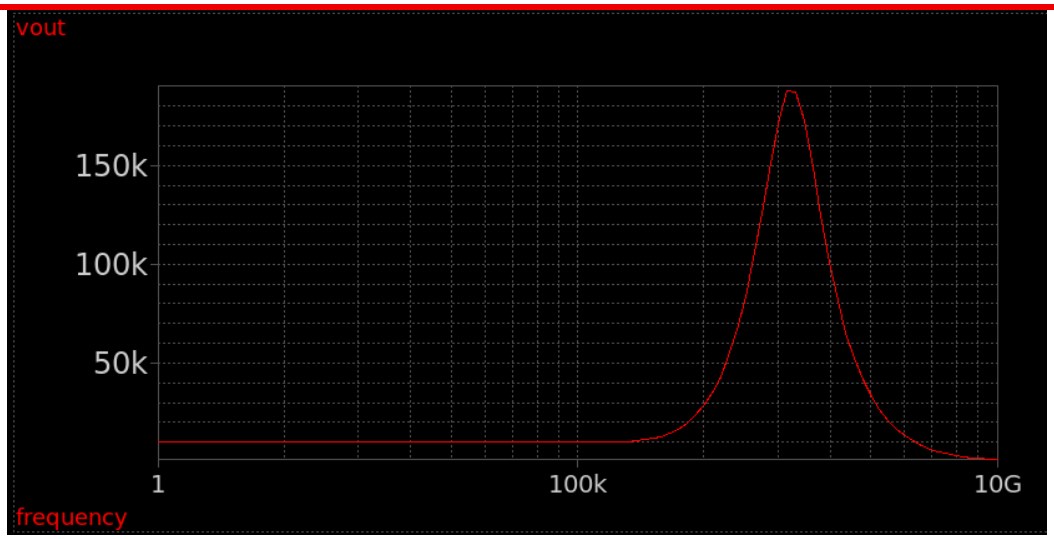

Figure 12 : Simulated output impedance magnitude showing inductive behavior at mid frequencies.

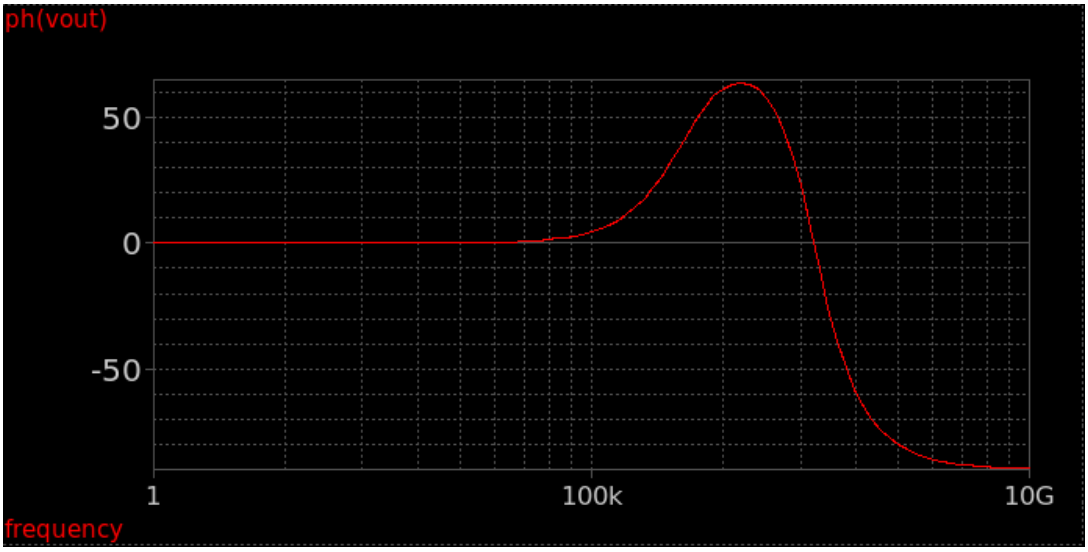

Figure 13 : Simulated output impedance Phase showing inductive behavior at mid frequencies.

Do you notice an inductive rise? Why? 4) Does $Zout$?

Yes, the plots clearly show an inductive rise in the output impedance.

1. At low frequencies, **Zout** starts at a low value approximately equal to **1/gm**, dominated by the transistor's transconductance.
2. As frequency increases, **Cgs** and **Rsig** form a feedback loop. When current flows through **Cgs**, it creates a voltage across **Rsig**, which modulates **Vgs** and affects the output. This feedback causes the circuit to resist changes in current — mimicking inductive behavior — and results in a rising **Zout**.
3. **Zout** peaks due to this feedback (a zero in the transfer function).

4. At high frequencies, **Cgd** begins to act as a short, bypassing the input, introducing a high-frequency pole and causing **Zout** to fall.

Analytically calculate the zeros, poles, and magnitude at low/high frequency for $Zout$?

From Simulation

Fz =1.17MHZ

Fp = 35.2MHZ

Analytical

	Name	TT-27.0
25	csg	32.87f
26	cdg	22.9f
27	cgd	3.073f
28	cbg	11.39f
29	cbd	8.969f
30	cbs	36.14f
31	idnth2	1.361e-24

We will use value from ADT and gm = 99.15u

$fz \approx 1 / 2\pi RsigCgs = 2.42MHz$

$fp \approx gm/2\pi(Cgs+Csb) = 228.32\ MHz$

the Fp is not accurate
using MATLAB Code in appendix

$$\frac{V_x}{i_x} = \frac{\left(1 + SR_{sig}\left(C_{gs} + C_{gd}\right)\right) r_0}{S^2\left[R_{sig}\left(C_{gs} + C_{gd}\right)C_{dB}r_0 + R_{sig}C_{gd}r_0C_{gs}\right] + S\left[C_{dB}r_0 + R_{sig}\left(C_{gs} + C_{gd}\right) + C_{gs}r_0 + g_m r_0 C_{gd}R_{sig}\right] + g_m r_0 + 1}$$

Result From MATLAB :

Zero: -1.438 MHz

Poles:

-1.225e+08 + j1.382e+08

-1.225e+08 + j-1.382e+08

fn = 29.390 MHz, zeta = 0.663

Method	Zero Frequency (fz)	Pole Frequency (fp)
Simplified Analytical	2.42MHz	228.32 MHz (inaccurate)
Ngspice .pz Simulation	1.17 MHz	35.2 MHz
MATLAB (Full Formula)	1.438 MHz	29.4 MHz

Comment :

When the poles of a system are complex conjugates, that is the mathematical definition of a **second-order, underdamped, resonant system**.

What this means practically:

- **In the Frequency Domain (AC Analysis):** This resonant behavior is what causes the sharp **peaking** in the frequency response.
- **In the Time Domain (Transient Analysis):** This same behavior is what causes the **ringing** and **overshoot** in the pulse response.

In short, the complex conjugate poles are the mathematical proof that links all the phenomena you observed in the lab (the peaking and the ringing) and confirms that the circuit behaves like a resonant system.

[Optional] How to solve the peaking/ringing problem?

Reducing Output Impedance Peaking and Ringing

In analog circuits, especially at high frequencies, peaking or ringing can appear in the output impedance due to the effect of internal capacitances and high resistance values. This usually happens in stages like the source follower or cascode, where capacitances such as CgsC_{gs}Cgs, CgdC_{gd}Cgd, and the source/load resistances form an underdamped system.

To reduce this effect, two main methods are commonly used:

1. **Adjusting Circuit Parameters**: By changing values like the source resistance RsigR_{sig}Rsig or load capacitance CLC_LCL, we can move the poles farther apart, which reduces the peaking.
2. **Adding a Compensation Network**: As explained in *Johns and Martin (2012), Section 4.4*, we can design a small compensation network that cancels the effect of negative input impedance, which helps reduce overshoots and ringing.

In the next part, both techniques are applied and their impact on circuit performance is shown.

Formula :

$$C_1 \cong \frac{g_{m1} C_{gs1} C_s}{(g_{m1} + G_{s1})(C_{gs1} + C_s)}$$

$$R_1 \cong \frac{(C_{gs1} + C_s)^2}{C_{gs1} C_s g_{m1}}$$

From ADT :

gm = 99.15u Cgs = 52.5fF Css = 60fF Gs1 = 47u

C = 18.8 fF

R = 40.6kohm

Schematic :

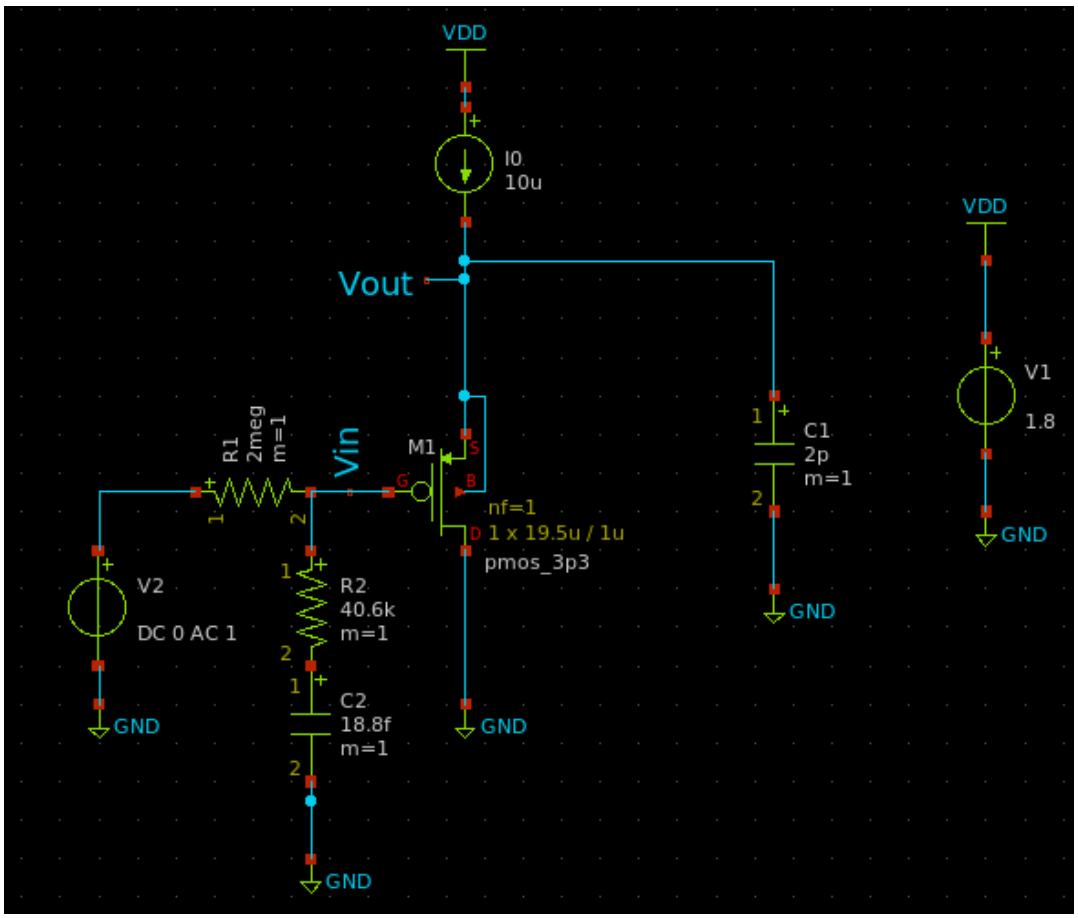

Figure 14 : Schematic of the compensation network added at the input node

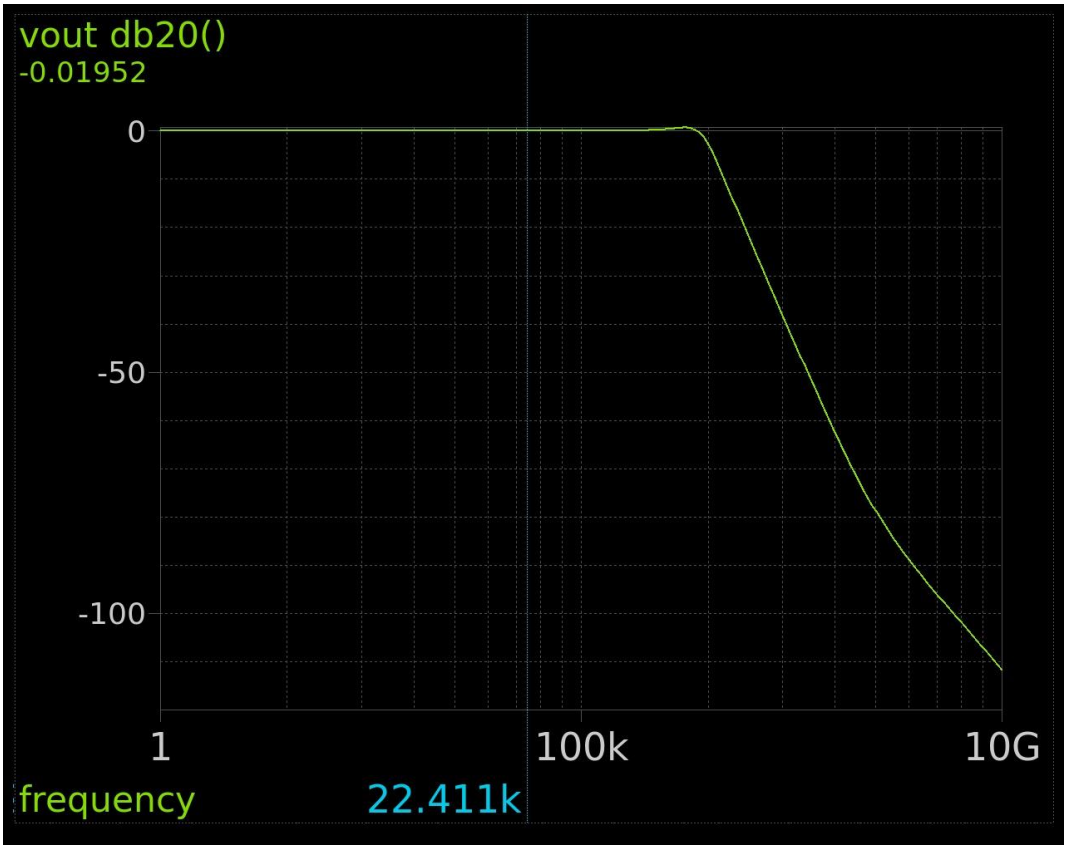

Figure 15 : AC magnitude response of the CD amplifier after input compensation, showing reduced peaking and improved frequency stability.

peaking = 1.055565e+00 at= 1.778279e+06

Comment :

The results show that the compensation network has successfully eliminated the frequency peaking. This is confirmed by the flat Bode plot and a peaking value near 1.0, indicating a stable, non-resonant response.

Appendix

Code for DC :

```
".control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
save @m.xm1.m0[vth]
save @m.xm1.m0[vdsat]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[gmbs]
save @m.xm1.m0[cdb]
save @m.xm1.m0[cgd]
save @m.xm1.m0[cgs]
save @m.xm1.m0[csb]
op
remzerovec
write lab_04_CD_dcop.raw
.endc
```

Code for Ac :

```
.control
save all
*op
ac dec 20 1 10g
meas ac peaking MAX vmag(vout) FROM=1 TO=10G
remzerovec
write lab_04_CD_ac.raw
.endc
```

Code for Ac parametric sweep :

```
.control
save all
let C_val=2p
let C_stop=8p
let C_mult=2
while C_val le C_stop
 alter C1 C_val
 ac dec 20 1 10g
 write lab_04_CD_ac_CLsweep.raw
 set appendwrite
 let C_val = C_val*C_mult
 end
.endc
```

Code for Trans parametric sweep :

```
control
save all
let c_val=2p
let c_stop=8p
let c_mult=2
while c_val le c_stop
 alter c1 c_val
 tran 10n 10u
 write lab_04_CD_tran_cLsweep.raw
 set appendwrite
  meas tran v_init find v(vout) at=0.5u
   meas tran v_settle find v(vout) at=3u
   meas tran v_peak max v(vout) from=2u to=6u
   run
   let denom = v_settle - v_init
   let num = v_peak - v_settle
   let overshoot = num * 100/ (denom + 1e-12)
   print c_val v_init v_settle v_peak overshoot
   let c_val = c_val*c_mult
end
.endc
```

Code for Zout :

```
.control
save all
ac dec 10 1 10g
meas ac peaking MAX vmag(vout) FROM=1 TO=10G
remzerovec
write lab_04_CD_ac.raw
.endc
```

Code for MATLAB :

```
clear; clc;

gm = 99.15e-6;    % S
ro = 4.28e6;      % Ohm
Cgs = 52.25e-15;  % F
Cgd = 3.073e-15;  % F
Csb = 26.34e-15;  % F
Rsig = 2e6;       s % Ohm

% Transfer Function Coefficients
num = [Rsig*(Cgs+Cgd)*ro, ro];
den = [Rsig*(Cgs+Cgd)*Csb*ro + Rsig*Cgd*Cgs, ...
    Csb*ro + Rsig*(Cgs+Cgd) + Cgs*ro + gm*ro*Cgd*Rsig, ...
    gm*ro + 1];

% Create Transfer Function
Zout_tf = tf(num, den);

% Poles, Zero, Natural Frequency, Damping
pz = pole(Zout_tf);
z = zero(Zout_tf);
fn = abs(pz(1)) / (2*pi);
zeta = -real(pz(1)) / abs(pz(1));

% Display Results
```

```
fprintf('Zero: %.3f MHz\n', z/(2*pi*1e6));
fprintf('Poles:\n%.3e + j%.3e\n%.3e + j%.3e\n', real(pz(1)), imag(pz(1)), real(pz(2)), imag(pz(2)));
fprintf('fn = %.3f MHz, zeta = %.3f\n', fn/1e6, zeta);

% Show Transfer Function
Zout_tf
```