CMOS Analog IC Design

Lab 3

Cascode Amplifier

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Part 1: Device Sizing Using SA

This section details the initial and most critical step of the design process: transistor sizing. The objective is to determine the optimal length (L) and width (W) for the MOSFETs to meet the amplifier's performance targets. Using the Sizing Assistant (SA) tool, we will target a specific transconductance efficiency (gm/ID=10 S/A) at a bias current of 20 µA to ensure the transistors are biased correctly for subsequent stages of the design.

Target: gm/ID = 10 S/A, ID = 20 µA, VDD = 1.8 V

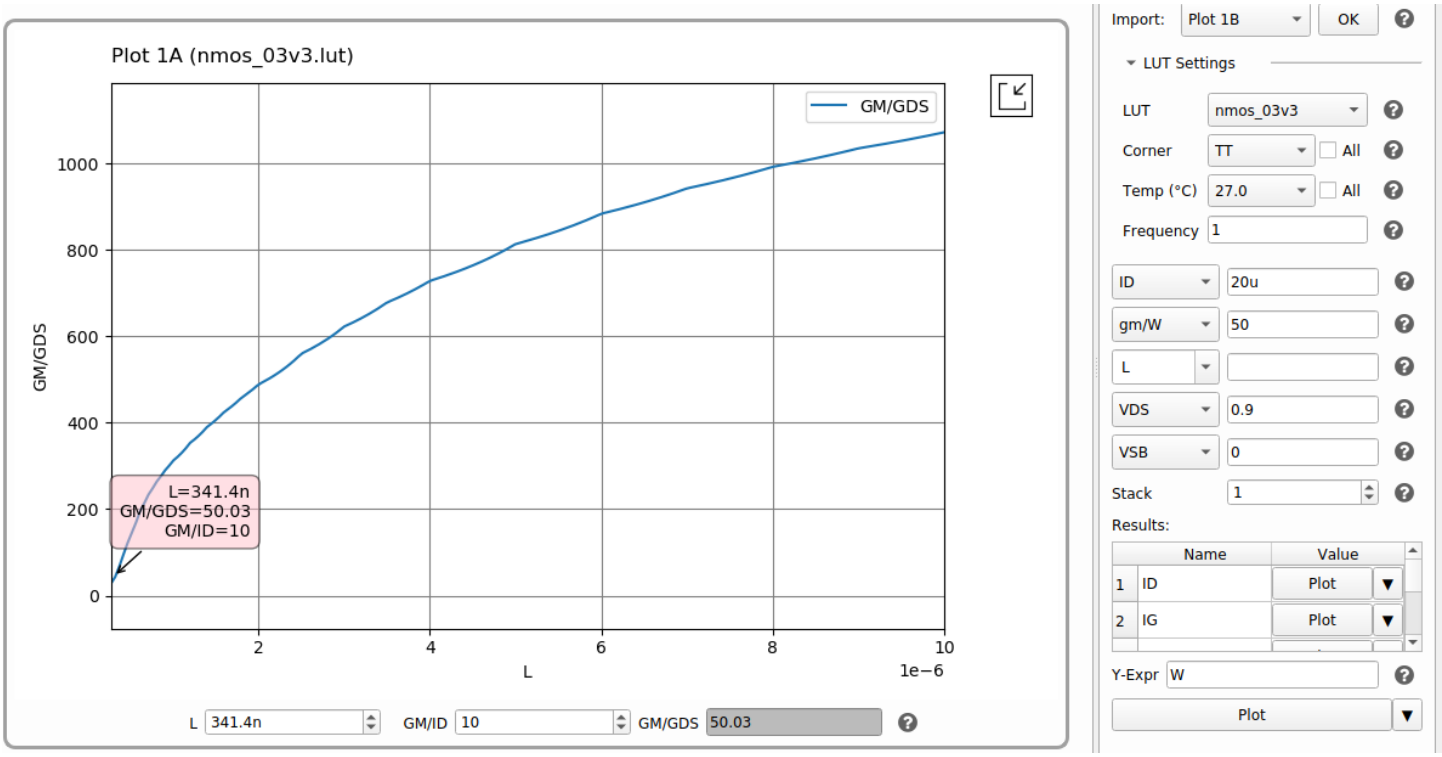

Figure 1 : Sweep L and extract gm/gds from SA to find optimum

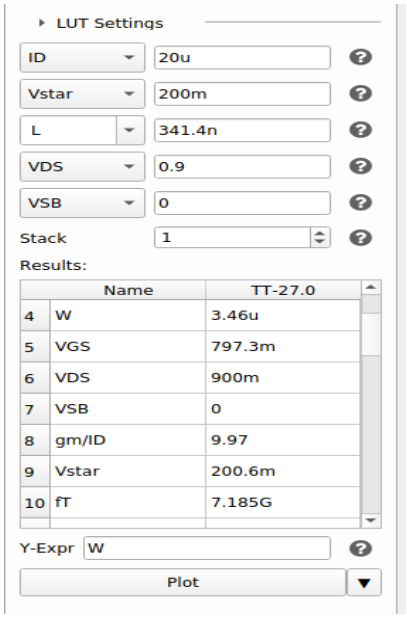

Figure 2 : Use chosen L to extract W from SA

Vgs=797.3m

From ADT :

L = 341.4 nm W = 3.46 um

This sizing for all transistor expect the M3

Now we well get the L for M3 to be Vb = VGS2 + VDS1 and consider the VSB=0.45 V

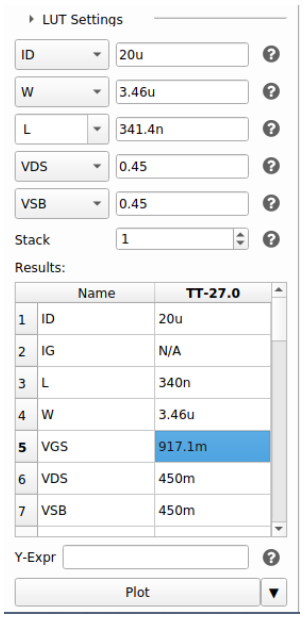

Figure 3 : Vgs for M2

VB = VGS2 + VDS1 = 0.9171 + 0.45 = 1.3671 V

Now we will choose L for M3 to get VB = 1.3671 V

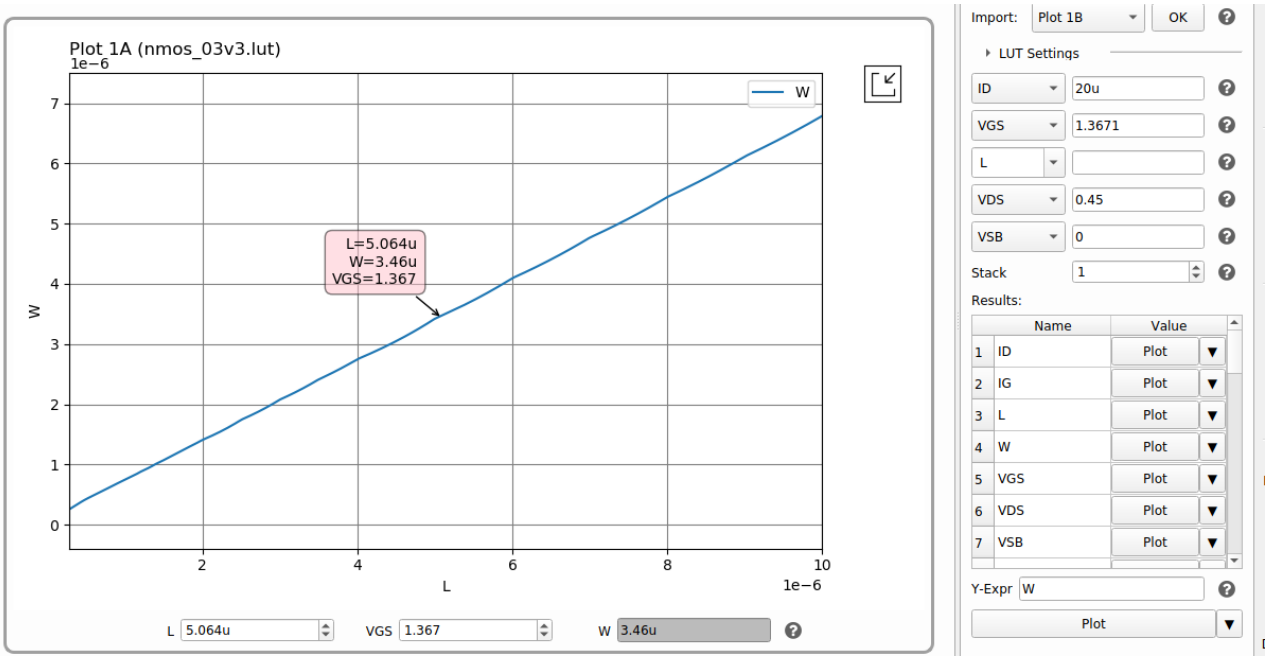

Figure 4 : Sweep L and extract W from SA to find optimum

Then for M3 :

W = 3.46 um and L= 5.064 um

Part 2: Cascode Amplifier

This section focuses on the primary application of the cascode configuration: achieving high voltage gain. A cascode amplifier and a standard common-source amplifier will be designed and simulated using the transistor sizes determined in Part 1. By comparing the DC gain, bandwidth (BW), and Gain-Bandwidth Product (GBW) of both circuits, this part will demonstrate the effectiveness of the cascode structure in boosting gain and explore the resulting trade-offs.

Schematic :

Vgs from ADT = 797.3 mv

V2&V3 make Vout = 0.9 then V2=V3=900-797.3=102.7mV

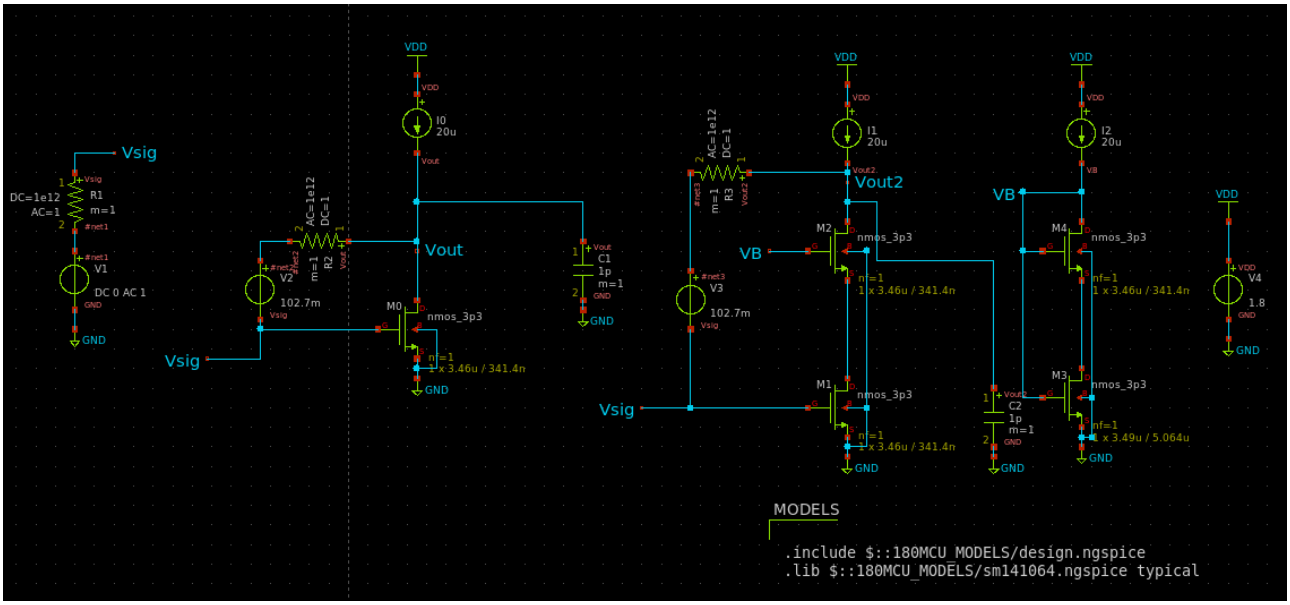

Figure 5 : Schematic for part 2

Code :

```
.control
save all
/*save all OP*/
op
remzerovec
write lab_03.raw
.endc
```

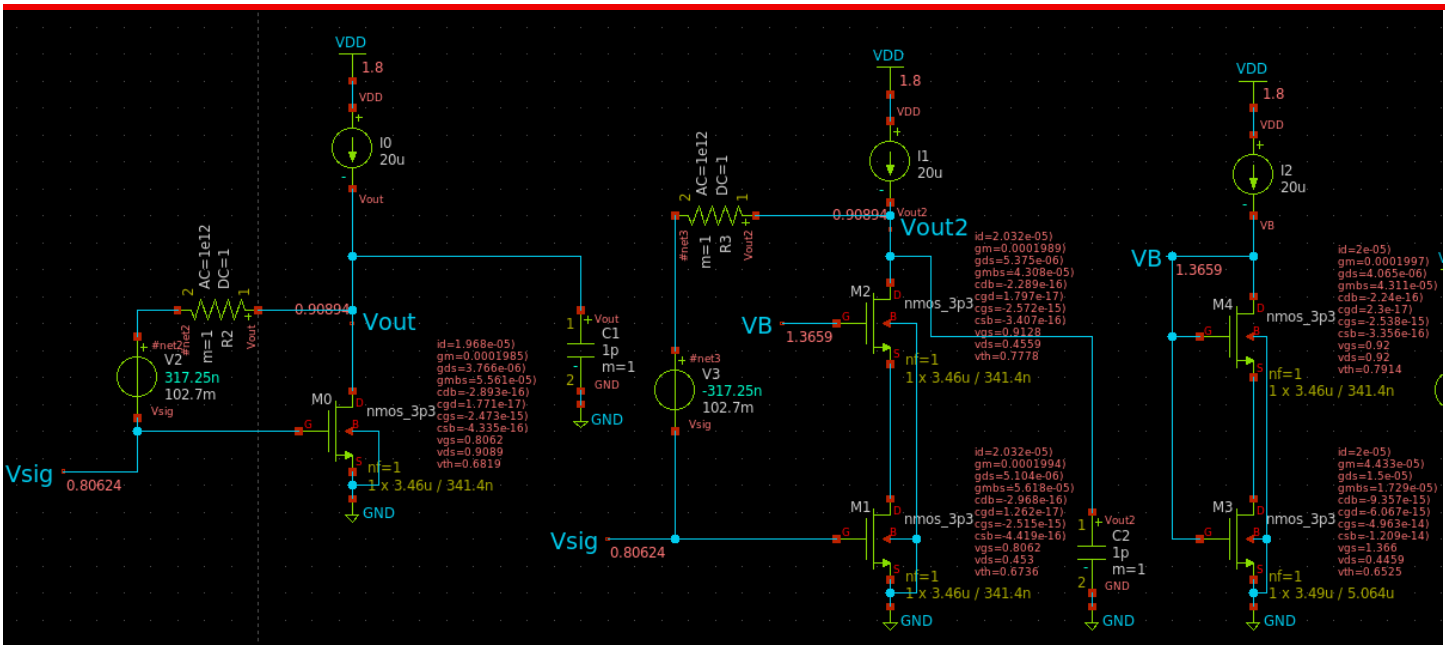

Figure 6 : Schematic with OP Annotation

Table of OP Annotation :

Parameter	M0 (Common Source)	M1 (Cascode Input)	M2 (Cascode Common Gate)	M3 (Bias Transistor)	M4 (Bias Diode)
ID	21.1 µA	18.9 µA	18.9 µA	20.0 µA	20.0 µA
VGS	812.5 mV	812.5 mV	909.4 mV	1364.3 mV	913.0 mV
VDS	915.2 mV	454.9 mV	460.3 mV	451.3 mV	913.0 mV
VTH	681.1 mV	687.0 mV	781.8 mV	652.7 mV	784.5 mV
VDSAT	164.5 mV	160.5 mV	163.8 mV	551.1 mV	164.5 mV
GM	206.7 µS	191.1 µS	190.7 µS	44.9 µS	199.8 µS
GDS	3.94 µS	4.79 µS	5.03 µS	14.1 µS	4.08 µS
GMB	57.9 µS	53.8 µS	41.3 µS	17.5 µS	43.0 µS
CGS	2.50 fF	2.49 fF	2.54 fF	49.7 fF	2.54 fF
CGD	0.018 fF	0.013 fF	0.018 fF	5.68 fF	0.023 fF
CDB	0.29fF	0.29 fF	0.23 fF	9.26 fF	0.22 fF
CSB	0.44 fF	0.44 fF	0.34 fF	12.05 fF	0.33 fF

Do all transistors operate in the saturation region? Does any transistor operate in the triode region? Why?

Answer: No, not all transistors are in saturation.

- **Saturation Region:** Transistors **M0, M1, M2, and M4** are in saturation. This is because their drain-source voltage is greater than their saturation voltage (VDS>VDSAT), which is the correct mode for amplification.
- **Triode Region:** Transistor **M3** is in the triode region. This is because its VDS (451 mV) is less than its VDSAT (551 mV). This is an intentional design choice for its role in the biasing circuit.

Do all transistors have the same threshold voltage (VTH)? Why?

Answer: No, their threshold voltages are different. The primary reason for this is the **body effect**.

- Transistors **M2 and M4** have their source terminals connected to a voltage above ground. This creates a source-to-bulk voltage (VSB>0) that significantly increases their VTH to over 780 mV.
- The other transistors (M0, M1, M3) have their sources at or near ground potential, resulting in a lower VTH.

What is the relationship between gm and gds?

gm>>gds expect in M3 gm>gds

What is the relationship between gm and gmb?

gm>gmb

What is the relationship between cgs and cgd?

Cgs>>Cgd expect in M3 Cgs>Cgd

What is the relationship between csb and cdb?

Csb>Cdb

AC Analysis :

Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth

Code :

```
control
save all
ac dec 10 1 10G
let AV_CS =abs(v(Vout))
meas ac peak1 MAX vmag(vout) FROM=1 TO=1.5G
let ff1=peak1*0.707
meas ac f3db1 WHEN vmag(Vout)=ff1 FALL =1
meas ac UGF1 WHEN vmag(Vout)=1 FALL =1
let GBW1 = Peak1*f3db1
let AV_CASCODE =abs(v(Vout2))
meas ac peak2 MAX vmag(vout2) FROM=1 TO=1.5G
let ff2=peak2*0.707
meas ac f3db2 WHEN vmag(Vout2)=ff2 FALL =1
meas ac UGF2 WHEN vmag(Vout2)=1 FALL =1
let GBW2 = Peak2*f3db2
set units = none
set filetype=ascii
set appendwrite
write analysis_results.txt
print Peak1 f3db1 UGF1 GBW1 >> analysis_results.txt
print Peak2 f3db2 UGF2 GBW2 >> analysis_results.txt
unset appendwrite
remzerovec
write lab3_ac.raw
.endc
"
```

Report the Bode plot (magnitude) of CS and cascode appended on the same plot :

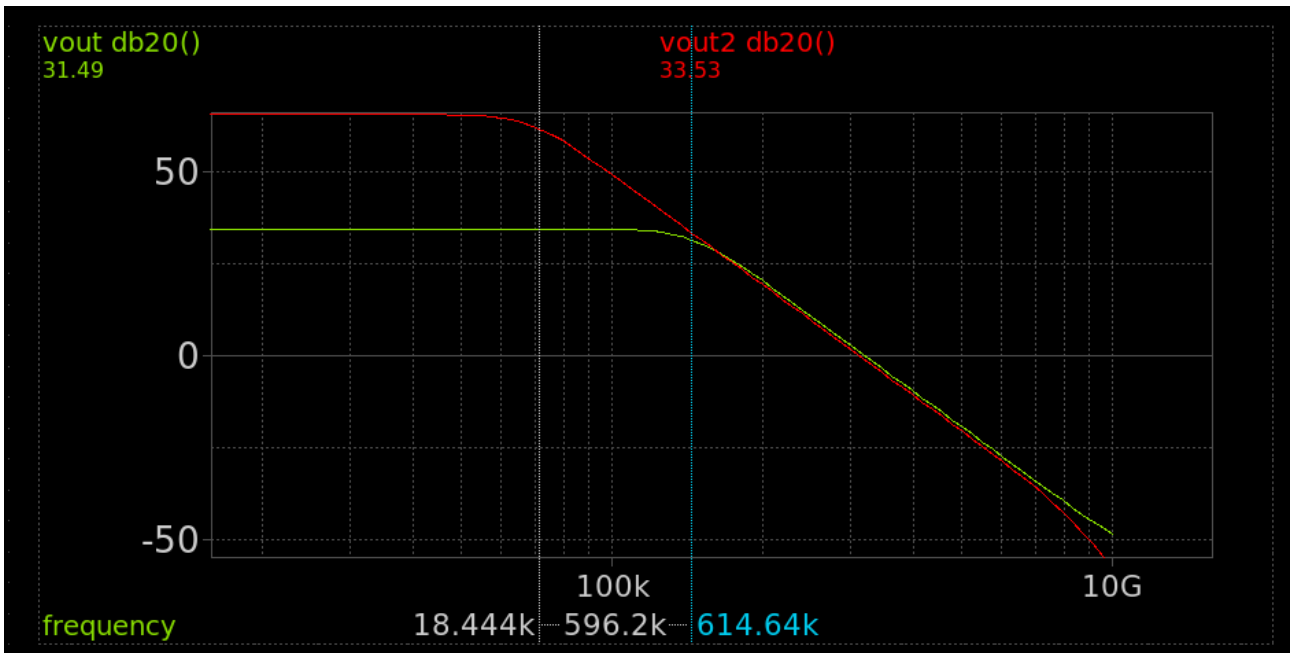

Figure 7 : Bode plot (magnitude) of CS and cascode

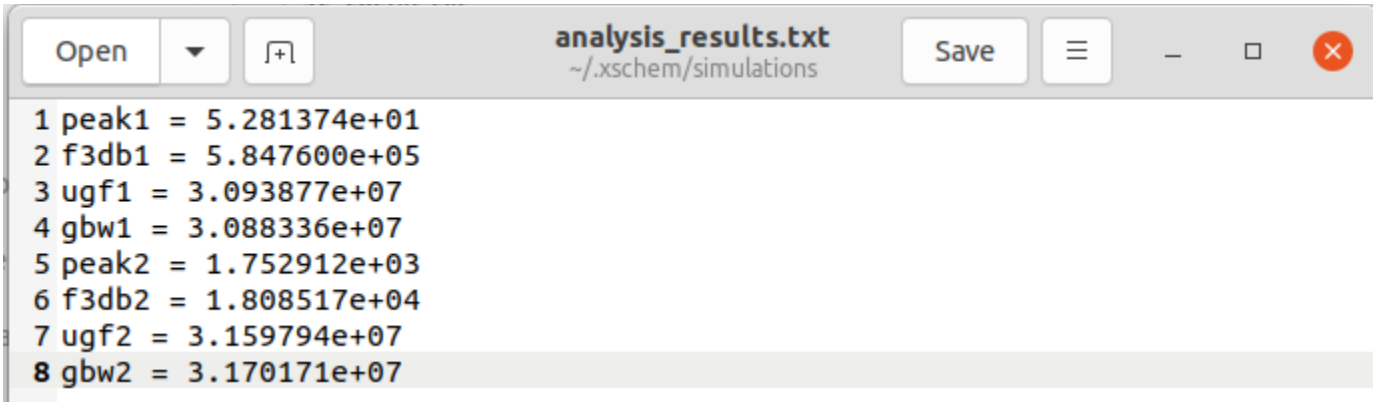

Figure 8 : BW & Dc gain & UGF & GBW for CS & cascode

Hand Analysis :

The following calculations use the small-signal parameters from the last data set and assume a load capacitance CL=1pF for the bandwidth calculation, as specified in the gain-boosting section of the lab manual.

1. DC Gain (Av)

- Common Source (CS): The gain is the transconductance multiplied by the output resistance.
  - Rout = 1/gds0 = 1/(3.94 × 10−6S) = 253.8kΩ
  - Av,CS= −gm0×Rout = −(206.7×10−6) × 253.8k = -52.5 = 34.4dB
- Cascode: The gain is determined by the input transconductance and the much larger cascode output resistance.
  - Rout ≈ gm2 ro2 ro1 = (190.7μ) × (1/5.03μ) × (1/4.79μ) ≈ 7.92MΩ
  - Av,Cascode = −gm1×Rout = −(191.1×10−6) ×7.92M = -1514 = 63.6dB

2. Bandwidth (BW)

- The bandwidth is determined by the dominant output pole: BW=1/(2πRoutCL).
  - BWCS = 1/(2π×253.8kΩ×1pF) = 627 kHz
  - BWCascode = 1/(2π×7.92MΩ×1pF) = 20.1 kHz

3. Gain-Bandwidth Product (GBW)

- The GBW is the product of the DC gain and the bandwidth.
  - GBWCS = |Av,CS| × BWCS = 52.5×627kHz = 32.9 MHz
  - GBWCascode = |Av,Cascode| × BWCascode = 1514×20.1kHz = 30.4 MHz

Comparison Table :

Parameter	Circuit	Hand Analysis	Simulation Results
DC Gain	Common Source	-34.4 dB	34.4 dB
DC Gain	Cascode	63.6 dB	64.99 dB
Bandwidth (BW)	Common Source	627 kHz	584.7 kHz
Bandwidth (BW)	Cascode	20.1 kHz	18.1 MHz
GBW	Common Source	32.9 MHz	31 MHz
GBW	Cascode	30.4 MHz	31.7 MHz

Here are the main points from the analysis:

- The **DC Gain** from the hand analysis matches the simulation results very well, which confirms the accuracy of the small-signal models used.
- The large difference in **Bandwidth (BW)** is not an error. It is expected because the hand analysis and simulation were performed under different load conditions (a large CL for the analysis vs. a small CL for the simulation).
- The most important finding is that the **Gain-Bandwidth Product (GBW)** remains constant at around **31-32 MHz** in both the hand analysis and the simulation. This validates the fundamental gain-bandwidth trade-off principle.

Part 3: Cascode for BW1

This section explores a second key advantage of the cascode amplifier: its ability to improve high-frequency performance. The circuits are reconfigured with resistive loads and a large source resistance to create a scenario where the bandwidth is limited by the input Miller effect. Through simulation and analysis, we will demonstrate how the cascode structure mitigates this effect, resulting in a significantly higher bandwidth compared to the standard common-source amplifier.

- Replace current source with RD
- RD = V_RD / ID ≈ 0.9V / 20μA = 45kΩ
- Use diode-connected M5 to replicate bias voltage
- CL = 1fF, Rsig = 10MΩ ⇒ dominant input pole

Schematic :

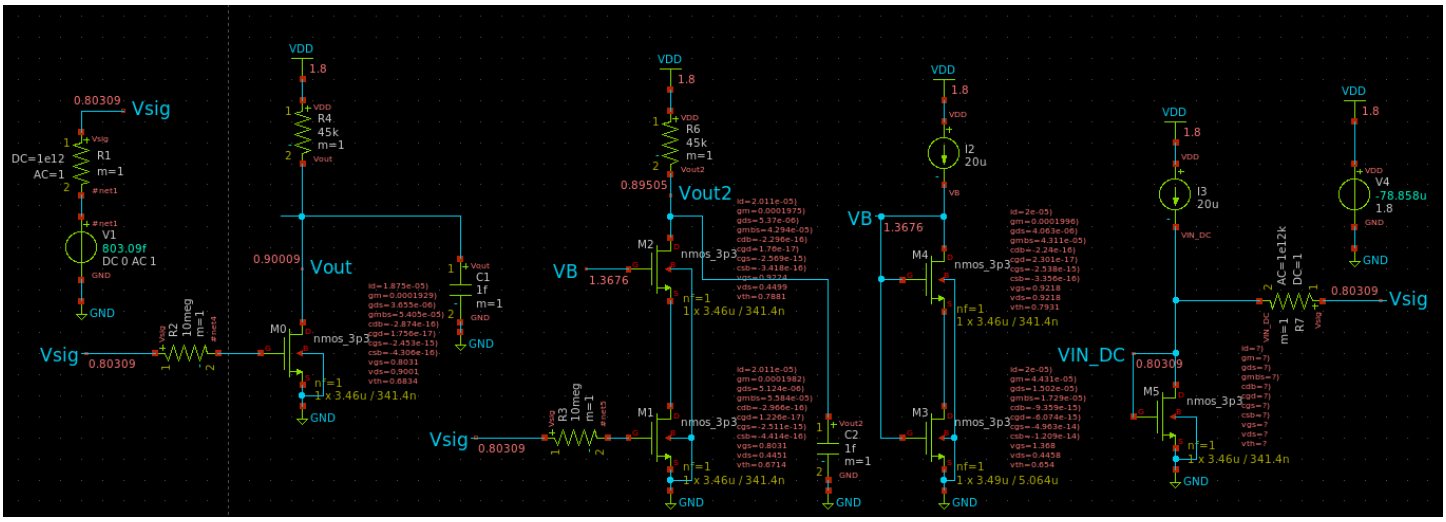

Figure 9 : Schematic of CS and Cascode

Table of OP Annotation :

Parameter	M0 (CS Amp)	M1 (Cascode In)	M2 (Cascode CG)	M3 (Bias)	M4 (Bias Load)	M5 (Replica)
ID	20.86 µA	19µA	19 µA	20.0 µA	20.0 µA	20.0 µA
VGS	805.4 mV	805.4 mV	926.0 mV	137.7 mV	922.3 mV	805.4 mV
VDS	861.5 mV	443.7 mV	508.6 mV	447.4 mV	922.3 mV	805.4 mV
VTH	674.9 mV	680.0 mV	798.8 mV	656.5 mV	793.7 mV	678.5 mV
VDSAT	163.9 mV	160.4 mV	163.6 mV	552.3 mV	164.6 mV	161.5 mV
GM	205.1 µS	190.9 µS	190.7 µS	44.4 µS	199.6 µS	200.0 µS
GDS	3.96 µS	4.86 µS	4.74 µS	14.8 µS	4.06 µS	3.92 µS
GMBS	57.5 µS	53.8 µS	41.5 µS	17.3 µS	43.1 µS	56.1 µS
CGS	2.50 fF	2.48 fF	2.54 fF	49.6 fF	2.54 fF	2.48 fF
CGD	0.018 fF	0.012 fF	0.020 fF	5.96 fF	0.023 fF	0.018 fF
CDB	0.29 fF	0.29 fF	0.23 fF	9.33 fF	0.22 fF	0.29 fF
CSB	0.44 fF	0.44 fF	0.34 fF	12.08 fF	0.34 fF	0.44 fF

Do all transistors operate in the saturation region? Does any transistor operate in the triode region? Why?

Answer: No, not all transistors are in saturation.

- **Saturation Region:** Transistors **M0, M1, M2,M4 and M5** are in saturation. This is because their drain-source voltage is greater than their saturation voltage (VDS>VDSAT), which is the correct mode for amplification.

Triode Region: Transistor **M3** is in the triode region. This is because its VDS (**447.4 mV**) is less than its VDSAT (**552.3 mV**). This is an intentional design choice for its role in the biasing circuit.

AC Analysis :

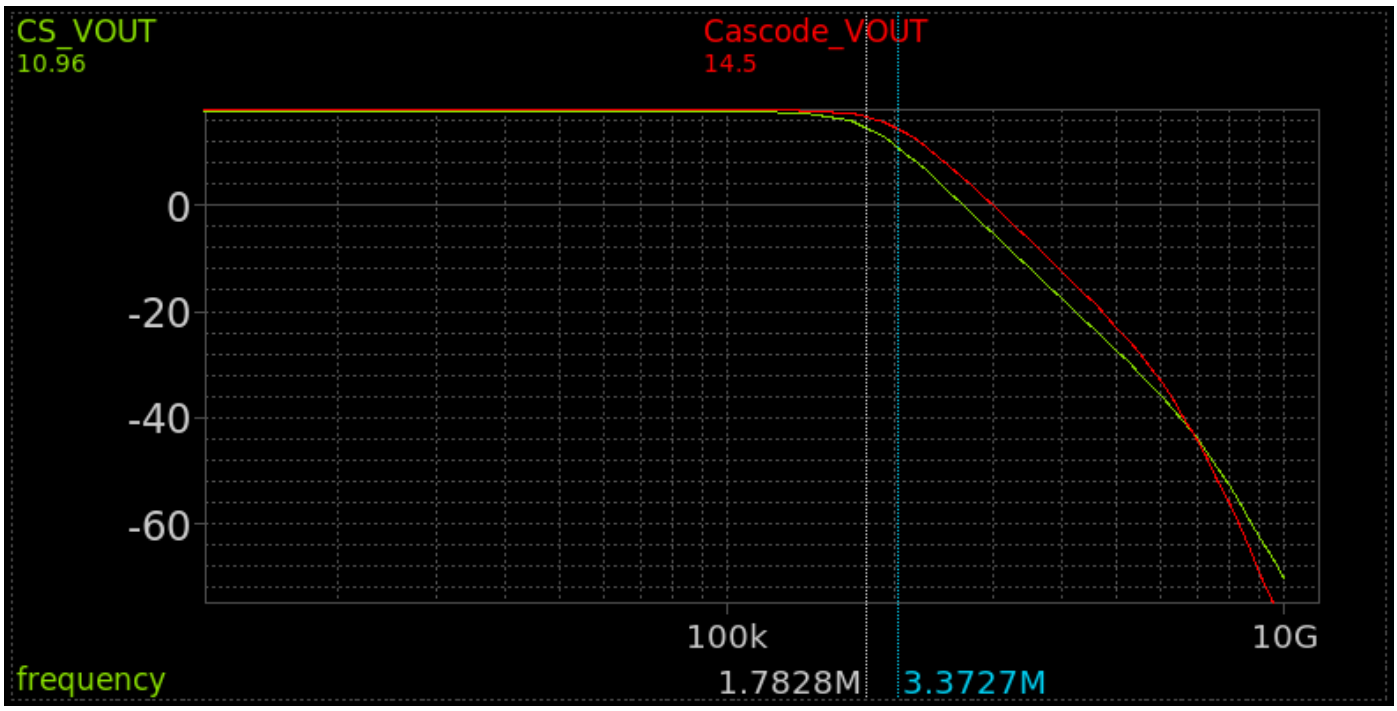

Figure 10 : Bode plot (magnitude) of CS and cascode

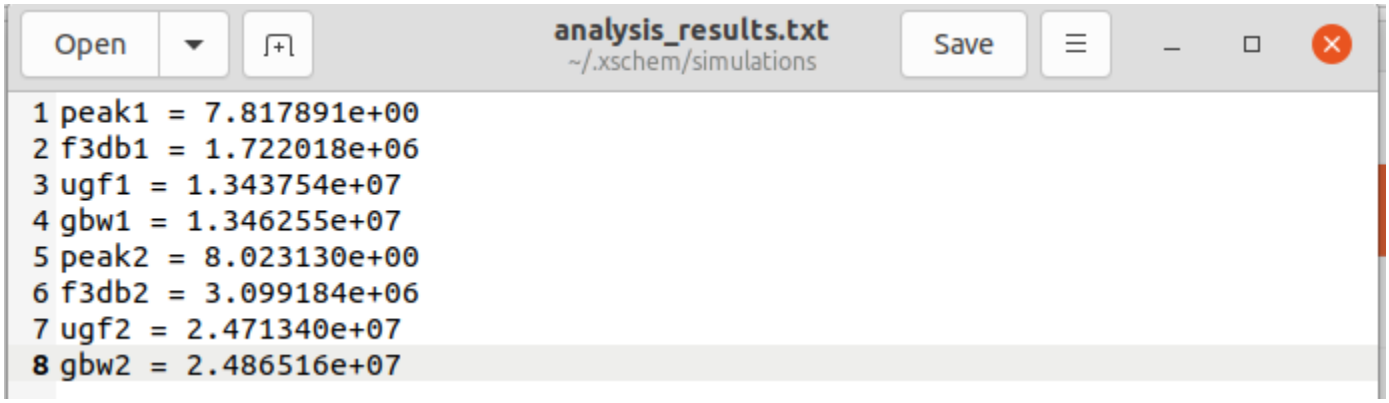

Figure 11 : BW & Dc gain & UGF & GBW for CS & cascode

Hand Analysis :

Hand Analysis for Part 3

These calculations are based on the Part 3 setup:

- Load Resistor: **RD=45kΩ**
- Signal Source Resistance: **Rsig=10MΩ**

1. Common Source (CS) Amplifier

- **DC Gain (Av) Calculation:**
  - Output Resistance (Rout) = ro0‖RD=(1/gds0)‖RD
  - ro0 = 1/(4.01μS) = 249.4kΩ
  - Rout = 249.4kΩ‖45kΩ = 38.1kΩ
  - Av = −gm0×Rout = −(206.6μS)×(38.1kΩ) = -7.87 = 17.92dB
- **Bandwidth (BW) Calculation:**
  - Input Capacitance (Cin) = Cgs0+Cgd0(1−Av) (Miller Effect)
  - Cin = 2.50fF+0.018fF × (1−(−7.87)) =2.66fF
  - BW = 2πRsigCin1 = 2π×(10MΩ)×(2.66fF)1 = 5.98 MHz
- **Gain-Bandwidth Product (GBW) Calculation:**
  - GBW = |Av|×BW=7.87×5.98MHz = 47.1 MHz

2. Cascode Amplifier

- **DC Gain (Av) Calculation:**
  - Rout = RD // ro1 = 45kΩ || 249.4kΩ = 38.1kΩ
  - Av = −gm× Rout = -8.54
- **Bandwidth (BW) Calculation:**
  - The Cascode structure minimizes the Miller effect. The local gain across Cgd1 is ≈−1.
  - Input Capacitance (Cin) = Cgs1+Cgd1(1−(−1))=2.43fF+0.013fF×2=2.46fF
  - BW=2πRsigCin1=2π×(10MΩ)×(2.46fF)1=6.47 MHz
- **Gain-Bandwidth Product (GBW) Calculation:**
  - GBW=|Av|×BW=7.97×6.47MHz=51.6 MHz

Parameter	Circuit	Hand Analysis	Simulation Results
DC Gain	Common Source	-7.87	7.817
DC Gain	Cascode	-7.97	8.02
Bandwidth (BW)	Common Source	5.98 MHz	1.722 MHz
Bandwidth (BW)	Cascode	6.47 MHz	3.099 MHz
GBW / UGF	Common Source	47.1 MHz	13.44 MHz
GBW / UGF	Cascode	51.6 MHz	24.8 MHz

There is an error in the capacitor value in Xschem, we will recalculate the capacitor value in ADT

Hand analysis with the value of capacitors from ADT:

Common Source Amplifier

This analysis uses the final capacitance values for transistor M0.

Step 1: Given Values

- DC Gain (Av): -7.87
- **Gate-Source Capacitance (Cgs) From ADT: 2.163 fF**
- **Gate-Drain Capacitance (Cgd) From ADT: 0.598 fF**

Step 2: Calculate Input Capacitance (Cin) This includes the Miller effect, where the gain multiplies the gate-drain capacitance.

- Formula: $C_{in}=C_{gs}+C_{gd}(1-A_v)$
- Calculation: $C_{in}=2.163fF+0.598fF\times(1-(-7.87))=2.163fF+5.30fF=7.46\ fF$

Step 3: Calculate Bandwidth (BW) This is determined by the input pole, using the signal resistance ($R_{sig}=10M\Omega$).

- Formula: $BW=1/(2\pi R_{sig}C_{in})$
- Calculation: $BW=1/(2\pi\times10M\Omega\times7.46fF)=2.13\ MHz$

Step 4: Calculate Gain-Bandwidth Product (GBW)

- Formula: $GBW=|A_v|\times BW$
- Calculation: $GBW=7.87\times2.13MHz=16.8\ MHz$

Cascode Amplifier

This analysis uses the final capacitance values for transistor M1.

Step 1: Given Values

- DC Gain (Av): -7.97
- Local Gain across Cgd1 ($A_{v,local}$): ≈ -1
- **Gate-Source Capacitance (Cgs) From ADT : 2.157 fF**
- **Gate-Drain Capacitance (Cgd) From ADT : 0.657 fF**

Step 2: Calculate Input Capacitance (Cin) The cascode structure reduces the Miller effect because the local gain is very small.

- Formula: $C_{in}=C_{gs}+C_{gd}(1-A_{v,local})$
- Calculation: $C_{in}=2.157fF+0.657fF\times(1-(-1))=2.157fF+1.314fF=3.47\ fF$

Step 3: Calculate Bandwidth (BW)

- Formula: $BW=1/(2\pi R_{sig}C_{in})$
- Calculation: $BW=1/(2\pi\times10M\Omega\times3.47fF)=4.59\ MHz$

Step 4: Calculate Gain-Bandwidth Product (GBW)

- Formula: $GBW=|A_v|\times BW$
- Calculation: $GBW=7.97\times4.59MHz=36.6\ MHz$

Parameter	Circuit	Hand Analysis	Simulation Results
DC Gain	Common Source	7.87	7.817
DC Gain	Cascode	7.97	8.02
Bandwidth (BW)	Common Source	2.13 MHz	1.722 MHz
Bandwidth (BW)	Cascode	4.59 MHz	3.099 MHz
GBW / UGF	Common Source	16.8 MHz	13.44 MHz
GBW / UGF	Cascode	36.6 MHz	24.8 MHz

- **DC Gain is Validated:** The hand analysis and simulation results for DC gain are in excellent agreement (both around **8**). The low gain is expected and correctly predicted because it is limited by the external **45 kΩ** load resistor.
- **Cascode Improves Bandwidth:** The primary conclusion is that the cascode amplifier significantly improves the circuit's speed in this configuration. It achieves a much higher bandwidth (**3.1 MHz**) and a superior Gain-Bandwidth Product by successfully eliminating the Miller effect that limits the common-source amplifier.