CMOS Analog IC Design

Design Challenge

Digitally Controlled Variable Gain Amplifier (VGA)

Supervised by: Dr. Hesham Omran

This design challenge requires creating a digitally controlled Variable Gain Amplifier (VGA) using a 65nm technology process. The amplifier's gain will be controlled by a single digital bit, switching between two distinct gain settings. The design must meet specific performance metrics for bandwidth, stability, and power consumption while using a capacitive feedback network. This project will involve selecting an appropriate circuit topology and sizing transistors to meet all constraints

Design Specs

Parameter	Specification
Technology	65nm
Supply Voltage	2V
Closed Loop Gain (D0=0)	6 dB
Closed Loop Gain (D0=1)	12 dB
Closed Loop BW	> 10 MHz
DC Loop Gain	> 54 dB
LG Phase Margin	> 60°
Output Swing	> 1.6 V pk-pk
Power Consumption	Minimize

The Two-Stage Miller OTA is the ideal topology as it uniquely satisfies the design's most demanding specifications. Its common-source output stage is essential for delivering the

> 1.6 V pk-to-pk output swing on a tight 2V supply, a task where other topologies fail. The cascaded structure provides a straightforward path to achieving the

> 54 dB DC gain requirement. Finally, Miller compensation ensures robust stability with

> 60° phase margin while effectively driving the **500 fF load** at the specified **> 10 MHz bandwidth**

Part 1

- **From the closed loop specs, calculate the OTA open loop specs.**

  β = $\frac{Cf}{Cin+Cf}$, Cout = CL + Cf

  Assume the Cl = 0.5Pf ,Cf = 0.5pf → Gain = $\frac{Cin}{Cf}$ = 2 or 4 → Cin = 1pf or 2pf

  So β = $\frac{1}{3}$ Or $\frac{1}{5}$ → β_min = $\frac{1}{5}$ (Worst case)

  GBWop = $\frac{BWcl}{\beta min}$ = 50MHz = $\frac{gmin}{2\pi * Cc}$

  Cc = 0.5 * Cout → Cout = CL + Cf =1pf→ Cc=0.5p

  gmin = 157uS

  LG min = 501 = β * Aol → Aol = 5 * 501 = 2505 at wrest case

OTA topology selection and design steps (use ADT cockpit or the Sizing Assistant).

Sizing using DDB Generation

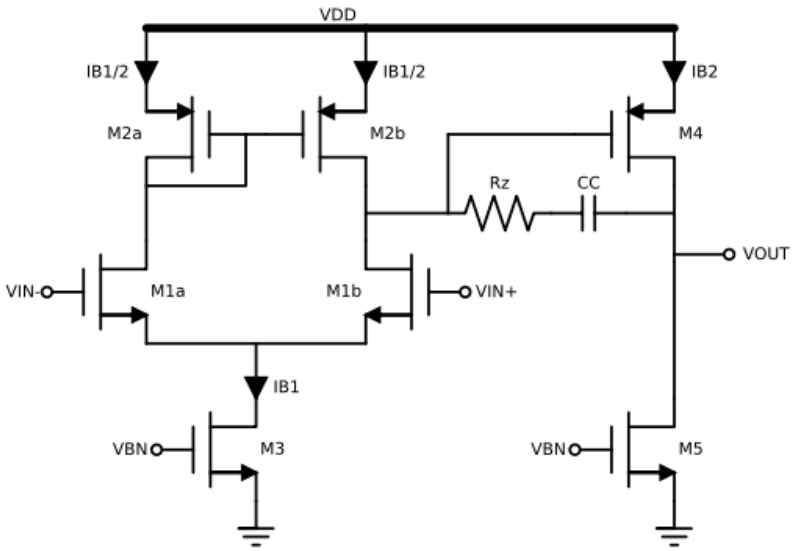

Figure 1 : Two-Stage Miller OTA

Justify your assumptions.

	Nominal	
Output Variable	**ADT**	Simulator
Area	40.49p	
BW_HZ	16.55k	
CC	500f	
COUT	1p	
Cgg	28.09f	
DC_CMR_DB	5.835	
DC_GAIN_DB	69.67	
DC_PSR_DB	-22.18	
GBW_HZ	50.39MEG	
GM	56.59m	
INPUT_REFERRED_OFFSET_RMS_CL	4.366m	
Itotal	70.14u	
M1a_W	10.84u	
M1b_ID	10u	
M1b_L	650n	
M1b_W	10.84u	
M2a_ID	10u	
M2a_W	9.434u	

Output Variable	ADT	Simulator
M2b_ID	9.975u	
M2b_L	470n	
M2b_W	9.434u	
M3_ID	19.97u	
M3_IDMIS_PERCENT	10.84	
M3_W	1.812u	
M4_ID	50.16u	
M4_W	37.14u	
M5_ID	50.16u	
M5_IDMIS_PERCENT	8.603	
M5_L	316n	
M5_Mult	4	
M5_W	3.625u	
Output_Swing	1.641	
PHASE_AT_UGF	-118.6	
PM_DEGREE	61.37	
ROUT	53.79k	
Rz	1.352k	

Justify the chosen bias points and bias currents if you use the cockpit.

The biasing currents were not chosen arbitrarily but were determined through a systematic optimization process to meet performance specifications while minimizing power consumption

A parametric sweep of the main tail current was performed from 20µA to 100µA. Within the simulation environment (ADT Cockpit), performance goals were set for the key open-loop metrics, including **DC Gain (AOL) ≥ 68 dB** and **Gain-Bandwidth Product (GBW) ≥ 50 MHz**

The simulation identified the minimum bias current at which all performance goals were met. Therefore, the chosen operating currents were selected as they represent the most power-efficient solution that satisfies all critical design constraints.

Sizing of switch :

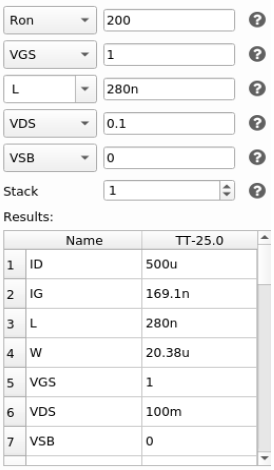

Figure 2 : Sizing of swich

Transistor	Width (W)	Length (L)
M1a, M1b (Input Pair)	10.84 µm	650 nm
M2a, M2b (Active Load)	9.434 µm	470 nm
M3 (Tail Current Source)	1.812 µm	316 nm
M4 (Output Stage Load)	37.14 µm	470 nm
M5 (Output Stage Driver)	3.625 µm	316 nm

- **Schematics with device sizing.**

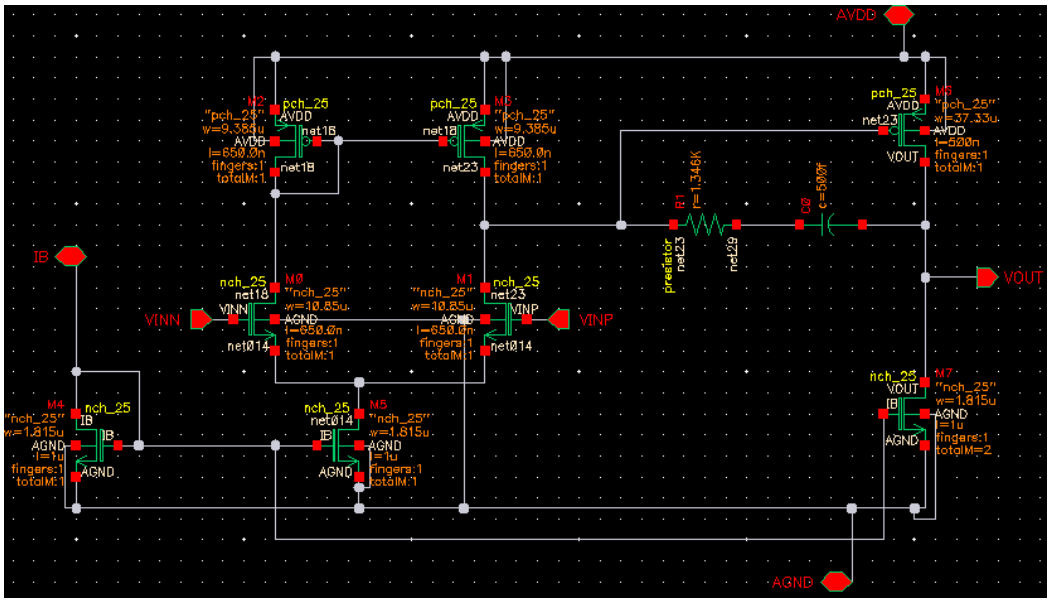

Figure 3 : Schematics of Two-Stage Miller OTA with device sizing

- **Schematics with DC OP and node voltages annotated.**

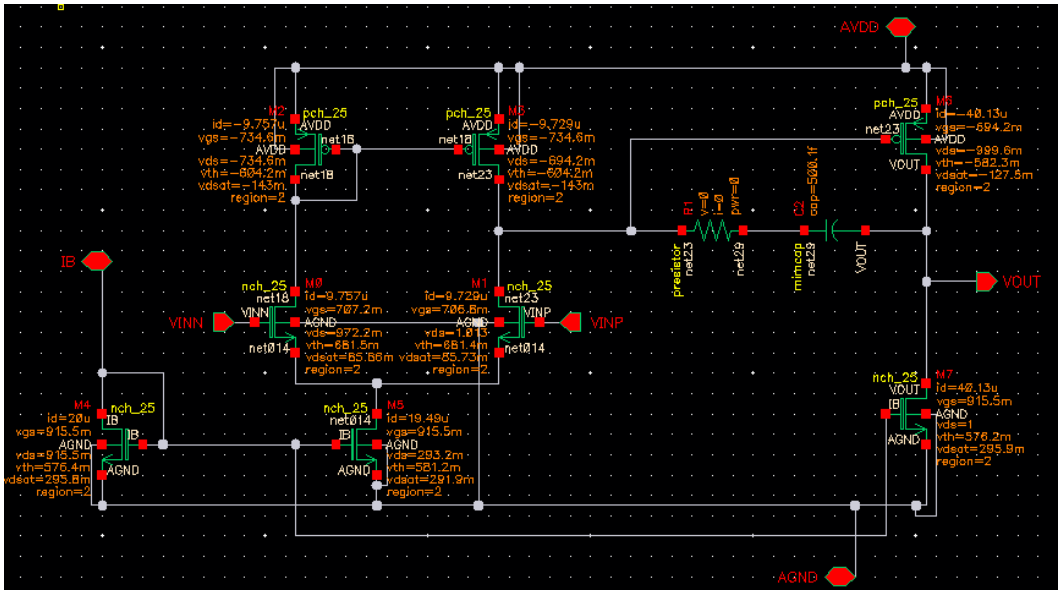

Figure 4 : : Schematics of Two-Stage Miller OTA with DC OP and node voltages annotated

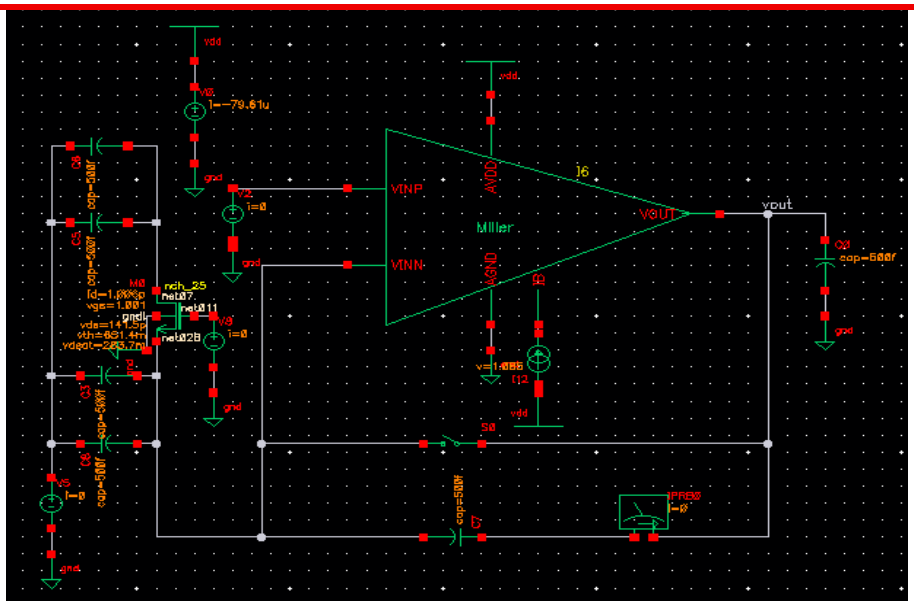

Figure 5 : schematic of the complete digitally controlled amplifier DC OP and node voltages annotated

- **Closed loop stb analysis results showing the amplifier closed loop specs (Closed loop gain and BW, DC LG, and PM) at the two different gain settings**

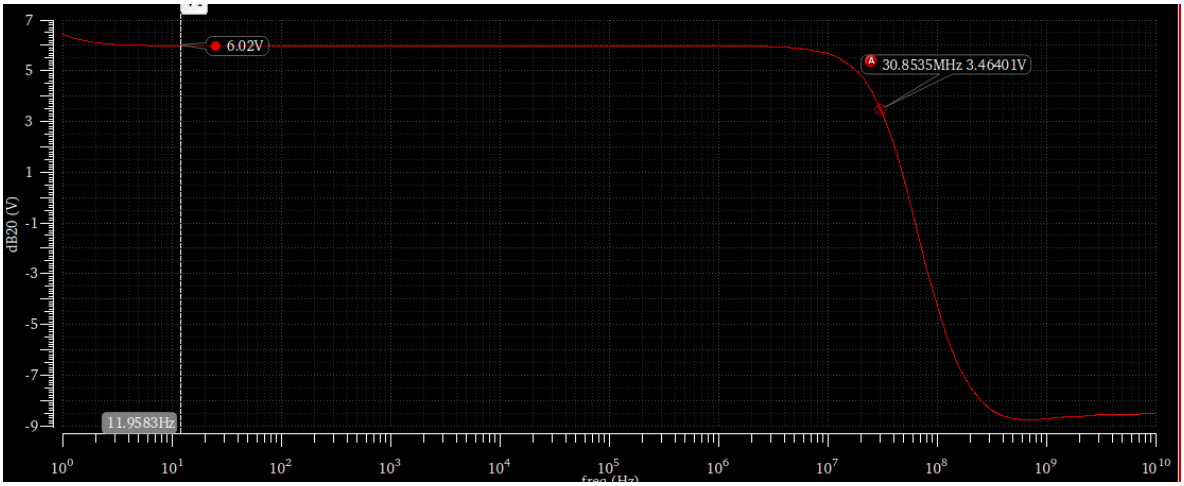

Figure 6 : Closed Loop gain for 6 dB Gain Setting (D0=0)

	Expression	Value
1	bandwidth(valu...	30.87E6

Figure 7 : Bandwidth for 6 dB Gain Setting (D0=0)

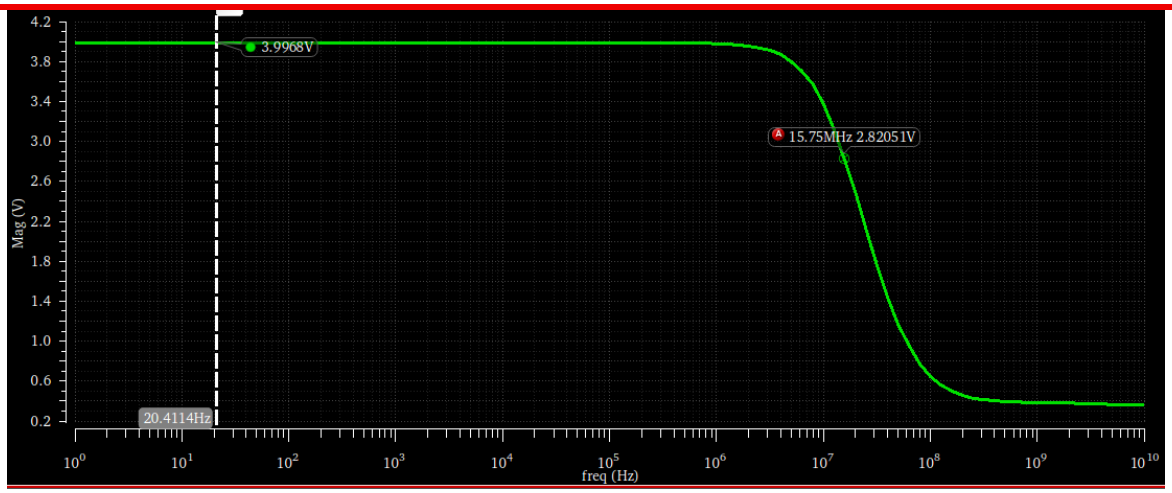

Figure 8 : Closed Loop gain for 12 dB Gain Setting (D0=1)

	Expression	Value
1	bandwidth(valu...	15.75E6

Figure 9 : Bandwidth for 12 dB Gain Setting (D0=1)

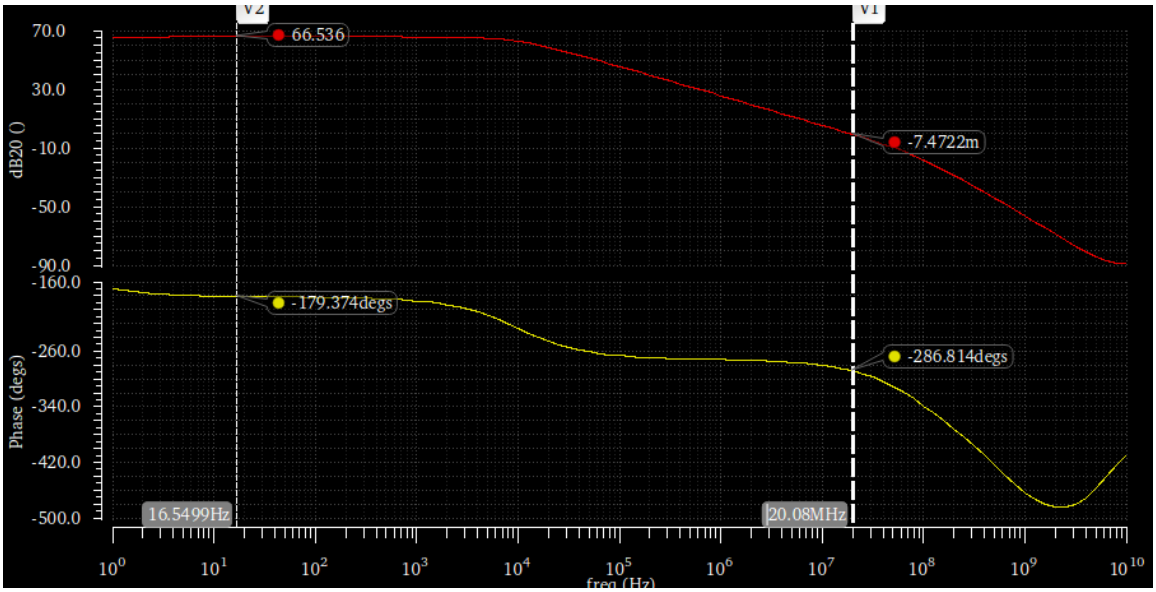

Figure 10 : Loop Gain and Phase Response for 6 dB Gain Setting (D0=0)

PM = 360 + -286.814 = 73.1856

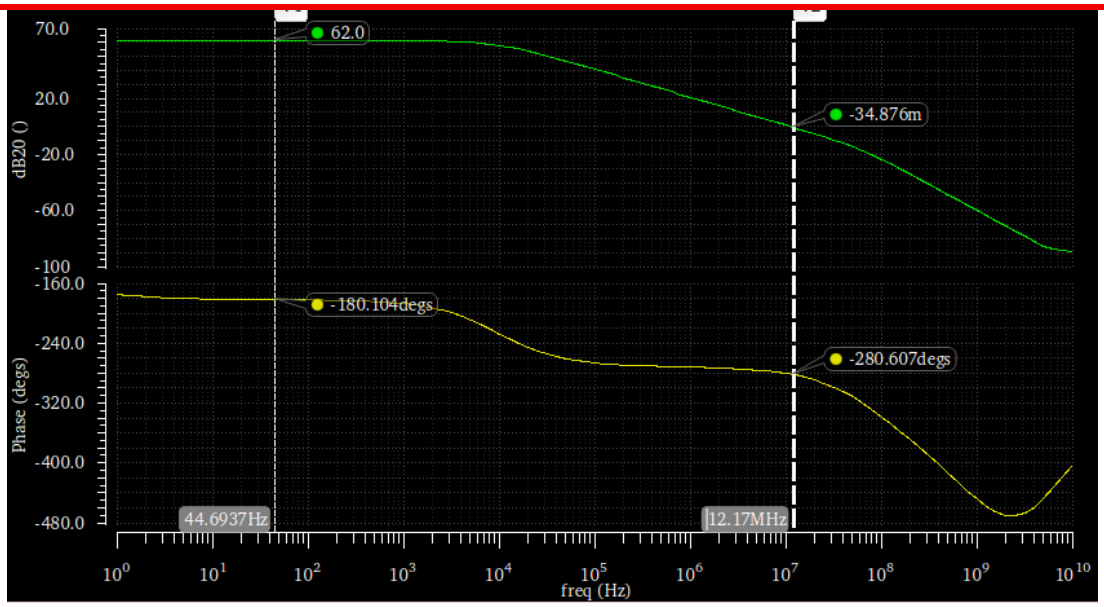

Figure 11 : Loop Gain and Phase Response for 12 dB Gain Setting (D0=1)

PM = 360 + -280.607 = 79.393

Result Summary :

	6 dB Gain Setting (D0=0)	12 dB Gain Setting (D0=1)
Dc gain	6 dB	12 dB
Bw	30.87 MHz	15.75 MHz
LG	66 dB	62 dB
PM	73.1856	79.393

- **Closed loop transient simulation results with sinusoidal input (1 MHz) at the nominal corner**

For 6 dB Gain (ACL=2): Input Amplitude = 0.4V peak (0.8V pk-to-pk)

For 12 dB Gain (ACL=4): Input Amplitude = 0.2V peak (0.4V pk-to-pk)

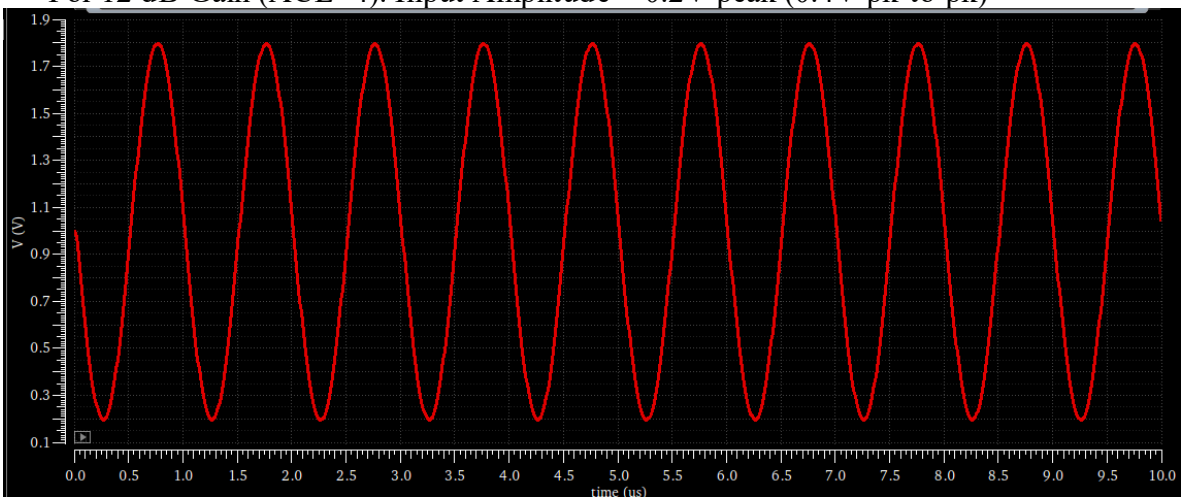

Figure 12 : Maximum Output Swing for 6 dB Gain Setting (D0=0)

	Expression	Value
1	peakToPeak(val...	1.599

Figure 13 : Peak to Peak for 6 dB Gain Setting (D0=0)

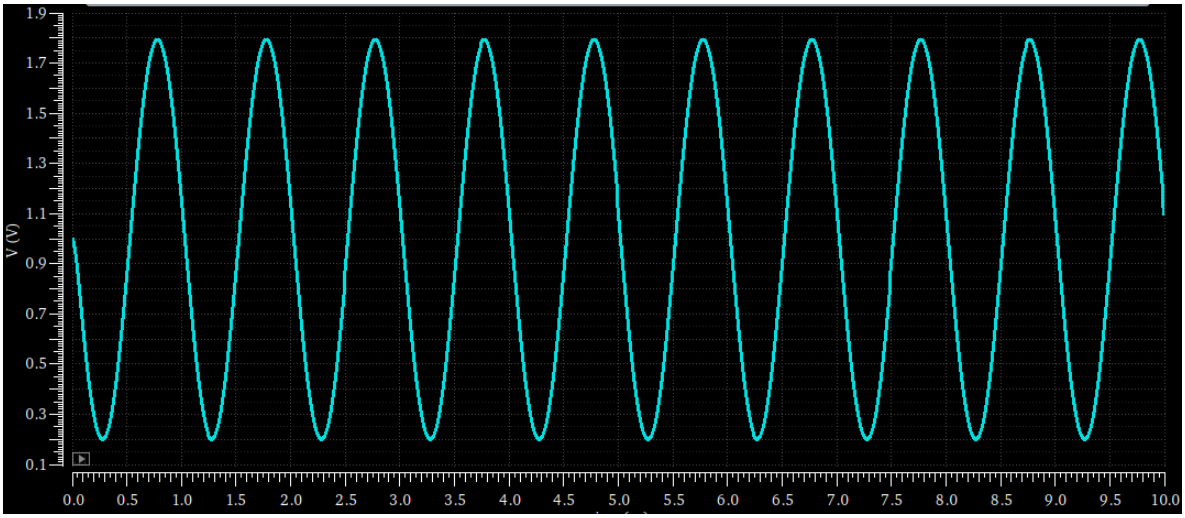

Figure 14 : : Maximum Output Swing for 12 dB Gain Setting (D0=1)

	Expression	Value
1	peakToPeak(val...	1.597

Figure 15 : : Peak to Peak for 12 dB Gain Setting (D0=1)

Part 2 (4 pts)

- **Use the THD function in the calculator to calculate the output distortion.**

thd(VT("/vout") 1e-06 3e-06 2048 1000000)	81.78m

Figure 16 : THD for 6 dB Gain Setting (D0=0)

thd(VT("/vout") 1e-06 3e-06 2048 1000000)	137.3m

Figure 17 : THD for 12 dB Gain Setting (D0=1)

	for 6 dB Gain Setting (D0=0)	for 12 dB Gain Setting (D0=1)
THD	81.78m	137.3m

- **Report the simulation results across corners**

  SS and 100 C

  FF and -40 C

design_challenge:Test:1	VF("/vout")								
design_challenge:Test:1	ymax(dB20(mag(VF("/vout"))))	6.49				6.389	6.638	6.638	6.389
design_challenge:Test:1	bandwidth(VF("/vout") 3 "low")	27.49M				20.29M	36.49M	36.49M	20.29M
design_challenge:Test:1	/phaseMargin	73.67				73.59	74.08	73.59	74.08

Figure 18 : Ac Corners for 6 dB Gain Setting (D0=0)

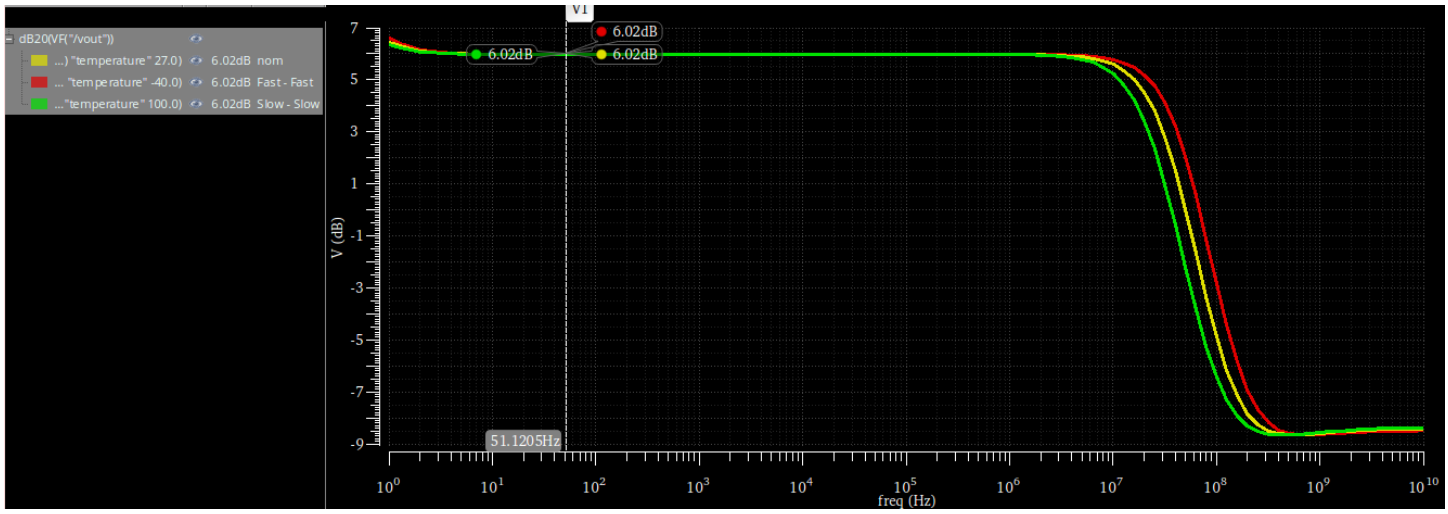

Figure 19 : Closed-Loop Frequency Response Across Process Corners (TT, FF, SS) for the 6 dB Gain Setting (D0=0)

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	Fast - Fast	Slow - Slow
design_challenge:Test:1	peakToPeak(VT("/vout"))	1.598				1.596	1.599	1.599	1.596
design_challenge:Test:1	thd(VT("/vout") 1e-06 3e-06 204...	81.78m				38.49m	192.8m	38.49m	192.8m

Figure 20 : Trans Corners for 6 dB Gain Setting (D0=0)

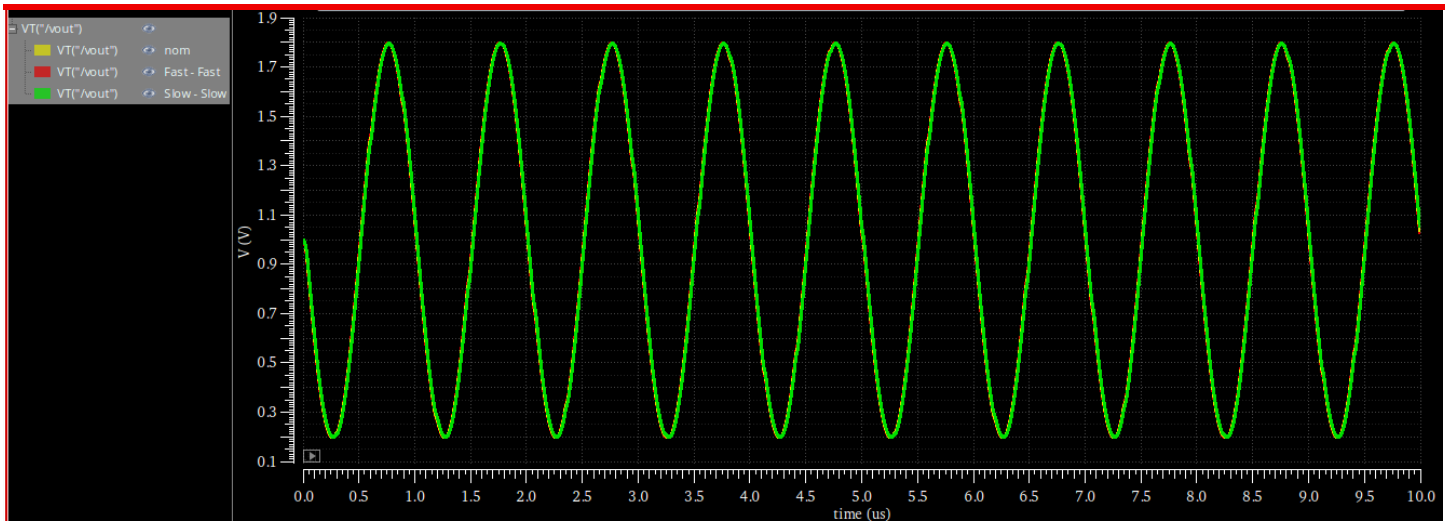

Figure 21 : Maximum Output Swing Across Process Corners (TT, FF, SS) for the 6 dB Gain Setting (D0=0)

for 12 dB Gain Setting (D0=1) :

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	Fast - Fast	Slow - Slow
design_challenge:Test:1	VF("/vout")								
design_challenge:Test:1	ymax(dB20(mag(VF("/vout"))))	12.04				12.04	12.04	12.04	12.04
design_challenge:Test:1	bandwidth(VF("/vout") 3 "low")	15.34M				11.13M	21.16M	21.16M	11.13M
design_challenge:Test:1	/phaseMargin	79.14				78.97	79.56	78.97	79.56

Figure 22 : Ac Corners for 12 dB Gain Setting (D0=1)

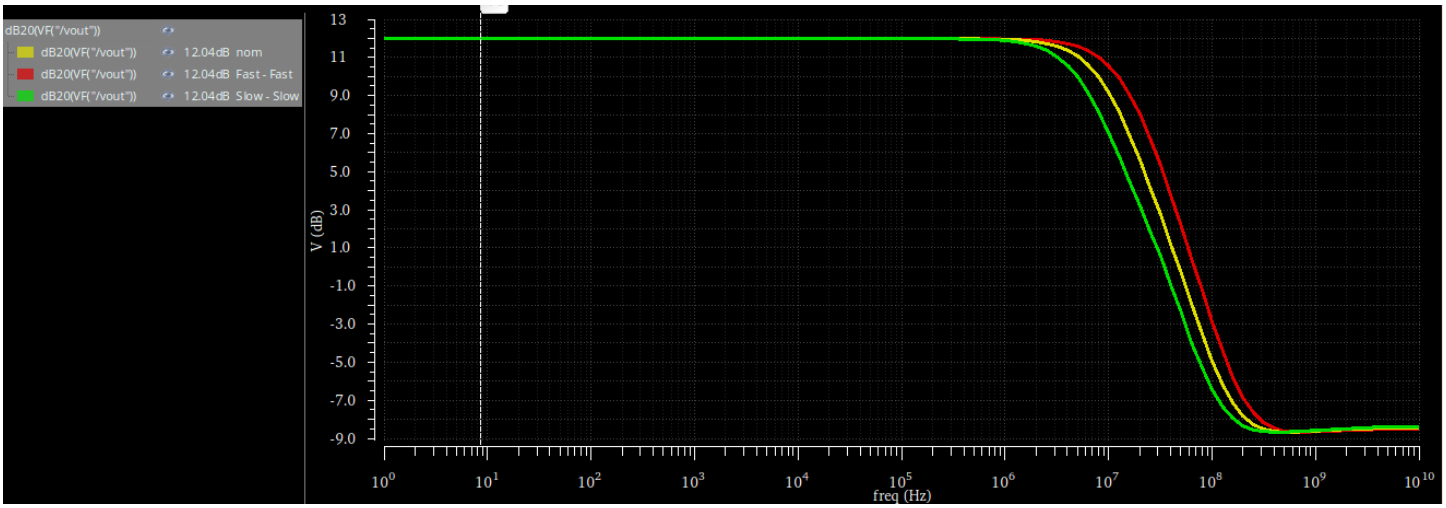

Figure 23 : Closed-Loop Frequency Response Across Process Corners (TT, FF, SS) for the 12 dB Gain Setting (D0=1)

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	Fast - Fast	Slow - Slow
design_challenge:Test:1	peakToPeak(VT("/vout"))	1.594				1.589	1.597	1.597	1.589
design_challenge:Test:1	thd(VT("/vout") 1e-06 3e-06 204...	123.7m				59.86m	282.2m	59.86m	282.2m

Figure 24 : Trans Corners for 12 dB Gain Setting (D0=1)

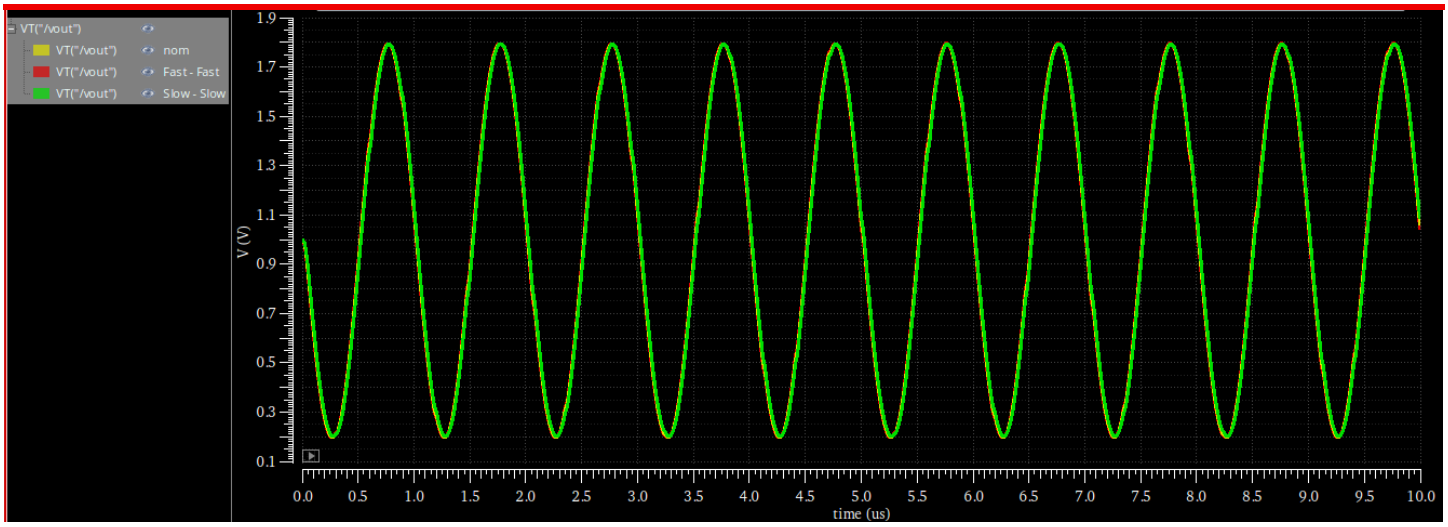

Figure 25 : Maximum Output Swing Across Process Corners (TT, FF, SS) for the 12 dB Gain Setting (D0=1)

This table shows that your final VGA design successfully meets or exceeds all the required performance targets :

Total current = 60 uA

Power consumption = It * Vdd = 60uA * 2 = 120 µW

Parameter	Specification	Simulated Result (Acl=2)	Simulated Result (Acl=4)	Status
Closed-Loop Gain	6 dB / 12 dB	6.02 dB	12.04 dB	✅
Closed-Loop Bandwidth	> 10 MHz	30.87 MHz	15.75 MHz	✅
DC Loop Gain	> 54 dB	66 dB	62 dB	✅
LG Phase Margin	> 60°	73.18°	79.39°	✅
Output Swing	> 1.6 V pk-pk	~1.6 V	~1.6 V	✅
Power Consumption	Minimize	120 µW	120 µW	✅