CMOS Analog IC Design

Lab 2

Common Source Amplifier

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PART 1: Sizing Chart

Design Specifications

The objective is to design a resistive-loaded Common Source (CS) amplifier with the following specifications:

- DC Gain: -10
- Supply Voltage (VDD): 2.5 V
- Current Consumption (IDQ): 10 µA

Feasibility Check and Initial Calculations

Voltage gain is approximated by:

$$|Av| \approx (2 \times VRD) / Vov$$

Assuming VRD = 1 V and desired gain |Av| = 10:

$$Vov = (2 \times 1) / 10 = 0.2\ V$$

This overdrive voltage is reasonable.

Calculate RD:

$$RD = VRD / IDQ = 1\ V / 10\ \mu A = 100\ k\Omega$$

V* Parameter

To compensate for MOSFET non-idealities, use:

$$V^* = 2ID / gm$$

Rewriting the gain:

$$|Av| \approx (2 \times VRD) / V^*$$

For VRD = 1 V and |Av| = 10:

$$V^*_Q = 0.2\ V$$

Choosing Transistor Length (L)

To ensure ro ≫ RD, choose a long channel length:

$$L = 2\ \mu m$$

Generate and Use Sizing Charts

Perform VGS sweep in ADT with:

W = 40 µm, L = 2 µm, VDS = 1.5 V

For Nmos :

Plot the v* and Vov

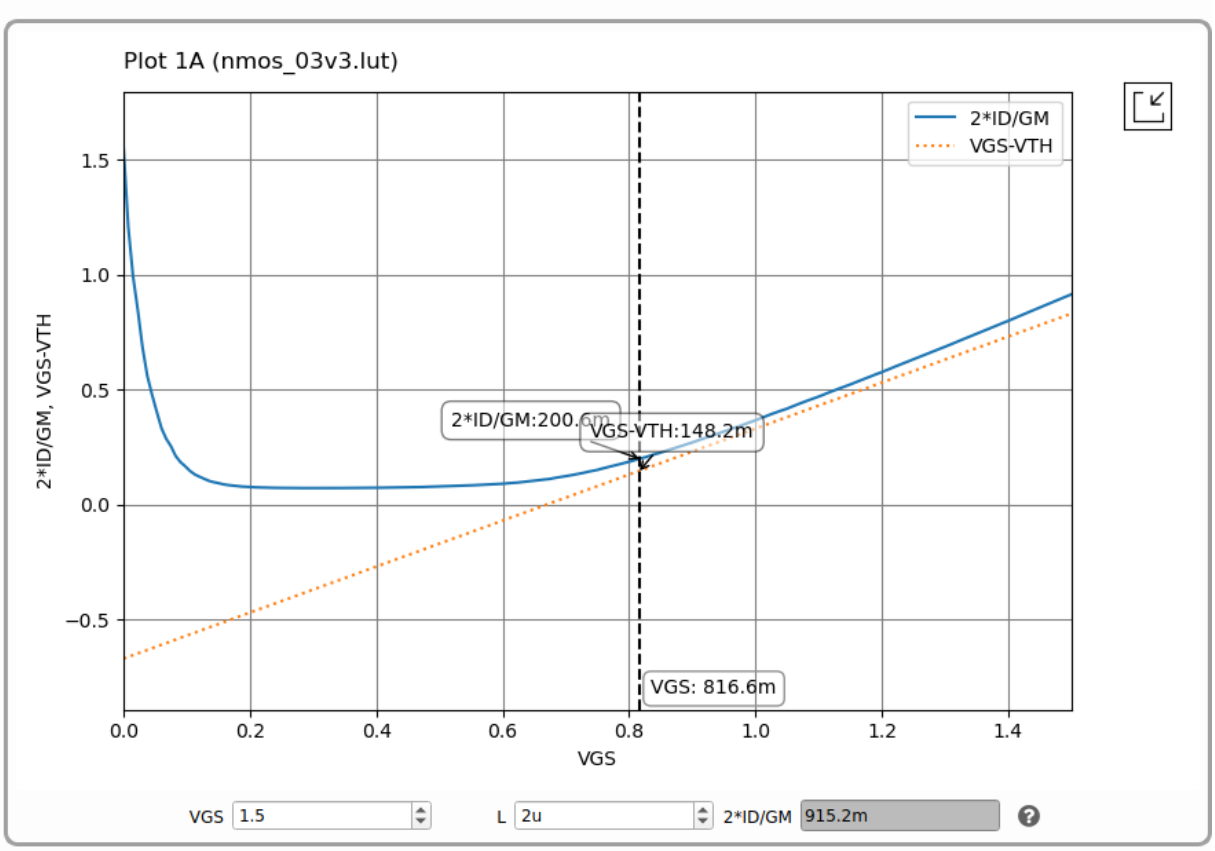


Figure 1 : Overlay plot of V and Vov vs VGS from simulation*

VGSQ = 816.6 mV

VovQ = 148.2 mV

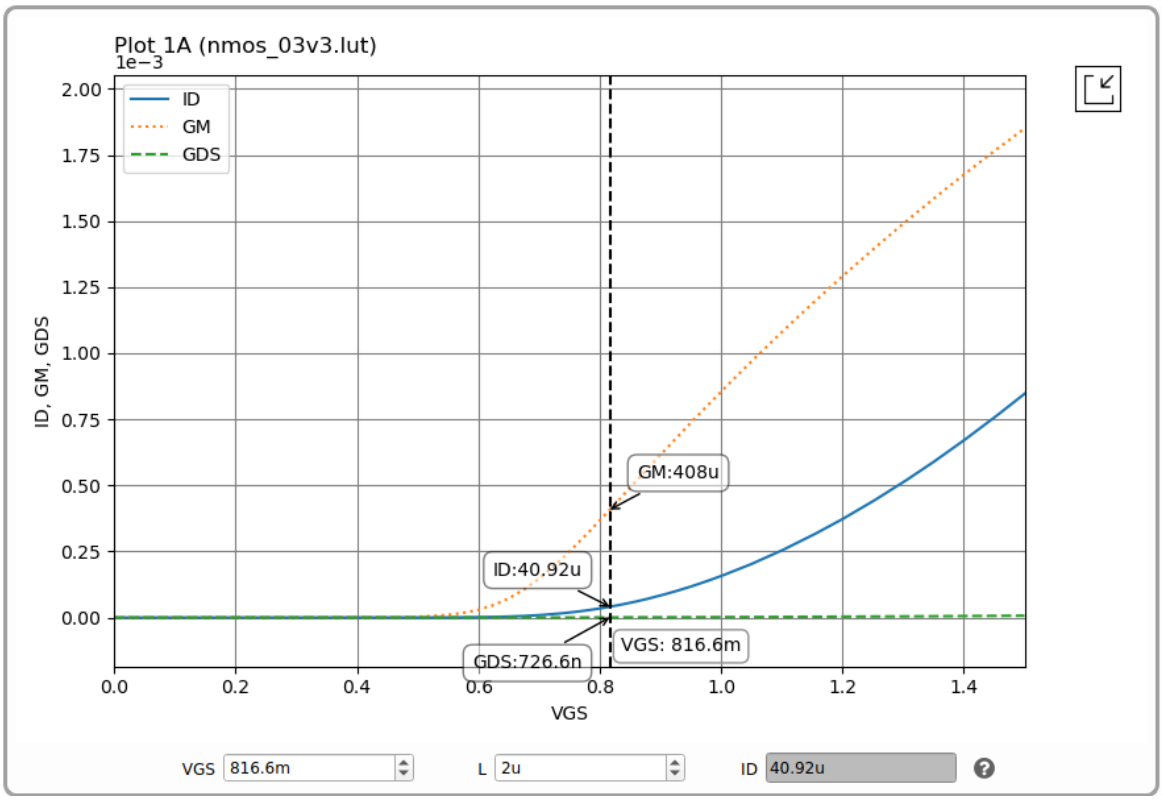


Figure 2 : plot of ID, gm, and gds vs. VGS from ADT.

ID_X = 40.92 uA

Gm_x = 408 uS

Gds_x = 726.6 nS

Then we will calculate the W

W_new = 40u *10u/40.92 = 9.775 um

Now we will use a new method to calculate W in ADT :

For NMOS :

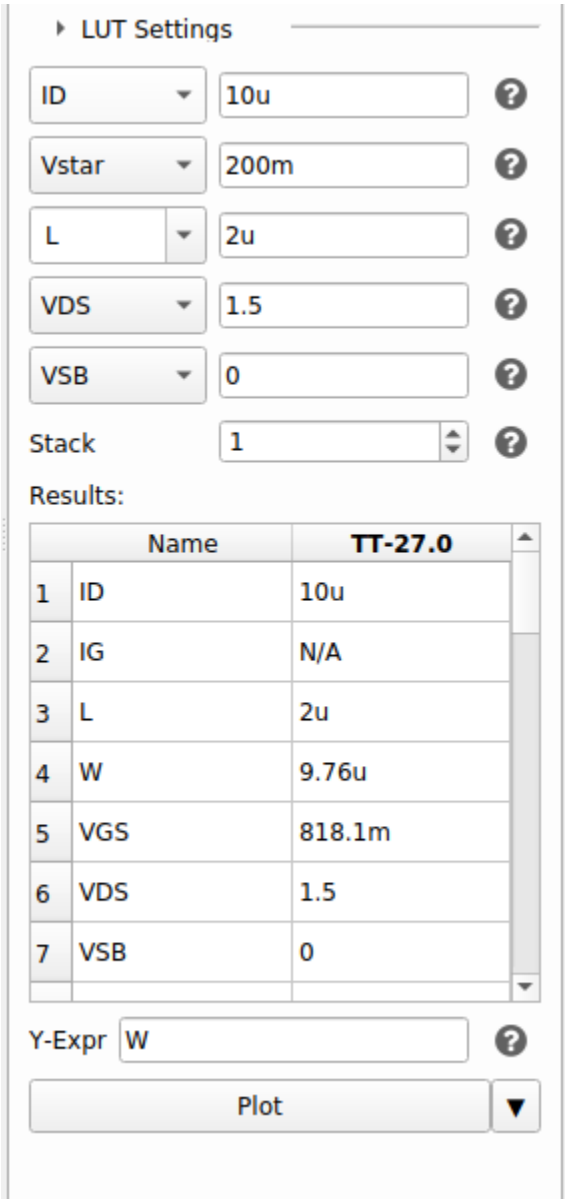


Figure 3 : calculate W from ADT

W = 9.76 um

VGS = 818.1 mV

For Pmos :

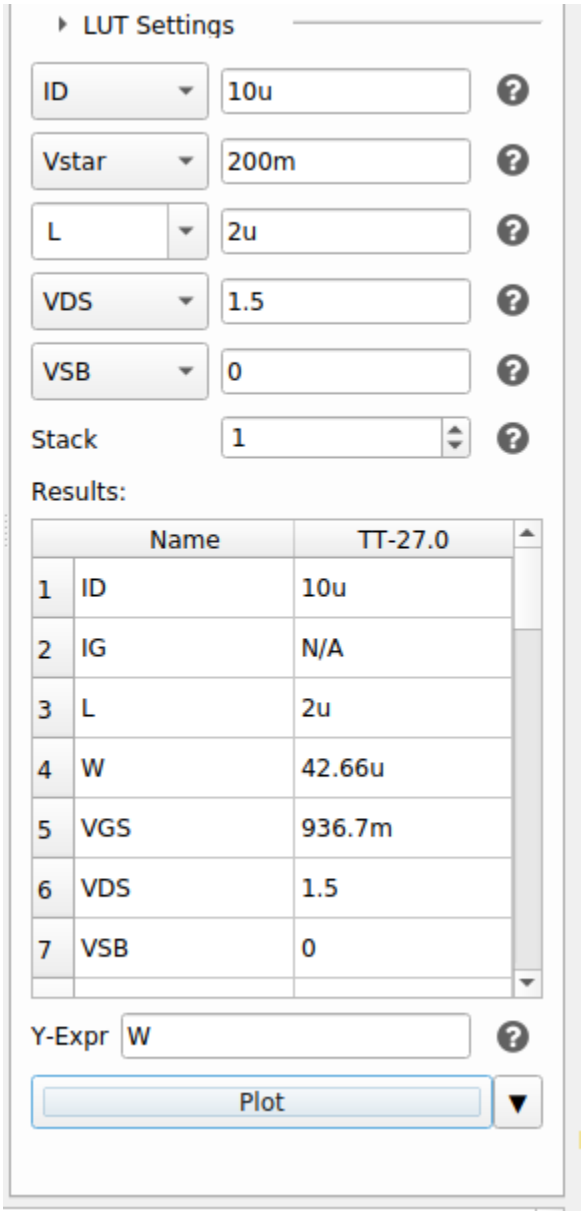


Figure 4 : calculate W from ADT

W = 42.66 um

VGS = 936.7 mV

PART 2: CS Amplifier

Schematic :

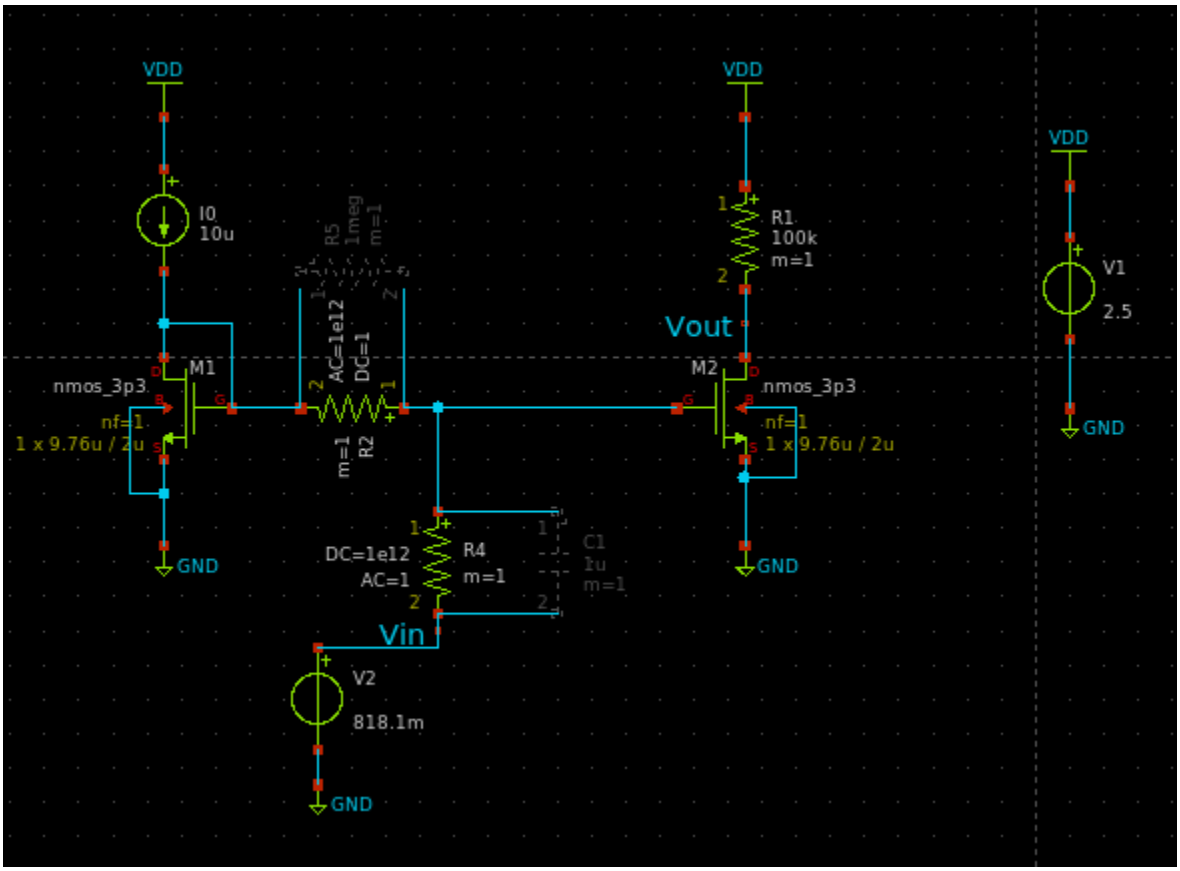


Figure 5 : Schematic of the CS amplifier with a replica biasing circuit.

OP Analysis :

1. Create a new folder for Lab 02 and place the xschemrc file in it.

2. Create the testbench schematic using the designed values of RD, W, and L.

3. Use replica biasing (M2 for I-to-V, M1 for V-to-I). Avoid voltage-mode biasing due to sensitivity to VTH variations.

4. Use 'res_ac' elements for switching between DC and AC connections to M1 gate.

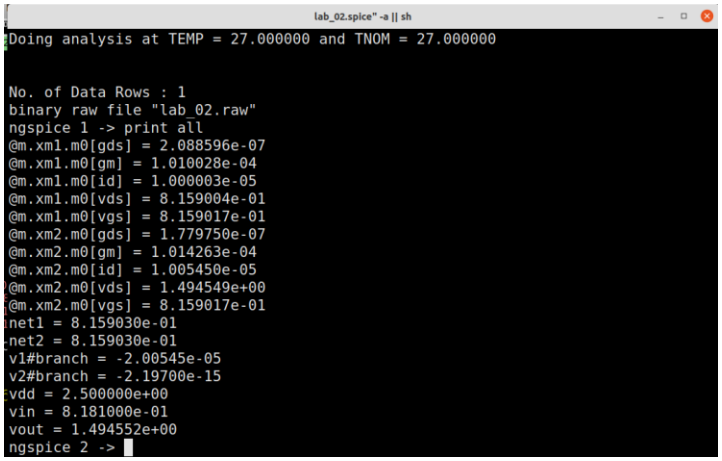
5. Run DC Operating Point (OP) analysis using the following control block:

Code :

```
.control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
op
write lab_02.raw
.endc
```

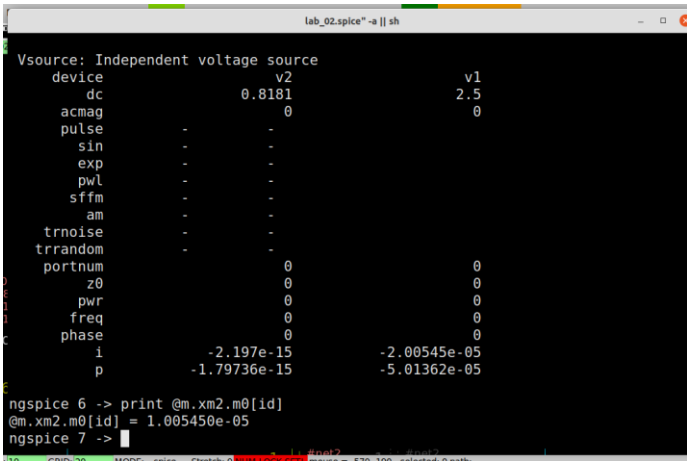
First way to show OP results :

Using print all



And using show all

print @m.xm2.m0[id]



2nd & 3rd ways to show op results :

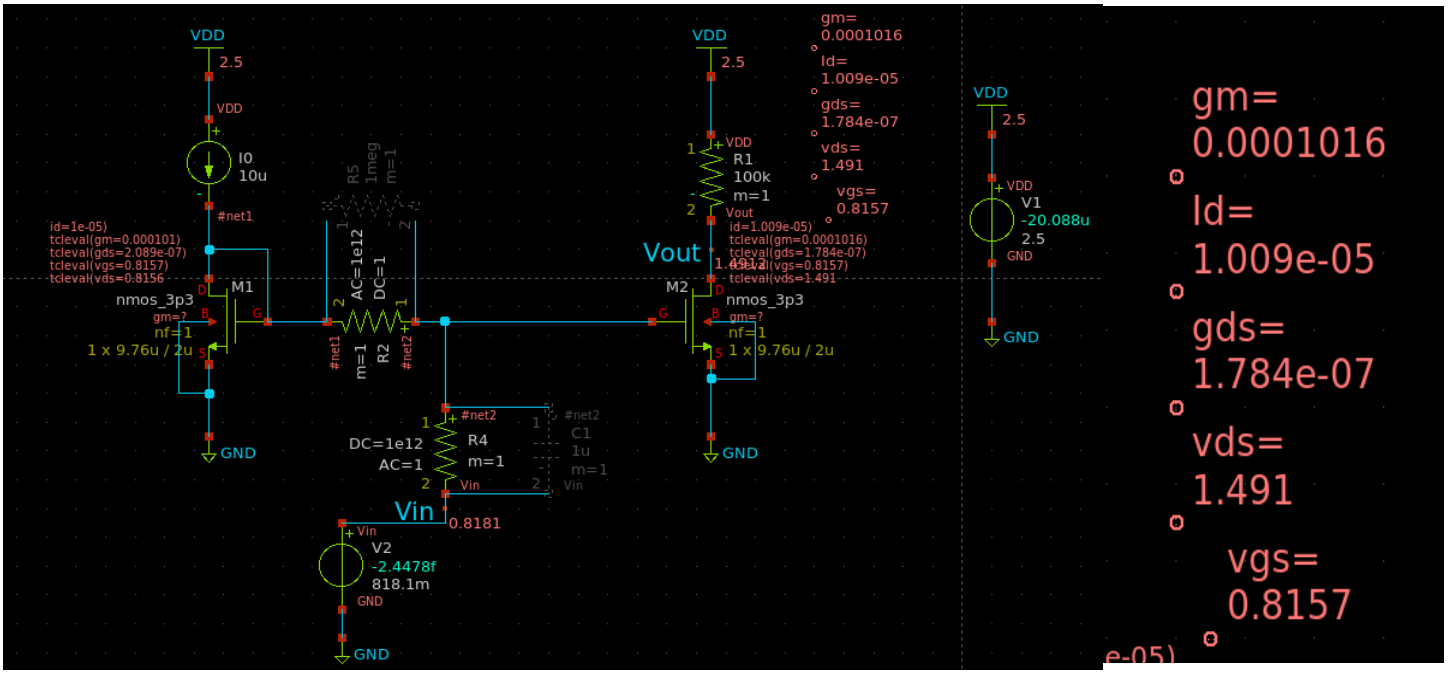


Figure 6 : Schematic with OP Annotation with two display methods

Report a snapshot for the key operating point (OP) parameters. Compare the results with the results you obtained in Part 1. Since we used design charts, the results should agree well.

Table one Comparing the results :

Parameter	Part 1 (ADT)	Part 2 (Xschem)	% Difference
Id	10.0 µA	10.09 µA	0.90%
VGS	818.1 mV	815.7 mV	0.29%
VDS	1.5 V	1.491 V	0.60%
gm	99.17 µS	101.6 µS	2.45%
gds	176.7 nS	178.4 nS	0.96%

Compare ro and RD. Is the assumption of ignoring ro justified in this case? Do you expect the error to remain the same if we use min L ?

ro = 1/gds = 1/178.4e-9 = 5.61 MΩ
ro/Rd =56 then ro >> Rd can ignore

if minimum (L) is used, ro significantly decreases due to stronger channel length modulation, and the approximation becomes inaccurate, introducing noticeable gain error.

Calculate the intrinsic gain of the transistor ?
|Av| = gm r o = 569.5

What is the relation (≪,,≫) between the amplifier gain and the intrinsic gain?
amplifier gain = |Av| = gm Rd ≈ 10
intrinsic gain = |Av| = gm ro = 569.5

amplifier gain << intrinsic gain

AC Analysis :

Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz).

Code :

```
.control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
save @m.xm1.m0[ro]
save @m.xm2.m0[id]
save @m.xm2.m0[gm]
save @m.xm2.m0[gds]
save @m.xm2.m0[vgs]
save @m.xm2.m0[vds]
save @m.xm2.m0[ro]
*op
ac dec 10 1 10g
remzerovec
write lab_02.raw
.endc
```

vout gain magnitude (in dB):

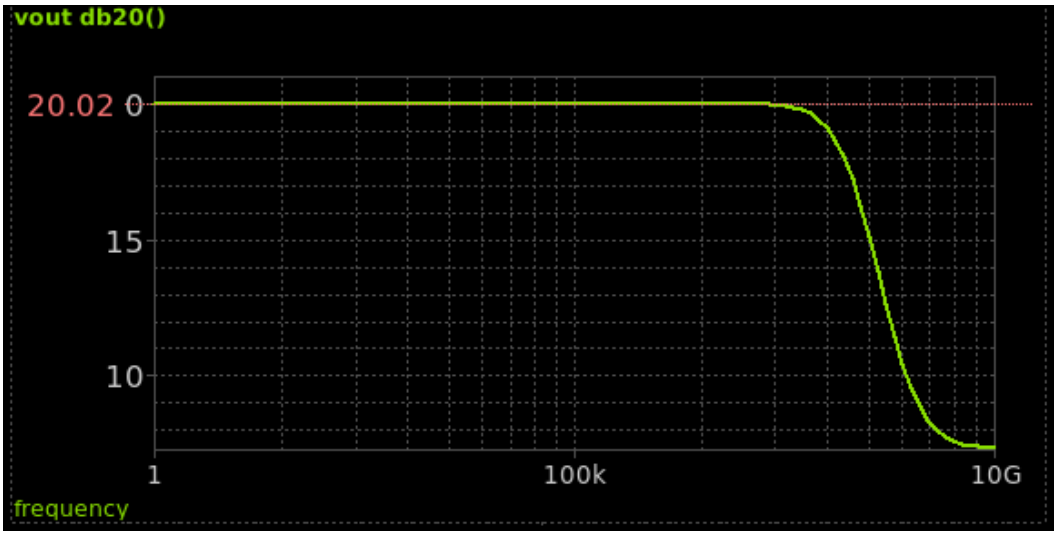


Figure 7 : vout gain magnitude AC simulation

DC gain ≈ -10

Gain Non-Linearity (Large Signal Operation DC Sweep) :

Change the testbench to perform large signal input sweep. Here we want the DC input to be directly applied to the amplifier input.

Schematic :

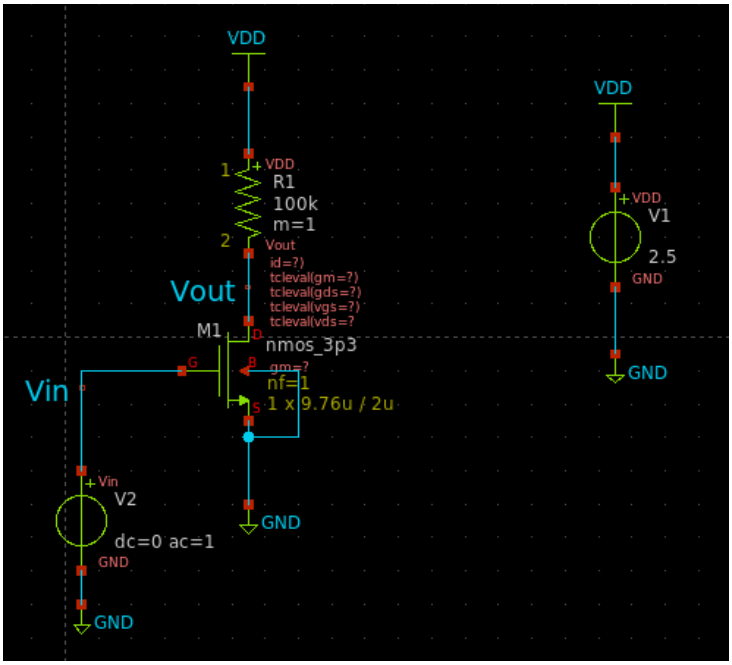


Figure 8 : Schematic of the CS amplifier with a direct DC voltage input.

Code :

```
. control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
*op
*ac dec 10 1 10g
dc V0 0 2.5 10m
remzerovec
write lab_02_dc.raw
.endc
```

Report VOUT vs VIN

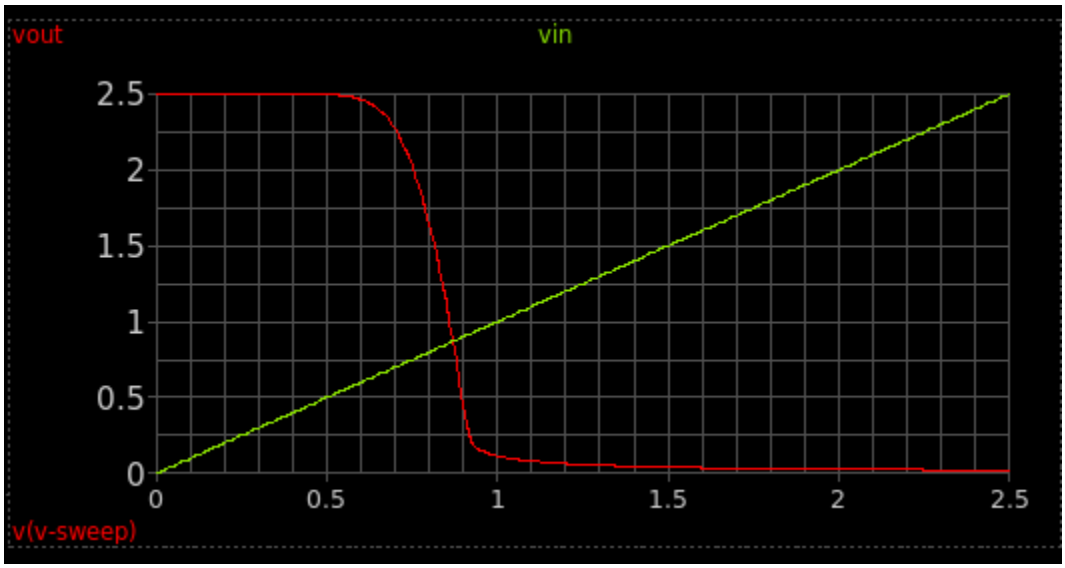


Figure 9 : VOUT vs VIN

Is the relation linear? Why?

No, the relationship is highly non-linear. Amplification only occurs within a small range around the DC bias point. Outside this range, the output is clipped as the transistor enters cutoff or triode regions.

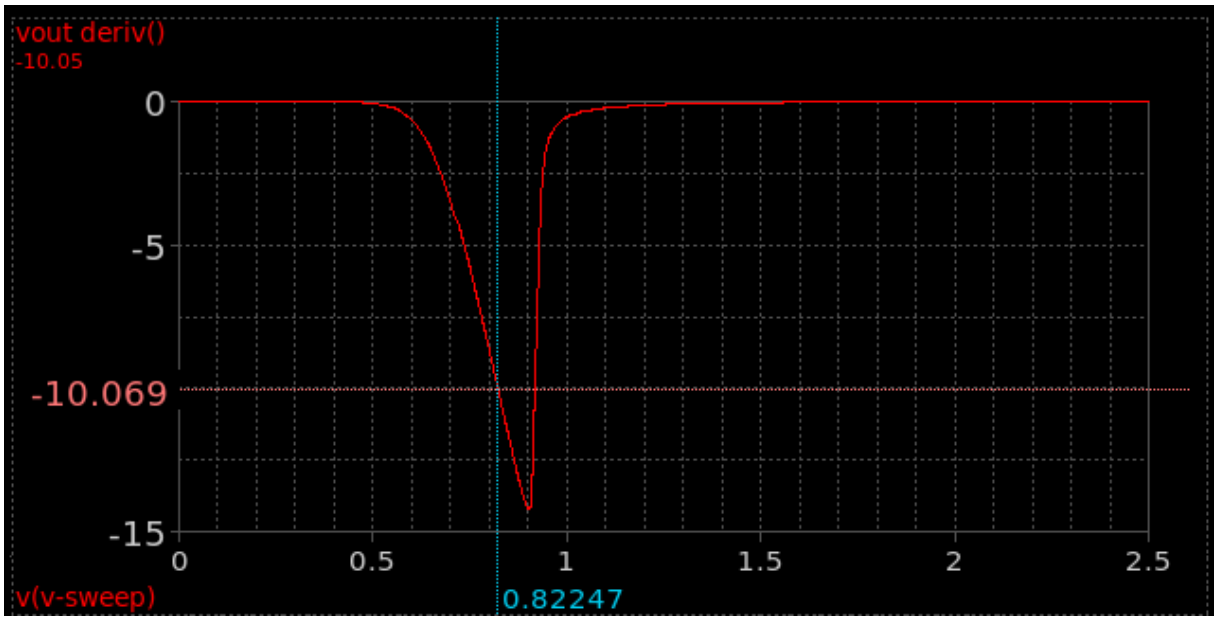


Figure 10 : Derivative of VOUT shows nonlinear gain

Is the gain linear (independent of the input, i.e., constant vs VIN)? Why?

No, the gain is not linear — it changes with VIN.
It peaks near the operating point and drops outside that region.

Gain Non-Linearity (Transient Analysis) :

Schematic :

Add:

- Large resistance (RFC) to pass DC bias
- Large coupling capacitor for AC signal (pF-range)

Apply input:

sin(0 10m 1meg)

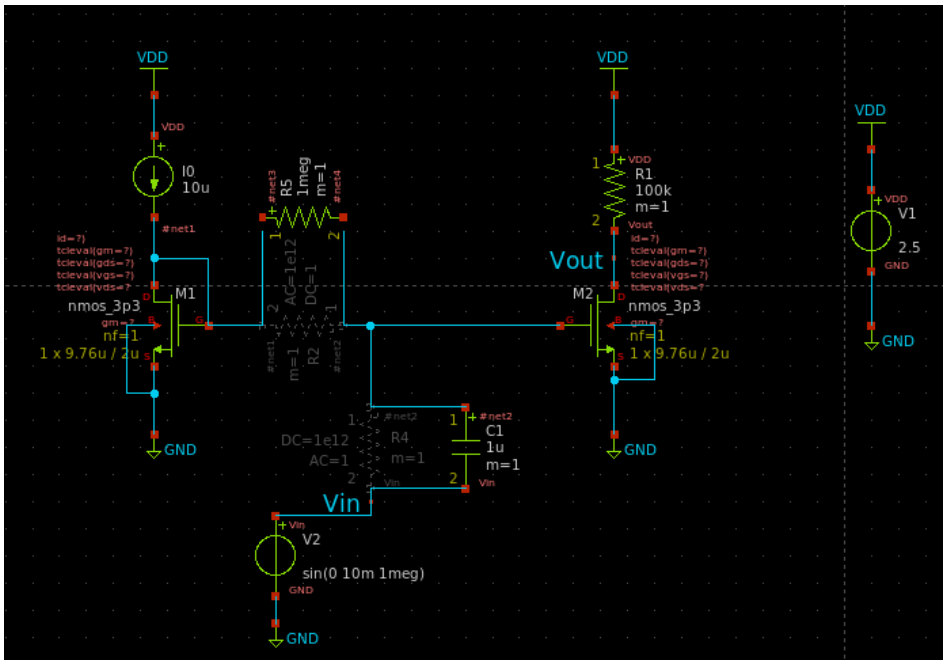


Figure 11 : Schematic of the CS amplifier with an AC-coupled input signal.

Code :

```
.control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
tran 0.1u 2u
remzerovec
write lab_02_tran.raw
.endc
```

Report vin, vout, and gm vs time.

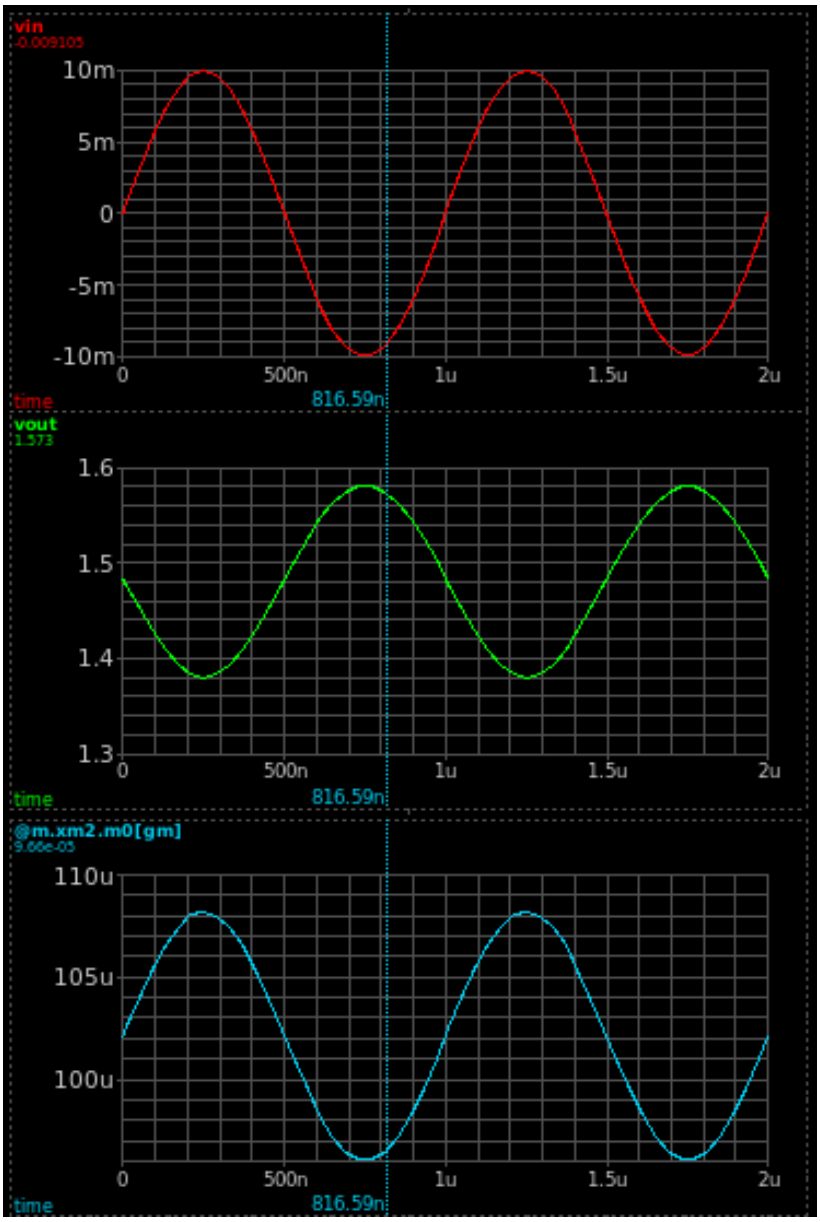


Figure 12 : vin, vout, and gm vs time.

Does gm vary with the input signal? What does that mean? Is this amplifier linear?

Yes, gm varies with the input signal.

This means the amplifier is **nonlinear**, since gain depends on the input amplitude.

Not linear

Gain Linearization (Negative Feedback) :

Schematic :

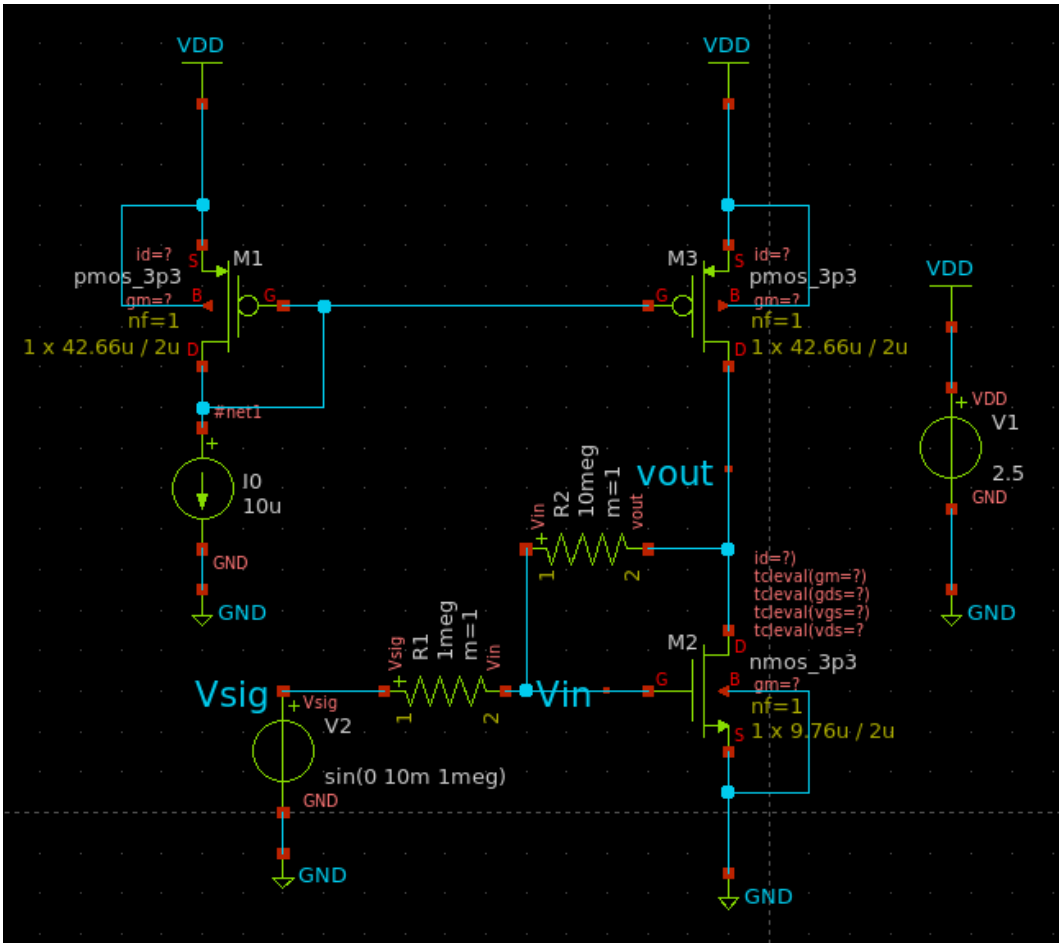


Figure 13 : Schematic of the CS amplifier with an active load and negative feedback.

Code :

```
.control
save all
save @m.xm1.m0[id]
save @m.xm1.m0[gm]
save @m.xm1.m0[gds]
save @m.xm1.m0[vgs]
save @m.xm1.m0[vds]
dc V0 0 2.5 10m
remzerovec
write lab_02_feedback.raw
.endc
```

VIN and VOUT vs VSIG (overlaid) & VOUT derivative vs VSIG :

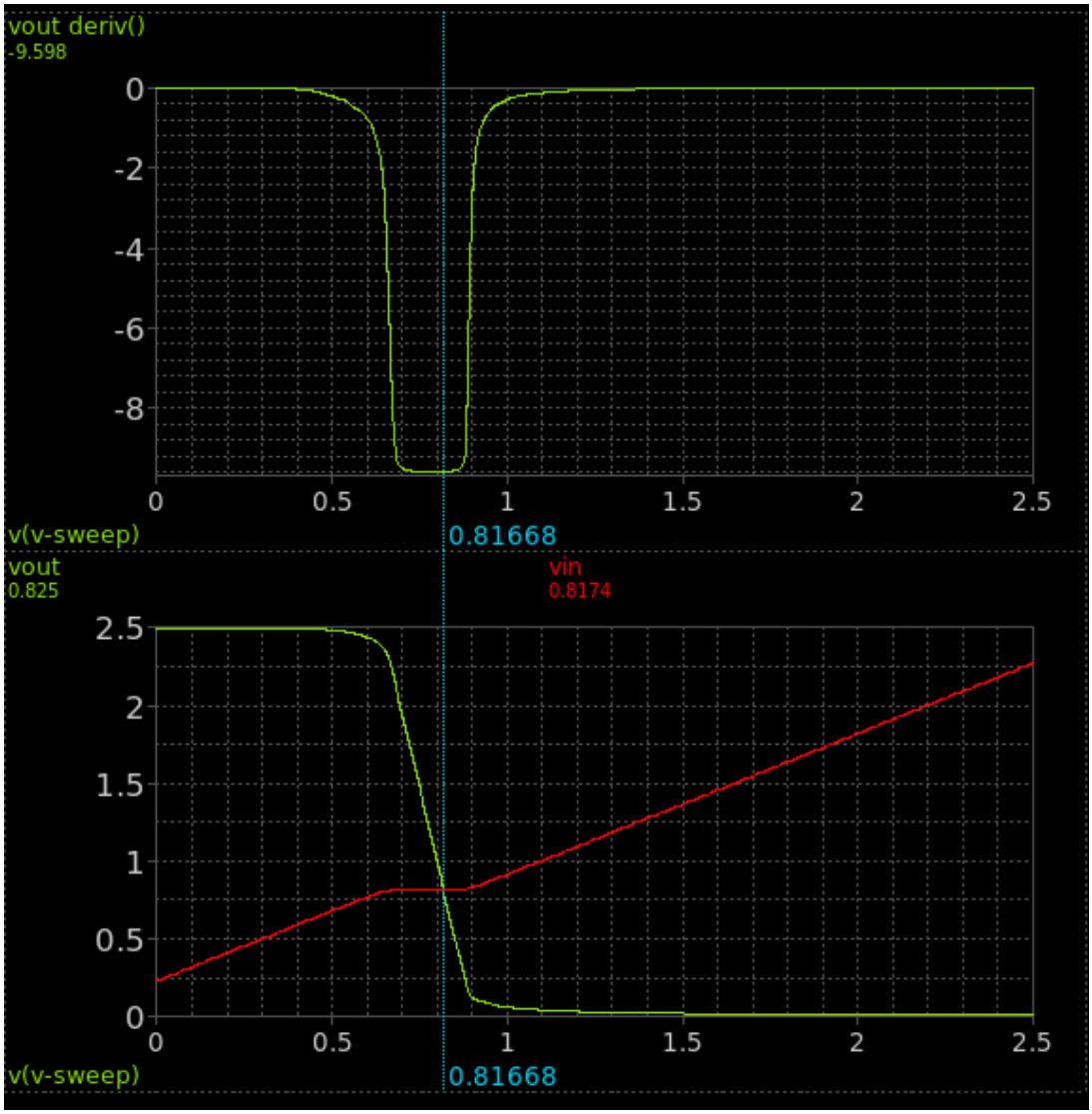


Figure 14 : VIN, VOUT, and VOUT derivative vs VSIG.

Is VOUT vs VSIG linear in the operating range of the amplifier? Why?

Yes, VOUT vs VSIG is approximately linear within the operating range of the amplifier.
Because in that range, the transistor operates in saturation and negative feedback keeps the gain stable, making VOUT change proportionally with VSIG.

Is the gain linear (independent of the input) in the operating range of the amplifier? Why?

Yes, the gain is approximately linear in the operating range of the amplifier.

Why?

Because within this range, the transistor stays in saturation and negative feedback keeps VIN nearly constant, making the gain (dVOUT/dVSIG) stable and input-independent.

VIN is almost constant in the operating range of the amplifier. What is its value? Why?

Vin = 816.68mv **≈ VGSQ**

Because negative feedback adjusts VOUT to keep VIN steady, ensuring the transistor stays in saturation for consistent amplification.

Analysis :

The linear input range is approximately:

Vin_range = VDD−2V∗ /|Av|

With VDD = 2.5V, V = 200 mV, and |Av| = 10

input range ≈ 0.21 V

This matches the simulation, where the gain is constant only within ±105 mV around VGSQ.

Run a transient simulation and report gm vs time. Compare this plot to the plot you previously obtained from the resistive loaded open-loop amplifier.

First we will change the sin(0 10m 1meg) to sin (VGS_Q 10m 1meg) -> (816.6m 10m 1meg)

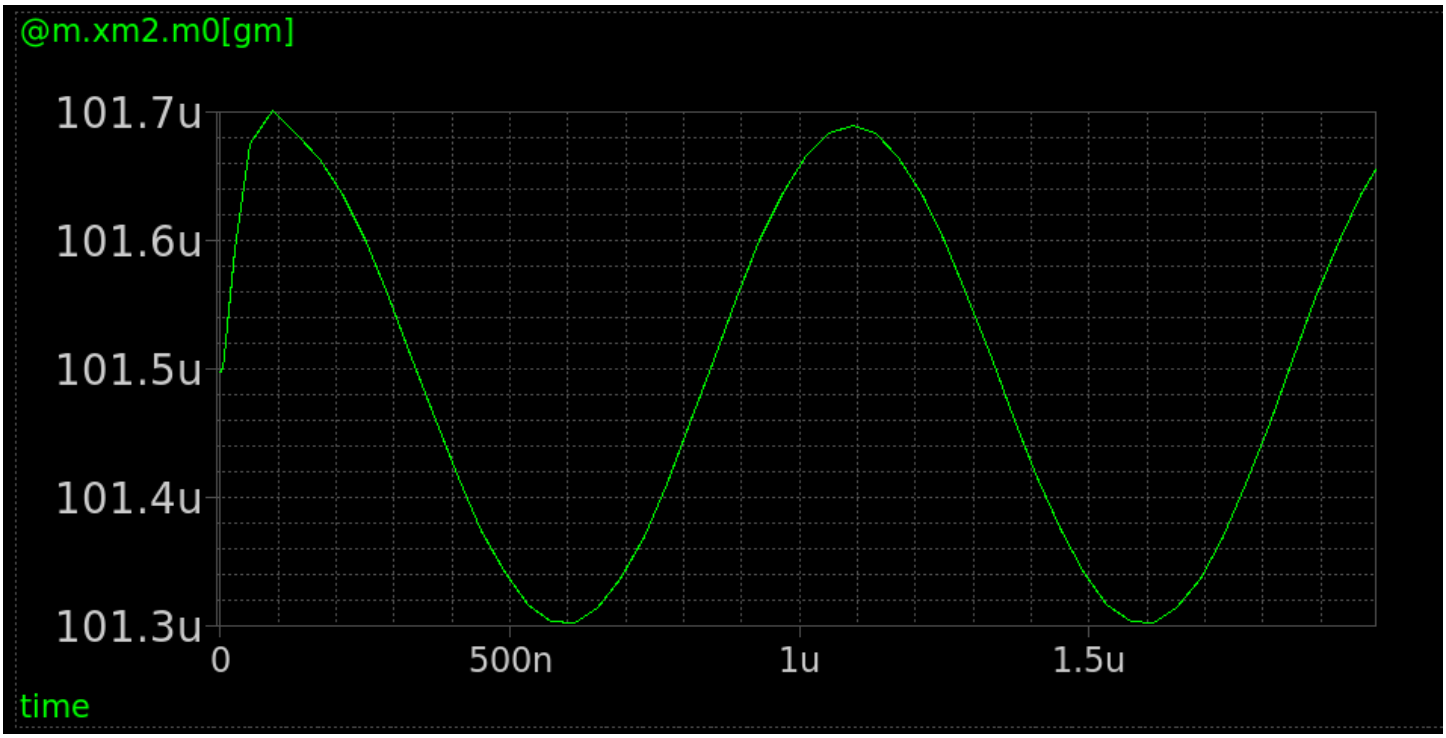


Figure 15 : Feedback Plots and gm Comparison

Comparison Between Feedback Amplifier and Open-Loop Amplifier Plots

1. **gm Behavior:**
    - **Open-loop (resistive load):**
        - gm **varies significantly** with the input signal.
        - As VIN changes, the MOSFET moves between cutoff, saturation, and triode → gain is **nonlinear**.
    - **With Feedback:**
        - gm stays **much more constant** throughout the input sweep.
        - Negative feedback stabilizes VIN near VGSQ → transistor remains in saturation → **gain is linearized**.
2. **Gain (dVOUT/dVSIG):**
    - **Open-loop:**
        - Gain is **peaked** near the quiescent point and drops off outside that narrow region.
    - **With feedback:**
        - Gain is **flat and consistent** across a wider input range.