CMOS Analog IC Design

Lab 7

gm/ID Design Methodology

5T_OTA design

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Part 1: gm/ID Design Charts

Using ADT Device Xplore, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS = VDD/3 = 0.6 and L = 0.28u, 0.4u:0.4u:2u

1) gm/gds
2) ID/W
3) gm/Cgg (use advanced Y expression)
4) VGS

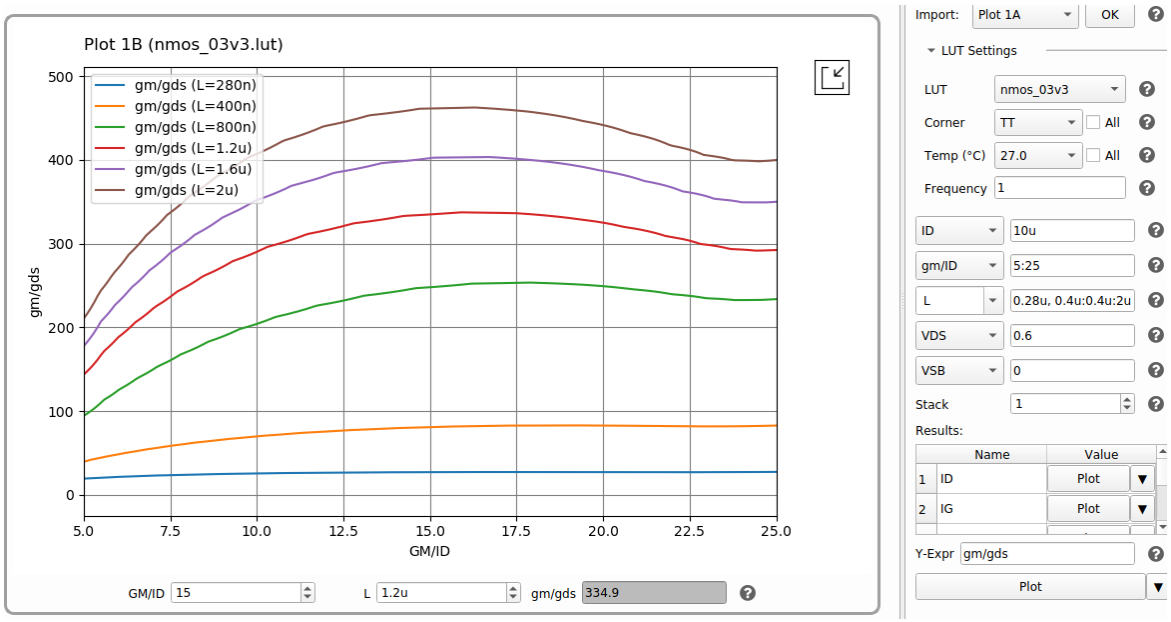

Figure 1 : gm/gds vs gm/id for Nmos

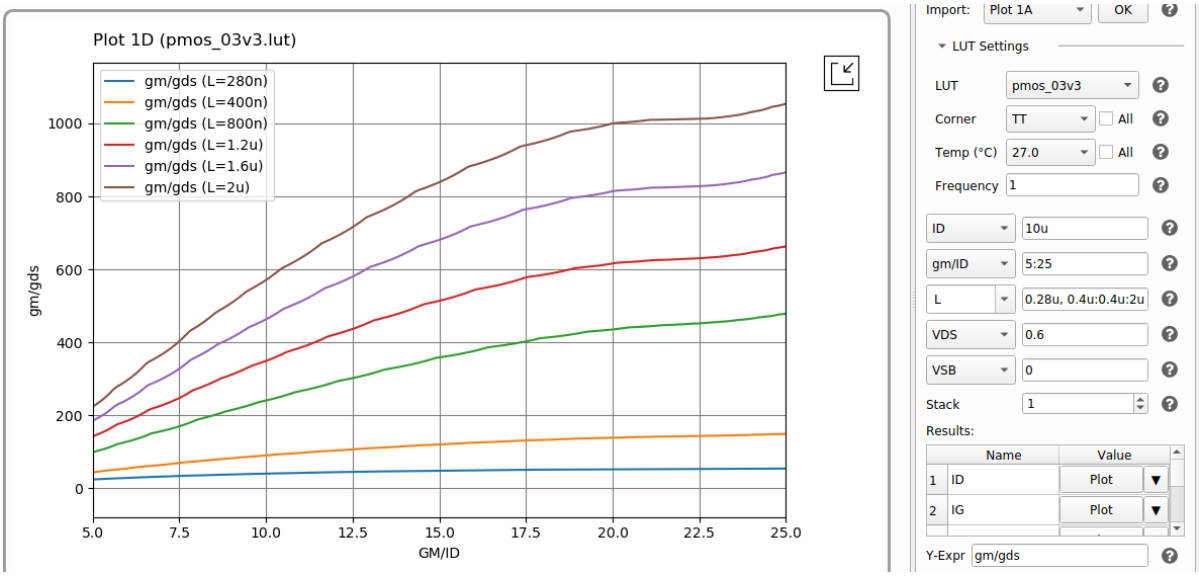

Figure 2 : gm/gds vs gm/id for Pmos

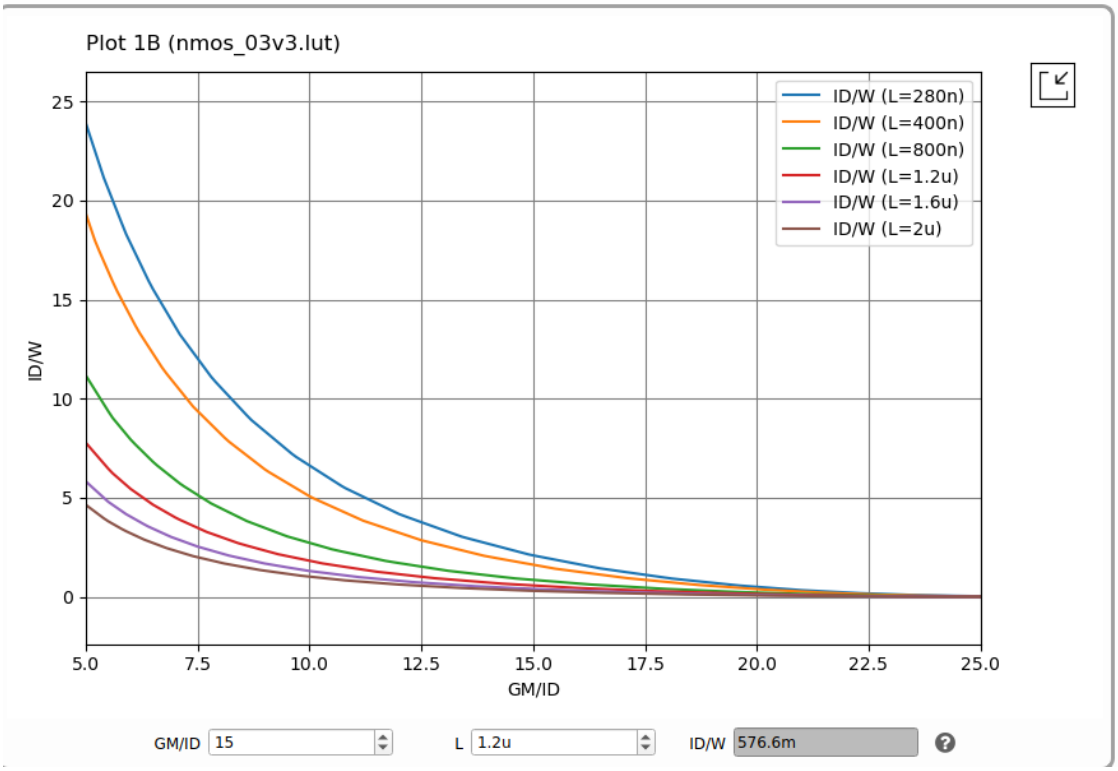

Figure 3 : : ID/W vs gm/id for Nmos

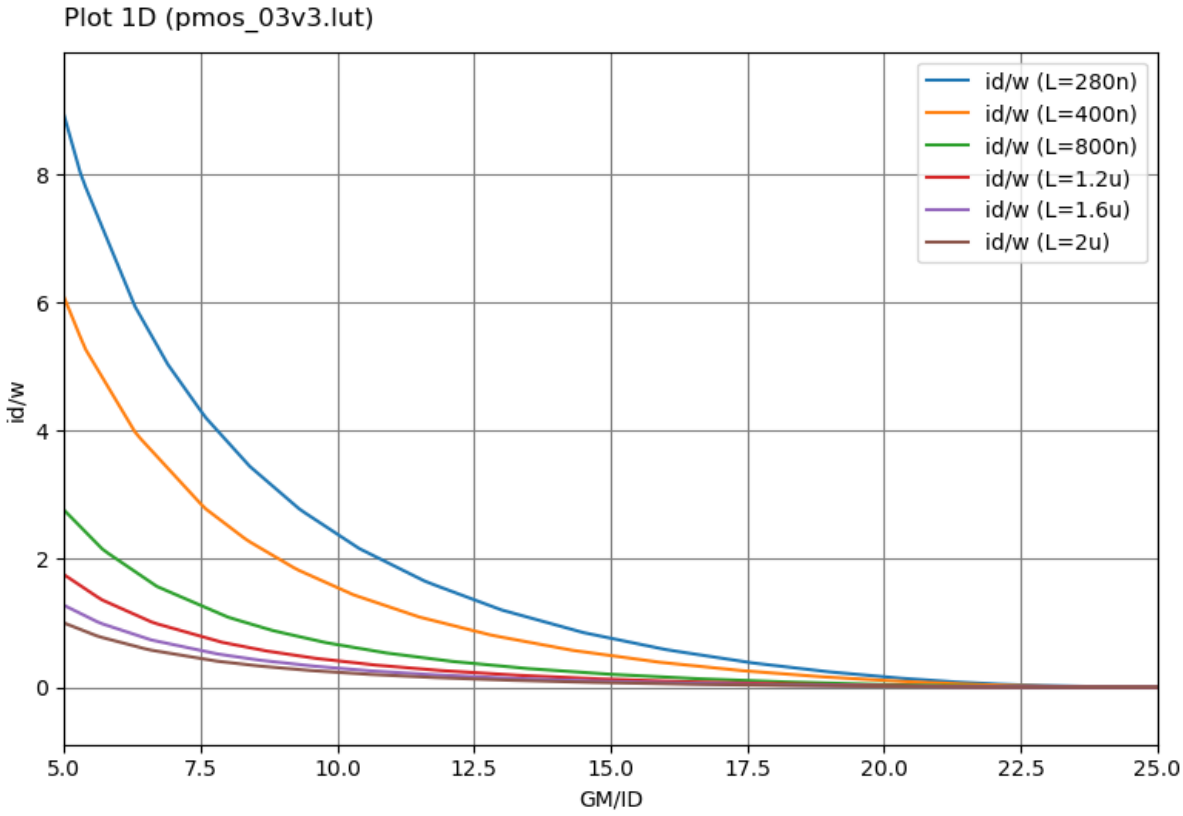

Figure 4 : : ID/W vs gm/id for Pmos

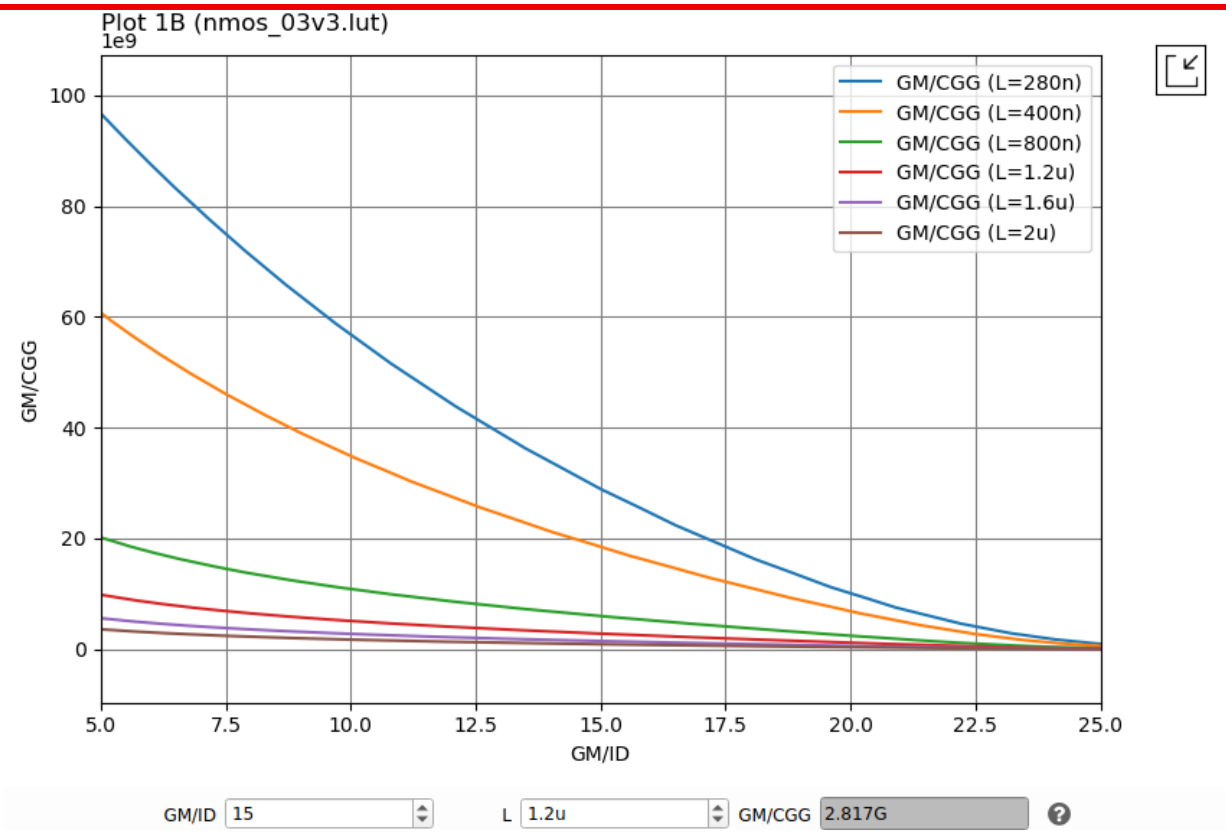

Figure 5 : gm/cgg vs gm/id for Nmos

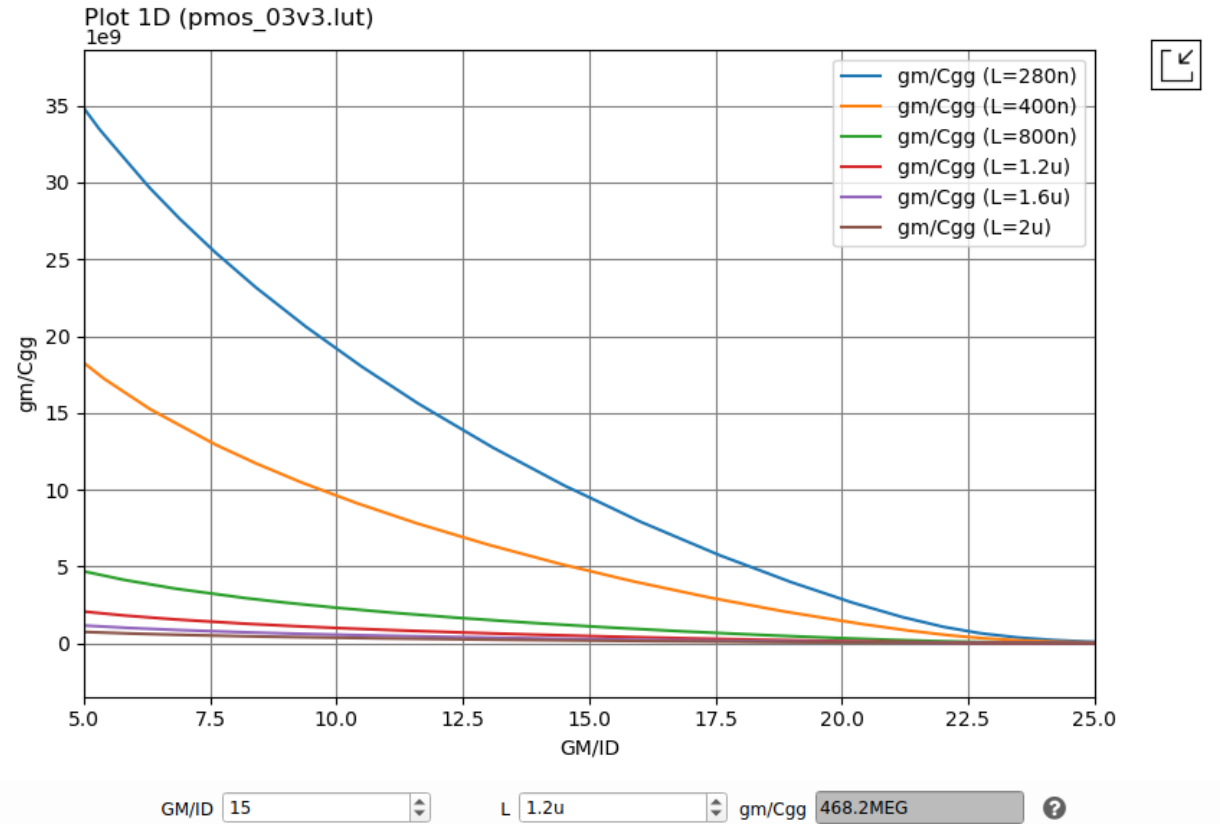

Figure 6 : gm/cgg vs gm/id for Pmos

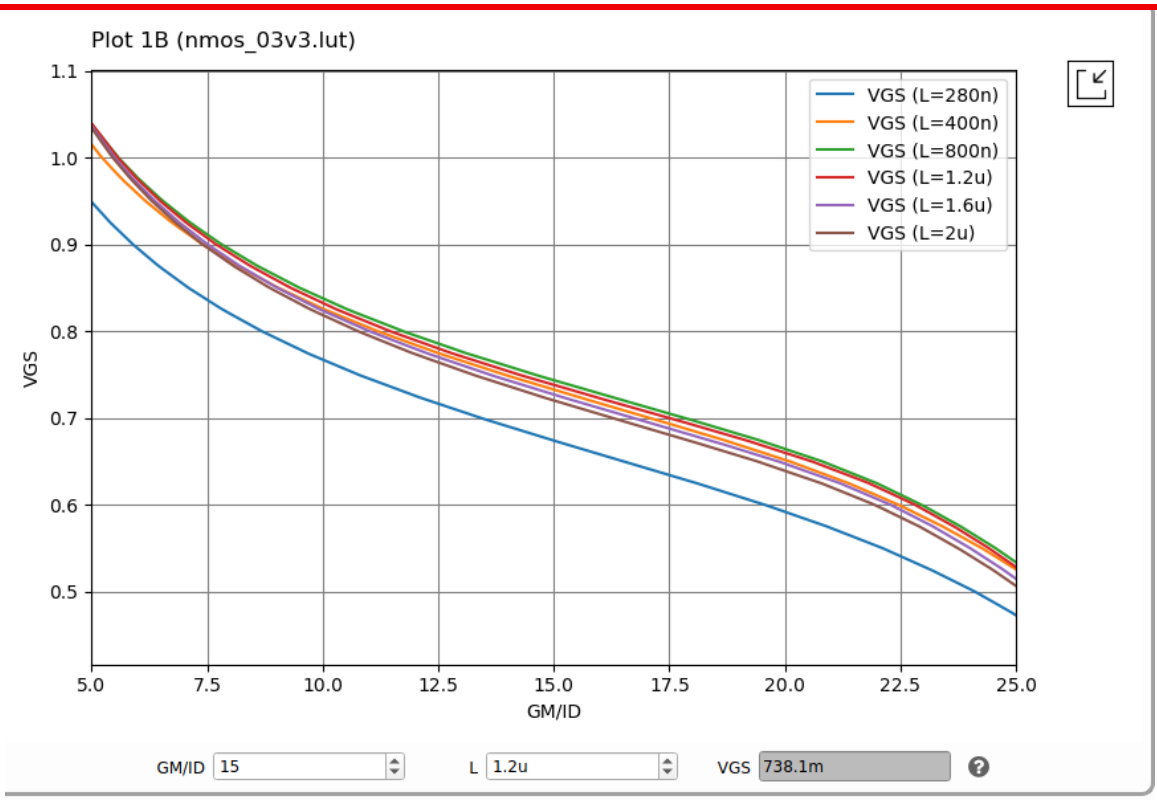

Figure 7 : Vgs vs gm/id for Nmos

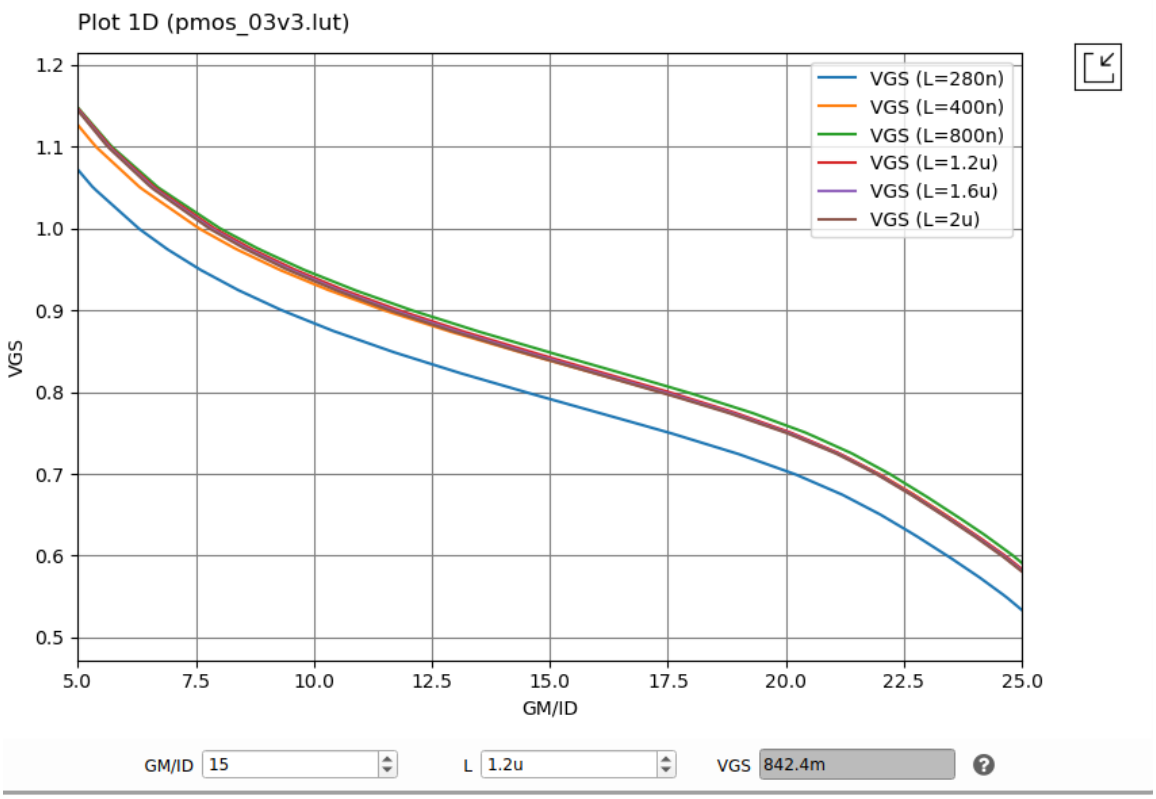

Figure 8 : : Vgs vs gm/id for Pmos

Part 2: OTA Design

Use an ideal external **10uA** DC current source in your test bench

Technology	0.18um CMOS
Supply voltage	1.8V
Load	5pF
Open loop DC voltage gain	>= 34dB
CMRR @ DC1	>= 74dB
Phase margin	>= 70o
CM input range – low	<= 1V
CM input range – high	>= 1.5V
GBW	>= 10MHz

For CM input range – low <= 1V and CM input range – high >= 1.5V

The range is near to VDD then we will use Nmos 5T-OTA

$$GBW = \frac{g_m}{2\pi C_L}$$

gm = 314.15 uS

Open loop DC voltage gain = gm*ron//rop

For simplicity we assume that ron = rop

This Open loop DC voltage gain = gm * ro/2

Gm/Gds >= 100

And we need gm/id for input pair in MI the me need the gm/id assume = 16

Then the id ≈ 19.6 µA

We need the id multiplication of Ireff

then iss = 40 and id = 20 multiplication of Ireff

First we will design the input pair and then the pmos Load and then Curren mirror

Design NMOS input pair :

Choose gm/id = 16.37 and gm/gds>100(To provide a safety margin that ensures the design remains robust and functional despite real-world manufacturing variations (PVT).)

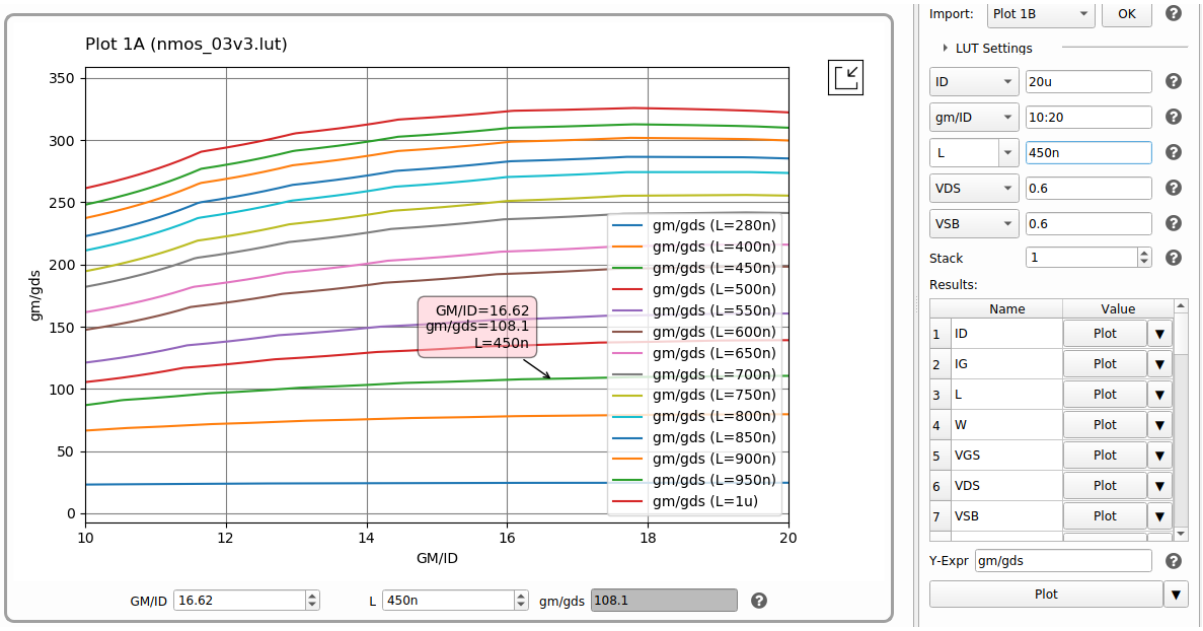

Figure 9 : gm/gds VS gm/id for input pair Nmos

Then with this information we can get the W form ADT

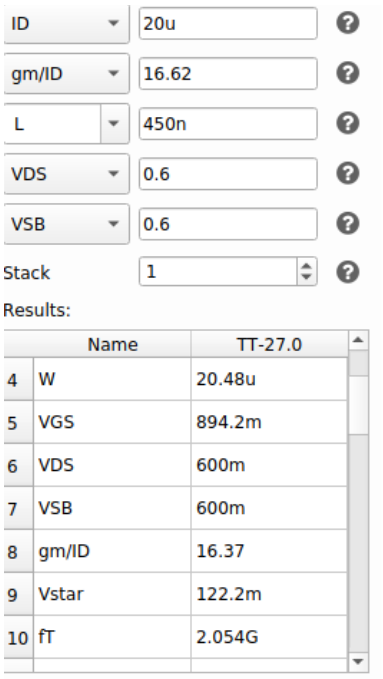

Figure 10 : W and L for Input pair Nmos

W = 20.48 um L = 450 nm

Design the PMOS load :

gm/id = 14 and It is expected to be smaller than gm/id for nmos (**Because holes in PMOS have lower mobility than NMOS, gm/id for the same bias conditions.)** and gm/gds>100 **(To provide a safety margin that ensures the design remains robust and functional despite real-world manufacturing variations (PVT).)**

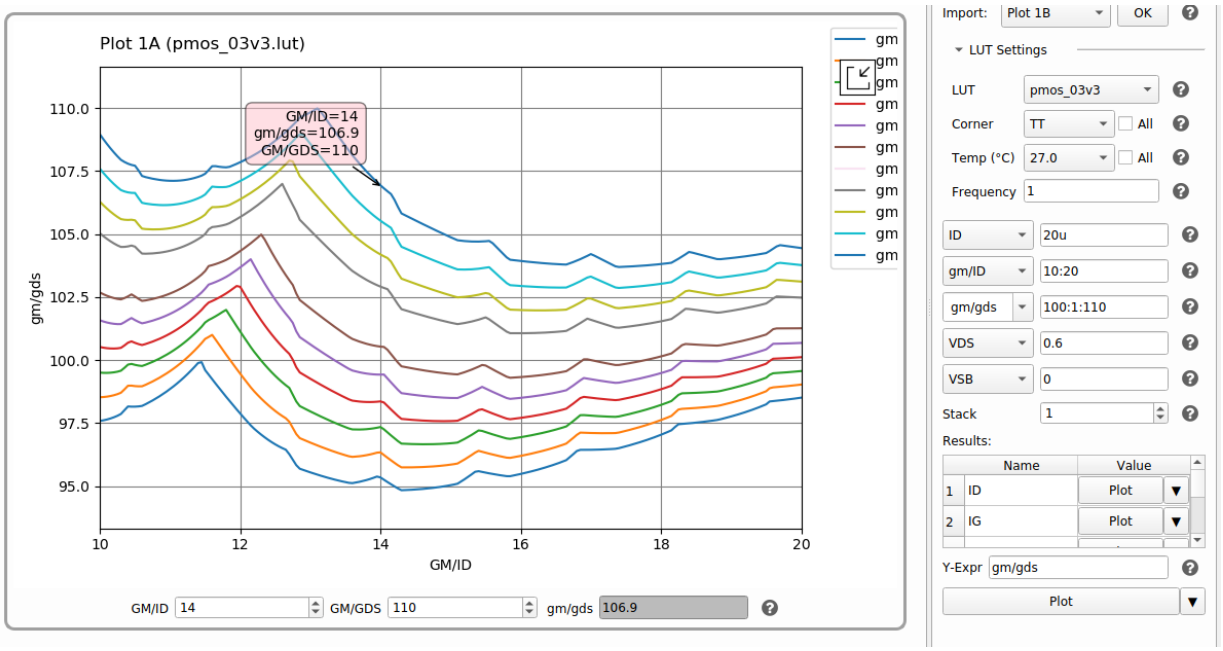

Figure 11 : : gm/gds VS gm/id for Pmos Load

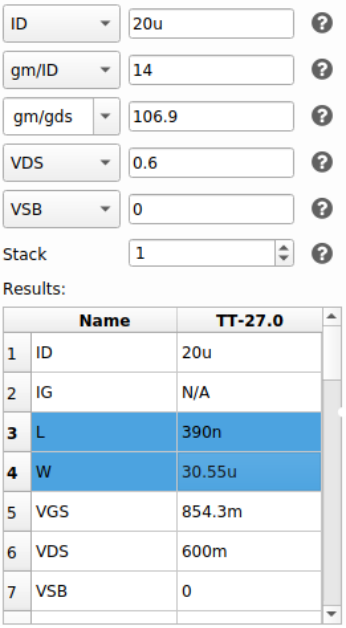

Figure 12 : W and L for Pmos Load

W=30.55 um L= 390nm

Design the current mirror :

$$A_{vCM} = \frac{V_{out}}{V_{iCM}} \approx -\frac{1}{2g_{m3,4}R_{SS}}$$

CMRR >= 74dB

From ADT gm 3,4 = 275.7u

RSS >= 181.388 Kohm

Assume gm/id = 15 then gm = 600uS then gm/gds = 108.8

And we plot the gm/id VS gm/gds and find the point have gm/gds = 108.8

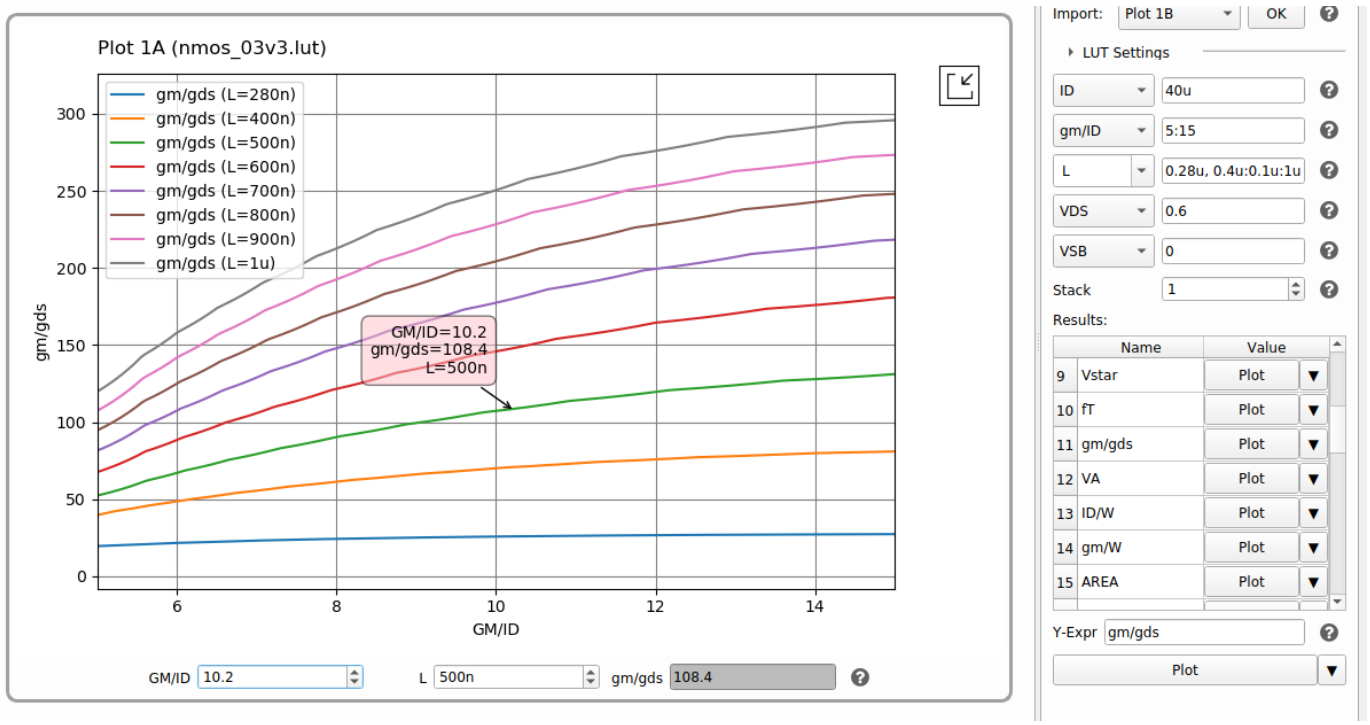

Figure 13 : gm/gds VS gm/id for CM

gm/id = 10.2

gm/gds = 108.4

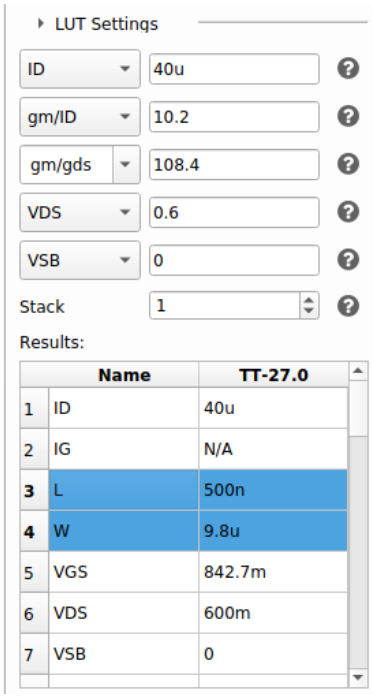

Figure 14 : W and L for CM

W = 9.8 um , L = 500 nm , Vstar = 198.4 mV , gm =403.3

The Final table of Result :

Transistor	W (µm)	L (µm)	gm (µS)	ID (µA)	gm/ID (S/A)	VDSsat (V)	Vov (V)	V* (V)
M1, M2	20.48	0.45	318	20	16	0.1	0.019	0.122
M3, M4	30.55	0.39	275.7	20	14	0.143	0.143	0.143
M5	9.8	0.5	403.3	40	10.2	0.1689	0.133	0.198

Tail CS in sat

$$V_{iCM} \geq V_{THN} + V_{ov1} + V_{ov5}$$

Input pair in sat

$$V_{iCM} \leq V_{DD} - |\boldsymbol{V_{THP}}| - |V_{ov3}| + V_{THN}$$

1.0276 < Vicm < 1.7576

Vicm_middle = 1.4 V

Part 3: Open-Loop OTA Simulation

Schematic :

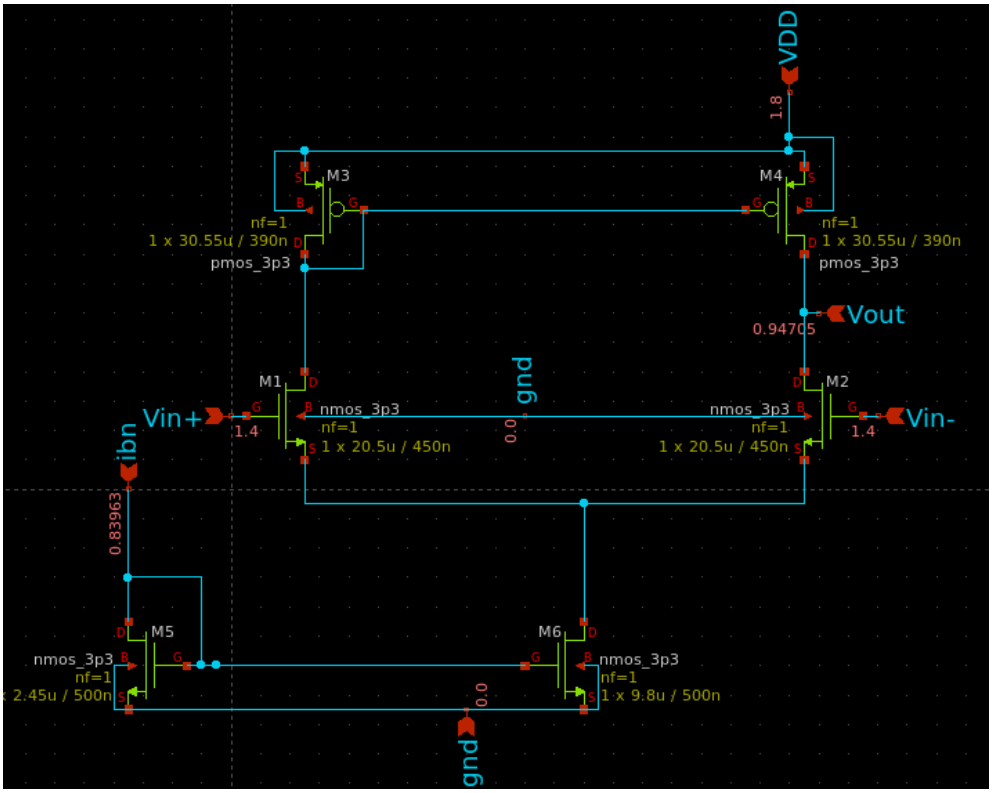

Figure 15 : Schematic of 5T-OTA

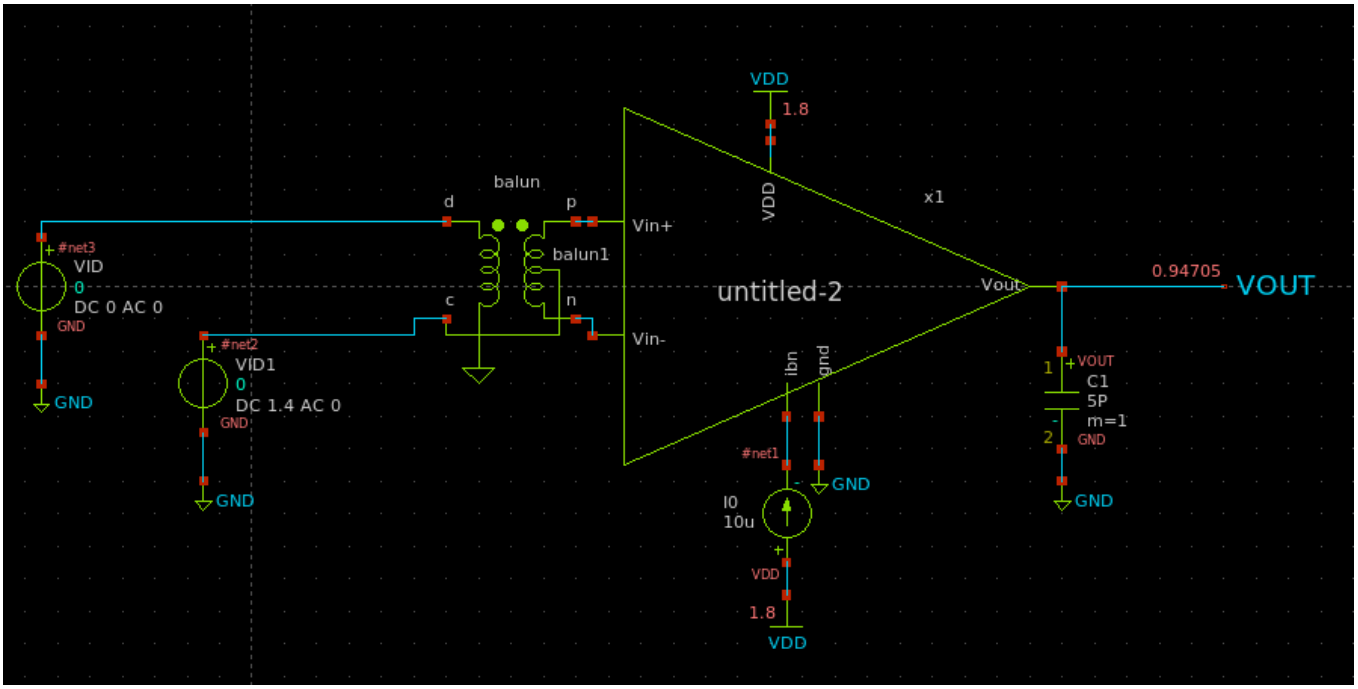

Figure 16 : Schematic for Part 3 simulation

OP Analysis :

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm6.m0           m.x1.xm5.m0           m.x1.xm3.m0
     model            nmos_3p3.8            nmos_3p3.8           pmos_3p3.12
        id          3.87837e-05                 1e-05          1.93927e-05
        gm          0.000399649          0.000101832          0.000274532
       gds          3.87008e-06          7.87165e-07          2.14302e-06
       vgs             0.839621             0.839621             0.852951
       vth             0.713453             0.706409             0.777967
       vds             0.526838             0.839616              0.85295
     vdsat             0.164435             0.169221             0.118576

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm4.m0           m.x1.xm1.m0           m.x1.xm2.m0
     model           pmos_3p3.12           nmos_3p3.12           nmos_3p3.12
        id          1.93927e-05          1.93919e-05          1.93919e-05
        gm          0.000274532          0.000321203          0.000321203
       gds          2.14302e-06          3.38827e-06          3.38827e-06
       vgs             0.852951             0.873151             0.873151
       vth             0.777967             0.859766             0.859766
       vds              0.85295             0.420198             0.420198
     vdsat             0.118576            0.0960988            0.0960988
```

Figure 17 : OP annotations

Is the current (and gm) in the input pair exactly equal?

M1 and M2 yes exactly equal

What is DC voltage at VOUT? Why?

Vout = Vdd -Vds4 = 1.8 – 0.85295 = 0.947 V

Vf = Vdd – vds 3 = 0.947V

The DC voltage at **VOUT** is approximately **0.947 V** because the PMOS load (M4) is diode-connected, forcing its drain-to-source voltage to remain at **Vds(sat)**. Consequently, the output node voltage is set by

$$V_{OUT} = V_{DD} - V_{DS4(sat)} = 1.8\,\text{V} - 0.85295\,\text{V} \approx 0.947\,\text{V}$$

Since M4 is diode-connected to M3, **VOUT** tracks the voltage at the mirror node (**Vf**), maintaining this fixed offset from V_{DD}.

Diff small signal ccs :

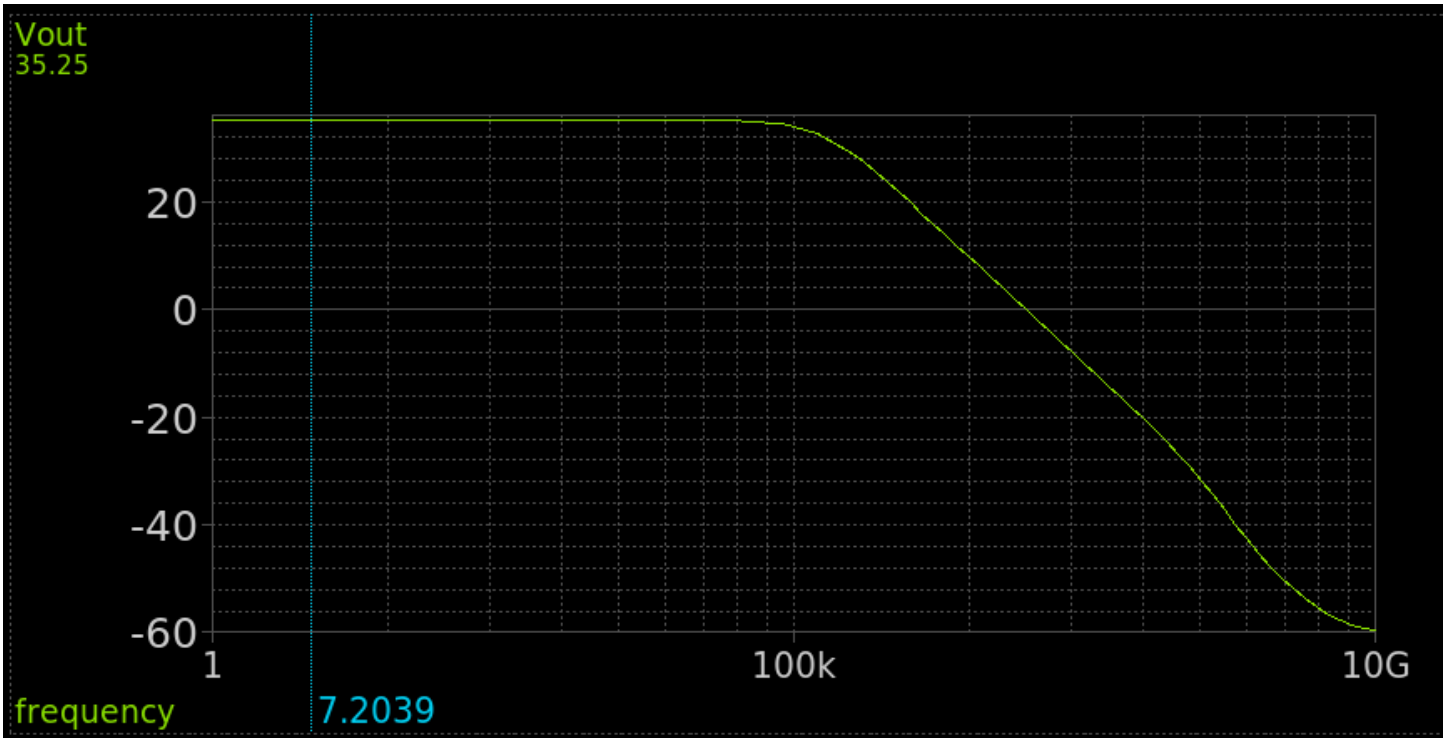

Figure 18 : diff gain (in dB) vs frequency.

```
gain                =  5.784350e+01 at=  1.000000e+00
bw                  =  1.738500e+05
gbw = 1.005609e+07
```

Figure 19 : gain & BW & GBW from simulation

Analytical :

DC gain = gm1,2*ro1//ro3 from OP annotation

DC gain = 58.07

Bw = 1/Rout*cl*2pi = 176.066KHz

	Simulation	Analytical
Dc gain (dB)	35.25	35.28
BW (KHZ)	173.85	176.066
GBW (MHZ)	10.05	10.22

CM small signal ccs:

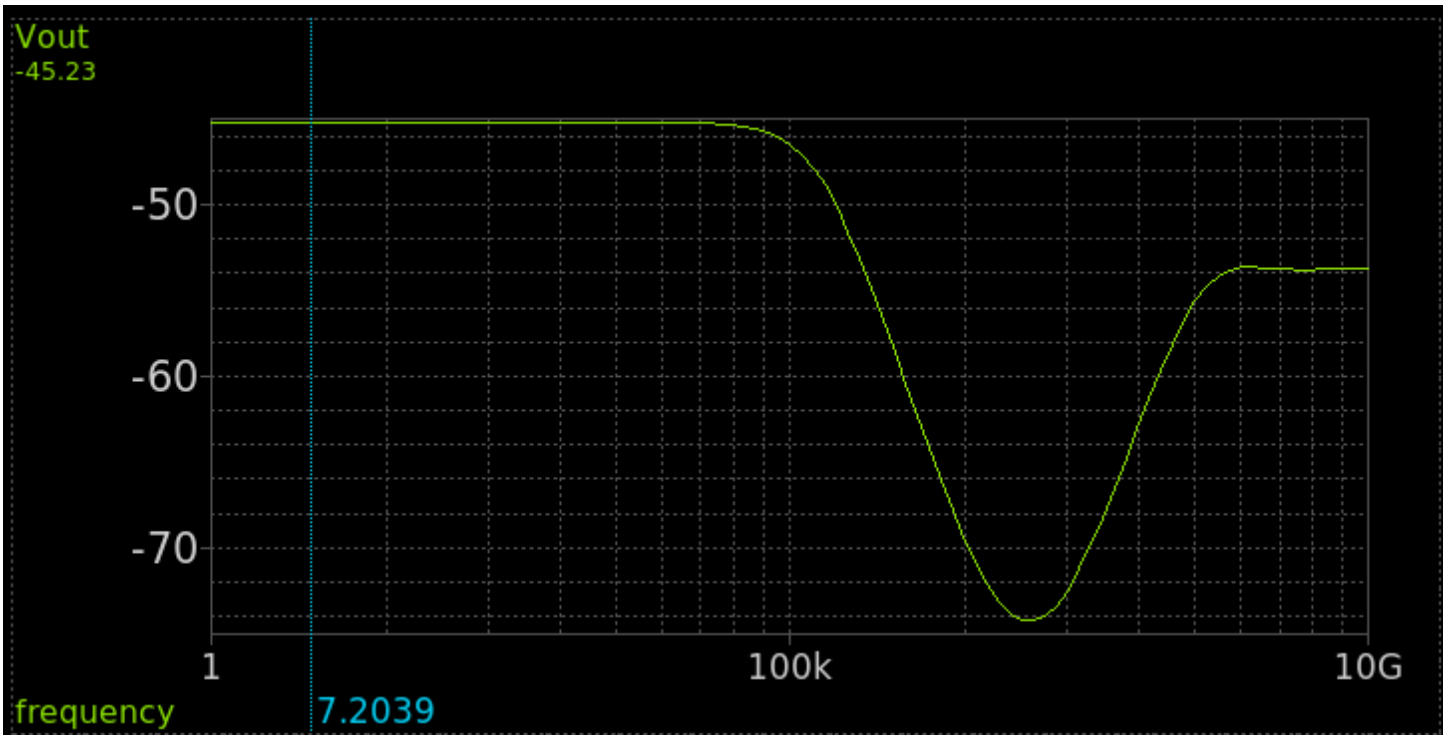

Figure 20 : CM gain in dB vs frequency.

```
No. of Data Rows : 101
cmgain                =  5.479506e-03 at=  1.000000e+00
```

Figure 21 : Cm Gain From simulation

Analytical:

$$A_{vCM} = \frac{V_{out}}{V_{iCM}} \approx -\frac{1}{2g_{m3,4}R_{SS}}$$

Rss = ro6

Avcm = 0.00704835

	Simulation	Analytical
Cm Gain (dB)	-45.23	-43

CMRR :

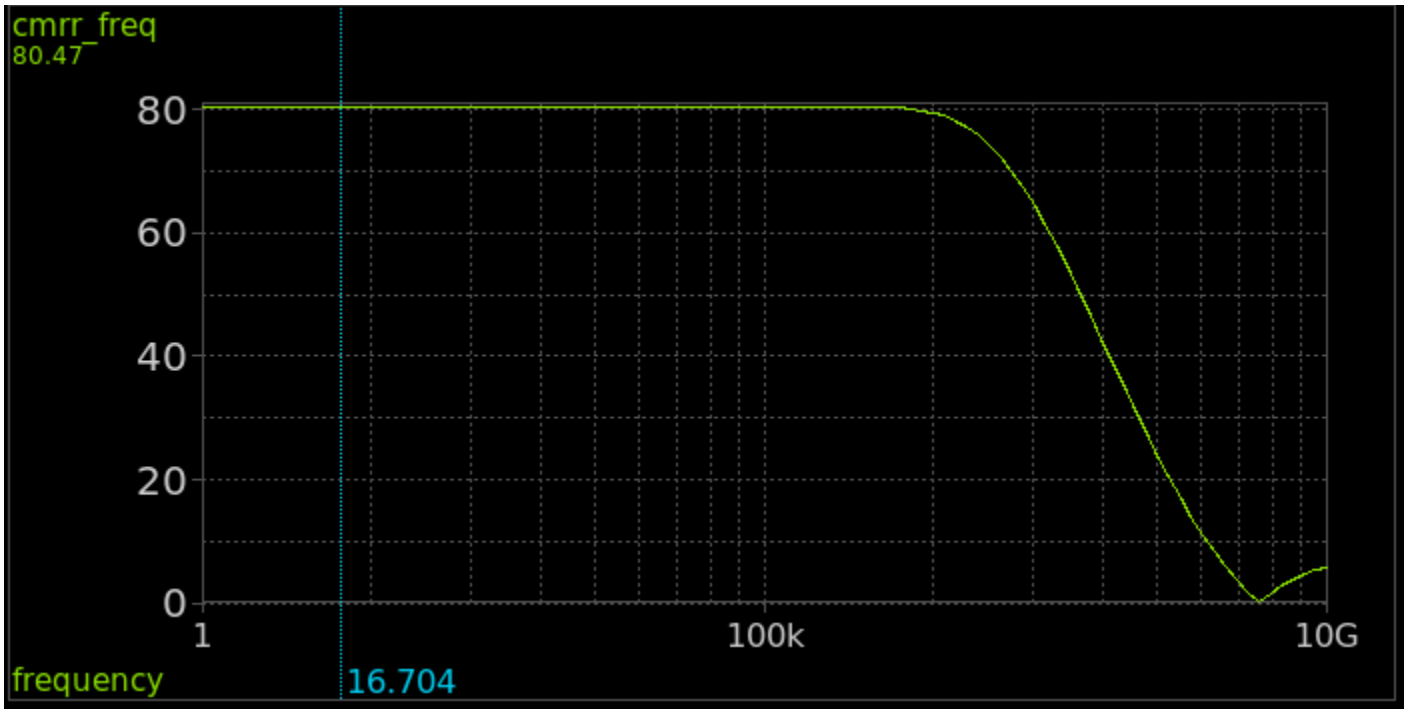

Figure 22 : CMRR in dB vs frequency at VICM at the middle of the CMIR.

Analytical

CMRR = Avd / Acm = 8236.8794 = 78.31dB

	Simulation	Analytical
CMRR (dB)	80.47	78.31

Diff large signal ccs:

VOUT vs VID Diff large signal

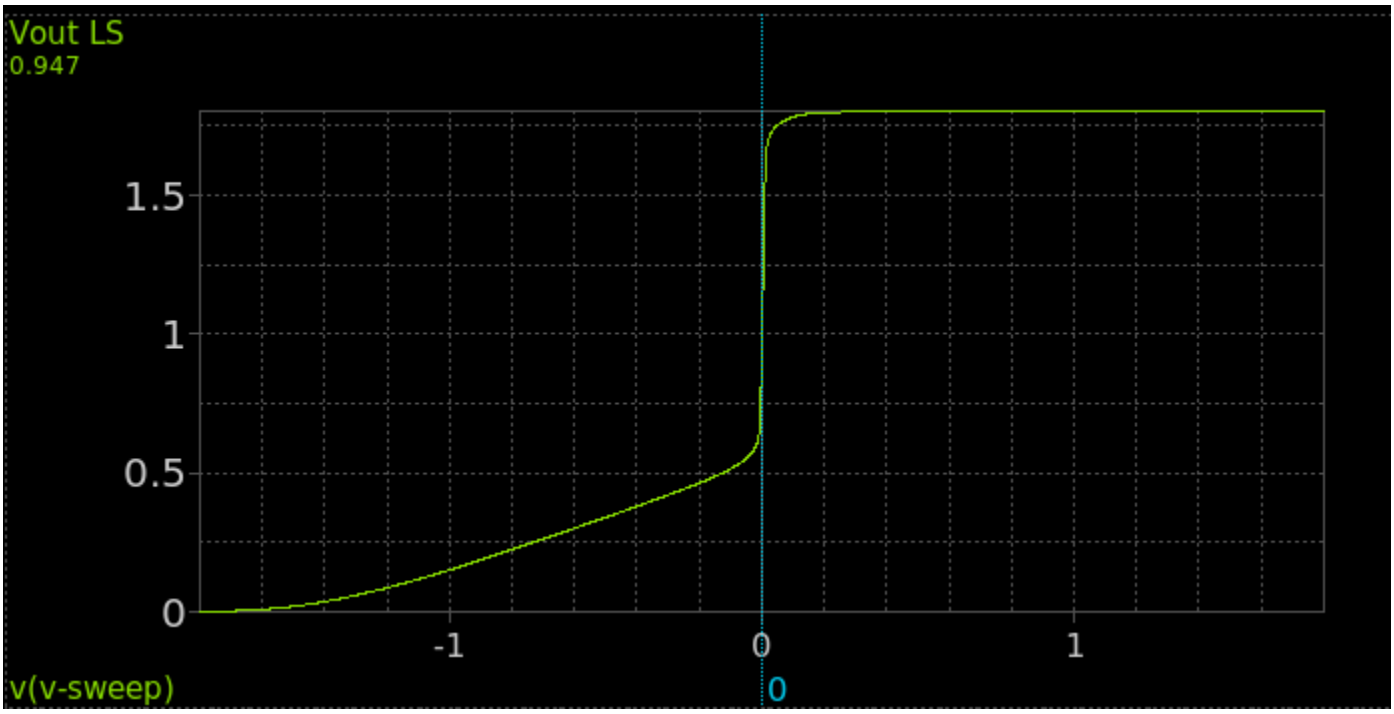

Figure 23 : VOUT vs VID Diff large signal

what is the value of Vout at VID = 0? Why?

Vout = 0.947 V

At **VID = 0** the output node sits at the diode-connected PMOS gate/drain voltage .

$$V_{OUT} \approx V_{DD} - |V_{SG4}|$$

the derivative of VOUT vs VID.

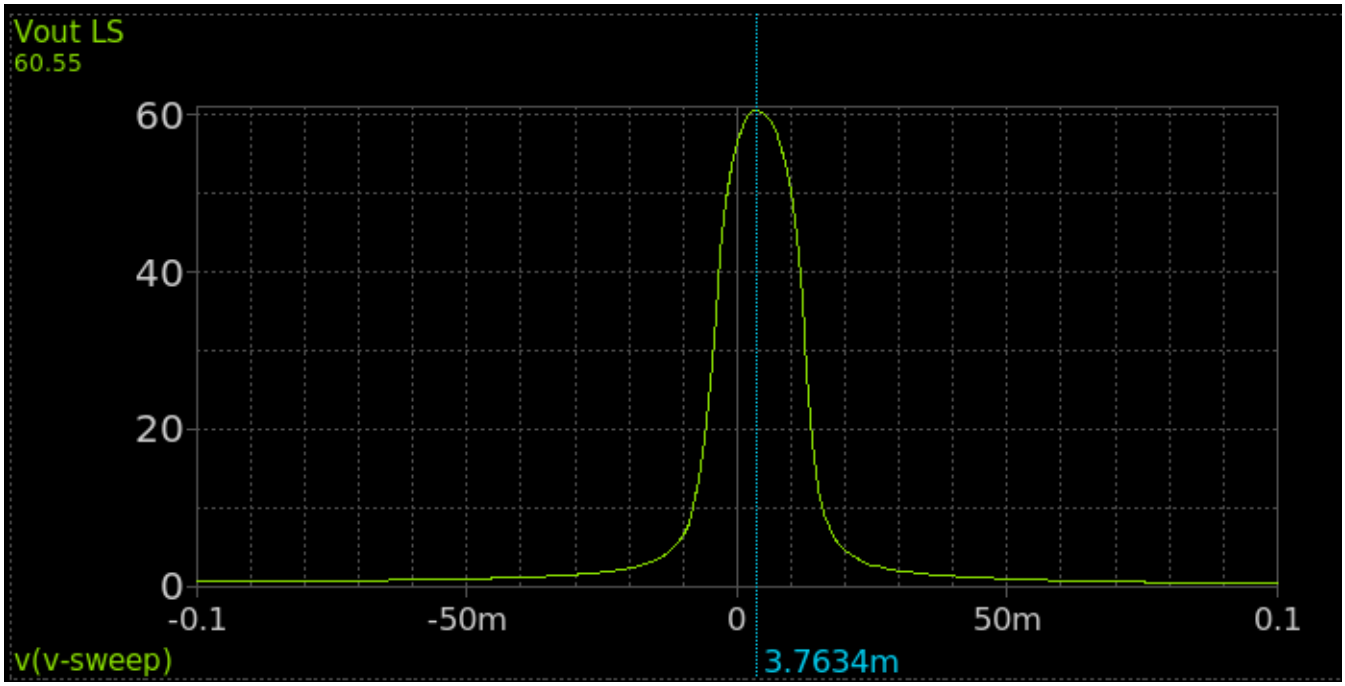

Figure 24 : the derivative of VOUT vs VID.

The peak of curve is 60.5 and the Avd = 57.8 is very close to Avd

The derivative of Vout vs VID peaks at the same value as Avd because mathematically the slope of the transfer curve at the operating point is the small-signal gain.

CM large signal ccs (GBW vs VICM):

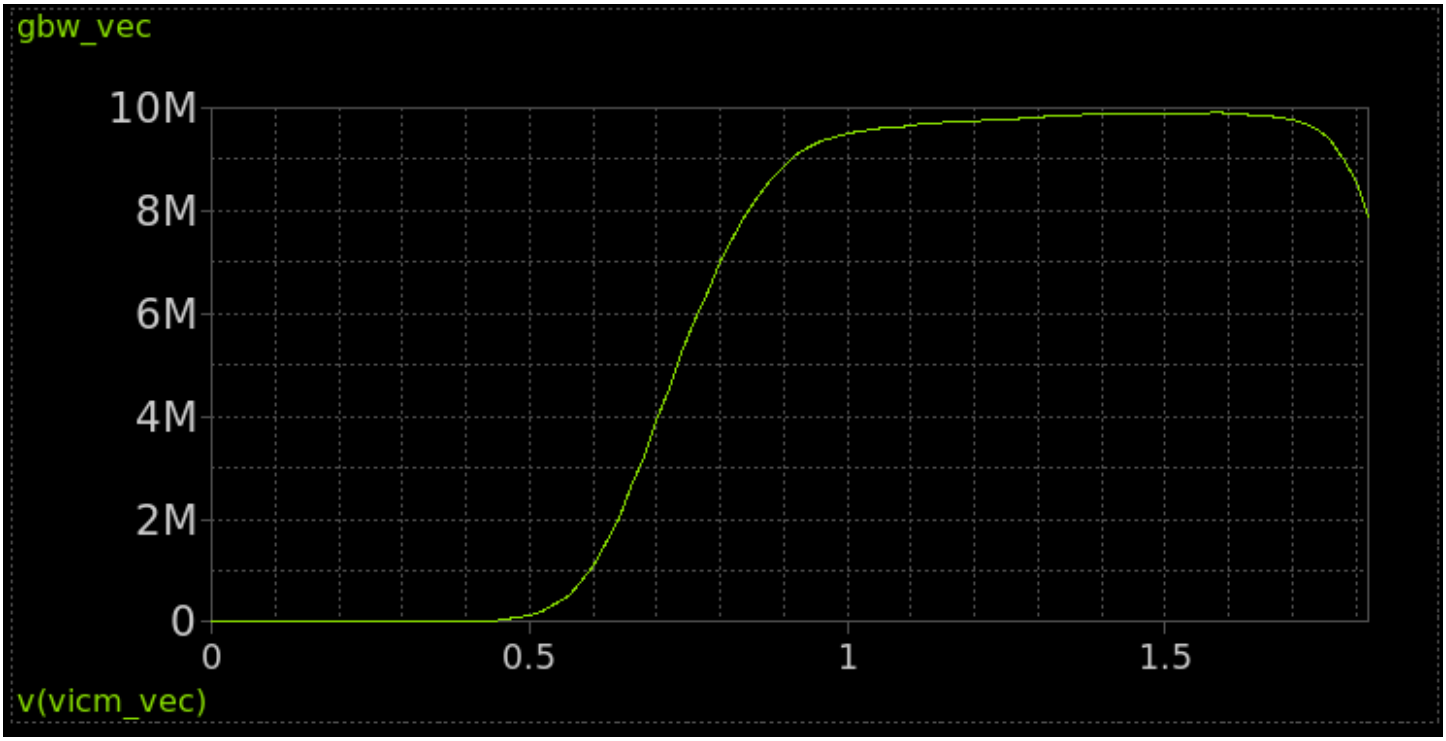

Figure 25 : GBW vs VICM

```
min_vincm = 9.007159e-01
max_vincm = 1.784058e+00
```

Figure 26 : Range of VinCm from simulation

If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?).

Because the NMOS body is tied to the substrate (usually ground), increasing the VinCM raises the VSB, increasing Vth and allowing the input range to extend up to VDD.

PART 4: Closed-Loop OTA Simulation :

Schematic :

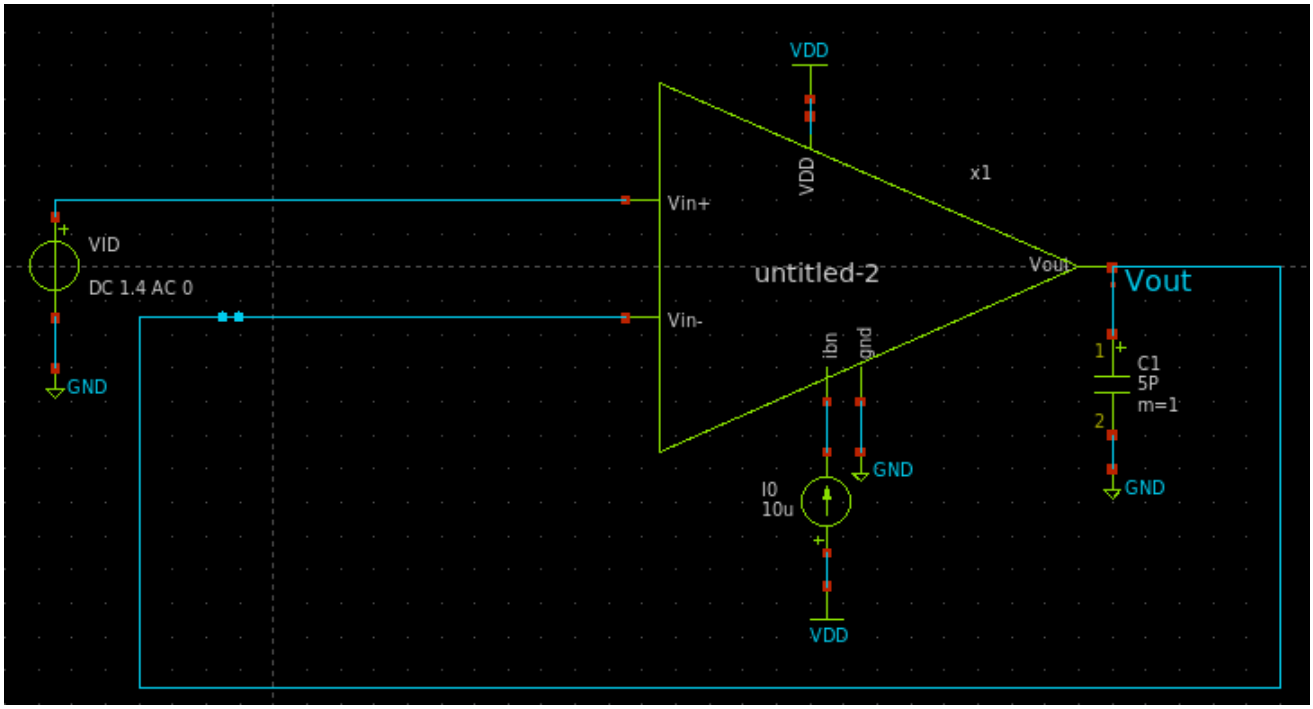

Figure 27 : Schematic of Closed Loop OTA

```
No. of Data Rows : 1
 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm6.m0          m.x1.xm5.m0          m.x1.xm3.m0
     model            nmos_3p3.8           nmos_3p3.8          pmos_3p3.12
        id          3.87785e-05                 1e-05          1.99442e-05
        gm            0.0003996          0.000101832          0.000279965
       gds            3.878e-06          7.87165e-07          2.19261e-06
       vgs             0.839621             0.839621             0.854925
       vth             0.713455             0.706409             0.777961
       vds             0.525482             0.839616             0.854924
     vdsat             0.164434             0.169221             0.119879

 BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x1.xm4.m0          m.x1.xm1.m0          m.x1.xm2.m0
     model          pmos_3p3.12          nmos_3p3.12          nmos_3p3.12
        id          1.88342e-05          1.99442e-05          1.88342e-05
        gm          0.000266112          0.000328176          0.000314796
       gds          2.95413e-06          3.47313e-06          2.57226e-06
       vgs             0.854925             0.874506             0.867023
       vth             0.779392             0.859422             0.858181
       vds             0.407482             0.419579             0.867022
     vdsat             0.118938            0.0969676            0.0938096
```

Figure 28 : OP annotation for Closed Loop OTA

Is the current (and gm) in the input pair exactly equal? Why?

For M1 and M2 the Id and gm is not exactly equal , because the amplifier's finite open-loop gain requires a small, non-zero differential voltage between the inputs to sustain the output, causing the two transistors to carry unequal currents (mismatch)

Calculate the mismatch in ID and gm.

$$\text{Mismatch } \% = \frac{|I_{D1} - I_{D2}|}{(I_{D1} + I_{D2})/2} \times 100$$

$$\text{Mismatch } \% = \frac{|19.94 - 18.83|}{(19.94 + 18.83)/2} \times 100 = \frac{1.11}{19.385} \times 100 \approx \mathbf{5.73\%}$$

$$\text{Mismatch } \% = \frac{|g_{m1} - g_{m2}|}{(g_{m1} + g_{m2})/2} \times 100$$

$$\text{Mismatch } \% = \frac{|328.2 - 314.8|}{(328.2 + 314.8)/2} \times 100 = \frac{13.4}{321.5} \times 100 \approx \mathbf{4.17\%}$$

Schematic to loop gain implementation

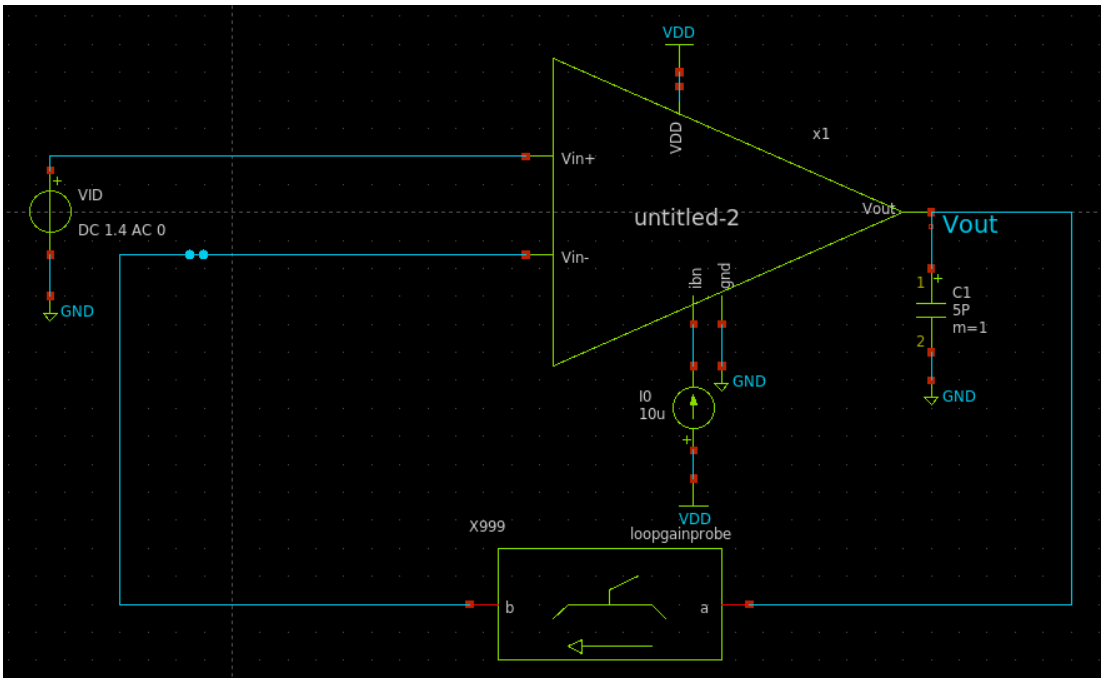

Figure 29 : Schematic to loop gain implementation

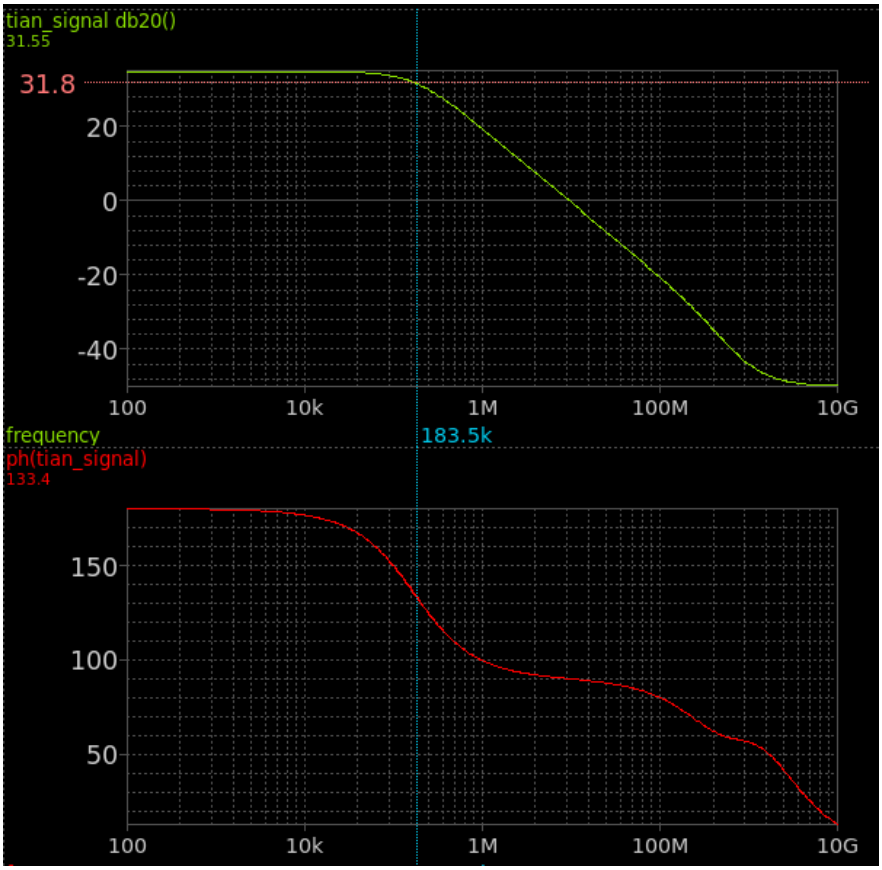

Figure 30 : loop gain in dB and phase vs frequency.

	open-loop OTA simulation	Closed-Loop OTA Simulation
Dc gain (dB)	35.24	34.8
GBW ((MHz)	10.05	10.083

The results are **very close** — the closed-loop case shows a **small DC gain drop** (35.24 → 34.8 dB) while **GBW** is essentially **unchanged** (10.05 → 10.083 MHz).

This **small gain loss** is **expected**: closing the loop and connecting the output back to the input introduces **loading**, a **small error** (non-infinite open-loop gain) and the **tiny differential input** needed to drive the loop, all of which reduce measured **DC gain** slightly.

Analytical :

Rout = ro2||ro4=388.8k||338.5k=181.4 kΩ

Dc gain = 20log(59.5) = 35.49 dB

Bw = 1/2pi*cl*Rout = 175.474KHz

GBW = 10.44 MHz

	Closed-Loop OTA Simulation	Analytical
Dc gain (dB)	34.8	35.49
GBW ((MHz)	10.083	10.44

```
No. of Data Rows : 401
gain_crossover_freq =  9.549225e+06
phaseatzerogain     =  9.006710e+01
pm = 8.993290e+01
binary raw file "stb.raw"
```

Figure 31: PM from simulation

This table shows that your final 5T-OTA design successfully meets or exceeds all the required performance targets.

Specification	Requirement	Achieved Result	Status
DC Voltage Gain	≥ 34 dB	35.25 dB	✅
Gain-Bandwidth (GBW)	≥ 10 MHz	10.05 MHz	✅
CMRR @ DC	≥ 74 dB	80.47 dB	✅
Phase Margin	≥ 70°	~89.9°	✅
CM Input Range (Low)	≤ 1 V	0.90 V	✅
CM Input Range (High)	≥ 1.5 V	1.78 V	✅