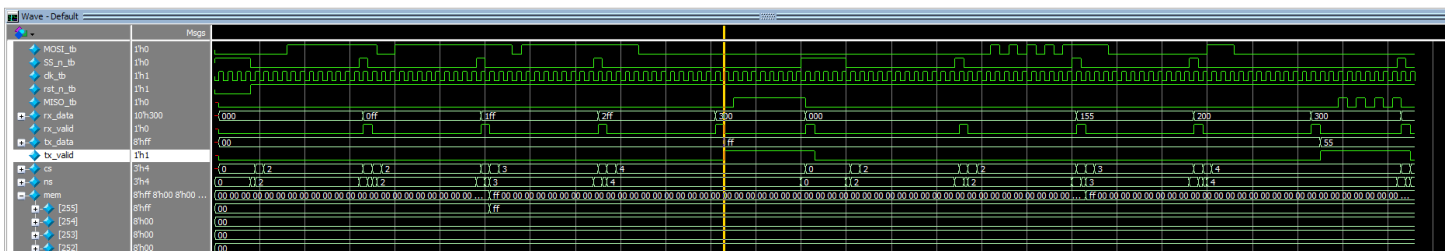


Project 2

Digital Design using Verilog &
FPGA flow using Vivado

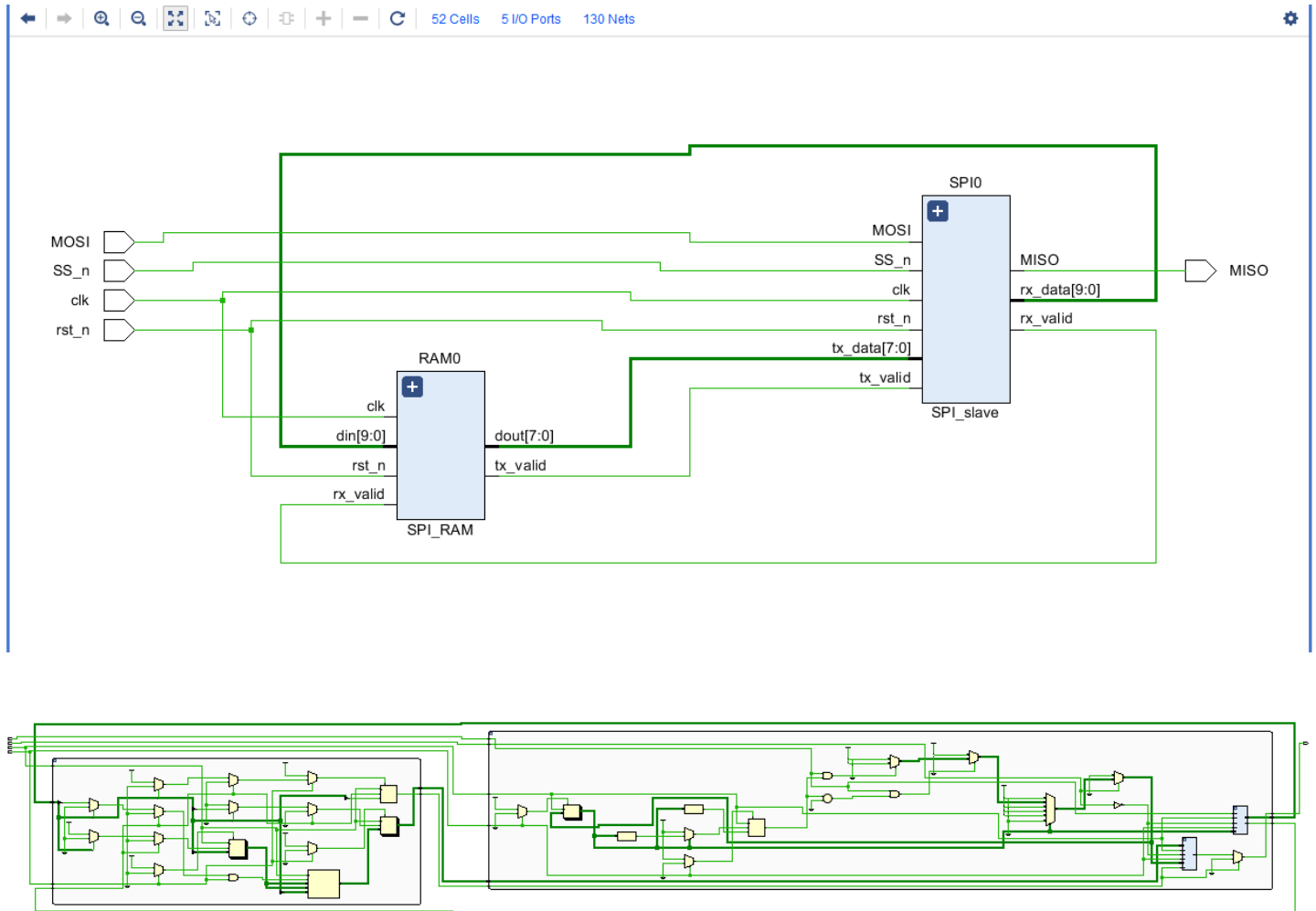
Team: 3_I mux
Ahmed Yosry Anwer Sayed
Mostafa Mohamed Osman
Abdallah Karim Motwea



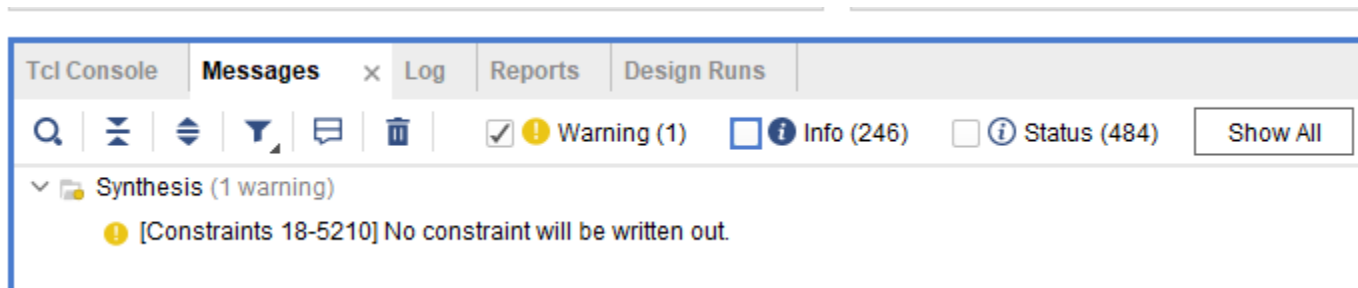
2. Synthesis and elaboration snippets for each encoding:

Gray:

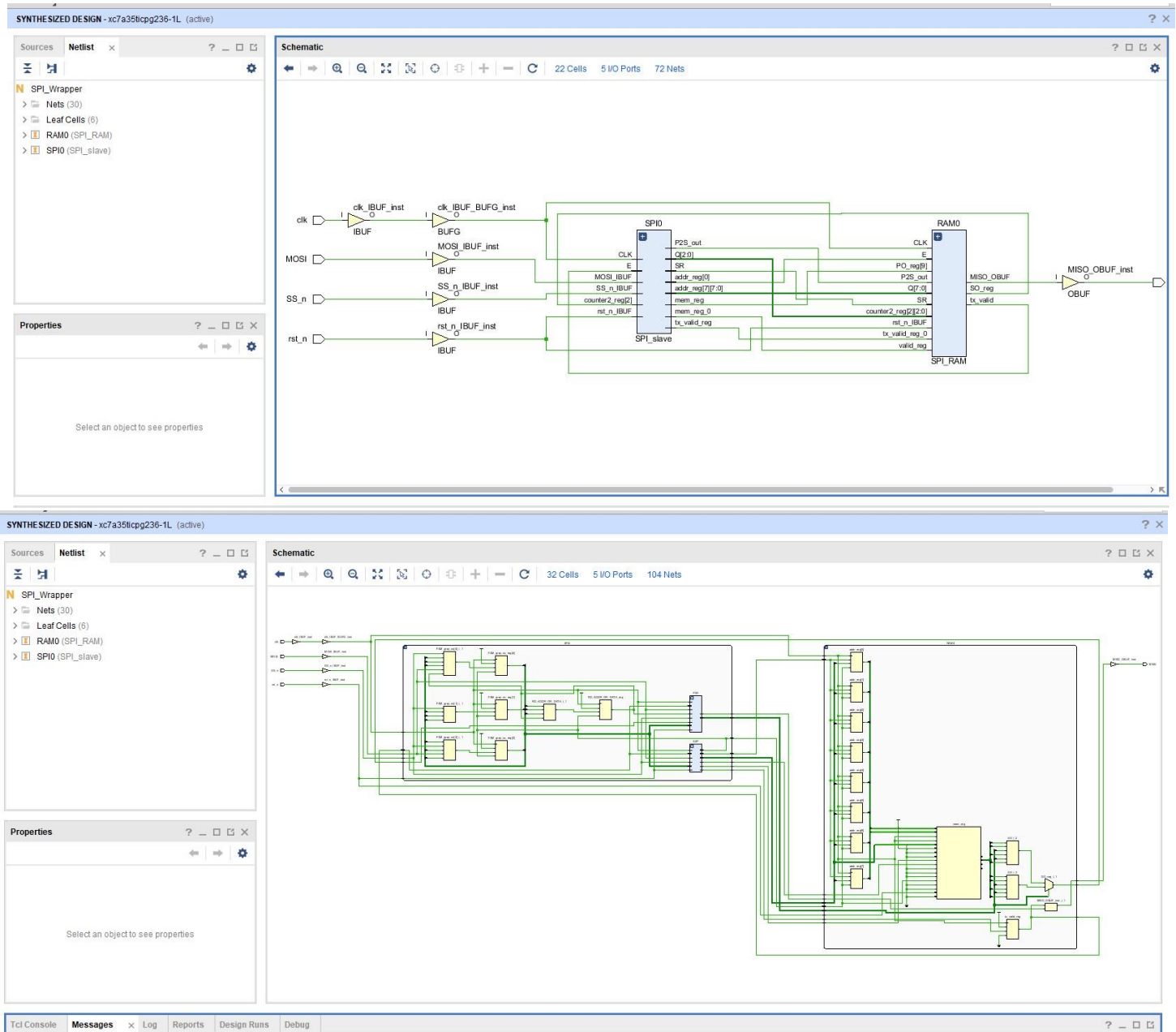
Schematic after elaboration:



Message tab after elaboration:



Schematic after synthesis:



Message tab after synthesis:

Tcl Console Messages x Log Reports Design Runs Debug

Warning (1) Info (238) Status (477) Show All

▼ Synthesis (1 warning)

⚠ [Constraints 18-5210] No constraint will be written out.

The report showing encoding used:

Schematic x synth_1_synth_synthesis_report_0 - synth_1 x

D:/Yosry/Studies/Digital IC/Design/Assignments/SPI Slave Interface/SPI_3ala_nadafa/SPI_3ala_nadafa/SPI_3ala_nadafa.runs/synth_1/SPI_Wrapper.vds

```

94 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:38 ; elapsed = 00:00:39 . Memory (MB): peak = 759.559 ; gain
95 -----
96 INFO: [Synth 8-5545] ROM "ten_flag" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
97 INFO: [Synth 8-5545] ROM "counter" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
98 INFO: [Synth 8-5545] ROM "counter2" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
99 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
100 INFO: [Synth 8-5544] ROM "RD_ADDR_OR_DATA" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
101 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
102 -----
103 State | New Encoding | Previous Encoding
104 -----
105 IDLE | 000 | 000
106 CHK_CMD | 001 | 001
107 READ_ADD | 011 | 011
108 READ_DATA | 010 | 100
109 WRITE | 111 | 010
110 -----
111 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_slave'
112 -----
113 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:38 ; elapsed = 00:00:40 . Memory (MB): peak = 759.559 ; gain = 502.320
114 -----
115

```

Utilization report:

Tcl Console Messages Log Reports Design Runs Utilization x Timing Debug

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	125	100	1	0.5	5	1
RAM0 (SPI_RAM)	3	9	1	0.5	0	0
SPI0 (SPI_slave)	122	91	0	0	0	0

utilization_1

Timing report:

Tcl Console Messages Log Reports Design Runs Utilization Timing x Debug

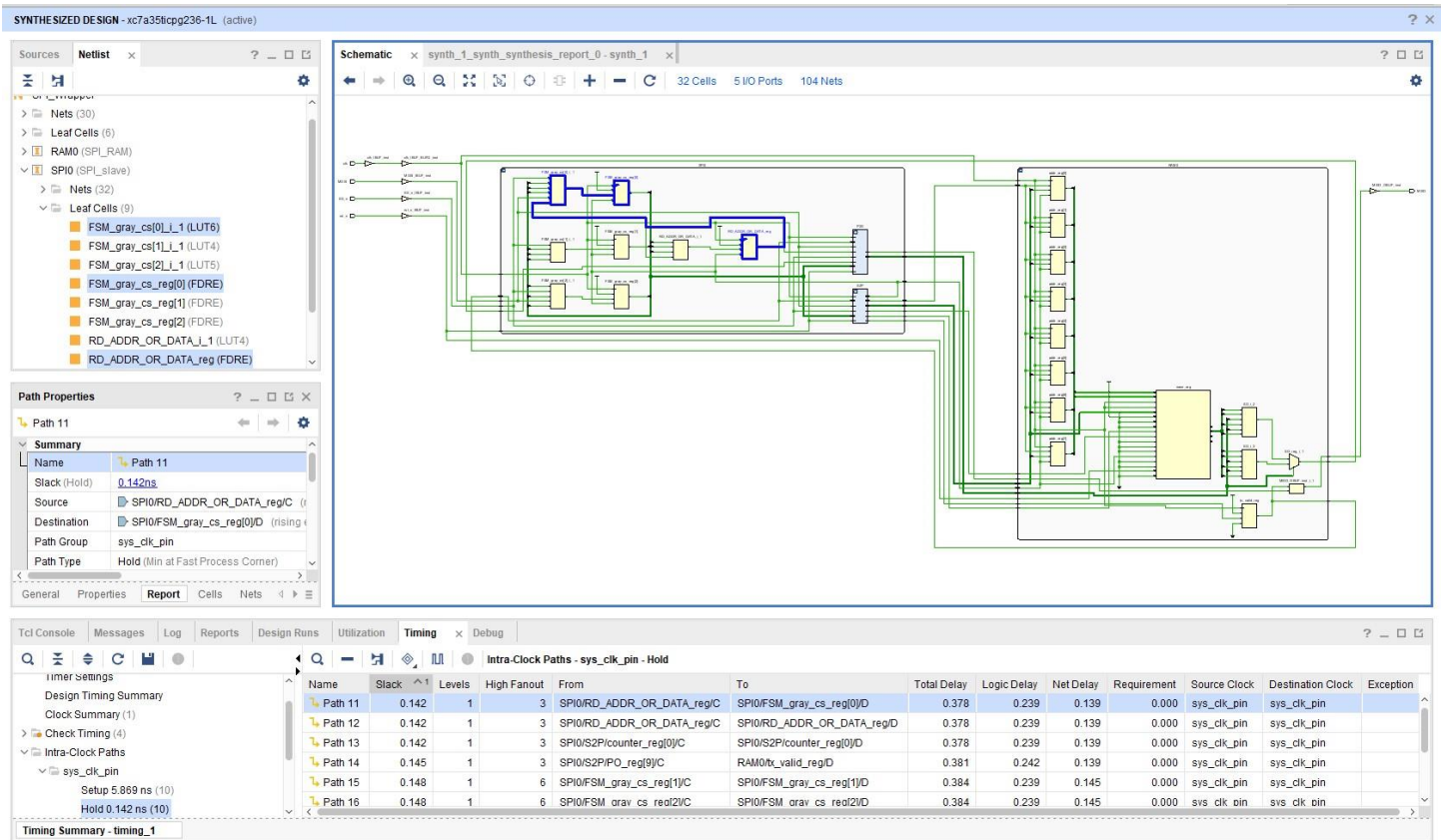
Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.869 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 252	Total Number of Endpoints: 252	Total Number of Endpoints: 103

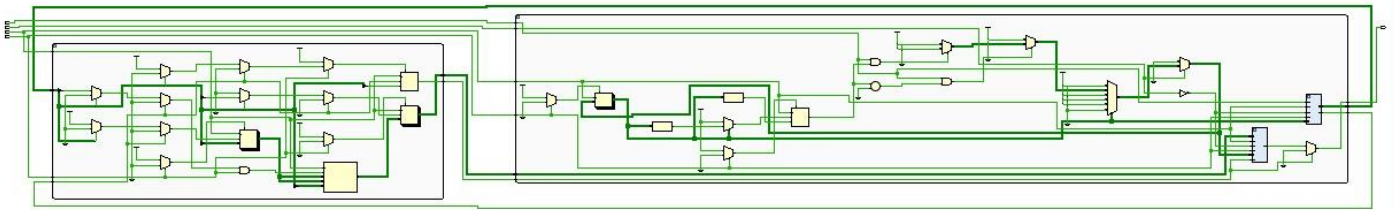
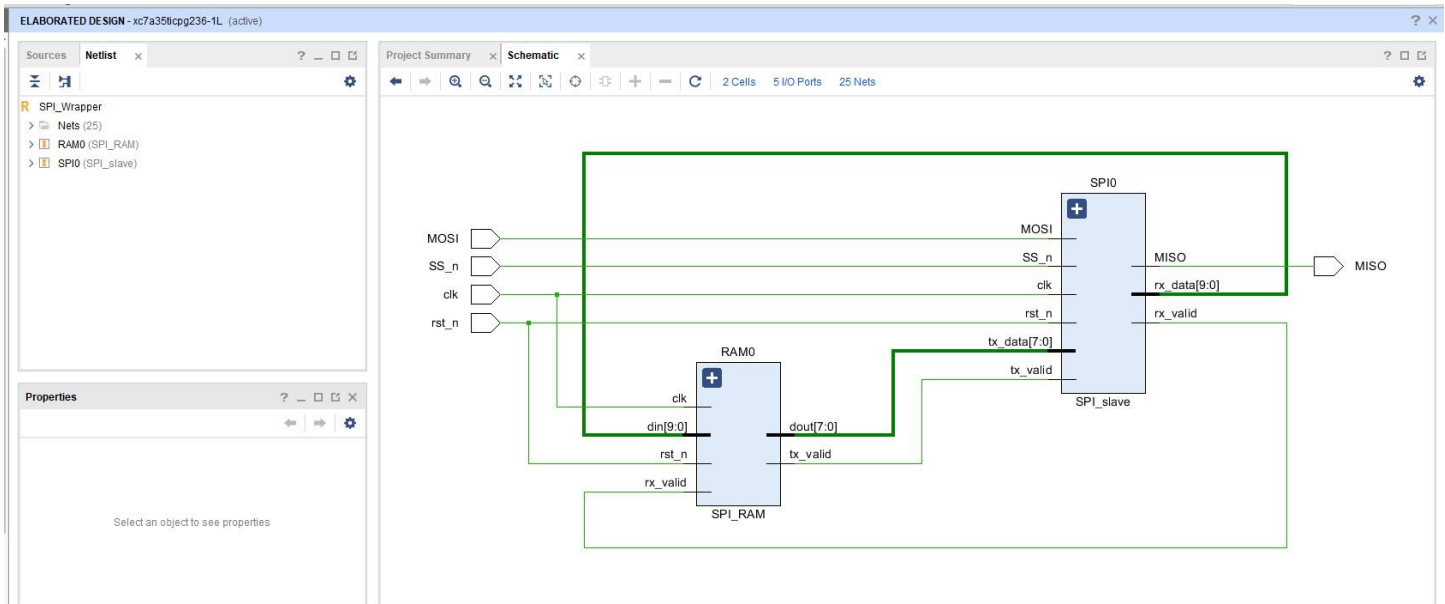
All user specified timing constraints are met.

Timing Summary - timing_1

The critical path highlighted in the schematic:



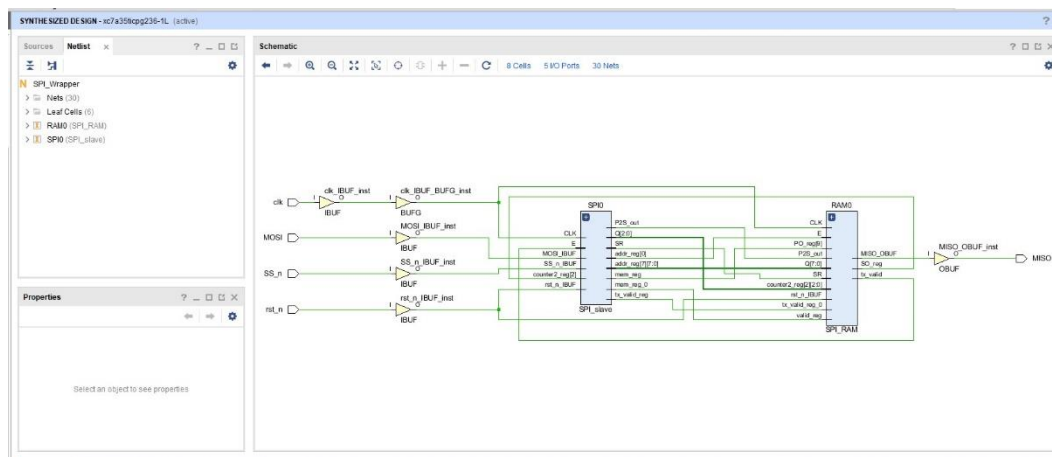
B. One hot: Schematic after elaboration:

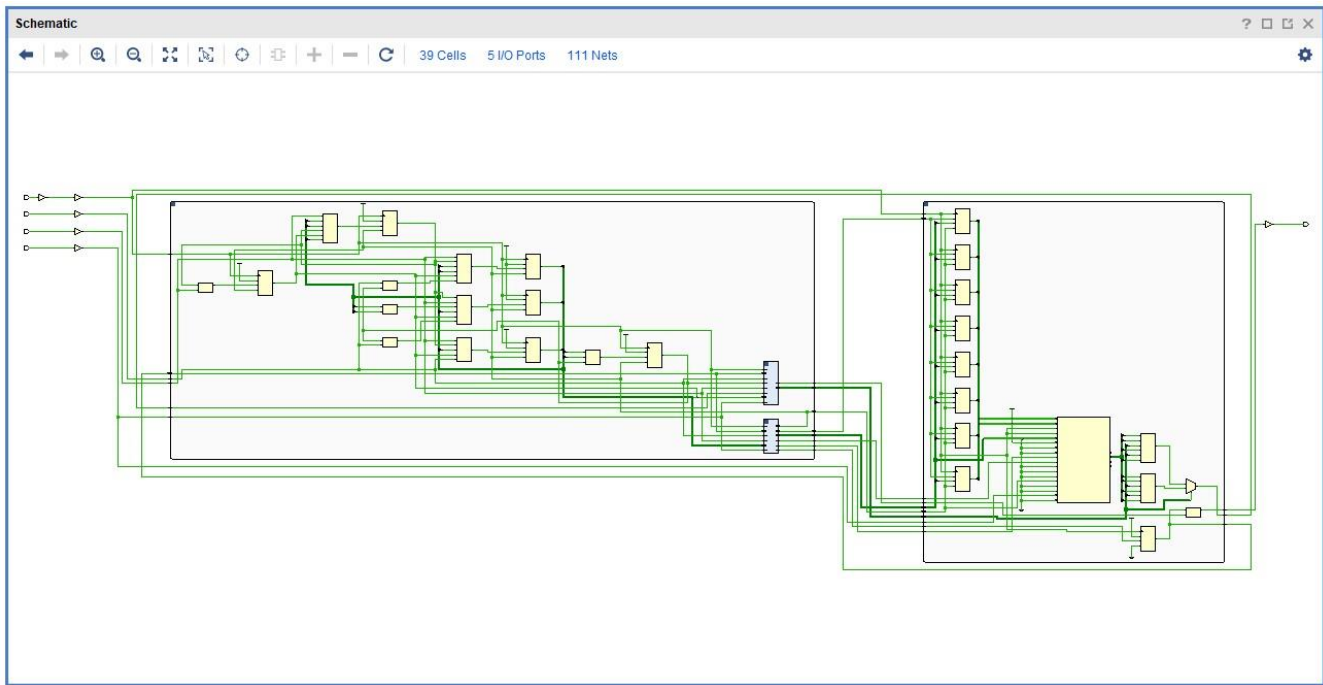


Message tab after elaboration:



Schematic after synthesis:





Message tab after synthesis:

Tcl Console Messages x Log Reports Design Runs Debug

Warning (1) Info (170) Status (329) Show All

▼ Synthesis (1 warning)

[Constraints 18-5210] No constraint will be written out.

The report showing encoding used:

```

94 Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:35 ; elapsed = 00:00:37 . Memory (MB): peak = 758.145 ; ga
95 -----
96 INFO: [Synth 8-5545] ROM "ten_flag" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
97 INFO: [Synth 8-5545] ROM "counter" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
98 INFO: [Synth 8-5545] ROM "counter2" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
99 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
100 INFO: [Synth 8-5544] ROM "RD_ADDR_OR_DATA" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
101 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
102 -----
103 State | New Encoding | Previous Encoding
104 -----
105 IDLE | 00001 | 000
106 CHK_CMD | 00010 | 001
107 READ_ADD | 00100 | 011
108 READ_DATA | 01000 | 100
109 WRITE | 10000 | 010
110 -----
111 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_slave'
112 -----
113 Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:36 ; elapsed = 00:00:37 . Memory (MB): peak = 758.145 ; gain = 500.617
114 -----
115 Report RTL Partitions:
116 +-----+
117 |RTL Partition|Replication|Instances|
118 +-----+
119 <

```


Utilization report:

Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Timing	Debug
Hierarchy							
Hierarchy							
Summary							
▼ Slice Logic							
▼ Slice LUTs (1%)							
LUT as Logic (1%)							
▼ Slice Registers (<1%)							
Register as Flip Flop (<1%)							
F7 Muxes (<1%)							
utilization_1							
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
▼ SPI_Wrapper	128	102	1	0.5	5	1	
RAM0 (SPI_RAM)	3	9	1	0.5	0	0	
SPI0 (SPI_slave)	125	93	0	0	0	0	

Timing report:

Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Timing	Debug
Design Timing Summary							
General Information							
Timer Settings							
Design Timing Summary							
Clock Summary (1)							
Check Timing (4)							
Intra-Clock Paths							
Inter-Clock Paths							
Other Path Groups							
Timing Summary - timing_1							
Setup							
Worst Negative Slack (WNS): 5.869 ns							
Total Negative Slack (TNS): 0.000 ns							
Number of Failing Endpoints: 0							
Total Number of Endpoints: 254							
Hold							
Worst Hold Slack (WHS): 0.142 ns							
Total Hold Slack (THS): 0.000 ns							
Number of Failing Endpoints: 0							
Total Number of Endpoints: 254							
Pulse Width							
Worst Pulse Width Slack (WPWS): 4.500 ns							
Total Pulse Width Negative Slack (TPWS): 0.000 ns							
Number of Failing Endpoints: 0							
Total Number of Endpoints: 105							
All user specified timing constraints are met.							

The critical path highlighted in the schematic:

SYNTHESIZED DESIGN - xc7a35t0pg236-1L (active)

Sources Netlist x ? _ □ □

counter(28)_L1 (LUT5)
counter(29)_L1 (LUT5)
counter(30)_L1 (LUT5)
counter(31)_L1 (LUT5)
counter(31)_L2 (LUT5)
counter(31)_L3 (LUT5)
counter(31)_L4 (LUT5)
counter(31)_L5 (LUT5)
counter(31)_L6 (LUT5)
counter(31)_L8 (LUT4)
counter(31)_L9 (LUT4)
counter(31)_L10 (LUT4)
counter(31)_L11 (LUT4)
counter_reg[0] (FDR)

Path Properties ? _ □ □

Path 11

Summary

Name Path 11

Slack (Hold) 0.142ns

Source SPI0/S2P/counter_reg[0]C (rising edge)

Destination SPI0/S2P/counter_reg[0]D (rising edge)

Path Group sys_clk_pin

Path Type Hold (Min at Fast Process Corner)

General Properties Report Cells Nets

Schematic x synth_1_synth_synthesis_report_0 - synth_1 x ? _ □ □

261 Cells 5 IO Ports 459 Nets

Tcl Console Messages Log Reports Design Runs Utilization Timing x Debug ? _ □ □

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (4)

Intra-Clock Paths

sys_clk_pin

Setup 5.869 ns (10)

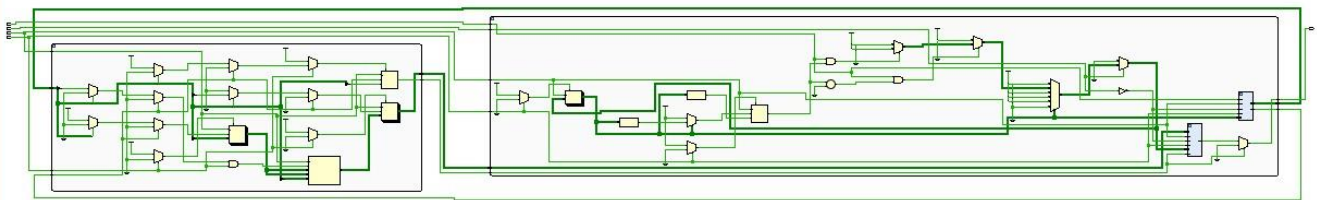
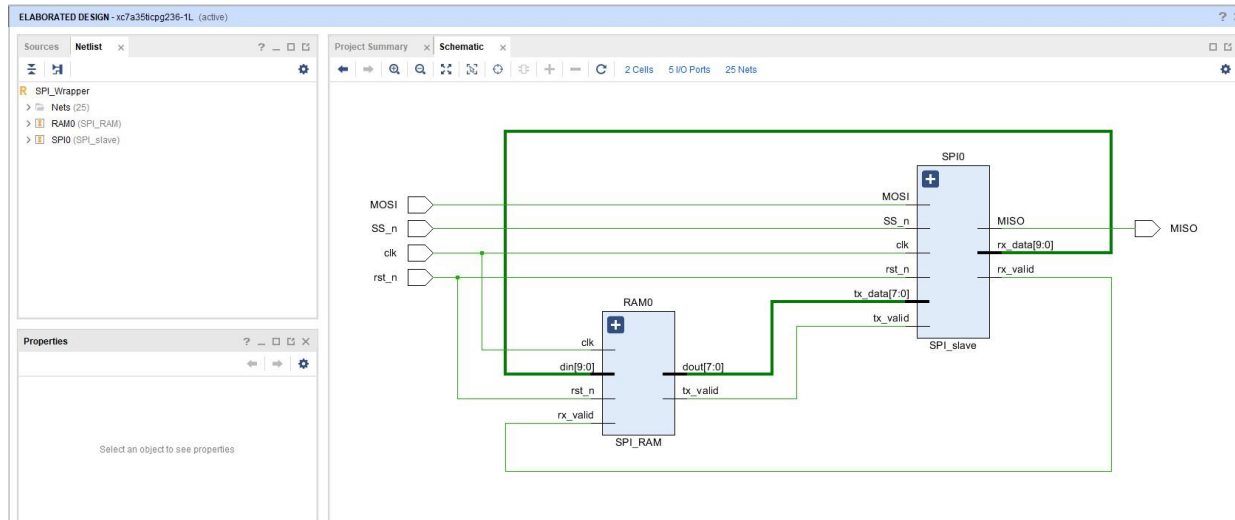
Hold 0.142 ns (10)

Timing Summary - timing_1

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 11	0.142	1	3	SPI0/S2P/counter_reg[0]C	SPI0/S2P/counter_reg[0]D	0.378	0.239	0.139	0.000	sys_clk_pin	sys_clk_pin	
Path 12	0.144	1	4	SPI0/RD_ADDR_OR_DATA_reg[0]C	SPI0/RD_ADDR_OR_DATA_reg[0]D	0.380	0.239	0.141	0.000	sys_clk_pin	sys_clk_pin	
Path 13	0.145	1	3	SPI0/S2P/PO_reg[0]C	RAM0tx_valid_reg[0]D	0.381	0.242	0.139	0.000	sys_clk_pin	sys_clk_pin	
Path 14	0.146	1	5	SPI0/FSM_onehot_cs_reg[3]C	SPI0/FSM_onehot_cs_reg[0]D	0.382	0.239	0.143	0.000	sys_clk_pin	sys_clk_pin	
Path 15	0.154	0	1	SPI0/S2P/temp0_reg[0]C	SPI0/S2P/PO_reg[0]D	0.282	0.141	0.141	0.000	sys_clk_pin	sys_clk_pin	
Path 16	0.158	0	2	SPI0/S2P/PO_reg[0]C	RAM0/addr_reg[0]D	0.286	0.141	0.145	0.000	sys_clk_pin	sys_clk_pin	

C. Sequential:

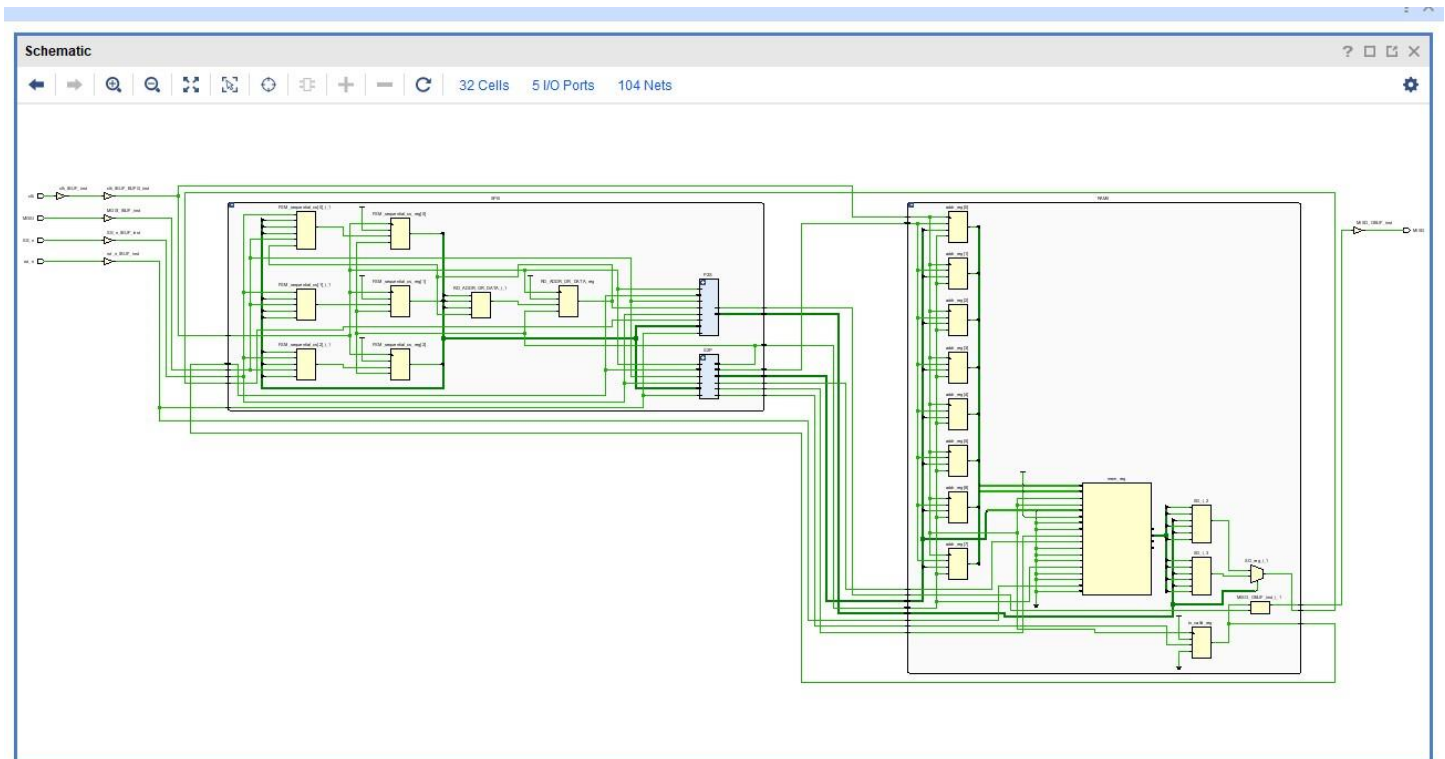
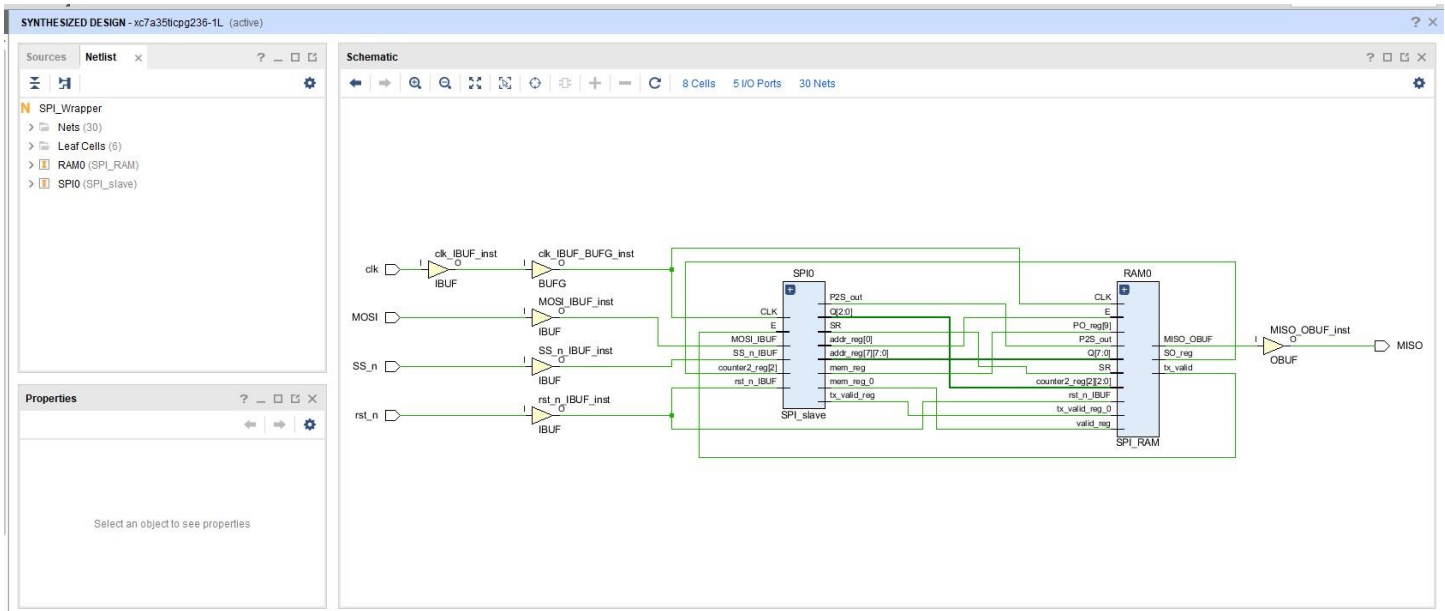
Schematic after elaboration:



Message tab after elaboration:



Schematic after synthesis:



Message tab after synthesis:

Tcl Console Messages x Log Reports Design Runs Debug

Warning (1) Info (240) Status (495) Show All

Synthesis (1 warning)

[Constraints 18-5210] No constraint will be written out.

The report showing encoding used:

```

.00 INFO: [Synth 8-5544] ROM "RD_ADDR_OR_DATA" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
.01 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
.02 -----
.03 State | New Encoding | Previous Encoding
.04 -----
.05 IDLE | 000 | 000
.06 CHK_CMD | 001 | 001
.07 READ_ADD | 010 | 011
.08 READ_DATA | 011 | 100
.09 WRITE | 100 | 010
.10 -----
.11 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_slave'
.12 -----
.13 Finished RIL Optimization Phase 2 : Time (s): cpu = 00:00:39 ; elapsed = 00:00:42 . Memory (MB): peak = 759.789 ; gain = 503.004
.14 -----
.15

```

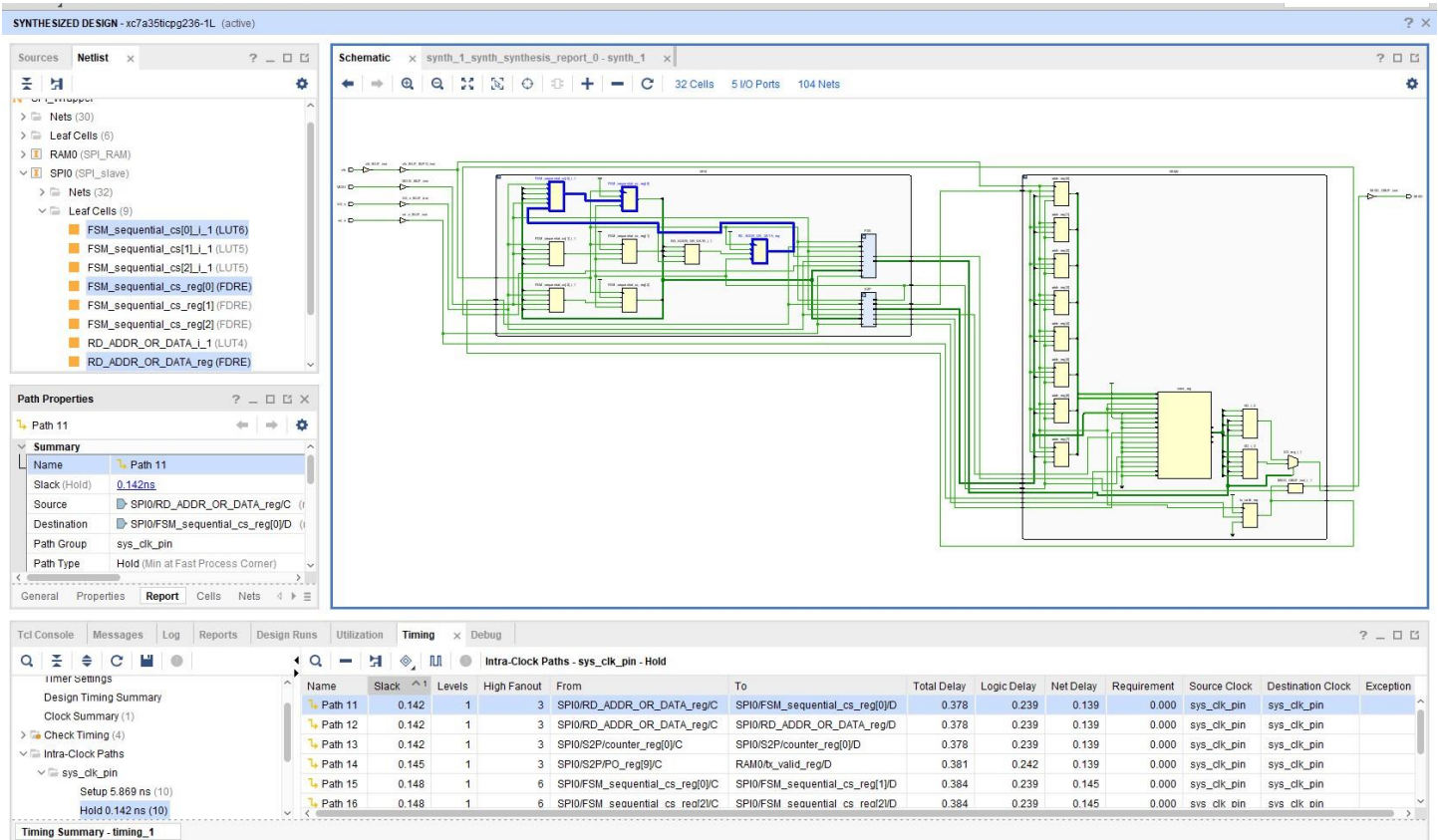
Utilization report after synthesis:

Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Timing	Debug
Hierarchy							
<div> <div> Hierarchy Summary Slice Logic <div> <div>Slice LUTs (1%)</div> <div> <div>LUT as Logic (1%)</div> </div> <div>Slice Registers (<1%)</div> <div> <div>Register as Flip Flop (<1%)</div> </div> </div> <div>F7 Muxes (<1%)</div> </div> <div>utilization_1</div> </div>							
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
SPI_Wrapper	125	100	1	0.5	5	1	
RAM0 (SPI_RAM)	3	9	1	0.5	0	0	
SPI0 (SPI_slave)	122	91	0	0	0	0	

Timing report after synthesis:

Tcl Console	Messages	Log	Reports	Design Runs	Utilization	Timing	Debug
Design Timing Summary							
<div> <div> General Information Timer Settings Design Timing Summary Clock Summary (1) Check Timing (4) Intra-Clock Paths Inter-Clock Paths Other Path Groups </div> <div> <div>Timing Summary - timing_1</div> </div> </div>							
Setup	Hold	Pulse Width					
Worst Negative Slack (WNS): 5.869 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS): 4.500 ns					
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns					
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0					
Total Number of Endpoints: 252	Total Number of Endpoints: 252	Total Number of Endpoints: 103					
All user specified timing constraints are met.							

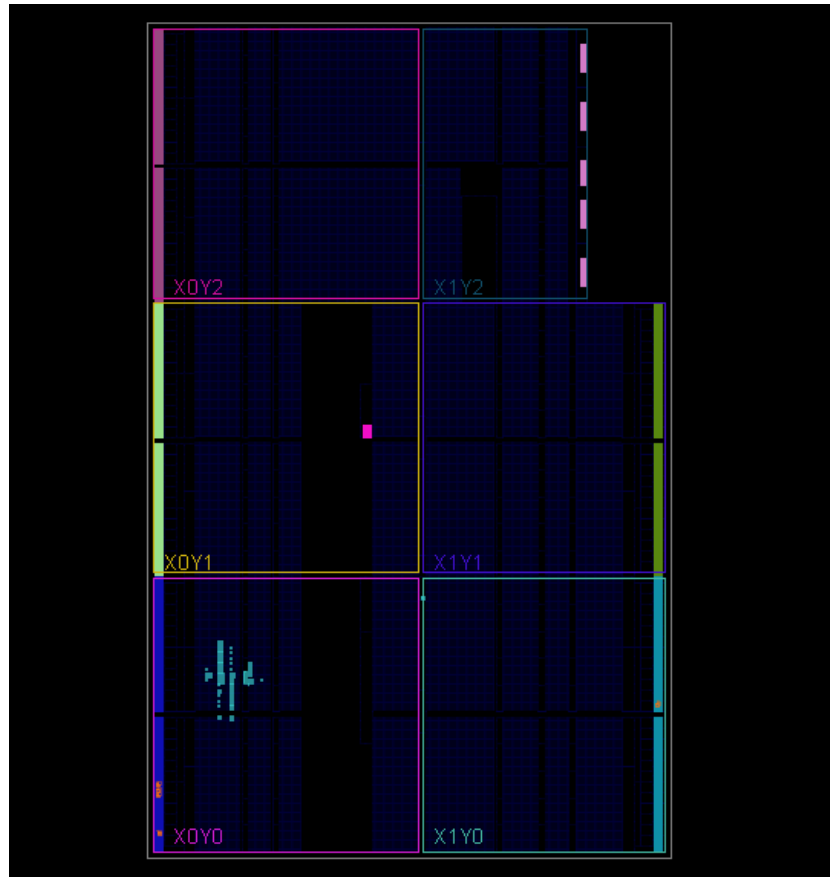
The critical path highlighted in the schematic:



3. Implementation snippets for each encoding:

A. Gray code:

FPGA device:



Utilization report after implementation:

Tcl ConsoleMessagesLogReportsDesign RunsPowerDRCMethodologyTimingUtilization x

Hierarchy

Hierarchy

Summary

▼ Slice Logic

▼ Slice LUTs (1%)

LUT as Logic (1%)

F7 Muxes (<1%)

▼ Slice Registers (<1%)

1

Name

Slice LUTs
(20800)

Slice Registers
(41600)

F7
Muxes
(16300)

Slice
(815
0)

LUT as Logic
(20800)

LUT Flip Flop Pairs
(20800)

Block RAM Tile
(50)

Bonded IOB
(106)

BUFGCTRL
(32)

▼ N SPI_Wrapper

4 RAM0 (SPI_RAM)

> 5 SPI0 (SPI_slave)

126100155126720.551

4914412205412270000

utilization_1

Timing report after implementation:

Tcl Console

Messages

Log

Reports

Design Runs

Power

DRC

Methodology

Timing

Utilization

Q

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Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (4)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

Setup

Hold

Pulse Width

Worst Negative Slack (WNS): 5.834 ns

Worst Hold Slack (WHS): 0.043 ns

Worst Pulse Width Slack (WPWS): 4.500 ns

Total Negative Slack (TNS): 0.000 ns

Total Hold Slack (THS): 0.000 ns

Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Total Number of Endpoints: 252

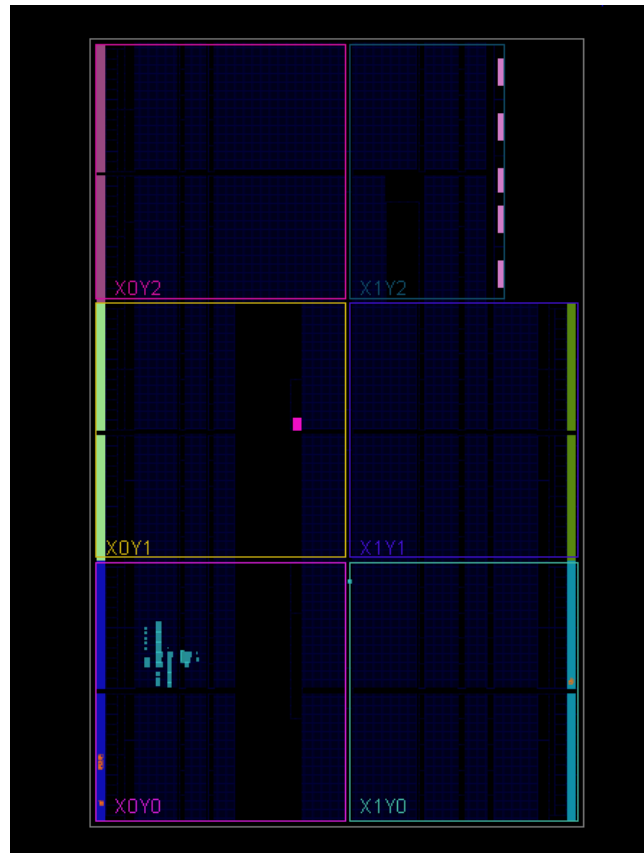
Total Number of Endpoints: 252

Total Number of Endpoints: 103

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

B. One hot: FPGA device:



Utilization report after implementation:

Tcl Console	Messages	Log	Reports	Design Runs	Power	DRC	Methodology	Timing	Utilization	x
Hierarchy										
<div> <div> <div>Hierarchy</div> <div>Summary</div> <div> <div>Slice Logic</div> <div> <div>Slice LUTs (1%)</div> <div>LUT as Logic (1%)</div> <div>F7 Muxes (<1%)</div> <div>Slice Registers (<1%)</div> </div> </div> </div> <div> <div>Name</div> <div>1</div> <div>Slice LUTs (20800)</div> <div>Slice Registers (41600)</div> <div>F7 Muxes (16300)</div> <div>Slice (815 0)</div> <div>LUT as Logic (20800)</div> <div>LUT Flip Flop Pairs (20800)</div> <div>Block RAM Tile (50)</div> <div>Bonded IOB (106)</div> <div>BUFGCTRL (32)</div> </div> </div>										
<div> <div>N SPI_Wrapper</div> <div>128</div> <div>102</div> <div>1</div> <div>51</div> <div>128</div> <div>71</div> <div>0.5</div> <div>5</div> <div>1</div> </div>										
<div> <div>RAM0 (SPI_RAM)</div> <div>4</div> <div>9</div> <div>1</div> <div>5</div> <div>4</div> <div>0</div> <div>0.5</div> <div>0</div> <div>0</div> </div>										
<div> <div>SPI0 (SPI_slave)</div> <div>124</div> <div>93</div> <div>0</div> <div>50</div> <div>124</div> <div>70</div> <div>0</div> <div>0</div> <div>0</div> </div>										

Timing report after implementation:

Tcl Console

Messages

Log

Reports

Design Runs

Power

DRC

Methodology

Timing

Utilization

Q

≡

⌵

●

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (1)

Check Timing (4)

Intra-Clock Paths

Inter-Clock Paths

Other Path Groups

Setup

Hold

Pulse Width

Worst Negative Slack (WNS): 5.684 ns

Worst Hold Slack (WHS): 0.046 ns

Worst Pulse Width Slack (WPWS): 4.500 ns

Total Negative Slack (TNS): 0.000 ns

Total Hold Slack (THS): 0.000 ns

Total Pulse Width Negative Slack (TPWS): 0.000 ns

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Number of Failing Endpoints: 0

Total Number of Endpoints: 254

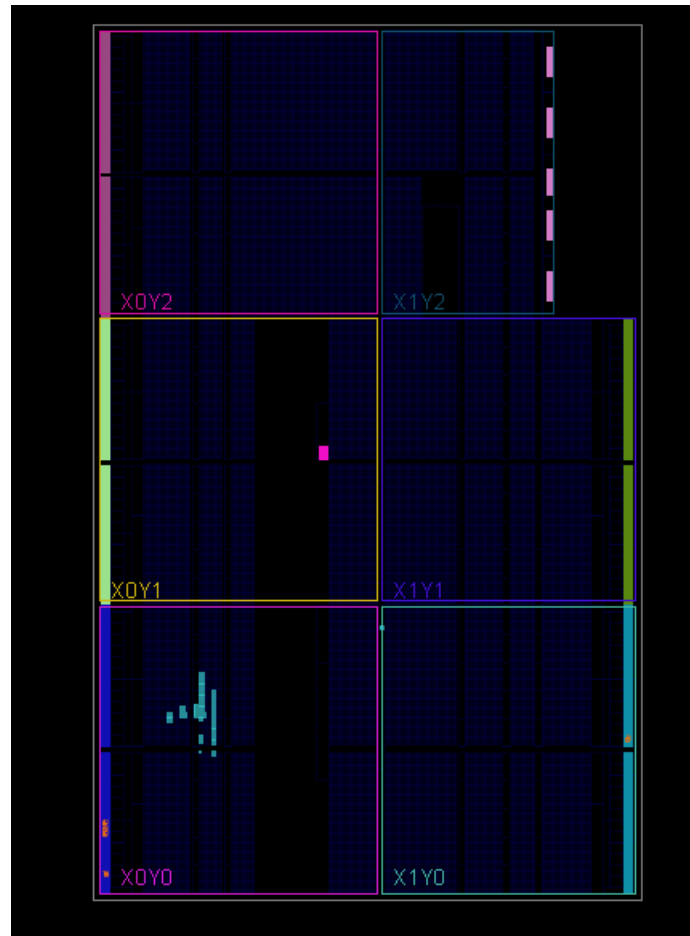
Total Number of Endpoints: 254

Total Number of Endpoints: 105

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

C. Sequential: FPGA device:



Utilization report after implementation:

Utilization										
Hierarchy										
Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
▼ N SPI_Wrapper	126	100	1	47	126	70	0.5	5	1	
RAM0 (SPI_RAM)	4	9	1	3	4	0	0.5	0	0	
SPI0 (SPI_slave)	122	91	0	46	122	68	0	0	0	

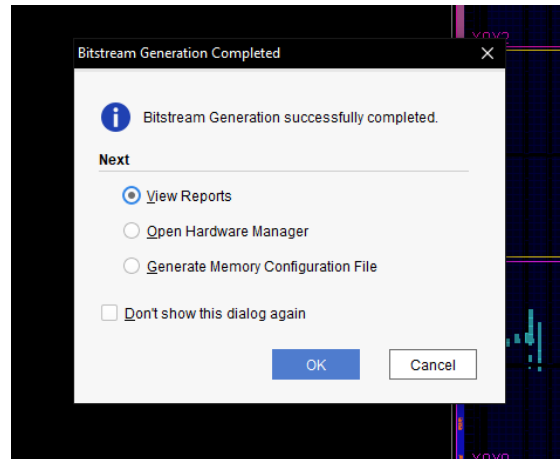
Timing report after implementation:

Tcl Console											Messages											Log											Reports											Design Runs											Power											DRC											Methodology											Timing											Utilization																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									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5. Generation of bitstream file:



6. Exporting netlist:

