Question 1 :

RTL code :

module file that is instantiated :

```
module reg_mux ( in , sel , out , clk , rst , en );
parameter INWIDTH = 18 ; // width of inputs
parameter OUTWIDTH = 18 ; // width of outputs
parameter RSTTYPE = "SYNC" ; // chooses the rst to be sync or async
input [INWIDTH-1:0] in ; // bypassed input
input sel , clk , en , rst ; // control signals
reg [INWIDTH-1:0] in_reg ; // registered input
output [OUTWIDTH-1:0] out ; // output of the block
// register block
always @(posedge clk) begin
  if (rst) begin
    in_reg <= 0 ; //rst the reg
  end else if (en) begin
    in_reg <= in ;//pass in to reg output
  end
end
//mux
assign out = (sel==1) ? in_reg:in; //sel=1 then pass the registered if sel=0 pass the
new value
endmodule
```

Total design file :

```
`include "mux_reg.v"
module Spartan6_DSP48A1 ( A , B , D , BCIN , C , PCIN , OPMODE
, clk , CARRYIN , RSTA , RSTB , RSTM , RSTP , RSTC , RSTD , RSTCARRYIN , RSTOPMODE
, CEA , CEB , CEM , CEP , CEC , CED , CECARRYIN , CEOPMODE , BCOUT , PCOUT
, P , M , CARRYOUT , CARRYOUTF );
//parameters
parameter A0REG = 0;
parameter A1REG = 1;
parameter B0REG = 0;
parameter B1REG = 1;
parameter CREG = 1;
parameter DREG = 1;
parameter MREG = 1;
parameter PREG = 1;
parameter CARRYINREG = 1;
parameter CARRYOUTREG = 1;
```

```
parameter OPMODEREG = 1;
parameter CARRYINSEL = "OPMODE5";
parameter B_INPUT = "DIRECT";
//inputs and outputs
input [17:0] A , B , D , BCIN ;
input [47:0] C , PCIN ;
input [7:0] OPMODE ;
input clk , CARRYIN , RSTA , RSTB , RSTM , RSTP , RSTC , RSTD , RSTCARRYIN , RSTOPMODE
, CEA , CEB , CEM , CEP , CEC , CED , CECARRYIN , CEOPMODE ;
output  [17:0] BCOUT ;
output  [47:0] PCOUT , P  ;
output  [35:0] M ;
output  CARRYOUT , CARRYOUTF ;
//wires and regs
wire [17:0] m1_out , m2_out , m3_out , m5_out , m6_out;
reg [17:0] mux1_out ;
wire[17:0] add1 , mux3_out ;
wire [47:0] m4_out , m10_out ;
reg [47:0]  x_out , z_out ;
wire[47:0] concat_out , add2 ;
wire [35:0]  m7_out ;
wire[35:0] mult_out ;
wire m8_out , m9_out ;
reg mux2_out  ;
wire  add2_cout ;
wire [7:0] m11_out ;
//handling two muxes with there parameters options
always @(*) begin
if ( CARRYINSEL =="OPMODE5" && CARRYINSEL =="CARRYIN") begin
  mux2_out = 0 ;
end else if (CARRYINSEL == "OPMODE5" ) begin
  mux2_out = m11_out[5] ;

end else if (CARRYINSEL == "CARRYIN") begin
  mux2_out = CARRYIN ;
  end
  end
always @(*) begin
if ( B_INPUT  != "DIRECT" && B_INPUT  != "CASCADE") begin
  mux1_out = 0 ;
end else if (B_INPUT == "DIRECT" ) begin
  mux1_out = B ;
end else if (B_INPUT == "CASECADE") begin
  mux1_out = BCIN ;
  end
  end
//assign statments
```

```
assign concat_out = { m1_out[11:0] , m6_out[17:0] , m5_out[17:0] } ;
assign BCOUT = m5_out ;
assign M = m7_out ;
assign CARRYOUT = m9_out ;
assign CARRYOUTF = CARRYOUT ;
assign P = m10_out ;
assign PCOUT = P ;
assign add1 = ( m11_out[6] == 0 ) ? m1_out+m2_out : m1_out-m2_out ;
assign {add2_cout , add2} = ( m11_out[7] == 0 ) ? z_out+x_out+m8_out : z_out-
(x_out+m8_out) ;
assign mult_out = m5_out * m6_out ;
assign mux3_out = (m11_out[4] == 0) ? m2_out:add1 ;
// x and z muxes
always @(*) begin
  case (m11_out[1:0])
    0 : x_out = 0 ;
    1 : x_out = m7_out ;
    2 : x_out = PCOUT ;
    3 : x_out = concat_out ;
  endcase
end
always @(*) begin
  case (m11_out[3:2])
    0 : z_out = 0 ;
    1 : z_out = PCIN ;
    2 : z_out = PCOUT ;
    3 : z_out = m4_out ;
  endcase
end
// instantiations
reg_mux #( .INWIDTH(18) , .OUTWIDTH(18) , .RSTTYPE("SYNC") ) m1 ( .in(D) ,
.sel(DREG) , .out(m1_out) , .clk(clk) , .rst(RSTD) , .en(CED) ); //DREG
reg_mux #( .INWIDTH(18) , .OUTWIDTH(18) , .RSTTYPE("SYNC") ) m2 ( .in(B) , .sel(B0REG)
, .out(m2_out) , .clk(clk) , .rst(RSTB) , .en(CEB) ); //B0REG
reg_mux #( .INWIDTH(18) , .OUTWIDTH(18) , .RSTTYPE("SYNC") ) m3 ( .in(A) , .sel(A0REG)
, .out(m3_out) , .clk(clk) , .rst(RSTA) , .en(CEA) ); //A0REG
reg_mux #( .INWIDTH(48) , .OUTWIDTH(48) , .RSTTYPE("SYNC") ) m4 ( .in(C) ,
.sel(CREG) , .out(m4_out) , .clk(clk) , .rst(RSTC) , .en(CEC) ); //CREG
reg_mux #( .INWIDTH(18) , .OUTWIDTH(18) , .RSTTYPE("SYNC") ) m5 ( .in(mux3_out) ,
.sel(B1REG) , .out(m5_out) , .clk(clk) , .rst(RSTB) , .en(CEB) ); //B1REG
reg_mux #( .INWIDTH(18) , .OUTWIDTH(18) , .RSTTYPE("SYNC") ) m6 ( .in(m3_out) ,
.sel(A1REG) , .out(m6_out) , .clk(clk) , .rst(RSTA) , .en(CEA) ); //A1REG
reg_mux #( .INWIDTH(36) , .OUTWIDTH(36) , .RSTTYPE("SYNC") ) m7 ( .in(mult_out) ,
.sel(MREG) , .out(m7_out) , .clk(clk) , .rst(RSTM) , .en(CEM) ); //MREG
reg_mux #( .INWIDTH(1) , .OUTWIDTH(1) , .RSTTYPE("SYNC") ) m8 ( .in(mux2_out) ,
.sel(CARRYINREG) , .out(m8_out) , .clk(clk) , .rst(RSTCARRYIN) , .en(CECARRYIN) );
//CYI
```

```
reg_mux #( .INWIDTH(1) , .OUTWIDTH(1) , .RSTTYPE("SYNC") ) m9 ( .in(add2_cout) ,
.sel(CARRYOUTREG) , .out(m9_out) , .clk(clk) , .rst(RSTCARRYIN) , .en(CECARRYIN) );
//CYO
reg_mux #( .INWIDTH(48) , .OUTWIDTH(48) , .RSTTYPE("SYNC") ) m10 ( .in(add2) ,
.sel(PREG) , .out(m10_out) , .clk(clk) , .rst(RSTP) , .en(CEP) ); //PREG
reg_mux #( .INWIDTH(8) , .OUTWIDTH(8) , .RSTTYPE("SYNC") ) m11 ( .in(OPMODE) ,
.sel(OPMODEREG) , .out(m11_out) , .clk(clk) , .rst(RSTOPMODE) , .en(CEOPMODE) );
//D0REG
endmodule
```

Test bench :

```
`include "mux_reg.v"
module Spartan6_DSP48A1_tb ();
//signal decleration
reg [17:0] A , B , D , BCIN ;
reg [47:0] C , PCIN ;
reg [7:0] OPMODE ;
reg clk , CARRYIN , RSTA , RSTB , RSTM , RSTP , RSTC , RSTD , RSTCARRYIN , RSTOPMODE
, CEA , CEB , CEM , CEP , CEC , CED , CECARRYIN , CEOPMODE ;
wire  [17:0] BCOUT ;
wire  [47:0] PCOUT , P  ;
wire  [35:0] M ;
wire  CARRYOUT , CARRYOUTF ;
//dut instantiation
Spartan6_DSP48A1 dut ( A , B , D , BCIN , C , PCIN , OPMODE
, clk , CARRYIN , RSTA , RSTB , RSTM , RSTP , RSTC , RSTD , RSTCARRYIN , RSTOPMODE
, CEA , CEB , CEM , CEP , CEC , CED , CECARRYIN , CEOPMODE , BCOUT , PCOUT
, P , M , CARRYOUT , CARRYOUTF );
// clock generation
initial begin
  clk = 0 ;
  forever begin
    #1 clk =~ clk ;
  end
end
//test
initial begin
  //intilization
  RSTA = 1 ;
  RSTB = 1 ;
  RSTM = 1 ;
  RSTP = 1 ;
  RSTC = 1 ;
  RSTD = 1 ;
  RSTCARRYIN = 1 ;
  RSTOPMODE = 1 ;
```

```
    CEA = 0 ;
    CEB = 0 ;
    CEM = 0 ;
    CEP = 0 ;
    CEC = 0 ;
    CED = 0 ;
    CECARRYIN = 0 ;
    CEOPMODE = 0 ;
    @(negedge clk );
     RSTA = 0 ;
    RSTB = 0 ;
    RSTM = 0 ;
    RSTP = 0 ;
    RSTC = 0 ;
    RSTD = 0 ;
    RSTCARRYIN = 0 ;
    RSTOPMODE = 0 ;
    CEA = 1 ;
    CEB = 1 ;
    CEM = 1 ;
    CEP = 1 ;
    CEC = 1 ;
    CED = 1 ;
    CECARRYIN = 1 ;
    CEOPMODE = 1 ;
    //randomization
    OPMODE[1:0] = 0;
    repeat(5) begin
      A = $random ;
      B = $random ;
      C = $random ;
      D = $random ;
      CARRYIN = $random ;
      BCIN = $random ;
      PCIN = $random ;
      @(negedge clk) ;
    end
    #5;
    OPMODE[1:0] = 1;
    repeat(5) begin
      A = $random ;
      B = $random ;
      C = $random ;
      D = $random ;
      CARRYIN = $random ;
      BCIN = $random ;
      PCIN = $random ;
```

```
    @(negedge clk) ;
  end
  #5;
  OPMODE[1:0] = 2;
  repeat(5) begin
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  OPMODE[1:0] = 3;
  repeat(5) begin
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  OPMODE[3:2] = 0;
  repeat(5) begin
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  OPMODE[3:2] = 1;
  repeat(5) begin
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
```

```
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  OPMODE[3:2] = 2;
  repeat(5) begin
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  OPMODE[3:2] = 3;
  repeat(5) begin
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  repeat(5) begin
    OPMODE[4] = $random;
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  repeat(5) begin
    OPMODE[5] = $random;
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
```

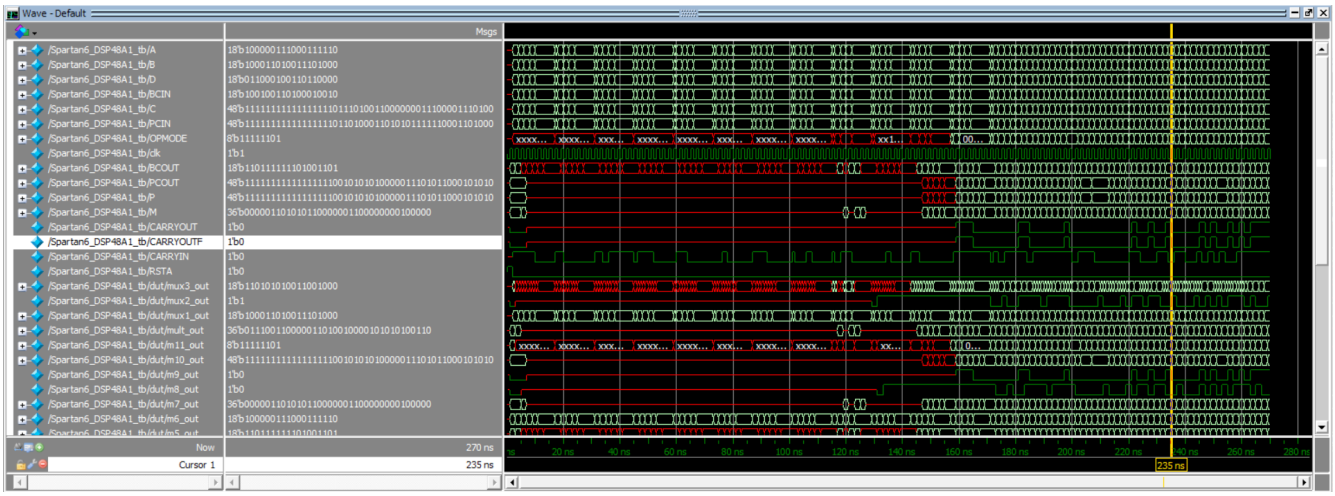
```
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  repeat(5) begin
    OPMODE[6] = $random;
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  repeat(5) begin
    OPMODE[7] = $random;
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  #5;
  repeat(50) begin
    OPMODE = $random;
    A = $random ;
    B = $random ;
    C = $random ;
    D = $random ;
    CARRYIN = $random ;
    BCIN = $random ;
    PCIN = $random ;
    @(negedge clk) ;
  end
  $stop;
end
//test monitor and results
initial begin
  $monitor (" A = %b B = %b , C = %b , D = %b , CARRYIN = %b , BCIN = %b , PCIN = %b
  , BCOUT = %b  , PCOUT = %b , P = %b , M = %b , CARRYOUT = %b , CARRYOUTF = %b "
  , A , B , C ,  D , CARRYIN , BCIN , PCIN
```

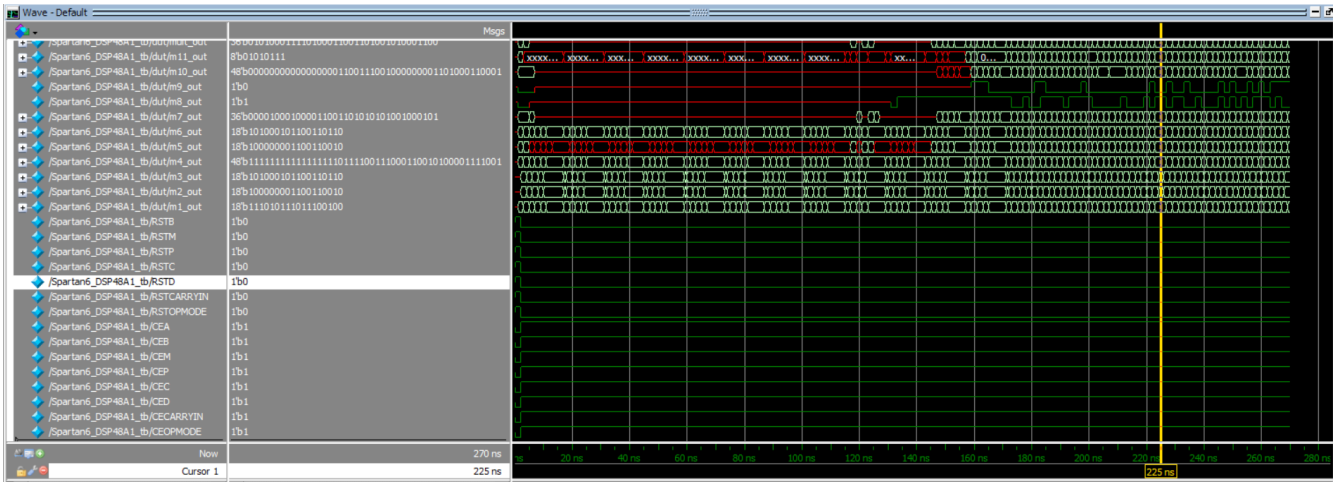
```
  , BCOUT , PCOUT , P , M , CARRYOUT , CARRYOUTF );
end
endmodule
```

Do file:

```
vlib work
vlog project1.v project1_tb.v
vsim -voptargs=+acc work.Spartan6_DSP48A1_tb
add wave *
add wave -position insertpoint  \
sim:/Spartan6_DSP48A1_tb/dut/mux3_out \
sim:/Spartan6_DSP48A1_tb/dut/mux2_out \
sim:/Spartan6_DSP48A1_tb/dut/mux1_out \
sim:/Spartan6_DSP48A1_tb/dut/mult_out \
sim:/Spartan6_DSP48A1_tb/dut/m11_out \
sim:/Spartan6_DSP48A1_tb/dut/m10_out \
sim:/Spartan6_DSP48A1_tb/dut/m9_out \
sim:/Spartan6_DSP48A1_tb/dut/m8_out \
sim:/Spartan6_DSP48A1_tb/dut/m7_out \
sim:/Spartan6_DSP48A1_tb/dut/m6_out \
sim:/Spartan6_DSP48A1_tb/dut/m5_out \
sim:/Spartan6_DSP48A1_tb/dut/m4_out \
sim:/Spartan6_DSP48A1_tb/dut/m3_out \
sim:/Spartan6_DSP48A1_tb/dut/m2_out \
sim:/Spartan6_DSP48A1_tb/dut/m1_out
run -all
#quit -sim
```

Questasim simulations:





Constraint file :

```
## This file is a general .xdc for the Basys3 rev B board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level
signal names in the project

## Clock signal
set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports clk]
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]


## Switches
#set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports {sw[0]}]
#set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports {sw[1]}]
#set_property -dict { PACKAGE_PIN W16   IOSTANDARD LVCMOS33 } [get_ports {sw[2]}]
```

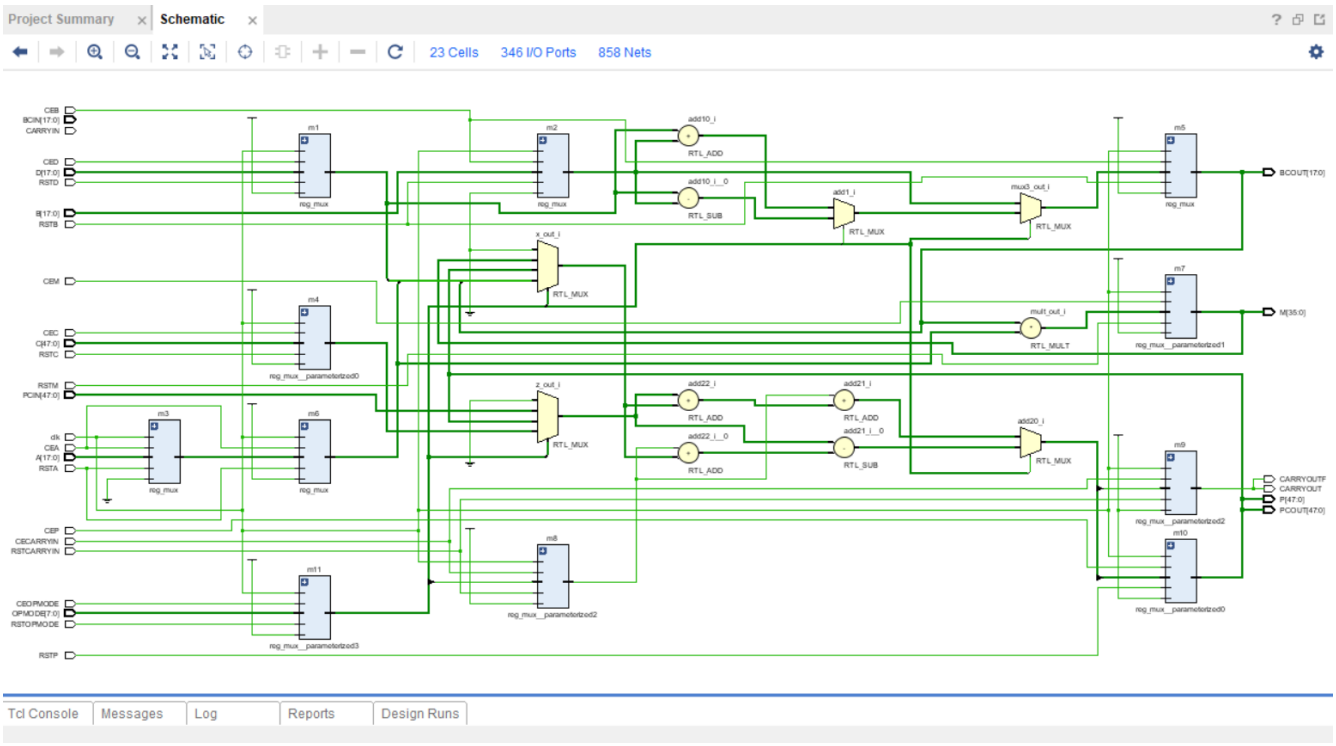
```
#set_property -dict { PACKAGE_PIN W17   IOSTANDARD LVCMOS33 } [get_ports {sw[3]}]
#set_property -dict { PACKAGE_PIN W15   IOSTANDARD LVCMOS33 } [get_ports {sw[4]}]
#set_property -dict { PACKAGE_PIN V15   IOSTANDARD LVCMOS33 } [get_ports {sw[5]}]
#set_property -dict { PACKAGE_PIN W14   IOSTANDARD LVCMOS33 } [get_ports {sw[6]}]
#set_property -dict { PACKAGE_PIN W13   IOSTANDARD LVCMOS33 } [get_ports {sw[7]}]
#set_property -dict { PACKAGE_PIN V2    IOSTANDARD LVCMOS33 } [get_ports {sw[8]}]
#set_property -dict { PACKAGE_PIN T3    IOSTANDARD LVCMOS33 } [get_ports {sw[9]}]
#set_property -dict { PACKAGE_PIN T2    IOSTANDARD LVCMOS33 } [get_ports {sw[10]}]
#set_property -dict { PACKAGE_PIN R3    IOSTANDARD LVCMOS33 } [get_ports {sw[11]}]
#set_property -dict { PACKAGE_PIN W2    IOSTANDARD LVCMOS33 } [get_ports {sw[12]}]
#set_property -dict { PACKAGE_PIN U1    IOSTANDARD LVCMOS33 } [get_ports {sw[13]}]
#set_property -dict { PACKAGE_PIN T1    IOSTANDARD LVCMOS33 } [get_ports {sw[14]}]
#set_property -dict { PACKAGE_PIN R2    IOSTANDARD LVCMOS33 } [get_ports {sw[15]}]


## LEDs
#set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports {led[0]}]
#set_property -dict { PACKAGE_PIN E19   IOSTANDARD LVCMOS33 } [get_ports {led[1]}]
#set_property -dict { PACKAGE_PIN U19   IOSTANDARD LVCMOS33 } [get_ports {led[2]}]
#set_property -dict { PACKAGE_PIN V19   IOSTANDARD LVCMOS33 } [get_ports {led[3]}]
#set_property -dict { PACKAGE_PIN W18   IOSTANDARD LVCMOS33 } [get_ports {led[4]}]
#set_property -dict { PACKAGE_PIN U15   IOSTANDARD LVCMOS33 } [get_ports {led[5]}]
#set_property -dict { PACKAGE_PIN U14   IOSTANDARD LVCMOS33 } [get_ports {led[6]}]
#set_property -dict { PACKAGE_PIN V14   IOSTANDARD LVCMOS33 } [get_ports {led[7]}]
#set_property -dict { PACKAGE_PIN V13   IOSTANDARD LVCMOS33 } [get_ports {led[8]}]
#set_property -dict { PACKAGE_PIN V3    IOSTANDARD LVCMOS33 } [get_ports {led[9]}]
#set_property -dict { PACKAGE_PIN W3    IOSTANDARD LVCMOS33 } [get_ports {led[10]}]
#set_property -dict { PACKAGE_PIN U3    IOSTANDARD LVCMOS33 } [get_ports {led[11]}]
#set_property -dict { PACKAGE_PIN P3    IOSTANDARD LVCMOS33 } [get_ports {led[12]}]
#set_property -dict { PACKAGE_PIN N3    IOSTANDARD LVCMOS33 } [get_ports {led[13]}]
#set_property -dict { PACKAGE_PIN P1    IOSTANDARD LVCMOS33 } [get_ports {led[14]}]
#set_property -dict { PACKAGE_PIN L1    IOSTANDARD LVCMOS33 } [get_ports {led[15]}]


##7 Segment Display
#set_property -dict { PACKAGE_PIN W7   IOSTANDARD LVCMOS33 } [get_ports {seg[0]}]
#set_property -dict { PACKAGE_PIN W6   IOSTANDARD LVCMOS33 } [get_ports {seg[1]}]
#set_property -dict { PACKAGE_PIN U8   IOSTANDARD LVCMOS33 } [get_ports {seg[2]}]
#set_property -dict { PACKAGE_PIN V8   IOSTANDARD LVCMOS33 } [get_ports {seg[3]}]
#set_property -dict { PACKAGE_PIN U5   IOSTANDARD LVCMOS33 } [get_ports {seg[4]}]
#set_property -dict { PACKAGE_PIN V5   IOSTANDARD LVCMOS33 } [get_ports {seg[5]}]
#set_property -dict { PACKAGE_PIN U7   IOSTANDARD LVCMOS33 } [get_ports {seg[6]}]

#set_property -dict { PACKAGE_PIN V7   IOSTANDARD LVCMOS33 } [get_ports dp]

#set_property -dict { PACKAGE_PIN U2   IOSTANDARD LVCMOS33 } [get_ports {an[0]}]
#set_property -dict { PACKAGE_PIN U4   IOSTANDARD LVCMOS33 } [get_ports {an[1]}]
```

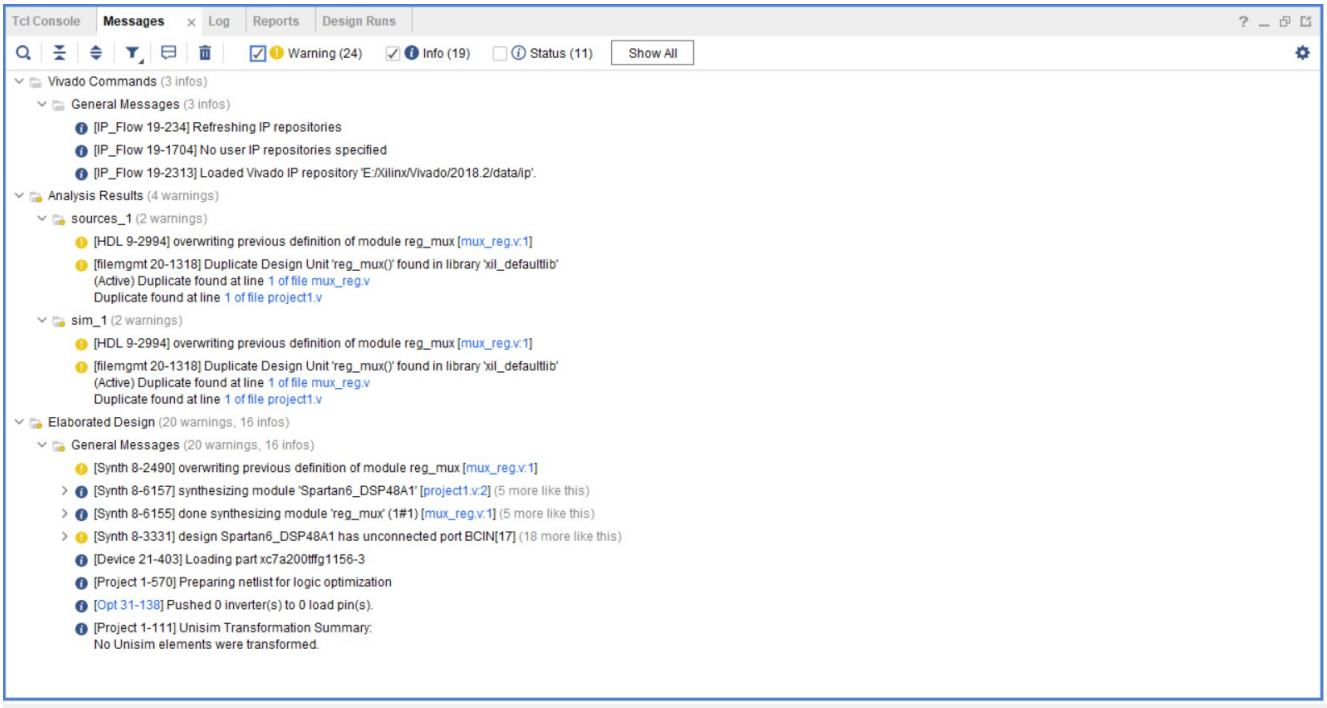
```
#set_property -dict { PACKAGE_PIN V4   IOSTANDARD LVCMOS33 } [get_ports {an[2]}]
#set_property -dict { PACKAGE_PIN W4   IOSTANDARD LVCMOS33 } [get_ports {an[3]}]


##Buttons
#set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports rst]
#set_property -dict { PACKAGE_PIN T18   IOSTANDARD LVCMOS33 } [get_ports btnU]
#set_property -dict { PACKAGE_PIN W19   IOSTANDARD LVCMOS33 } [get_ports btnL]
#set_property -dict { PACKAGE_PIN T17   IOSTANDARD LVCMOS33 } [get_ports btnR]
#set_property -dict { PACKAGE_PIN U17   IOSTANDARD LVCMOS33 } [get_ports btnD]


##Pmod Header JA
#set_property -dict { PACKAGE_PIN J1   IOSTANDARD LVCMOS33 } [get_ports {JA[0]}];#Sch
name = JA1
#set_property -dict { PACKAGE_PIN L2   IOSTANDARD LVCMOS33 } [get_ports {JA[1]}];#Sch
name = JA2
#set_property -dict { PACKAGE_PIN J2   IOSTANDARD LVCMOS33 } [get_ports {JA[2]}];#Sch
name = JA3
#set_property -dict { PACKAGE_PIN G2   IOSTANDARD LVCMOS33 } [get_ports {JA[3]}];#Sch
name = JA4
#set_property -dict { PACKAGE_PIN H1   IOSTANDARD LVCMOS33 } [get_ports {JA[4]}];#Sch
name = JA7
#set_property -dict { PACKAGE_PIN K2   IOSTANDARD LVCMOS33 } [get_ports {JA[5]}];#Sch
name = JA8
#set_property -dict { PACKAGE_PIN H2   IOSTANDARD LVCMOS33 } [get_ports {JA[6]}];#Sch
name = JA9
#set_property -dict { PACKAGE_PIN G3   IOSTANDARD LVCMOS33 } [get_ports {JA[7]}];#Sch
name = JA10

##Pmod Header JB
#set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 } [get_ports {JB[0]}];#Sch
name = JB1
#set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 } [get_ports {JB[1]}];#Sch
name = JB2
#set_property -dict { PACKAGE_PIN B15   IOSTANDARD LVCMOS33 } [get_ports {JB[2]}];#Sch
name = JB3
#set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33 } [get_ports {JB[3]}];#Sch
name = JB4
#set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 } [get_ports {JB[4]}];#Sch
name = JB7
#set_property -dict { PACKAGE_PIN A17   IOSTANDARD LVCMOS33 } [get_ports {JB[5]}];#Sch
name = JB8
#set_property -dict { PACKAGE_PIN C15   IOSTANDARD LVCMOS33 } [get_ports {JB[6]}];#Sch
name = JB9
#set_property -dict { PACKAGE_PIN C16   IOSTANDARD LVCMOS33 } [get_ports {JB[7]}];#Sch
name = JB10
```

```
##Pmod Header JC
#set_property -dict { PACKAGE_PIN K17   IOSTANDARD LVCMOS33 } [get_ports {JC[0]}];#Sch
name = JC1
#set_property -dict { PACKAGE_PIN M18   IOSTANDARD LVCMOS33 } [get_ports {JC[1]}];#Sch
name = JC2
#set_property -dict { PACKAGE_PIN N17   IOSTANDARD LVCMOS33 } [get_ports {JC[2]}];#Sch
name = JC3
#set_property -dict { PACKAGE_PIN P18   IOSTANDARD LVCMOS33 } [get_ports {JC[3]}];#Sch
name = JC4
#set_property -dict { PACKAGE_PIN L17   IOSTANDARD LVCMOS33 } [get_ports {JC[4]}];#Sch
name = JC7
#set_property -dict { PACKAGE_PIN M19   IOSTANDARD LVCMOS33 } [get_ports {JC[5]}];#Sch
name = JC8
#set_property -dict { PACKAGE_PIN P17   IOSTANDARD LVCMOS33 } [get_ports {JC[6]}];#Sch
name = JC9
#set_property -dict { PACKAGE_PIN R18   IOSTANDARD LVCMOS33 } [get_ports {JC[7]}];#Sch
name = JC10

##Pmod Header JXADC
#set_property -dict { PACKAGE_PIN J3   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[0]}];#Sch name = XA1_P
#set_property -dict { PACKAGE_PIN L3   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[1]}];#Sch name = XA2_P
#set_property -dict { PACKAGE_PIN M2   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[2]}];#Sch name = XA3_P
#set_property -dict { PACKAGE_PIN N2   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[3]}];#Sch name = XA4_P
#set_property -dict { PACKAGE_PIN K3   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[4]}];#Sch name = XA1_N
#set_property -dict { PACKAGE_PIN M3   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[5]}];#Sch name = XA2_N
#set_property -dict { PACKAGE_PIN M1   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[6]}];#Sch name = XA3_N
#set_property -dict { PACKAGE_PIN N1   IOSTANDARD LVCMOS33 } [get_ports
{JXADC[7]}];#Sch name = XA4_N


##VGA Connector
#set_property -dict { PACKAGE_PIN G19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[0]}]
#set_property -dict { PACKAGE_PIN H19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[1]}]
#set_property -dict { PACKAGE_PIN J19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[2]}]
#set_property -dict { PACKAGE_PIN N19   IOSTANDARD LVCMOS33 } [get_ports {vgaRed[3]}]
#set_property -dict { PACKAGE_PIN N18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[0]}]
#set_property -dict { PACKAGE_PIN L18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[1]}]
#set_property -dict { PACKAGE_PIN K18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[2]}]
#set_property -dict { PACKAGE_PIN J18   IOSTANDARD LVCMOS33 } [get_ports {vgaBlue[3]}]
```

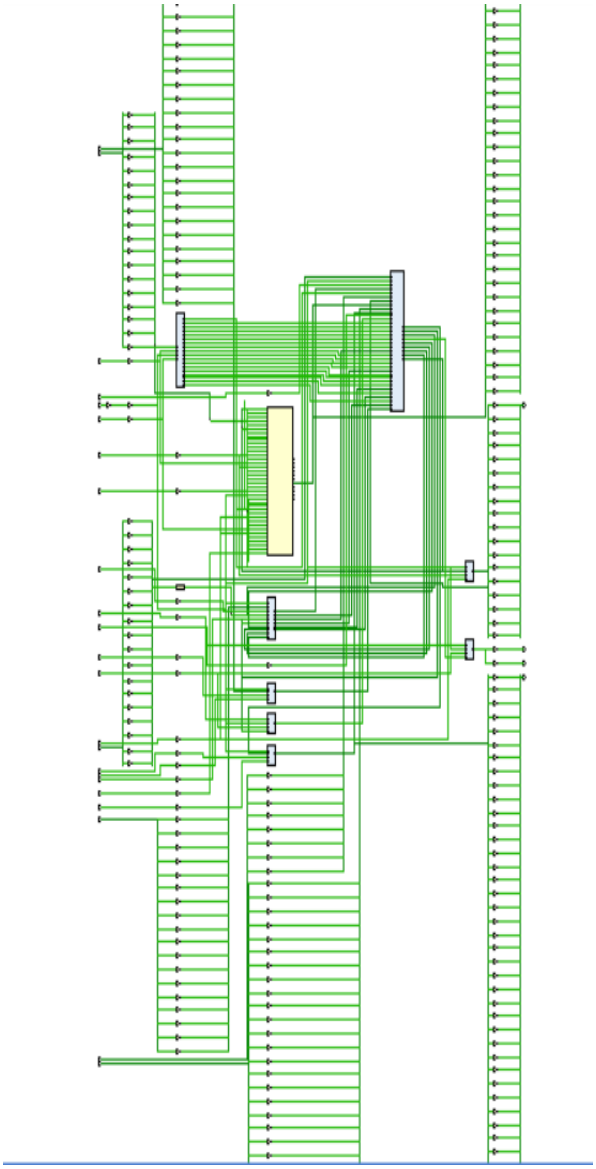
```
#set_property -dict { PACKAGE_PIN J17   IOSTANDARD LVCMOS33 } [get_ports
{vgaGreen[0]}]
#set_property -dict { PACKAGE_PIN H17   IOSTANDARD LVCMOS33 } [get_ports
{vgaGreen[1]}]
#set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports
{vgaGreen[2]}]
#set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports
{vgaGreen[3]}]
#set_property -dict { PACKAGE_PIN P19   IOSTANDARD LVCMOS33 } [get_ports Hsync]
#set_property -dict { PACKAGE_PIN R19   IOSTANDARD LVCMOS33 } [get_ports Vsync]


##USB-RS232 Interface
#set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [get_ports RsRx]
#set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33 } [get_ports RsTx]


##USB HID (PS/2)
#set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports
PS2Clk]
#set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33   PULLUP true } [get_ports
PS2Data]


##Quad SPI Flash
##Note that CCLK_0 cannot be placed in 7 series devices. You can access it using the
##STARTUPE2 primitive.
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[0]}]
#set_property -dict { PACKAGE_PIN D19   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[1]}]
#set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[2]}]
#set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports {QspiDB[3]}]
#set_property -dict { PACKAGE_PIN K19   IOSTANDARD LVCMOS33 } [get_ports QspiCSn]


## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]

## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
```

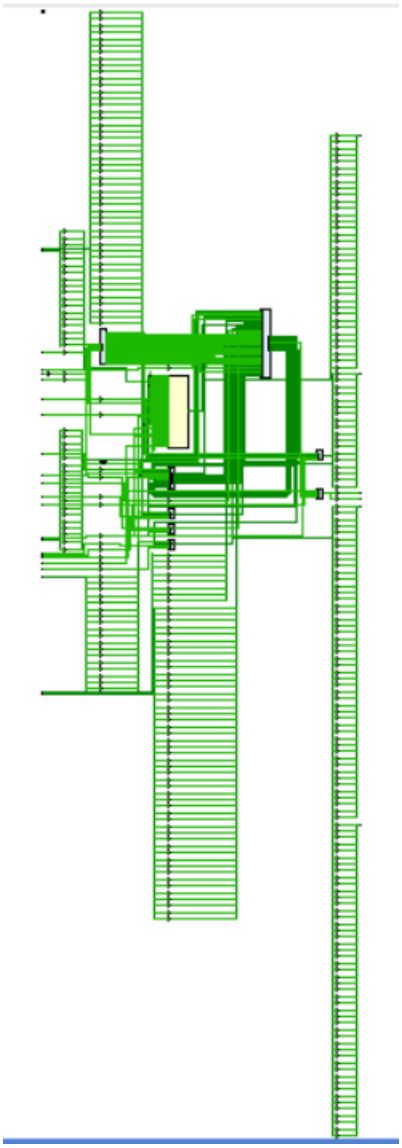
Snippets from schematic and message tab after elaboration :

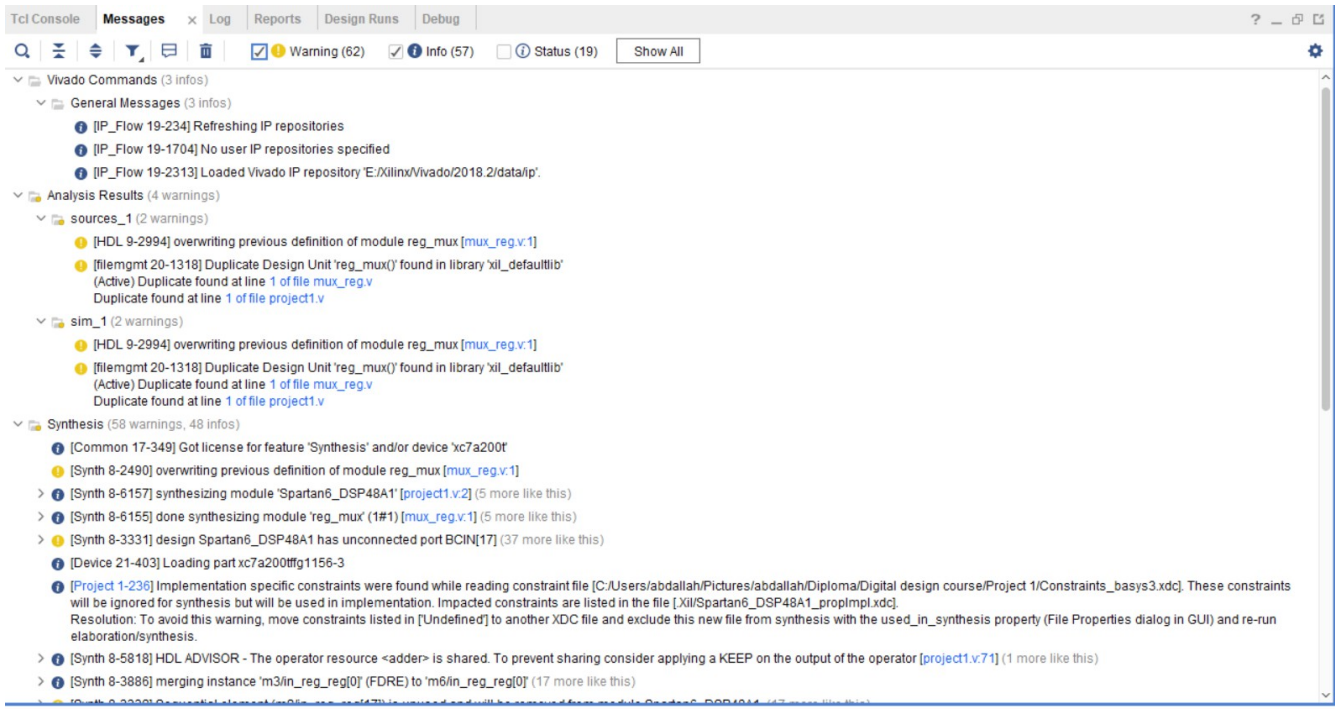




Snippets from schematic , message tab , utilization and timing report after synthesis :






Tcl Console
Messages
Log
Reports
Design Runs
Debug
Warning (62)
Info (57)
Status (19)
Show All
Vivado Commands (3 infos)
General Messages (3 infos)
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'E:/Xilinx/Vivado/2018.2/data/ip'.
Analysis Results (4 warnings)
sources_1 (2 warnings)
[HDL 9-2994] overwriting previous definition of module reg_mux [mux_reg.v:1]
[filemgmt 20-1318] Duplicate Design Unit 'reg_mux()' found in library 'xil_defaultlib'
(Active) Duplicate found at line 1 of file mux_reg.v
Duplicate found at line 1 of file project1.v
sim_1 (2 warnings)
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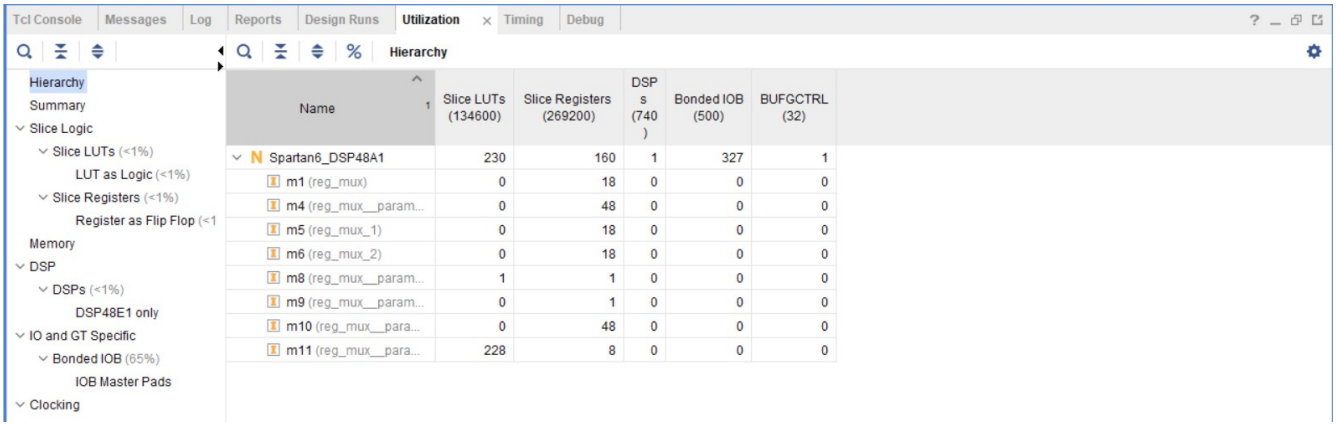
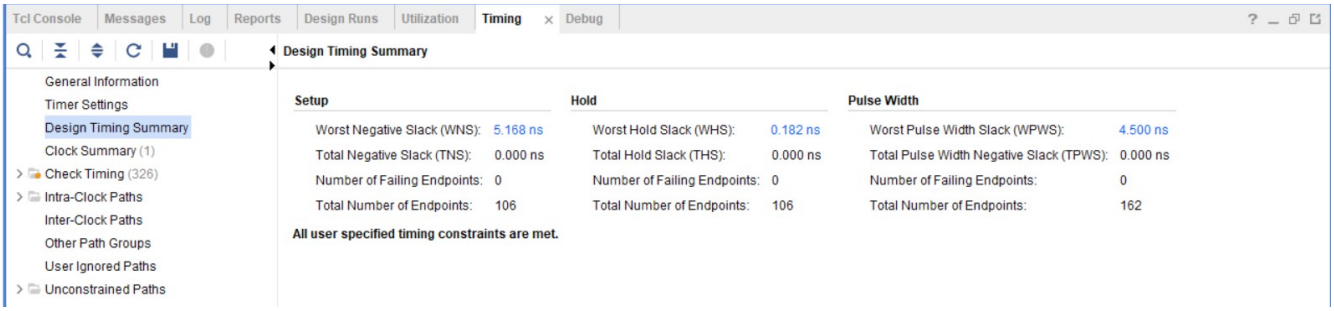
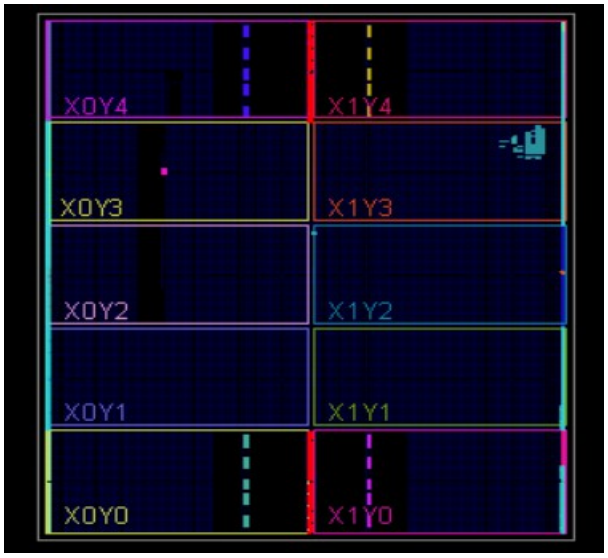
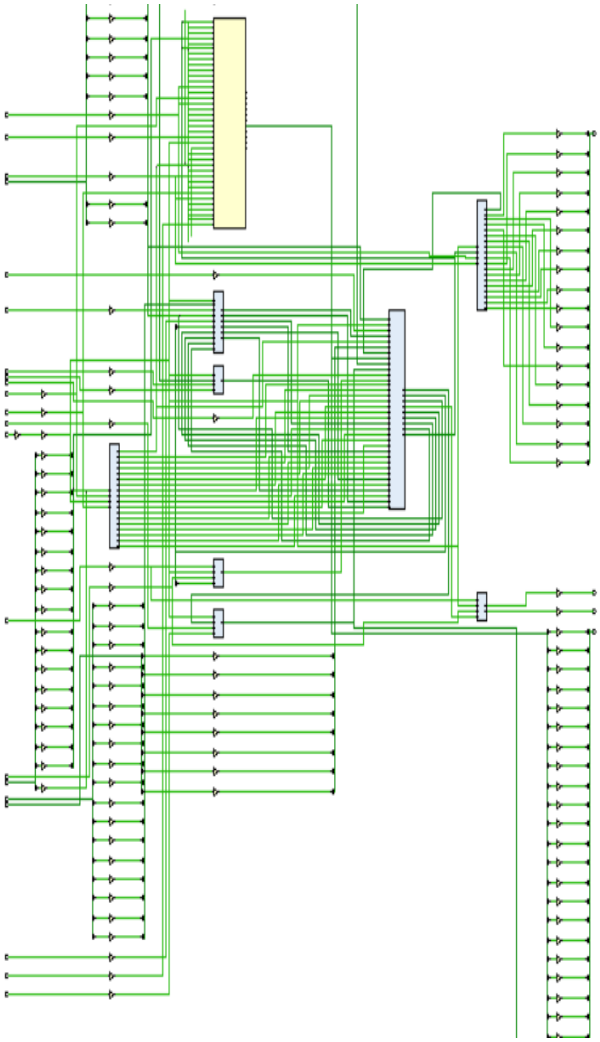
[filemgmt 20-1318] Duplicate Design Unit 'reg_mux()' found in library 'xil_defaultlib'
(Active) Duplicate found at line 1 of file mux_reg.v
Duplicate found at line 1 of file project1.v
Synthesis (58 warnings, 48 infos)
[Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a200t'
[Synth 8-2490] overwriting previous definition of module reg_mux [mux_reg.v:1]
[Synth 8-6157] synthesizing module 'Spartan6_DSP48A1' [project1.v:2] (5 more like this)
[Synth 8-6155] done synthesizing module 'reg_mux' (1#1) [mux_reg.v:1] (5 more like this)
[Synth 8-3331] design Spartan6_DSP48A1 has unconnected port BCIN[17] (37 more like this)
[Device 21-403] Loading part xc7a200tffg1156-3
[Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/abdallah/Pictures/abdallah/Diploma/Digital design course/Project 1/Constraints_basys3.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Spartan6_DSP48A1_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in ['Undefined'] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
[Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [project1.v:71] (1 more like this)
[Synth 8-3886] merging instance 'm3/in_reg_reg[0]' (FDRE) to 'm6/in_reg_reg[0]' (17 more like this)

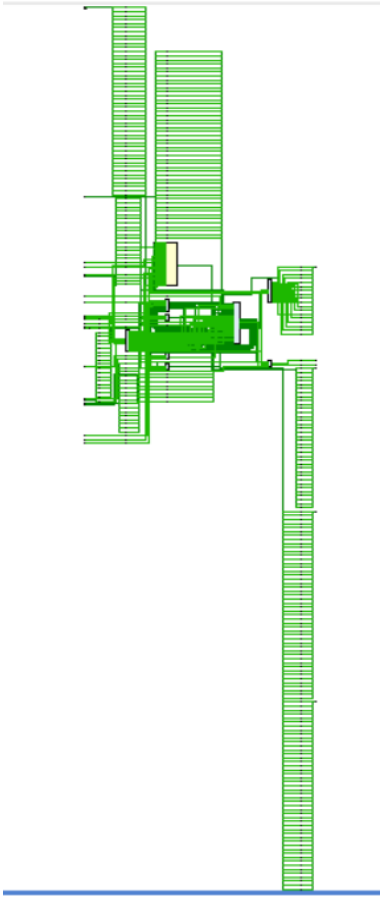

Tcl Console
Messages
Log
Reports
Design Runs
Utilization
Timing
Debug
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop (<1
Memory
DSP
DSPs (<1%)
DSP48E1 only
IO and GT Specific
Bonded IOB (65%)
IOB Master Pads
Clocking
Name
Slice LUTs (134600)
Slice Registers (269200)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
Spartan6_DSP48A1 230 160 1 327 1
m1 (reg_mux) 0 18 0 0 0
m4 (reg_mux__param... 0 48 0 0 0
m5 (reg_mux_1) 0 18 0 0 0
m6 (reg_mux_2) 0 18 0 0 0
m8 (reg_mux__param... 1 1 0 0 0
m9 (reg_mux__param... 0 1 0 0 0
m10 (reg_mux__para... 0 48 0 0 0
m11 (reg_mux__para... 228 8 0 0 0

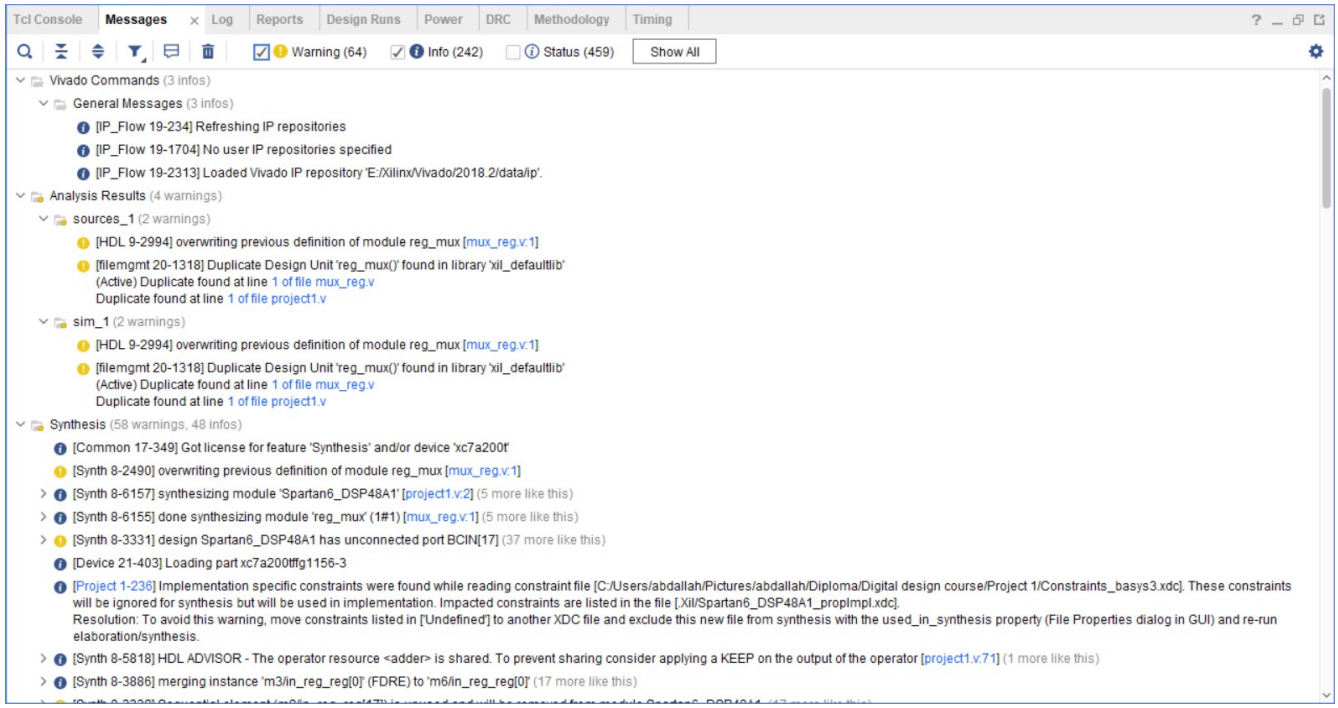

Tcl Console
Messages
Log
Reports
Design Runs
Utilization
Timing
Debug
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Setup
Worst Negative Slack (WNS): 5.168 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 106
Hold
Worst Hold Slack (WHS): 0.182 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 106
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 162
All user specified timing constraints are met.

Snippets from schematic , message tab , utilization and timing report after implementation :








Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Warning (64)
Info (242)
Status (459)
Show All
Vivado Commands (3 infos)
General Messages (3 infos)
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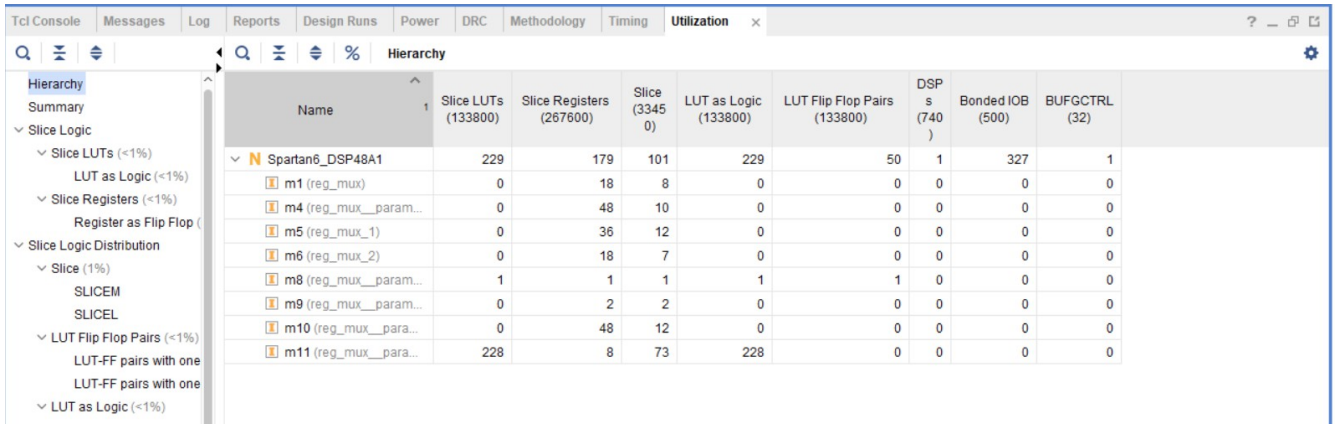
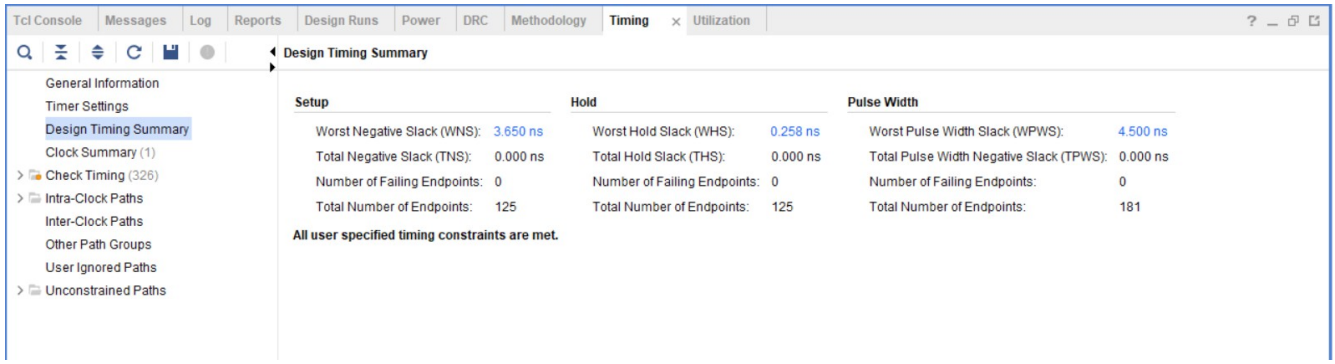

Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Utilization
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop (
Slice Logic Distribution
Slice (1%)
SLICEM
SLICEL
LUT Flip Flop Pairs (<1%)
LUT-FF pairs with one
LUT-FF pairs with one
LUT as Logic (<1%)
Name
Slice LUTs (133800)
Slice Registers (267600)
Slice (33450)
LUT as Logic (133800)
LUT Flip Flop Pairs (133800)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
Spartan6_DSP48A1 229 179 101 229 50 1 327 1
m1 (reg_mux) 0 18 8 0 0 0 0 0
m4 (reg_mux__param... 0 48 10 0 0 0 0 0
m5 (reg_mux_1) 0 36 12 0 0 0 0 0
m6 (reg_mux_2) 0 18 7 0 0 0 0 0
m8 (reg_mux__param... 1 1 1 1 1 0 0 0
m9 (reg_mux__param... 0 2 2 0 0 0 0 0
m10 (reg_mux__para... 0 48 12 0 0 0 0 0
m11 (reg_mux__para... 228 8 73 228 0 0 0 0


Tcl Console
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Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (326)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths
Setup
Worst Negative Slack (WNS): 3.650 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 125
Hold
Worst Hold Slack (WHS): 0.258 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 125
Pulse Width
Worst Pulse Width Slack (WPWS): 4.500 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 181
All user specified timing constraints are met.