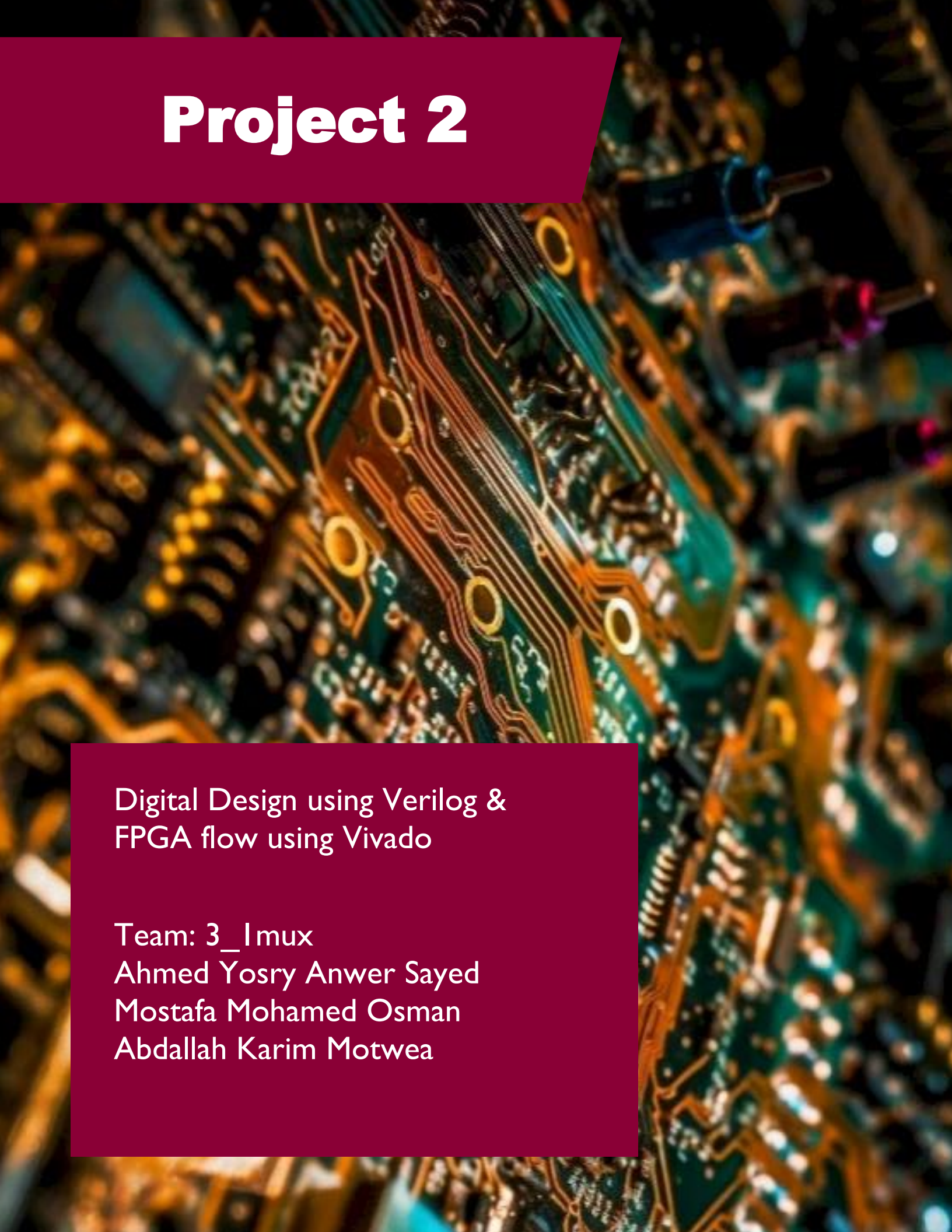
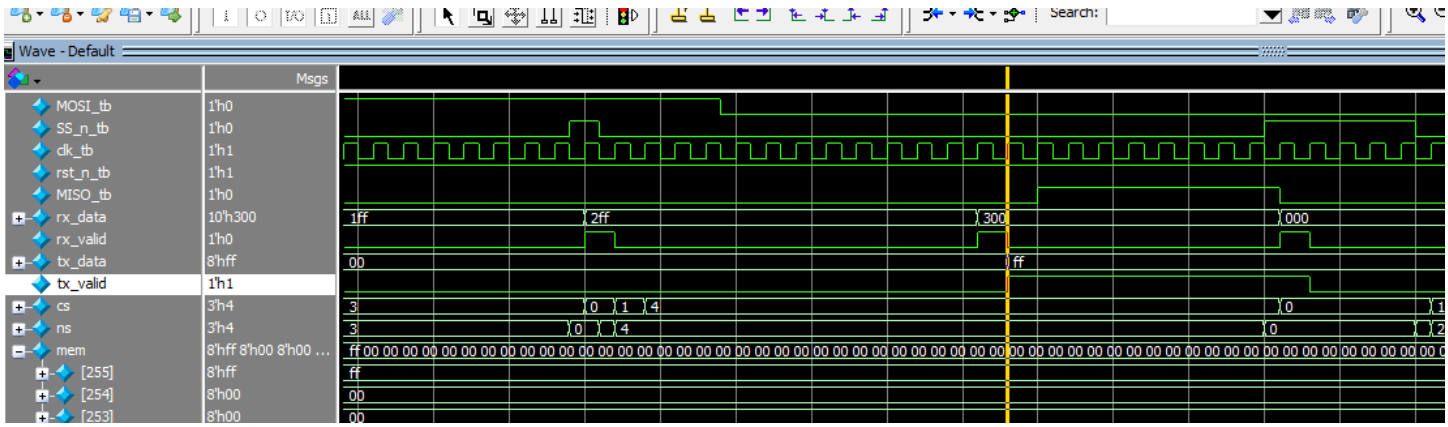


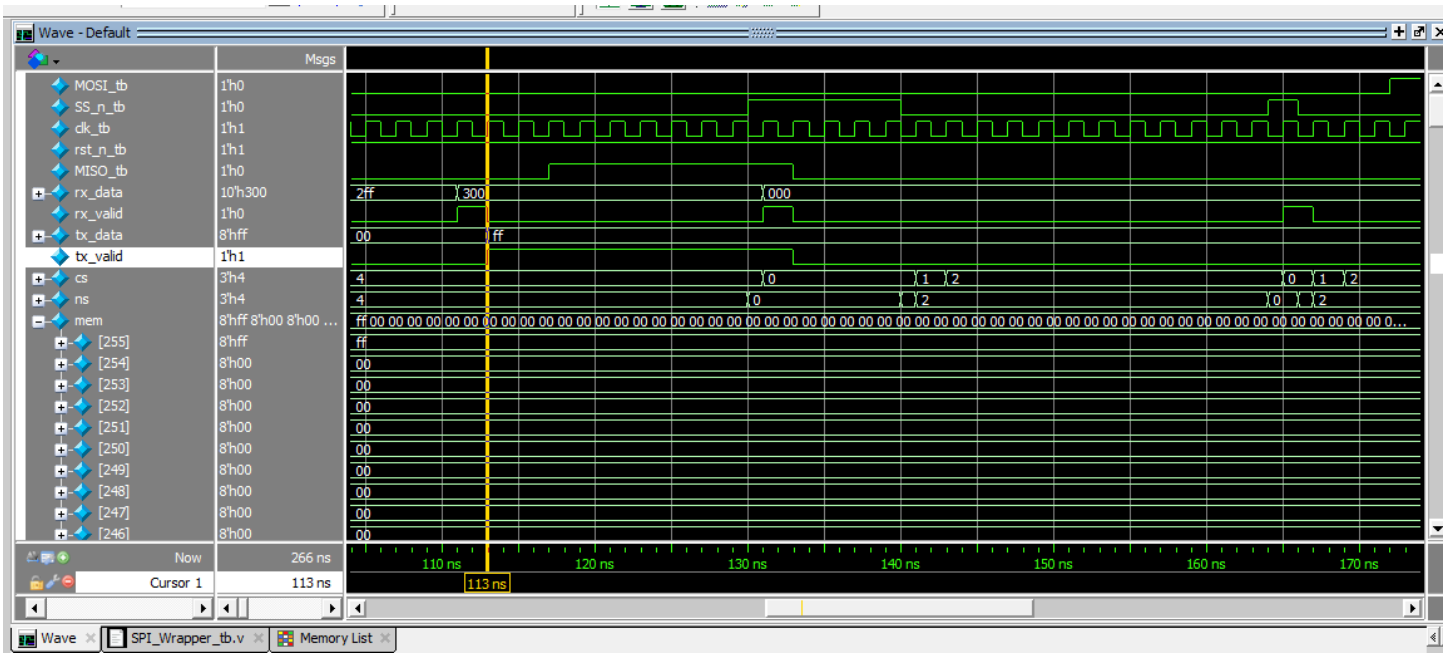
Project 2

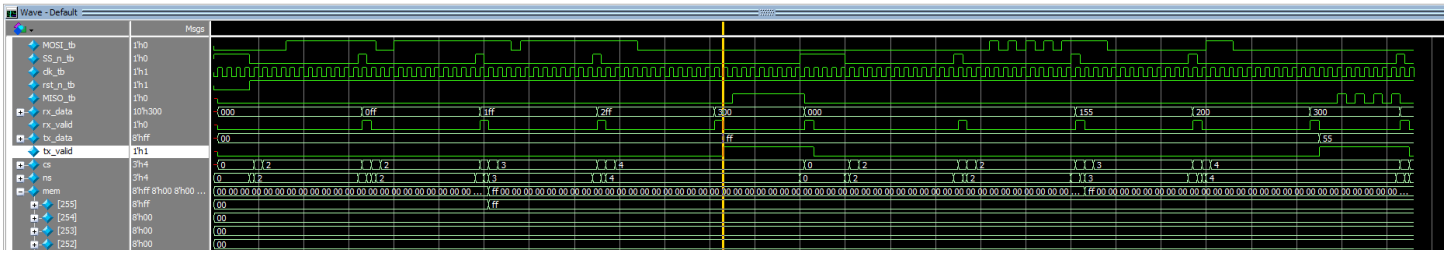
Digital Design using Verilog &
FPGA flow using Vivado

Team: 3_1mux
Ahmed Yosry Anwer Sayed
Mostafa Mohamed Osman
Abdallah Karim Motwea

1. Snippets from the waveforms captured from Questa Sim:



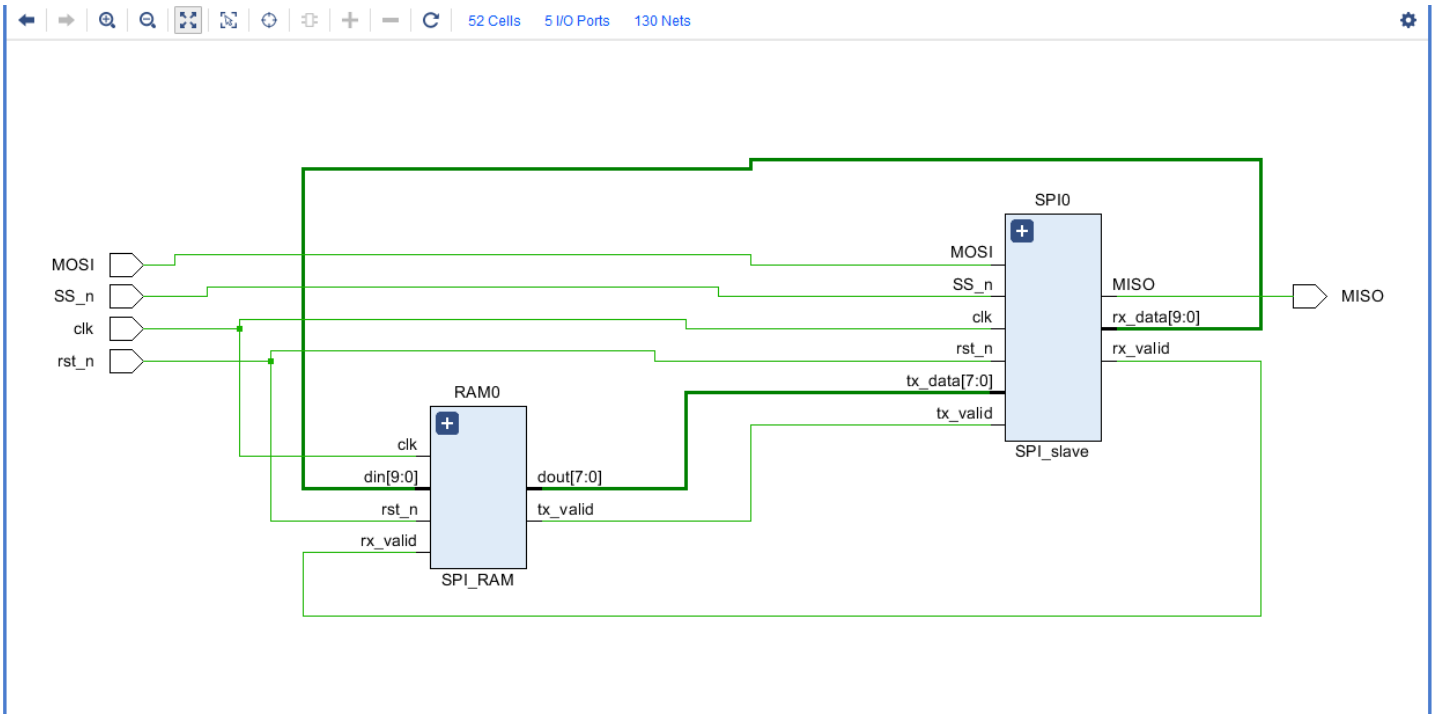


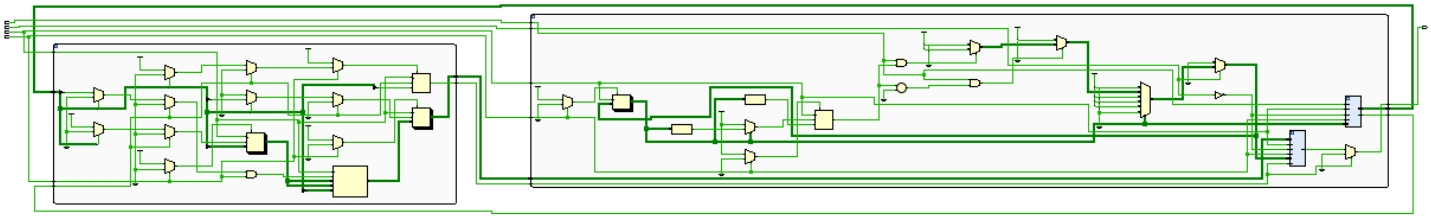


2. Synthesis and elaboration snippets for each encoding:

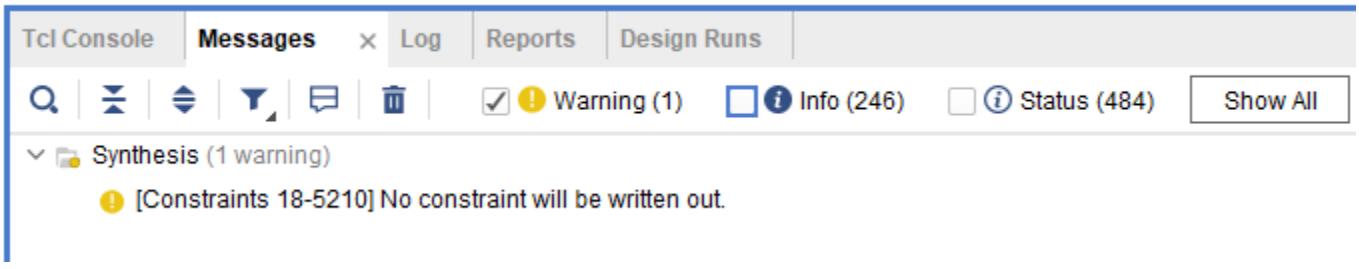
Gray:

Schematic after elaboration:

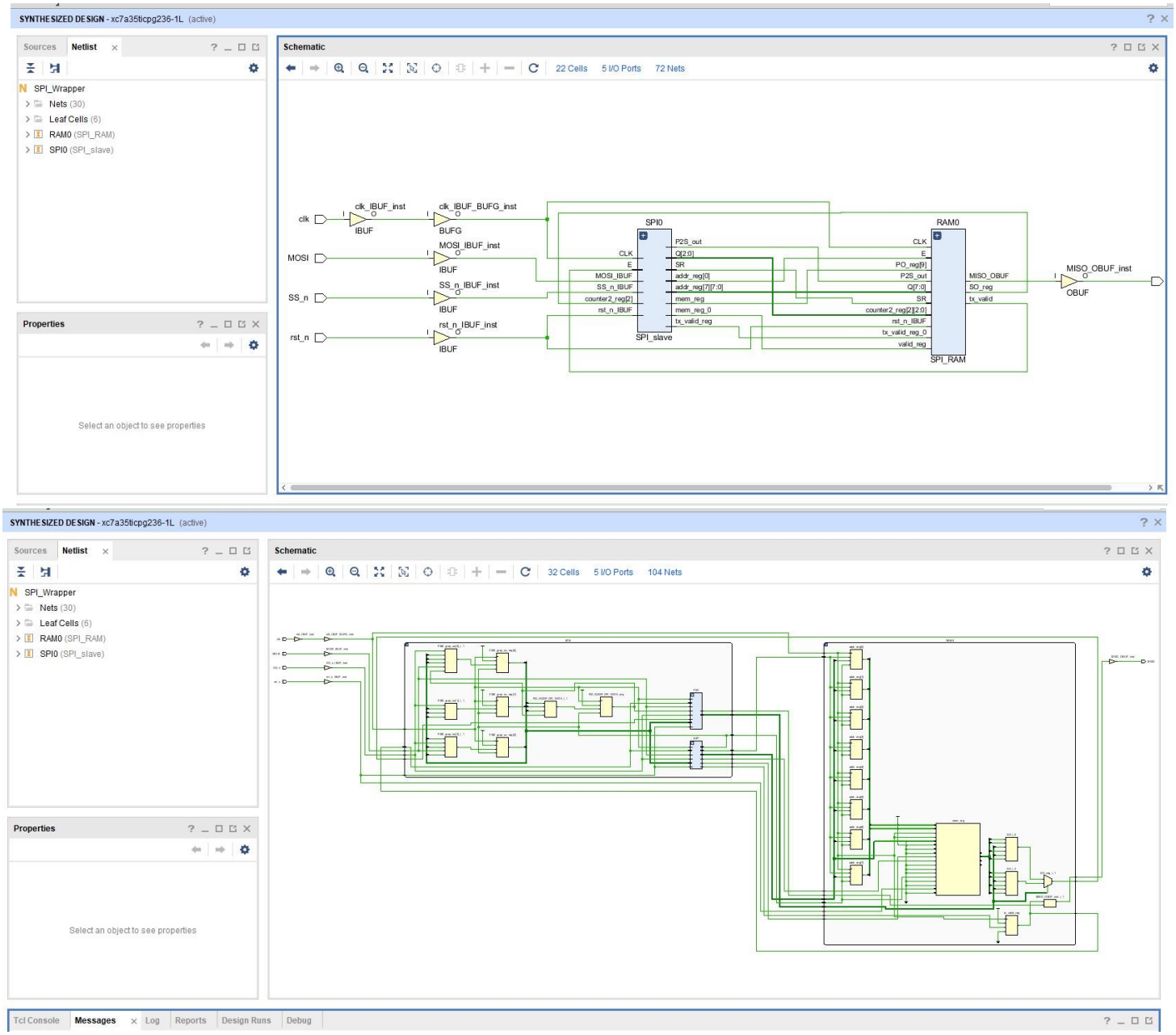




Message tab after elaboration:



Schematic after synthesis:



Message tab after synthesis:

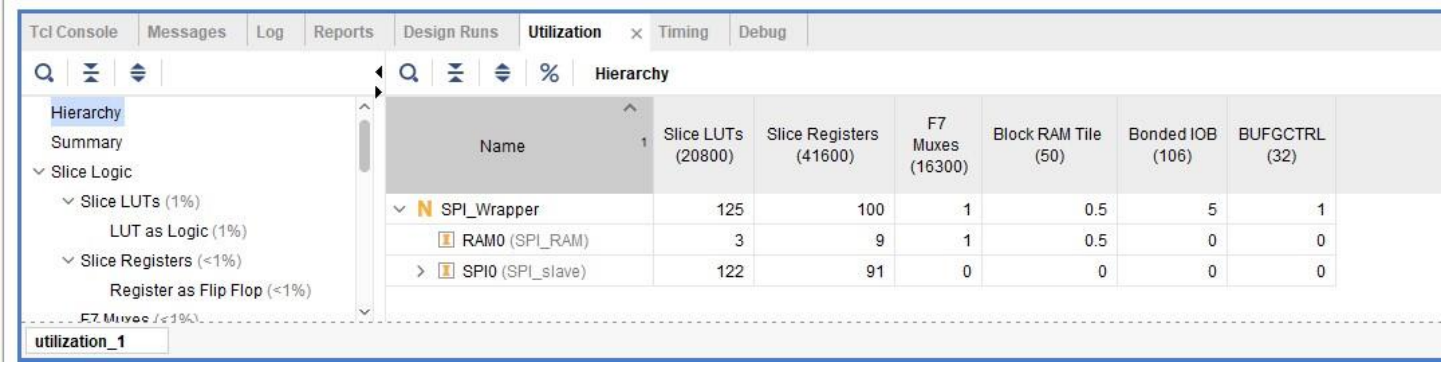
The report showing encoding used:

Schematic | synth_1_synth_synthesis_report_0 - synth_1

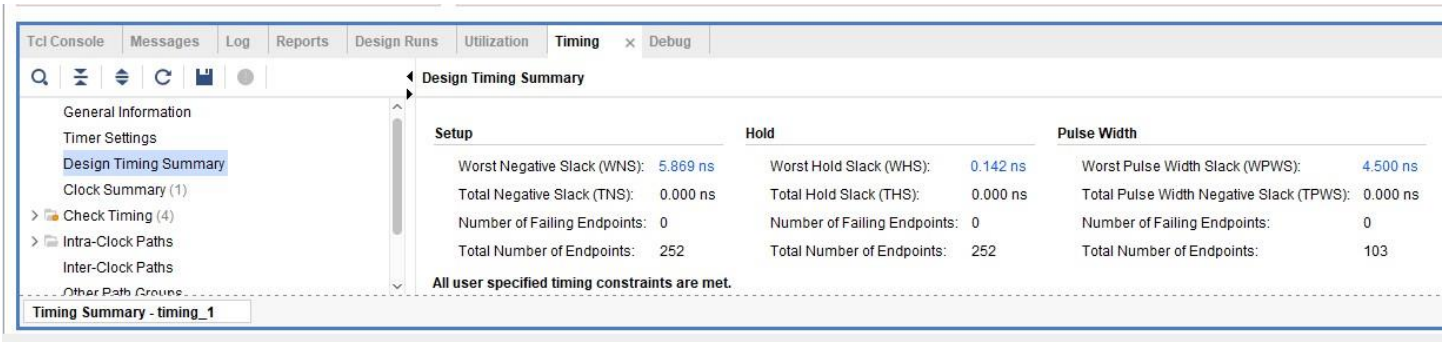
D:/Yosry/Studies/Digital IC/Design/Assignments/SPI Slave Interface/SPI 3ala nadafa/SPI_3ala_nadafa/SPI_3ala_nadafa.runs/synth_1/SPI_Wrapper.vds

```
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:38 ; elapsed = 00:00:39 . Memory (MB): peak = 759.559 ; gain
---------------------------------------------------------------------------
INFO: [Synth 8-5545] ROM "ten_flag" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter2" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
INFO: [Synth 8-5544] ROM "RD_ADDR_OR_DATA" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
-----------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
-----------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                              000
                 CHK_CMD |                              001 |                              001
                READ_ADD |                              011 |                              011
               READ_DATA |                              010 |                              100
                   WRITE |                              111 |                              010
-----------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_slave'
---------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:38 ; elapsed = 00:00:40 . Memory (MB): peak = 759.559 ; gain = 502.320
---------------------------------------------------------------------------
```

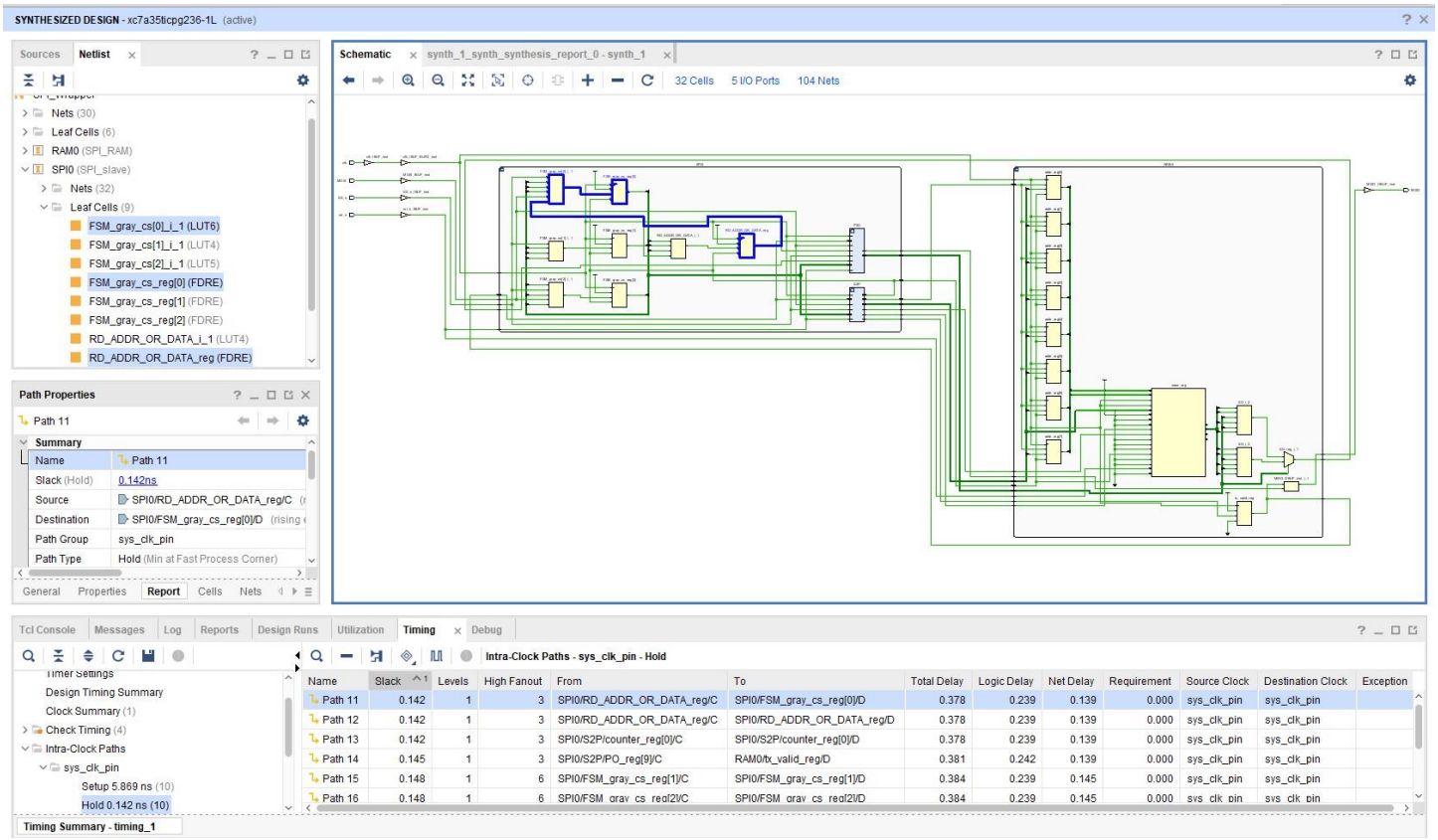
Utilization report:



Timing report:

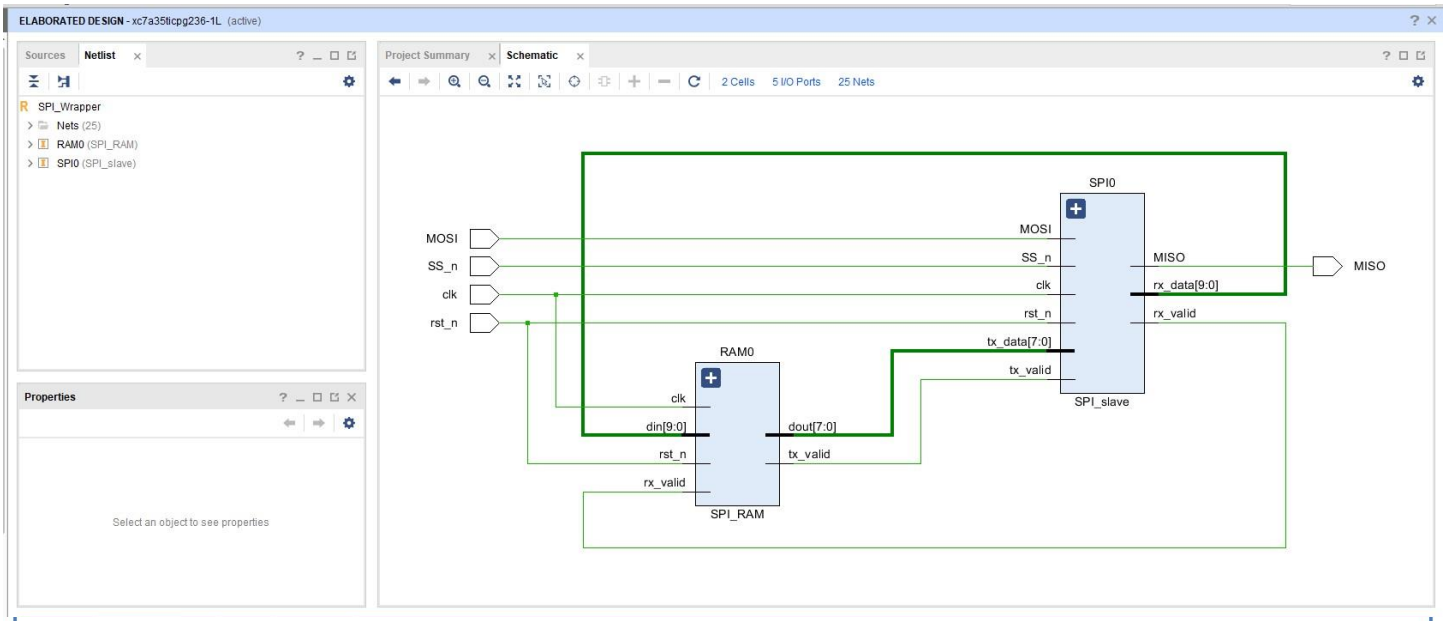


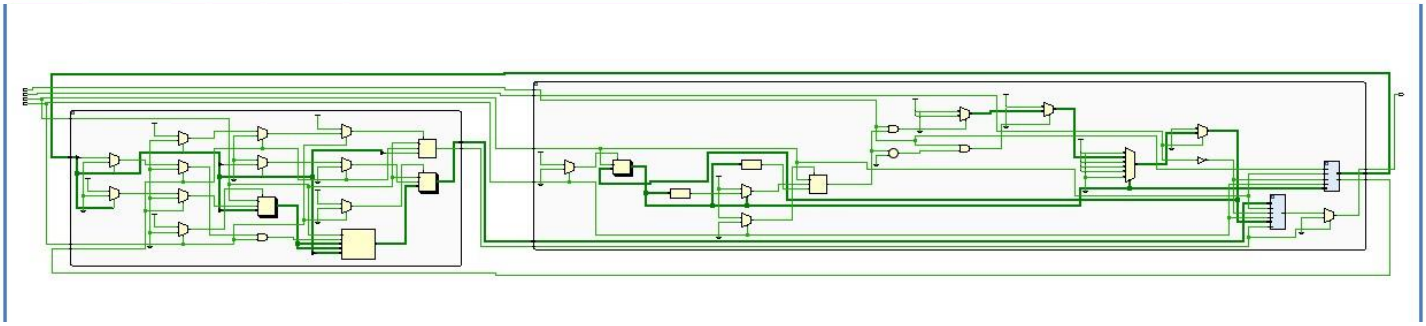
The critical path highlighted in the schematic:



B. One hot:

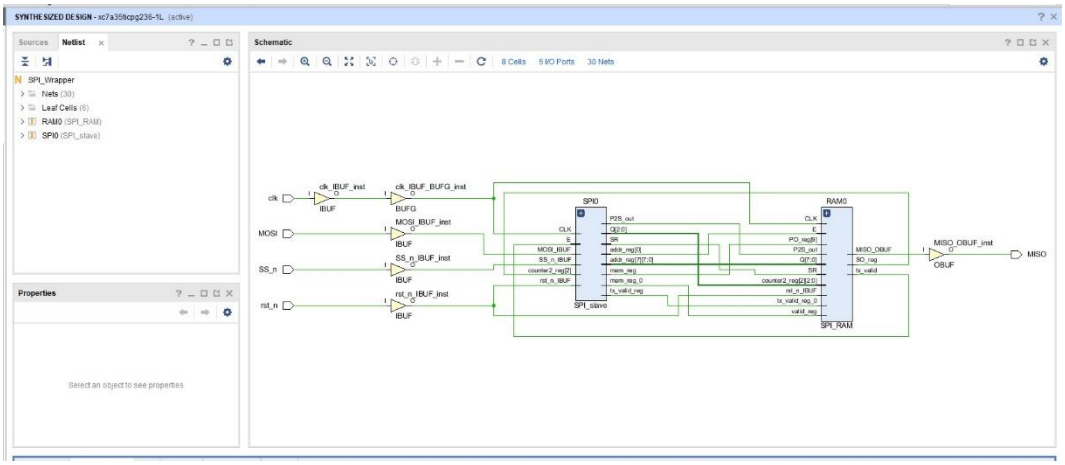
Schematic after elaboration:

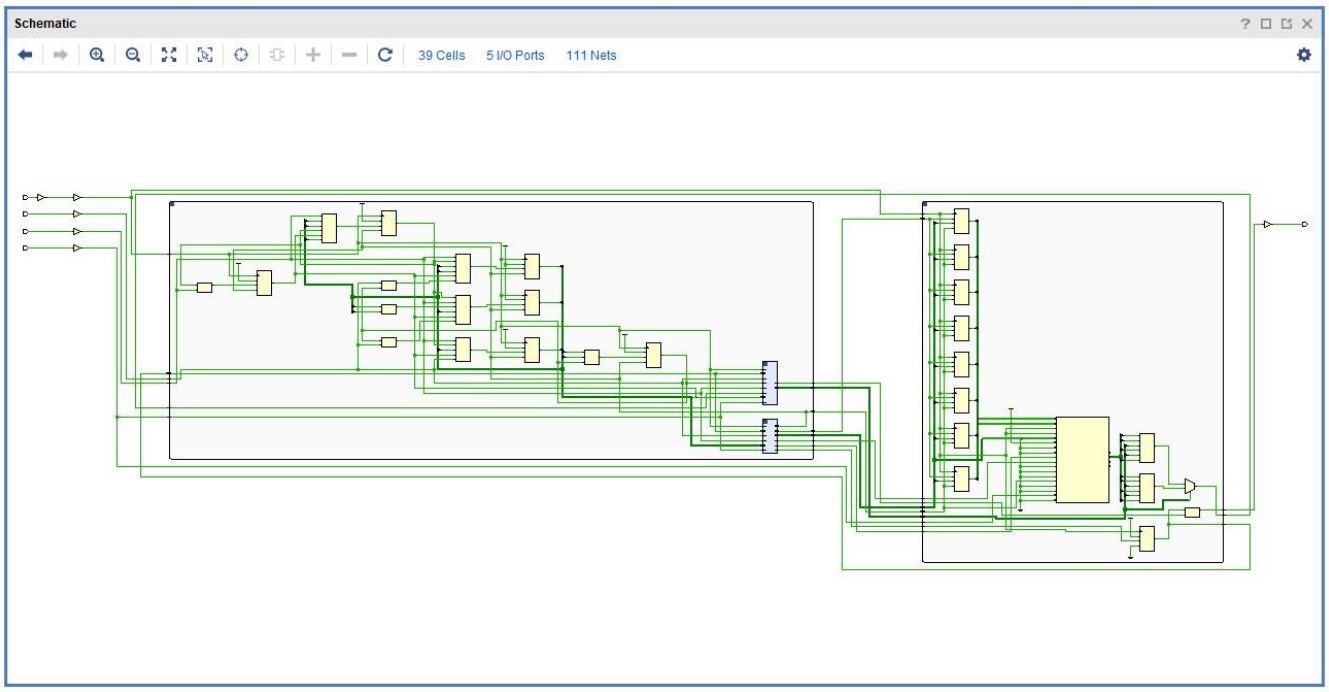




Message tab after elaboration:

Schematic after synthesis:





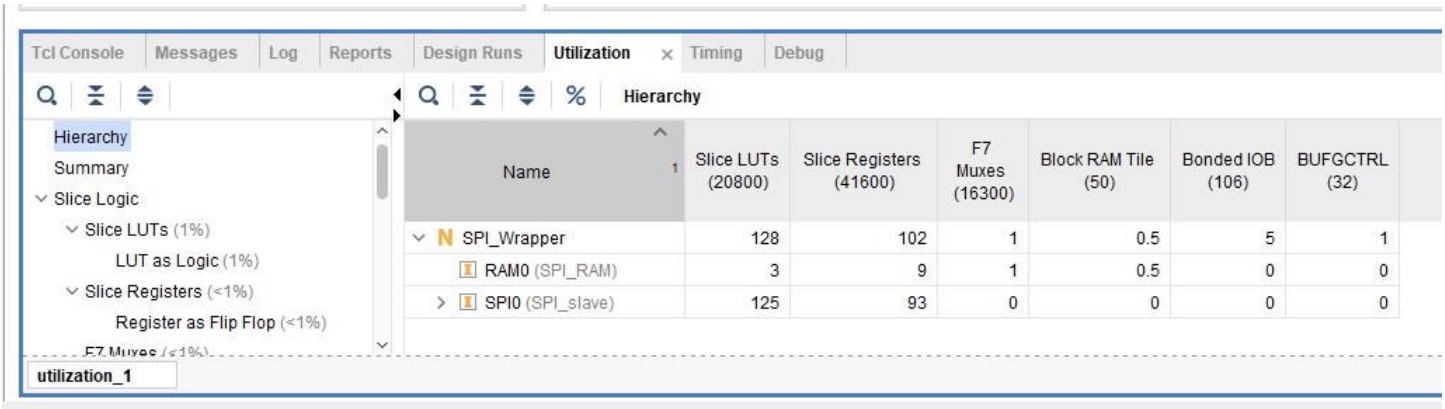
Message tab after synthesis:

The report showing encoding used:

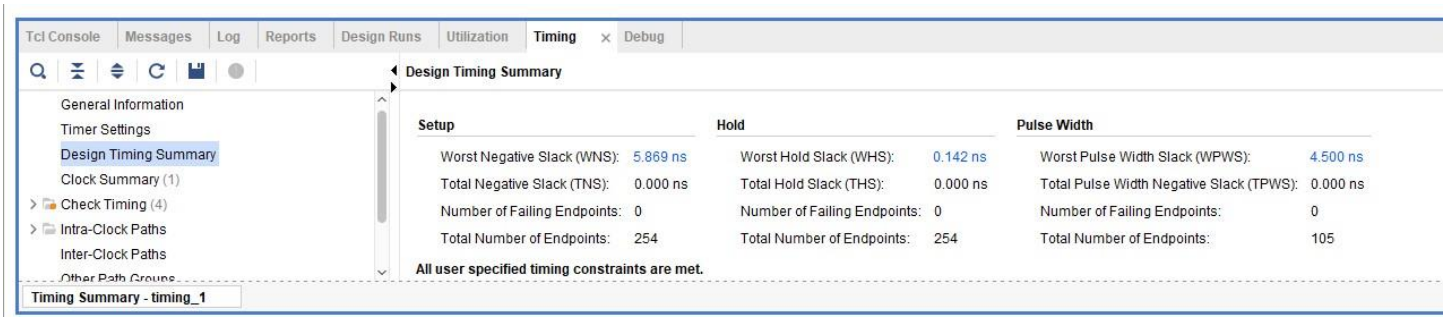
```
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:35 ; elapsed = 00:00:37 . Memory (MB): peak = 758.145 ; ga
---------------------------------------------------------------------------------
INFO: [Synth 8-5545] ROM "ten_flag" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "counter2" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI_slave'
INFO: [Synth 8-5544] ROM "RD_ADDR_OR_DATA" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                            00001 |                              000
                  CHK_CMD |                            00010 |                              001
                 READ_ADD |                            00100 |                              011
                READ_DATA |                            01000 |                              100
                   WRITE |                            10000 |                              010
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_slave'
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:36 ; elapsed = 00:00:37 . Memory (MB): peak = 758.145 ; gain = 500.617
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
```

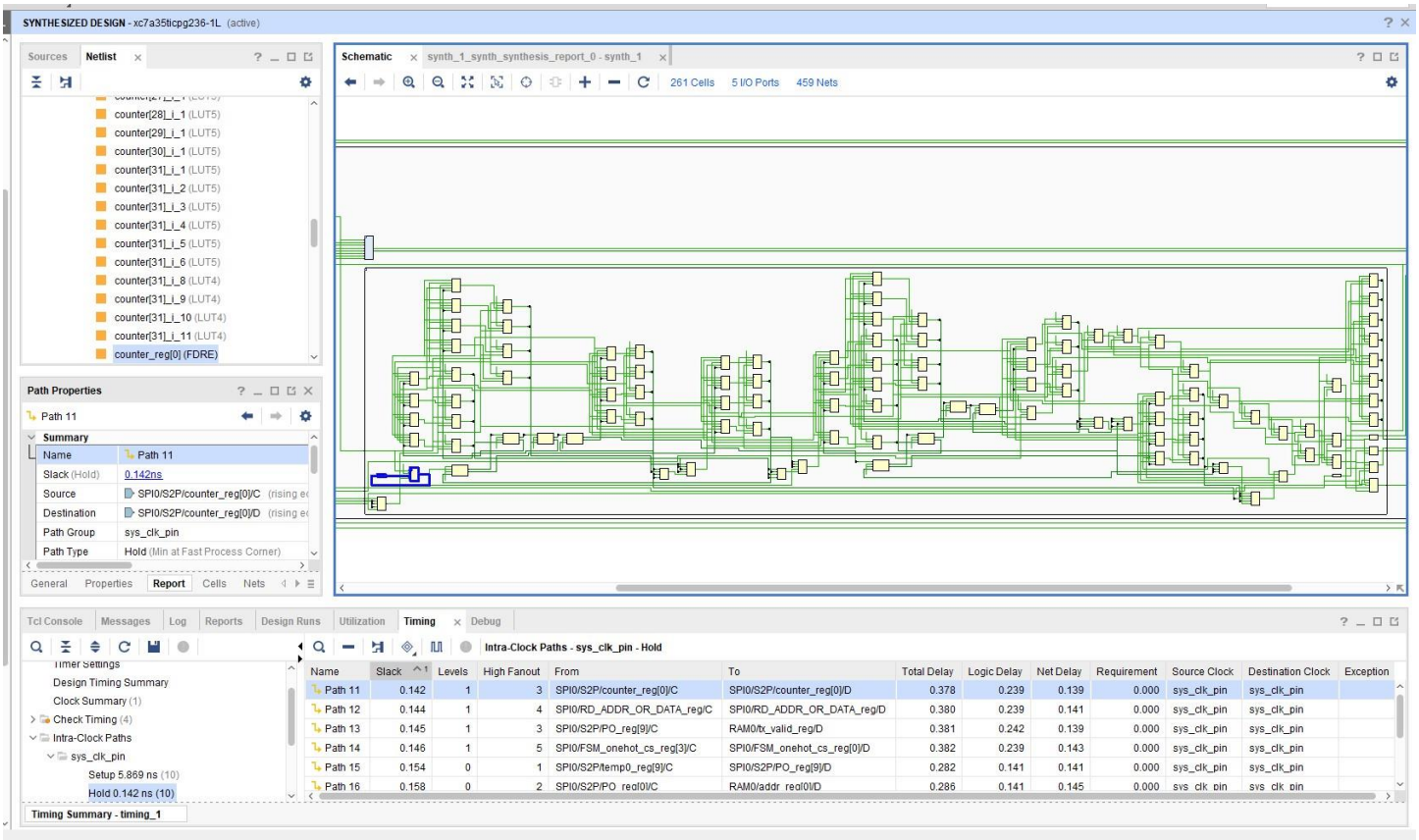
Utilization report:



Timing report:

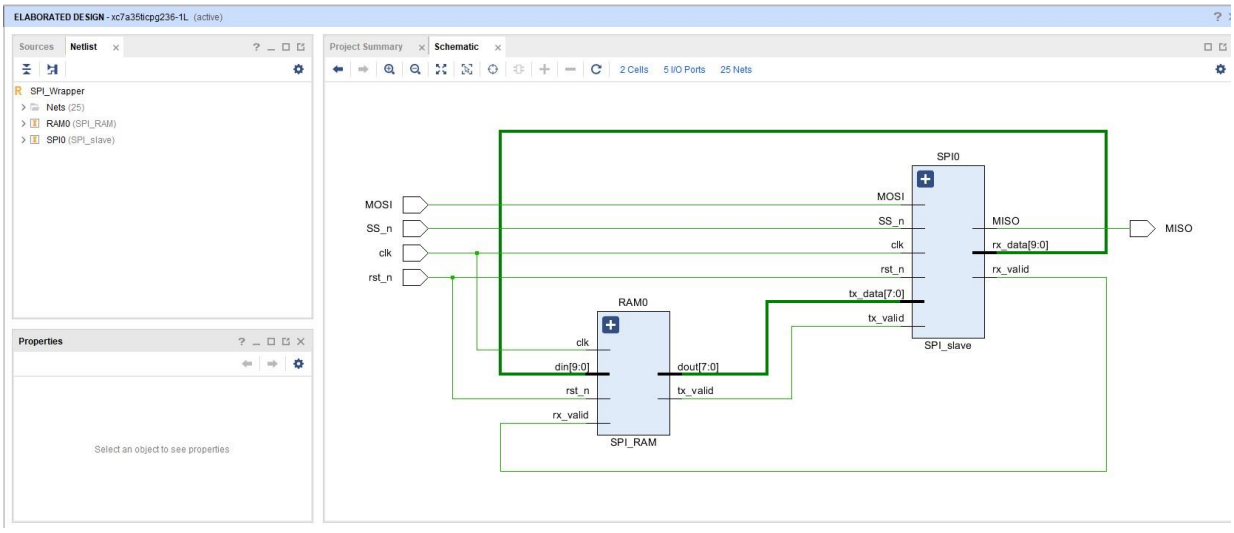


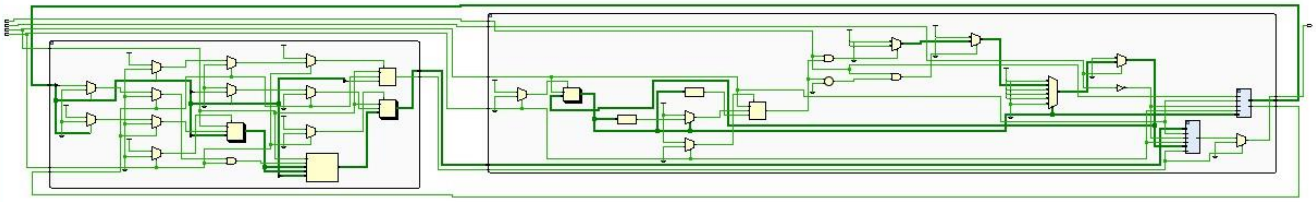
The critical path highlighted in the schematic:



C. Sequential:

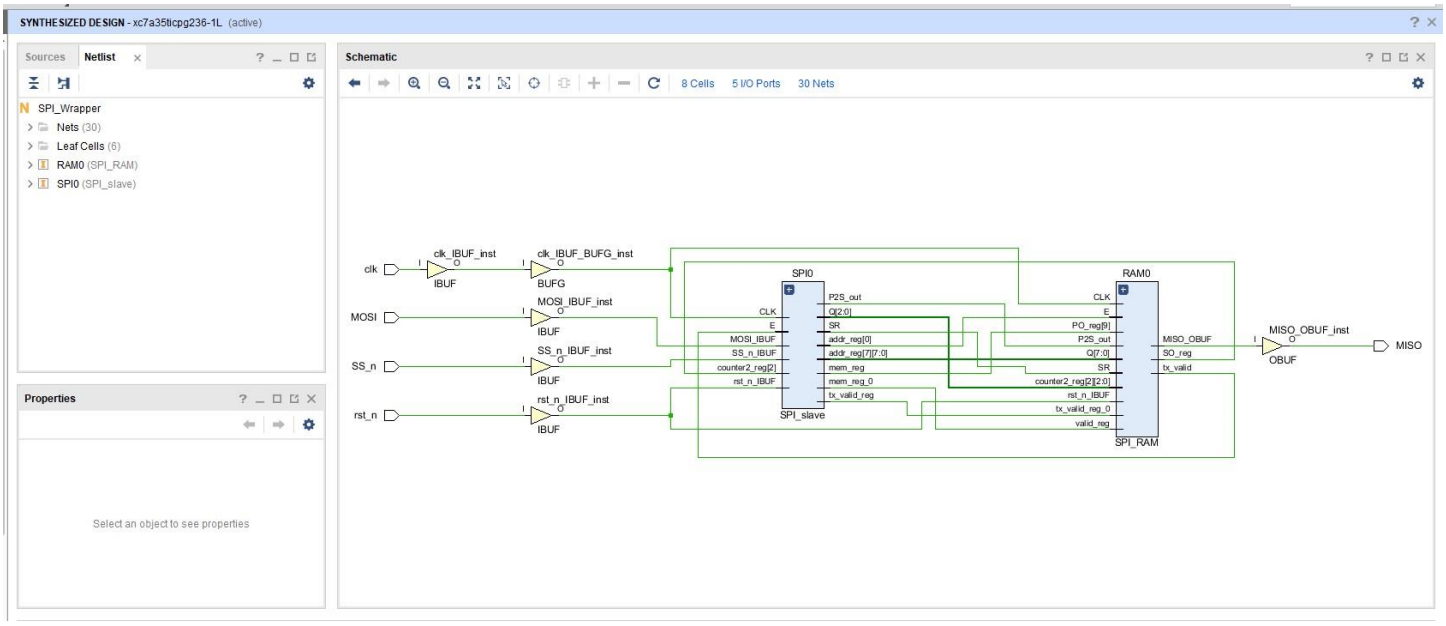
Schematic after elaboration:

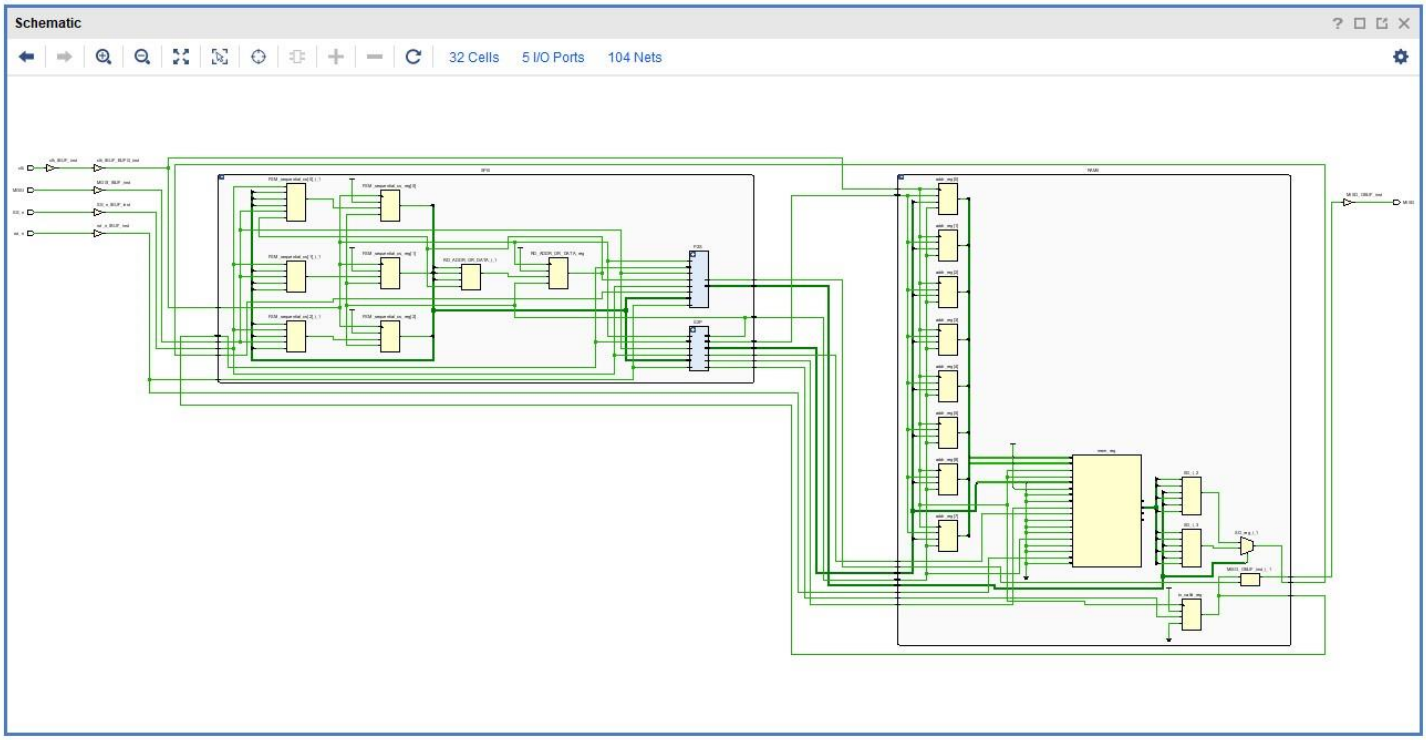




Message tab after elaboration:

Schematic after synthesis:



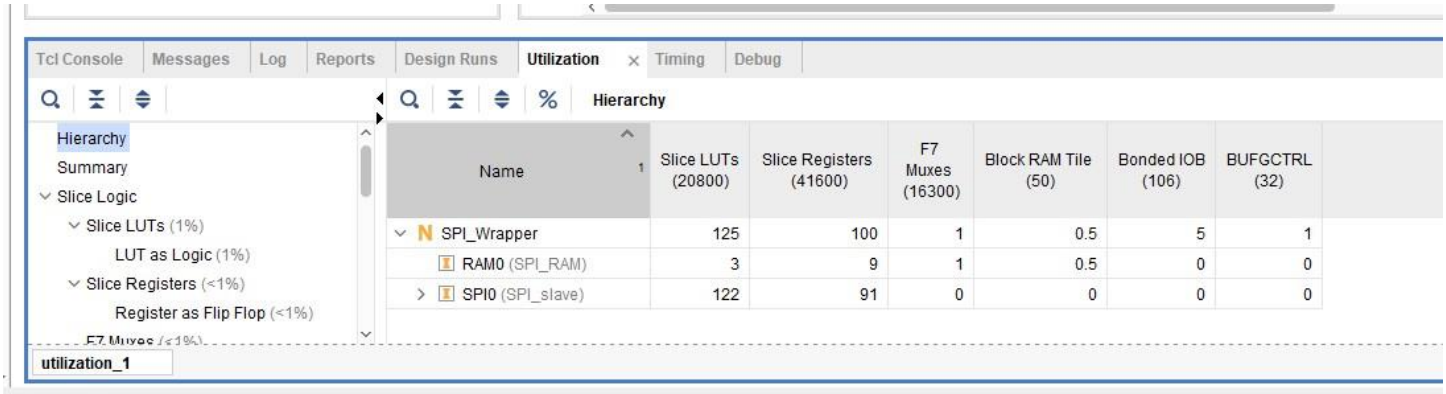


Message tab after synthesis:

The report showing encoding used:

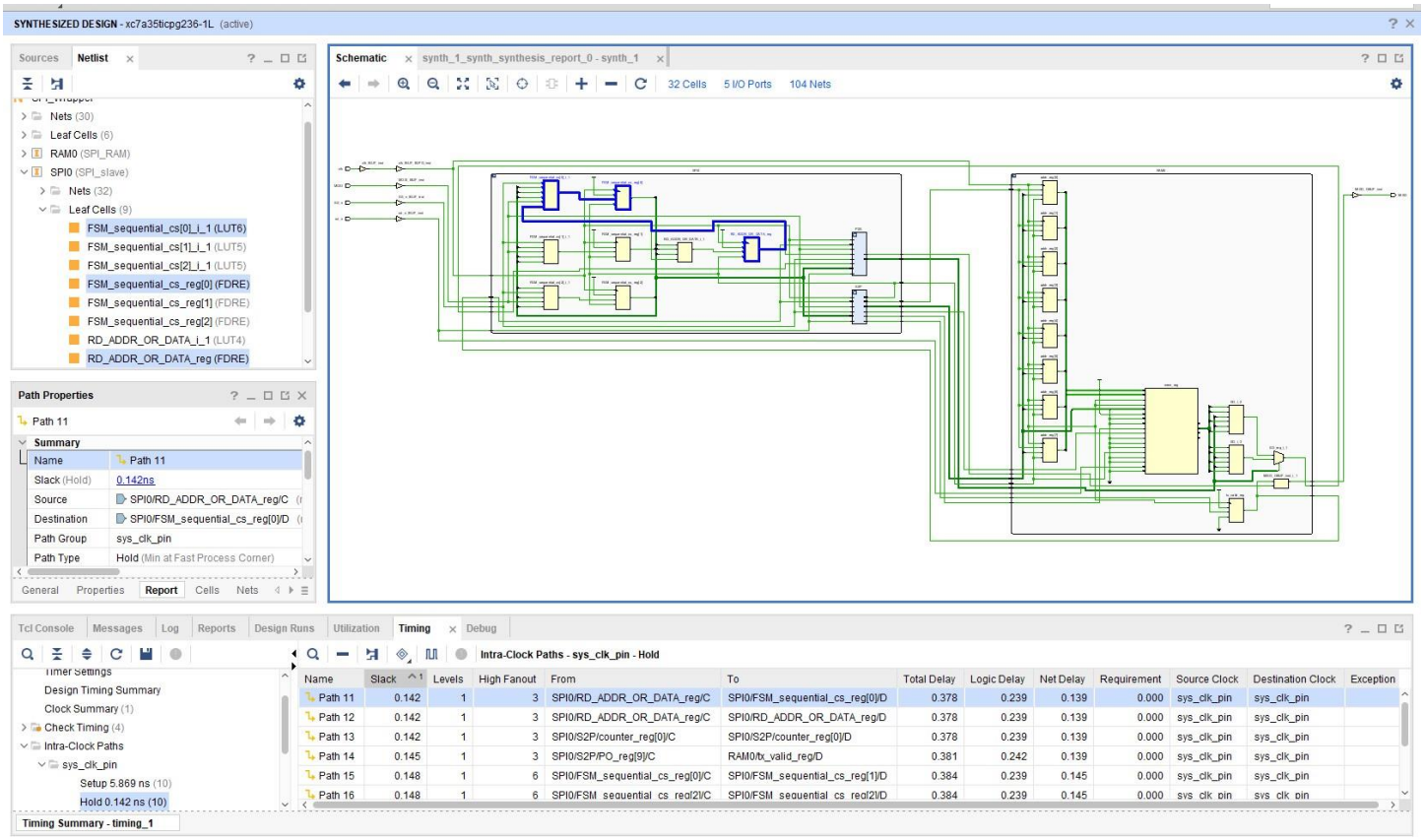
```
INFO: [Synth 8-5544] ROM "RD_ADDR_OR_DATA" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
---------------------------------------------------------------------------------------------------
                   State |                     New Encoding |               Previous Encoding
---------------------------------------------------------------------------------------------------
                    IDLE |                              000 |                              000
                 CHK_CMD |                              001 |                              001
                READ_ADD |                              010 |                              011
               READ_DATA |                              011 |                              100
                   WRITE |                              100 |                              010
---------------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_slave'
---------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:39 ; elapsed = 00:00:42 . Memory (MB): peak = 759.789 ; gain = 503.004
---------------------------------------------------------------------------
```

Utilization report after synthesis:



Timing report after synthesis:

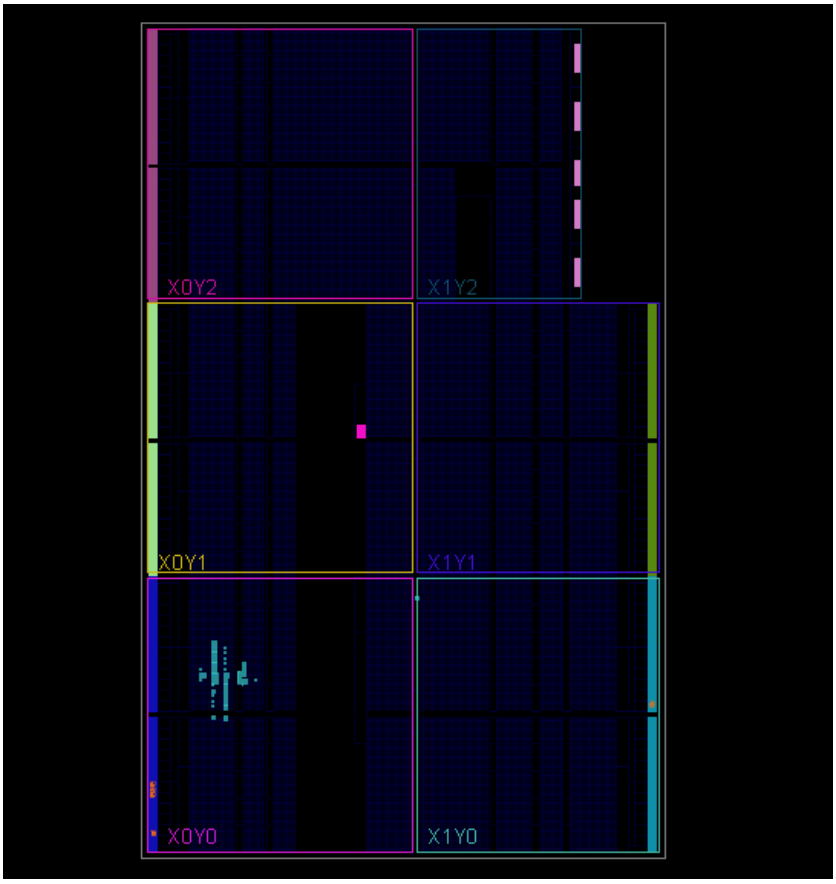
The critical path highlighted in the schematic:



3. Implementation snippets for each encoding:

A. Gray code:

FPGA device:



Utilization report after implementation:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (1%)
    - LUT as Logic (1%)
  - F7 Muxes (<1%)
  - Slice Registers (<1%)

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI_Wrapper	126	100	1	55	126	72	0.5	5	1
RAM0 (SPI_RAM)	4	9	1	4	4	0	0.5	0	0
SPI0 (SPI_slave)	122	91	0	54	122	70	0	0	0

utilization_1

Timing report after implementation:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (4)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

Design Timing Summary

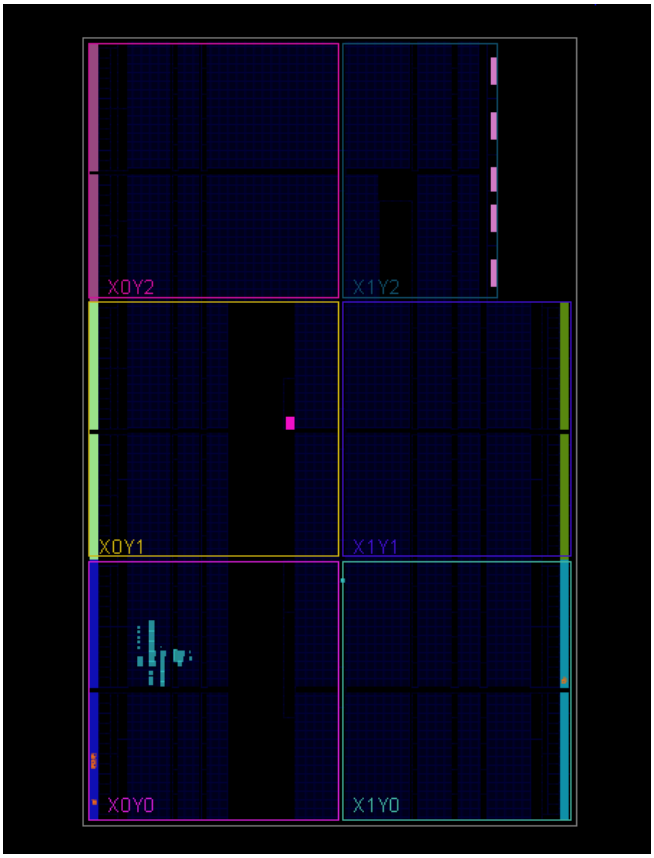
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.834 ns	Worst Hold Slack (WHS):	0.043 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	252	Total Number of Endpoints:	252	Total Number of Endpoints:	103

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

B. One hot:

FPGA device:



Utilization report after implementation:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (1%)
    - LUT as Logic (1%)
  - F7 Muxes (<1%)
  - Slice Registers (<1%)

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Wrapper	128	102	1	51	128	71	0.5	5	1
RAM0 (SPI_RAM)	4	9	1	5	4	0	0.5	0	0
SPI0 (SPI_slave)	124	93	0	50	124	70	0	0	0

utilization_1

Timing report after implementation:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (4)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

Design Timing Summary

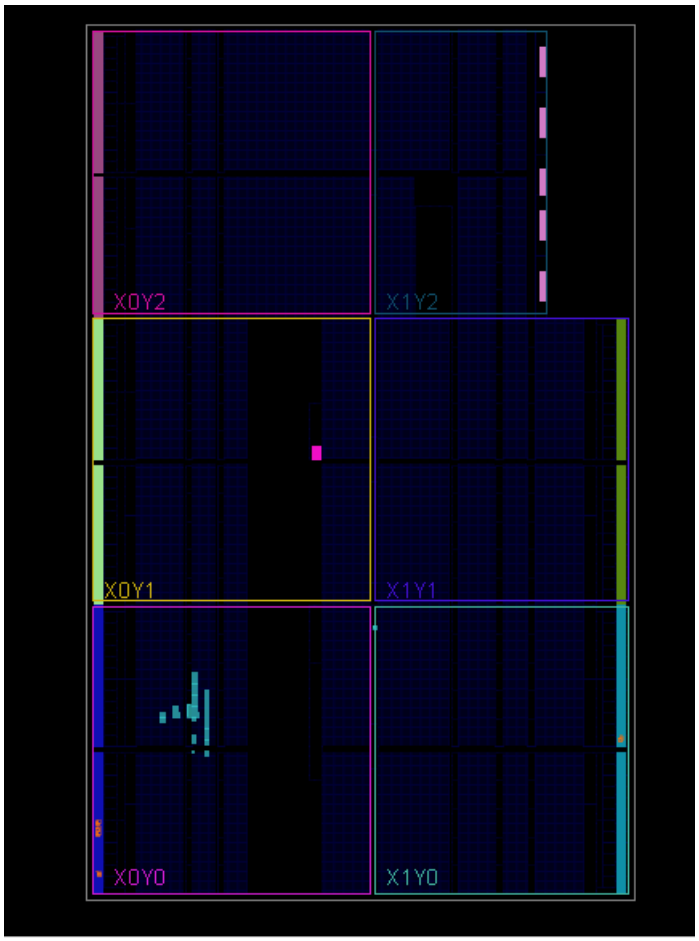
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.684 ns	Worst Hold Slack (WHS):	0.046 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	254	Total Number of Endpoints:	254	Total Number of Endpoints:	105

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

C. Sequential:

FPGA device:



Utilization report after implementation:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (1%)
    - LUT as Logic (1%)
  - F7 Muxes (<1%)
  - Slice Registers (<1%)

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Wrapper	126	100	1	47	126	70	0.5	5	1
RAM0 (SPI_RAM)	4	9	1	3	4	0	0.5	0	0
SPI0 (SPI_slave)	122	91	0	46	122	68	0	0	0

utilization_1

Timing report after implementation:

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing | Utilization

Design Timing Summary

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (4)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.652 ns	Worst Hold Slack (WHS):	0.170 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	252	Total Number of Endpoints:	252	Total Number of Endpoints:	103

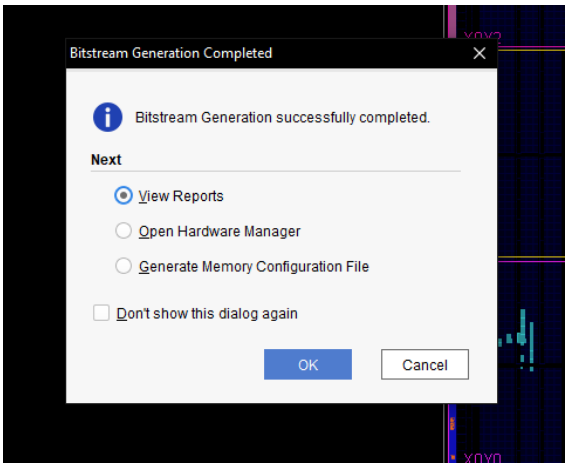
All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

4. Choosing the encoding based on the best timing report that gives the highest setup/hold slack after implementation to operate at the highest frequency possible:

Sequential gives the best timing report as it has the largest Worst Hold Slack.

5. Generation of bitstream file:



6. Exporting netlist: