



# **ANALOG IC DESIGN**

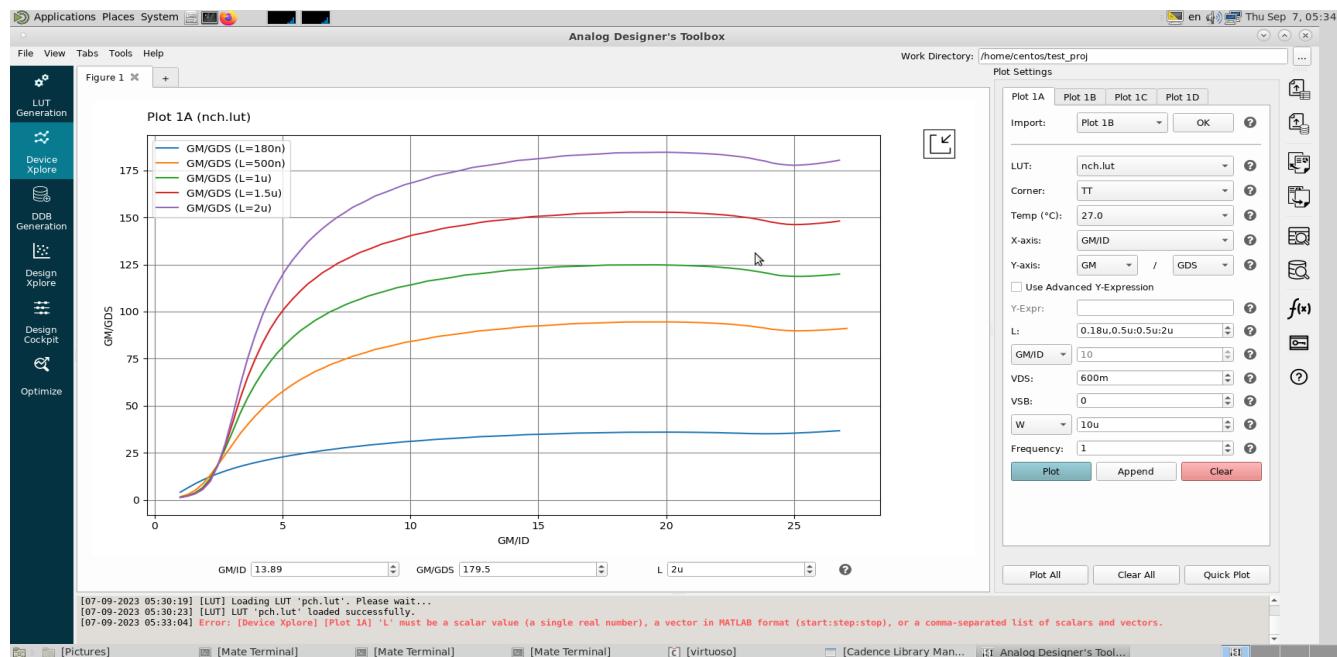
**LAB NO.11**

**(Mini project 2)**

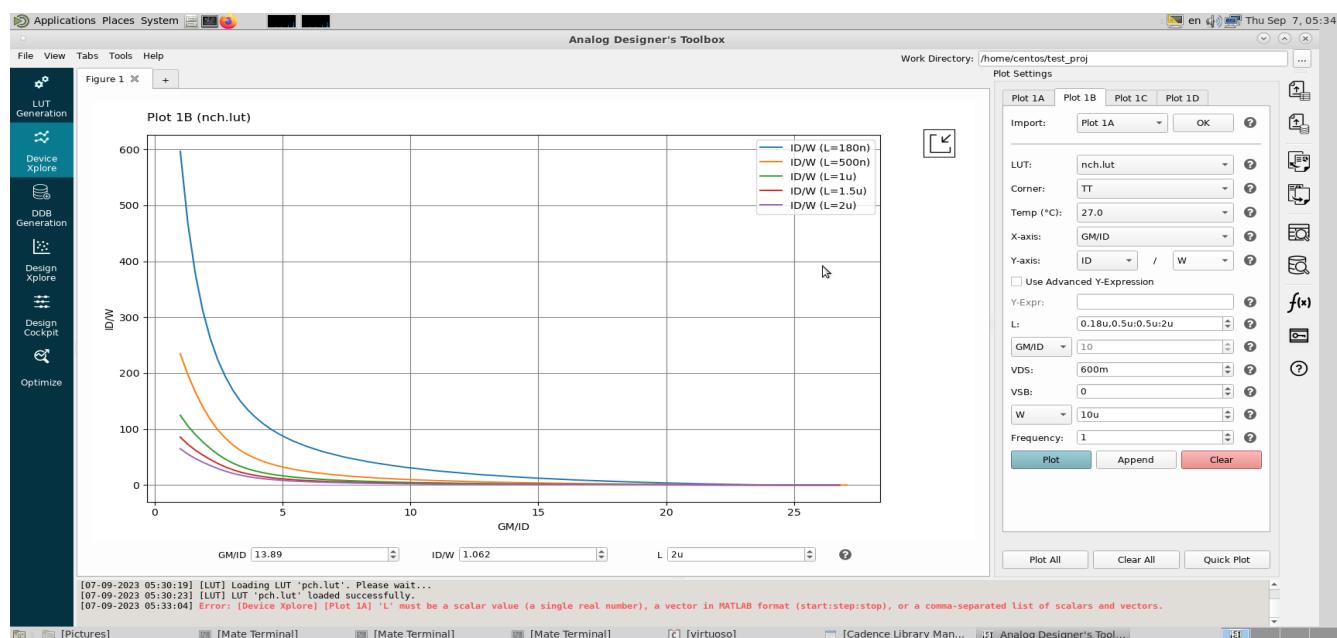
# Part 1( gm/id design charts):

## 1.NMOS:

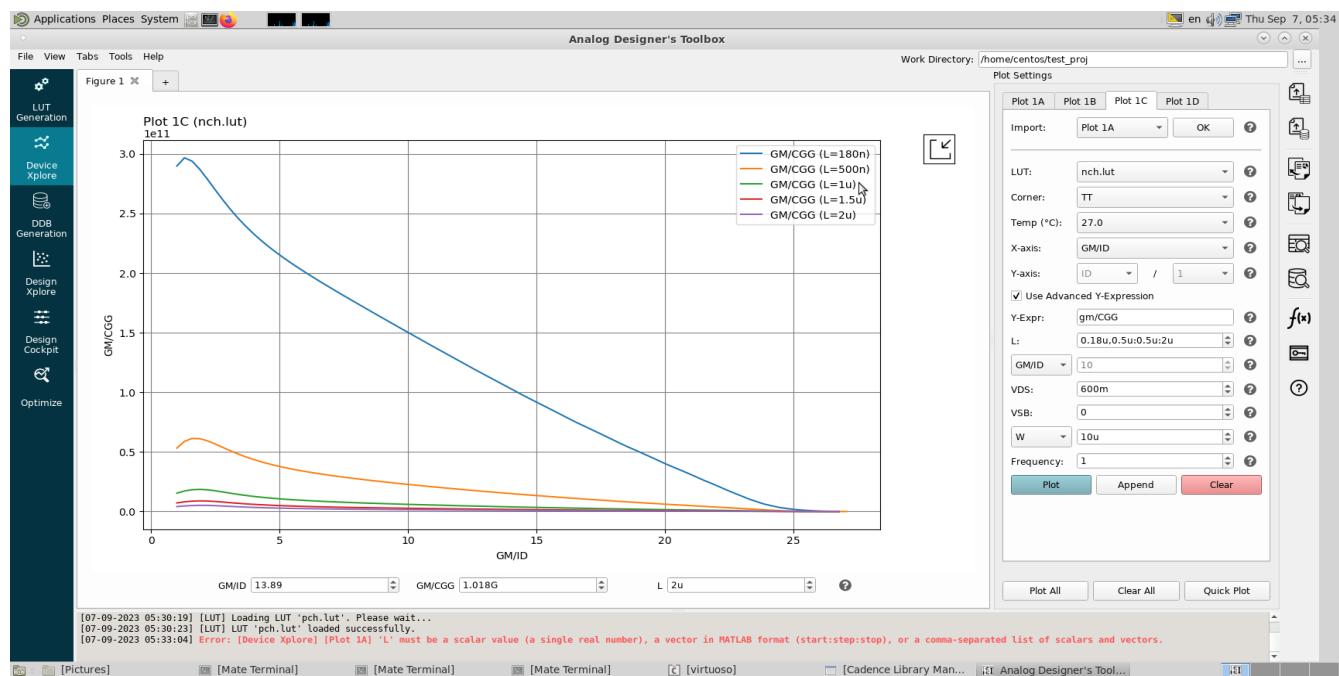
gm/gds:



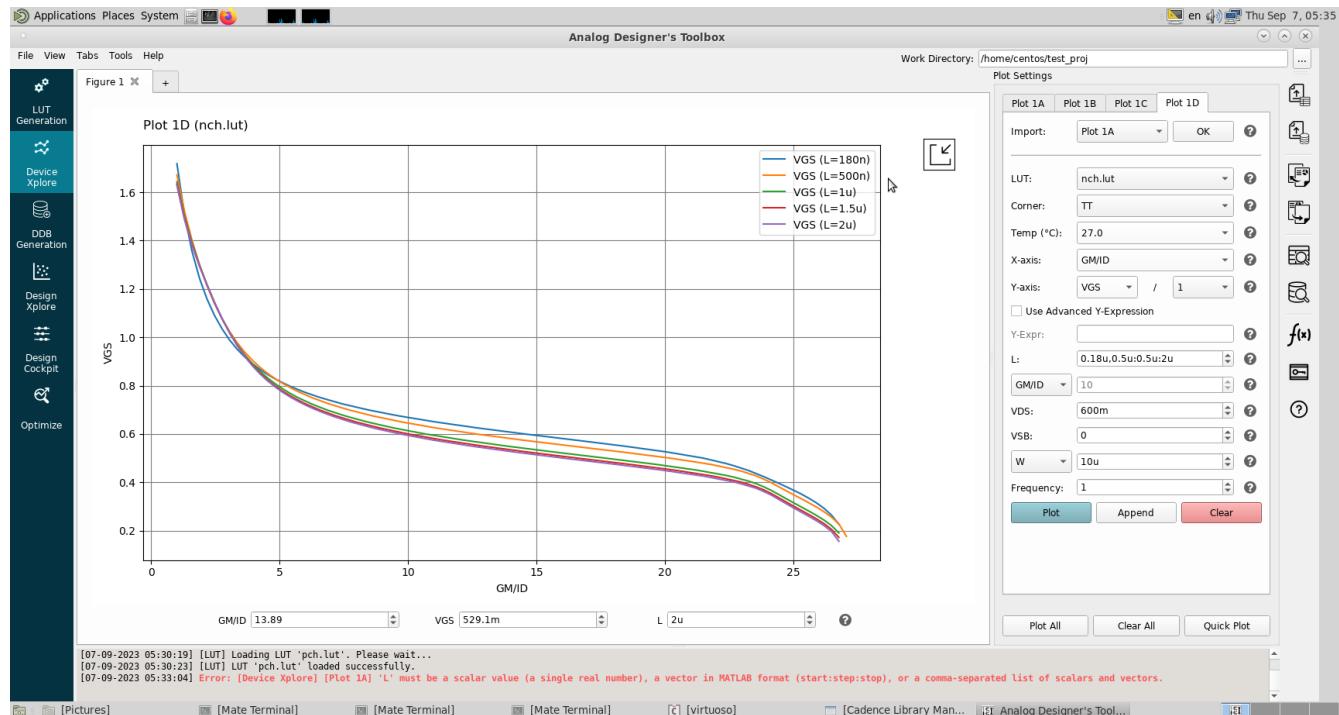
ID/W:



## gm/Cgg:

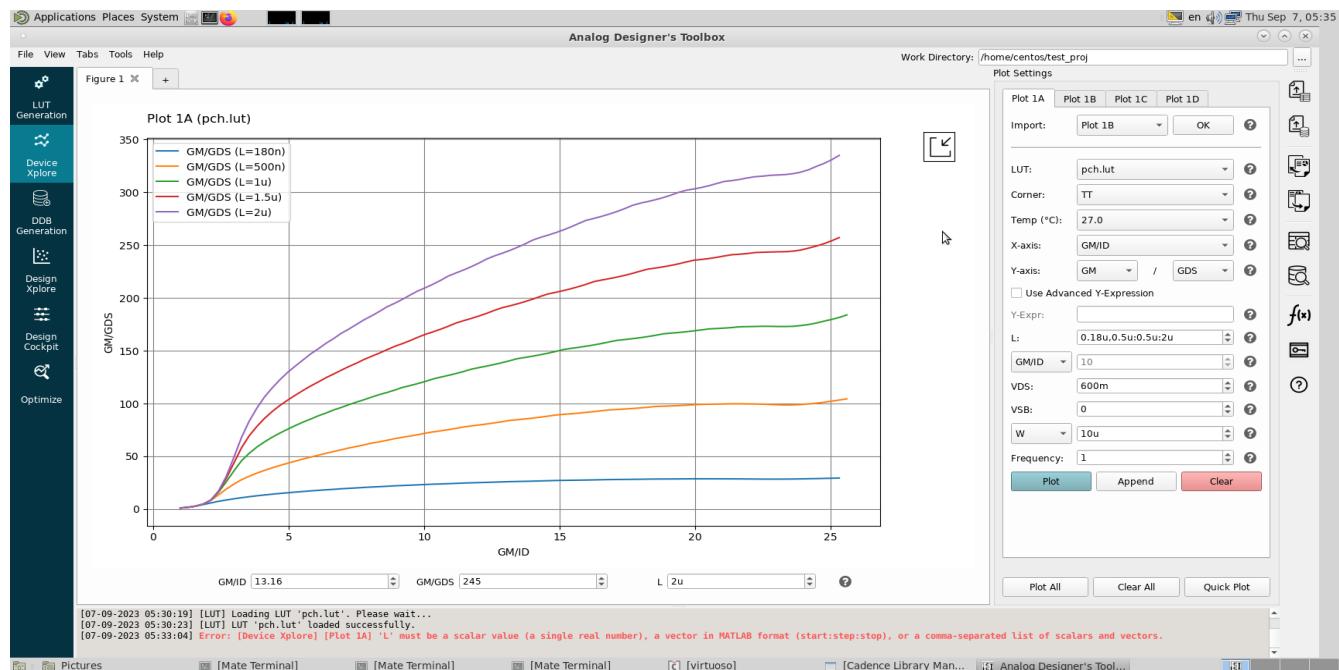


## VGS:

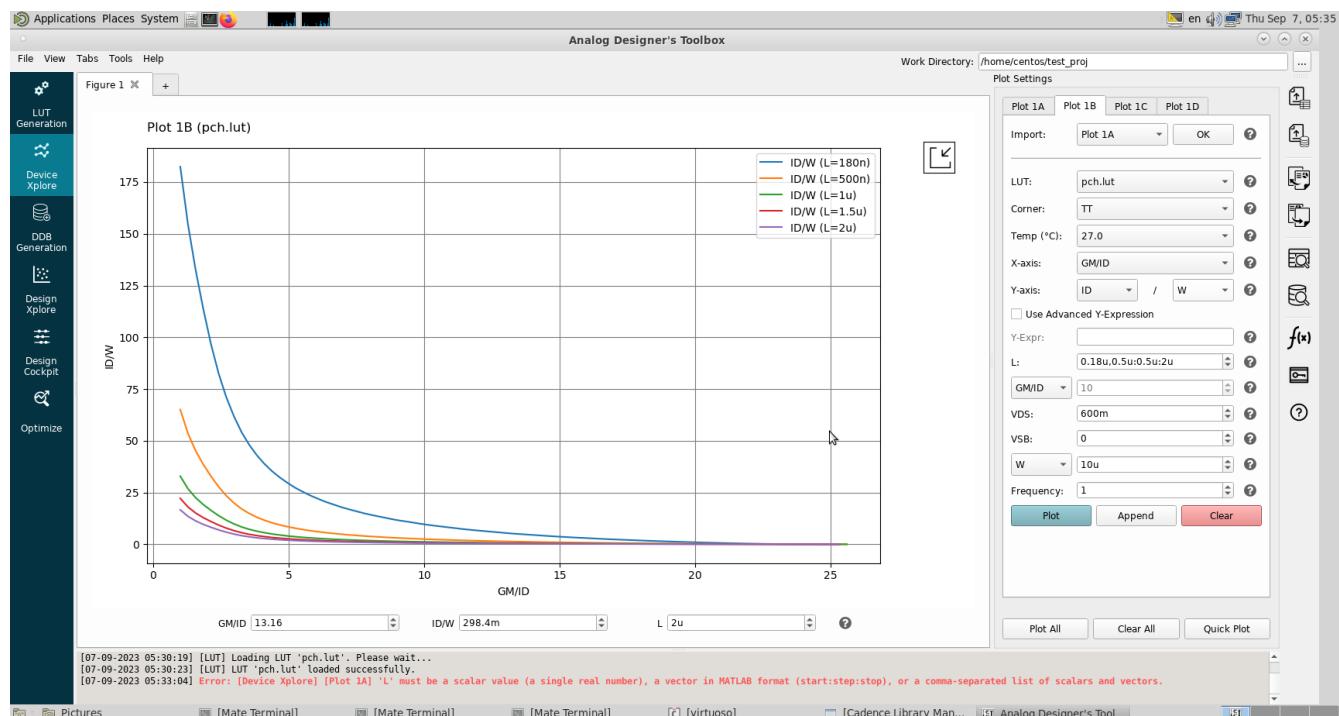


## 2.PMOS:

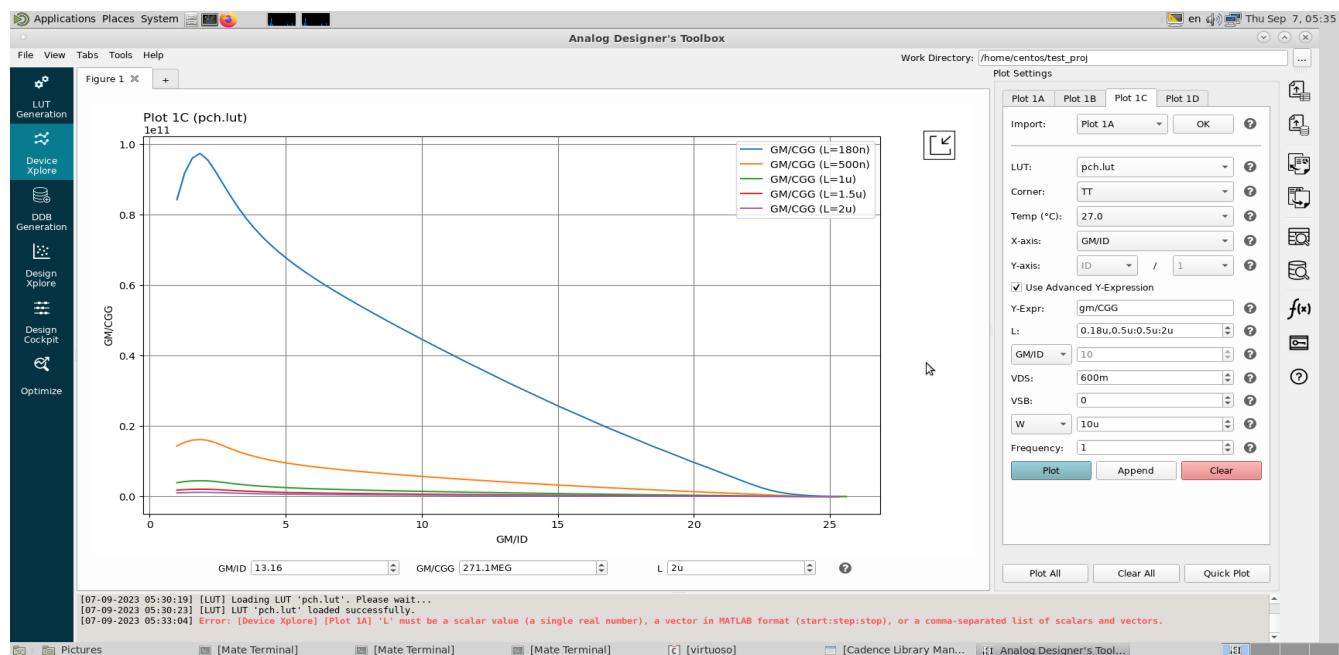
gm/gds:



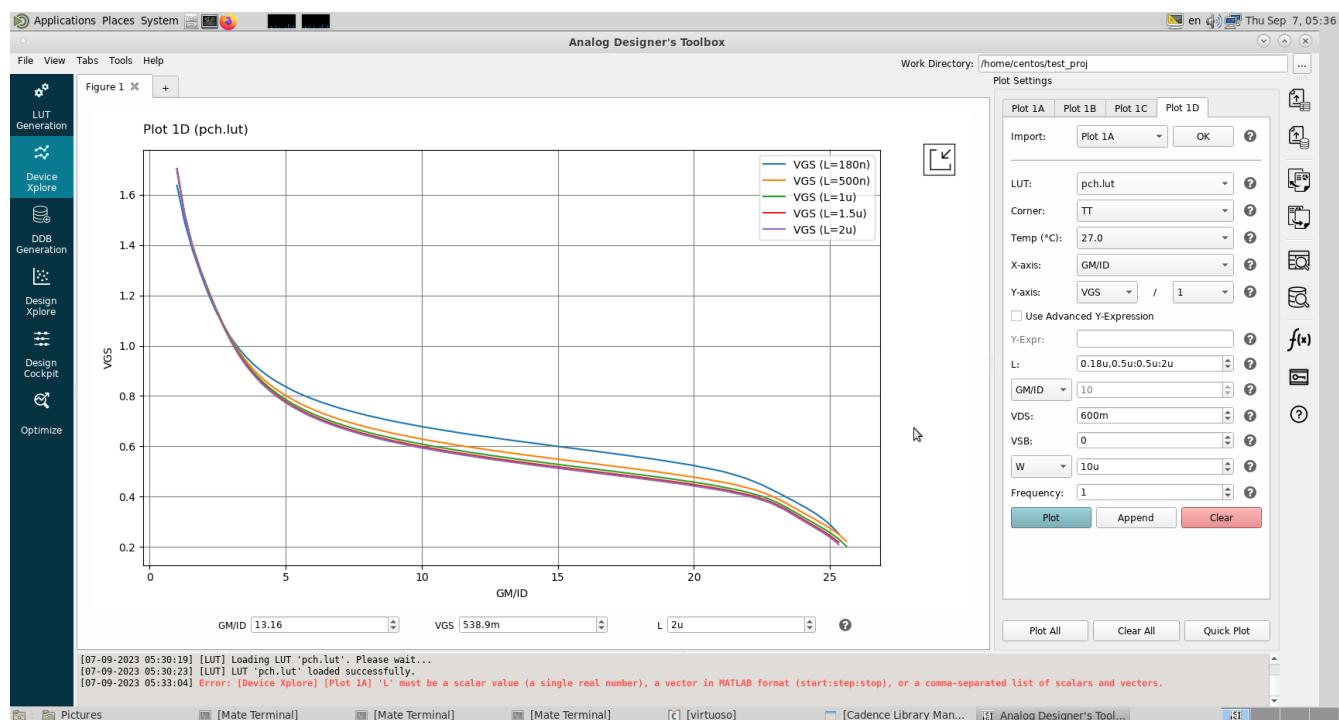
ID/W:



## gm/Cgg:



## VGS:



## Part 2 (OTA design):

### 1. SPECS required ,topolgy selection , givens and assumptions:

The desirable specs are :

Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Closed loop gain	2	2
Phase margin	$\geq 70^\circ$	$\geq 70^\circ$
OTA current	$\leq 80\mu A$	$\leq 80\mu A$
CMFB circuit current	$\leq 40\mu A$	$\leq 40\mu A$
CM input range – low	$\leq 0$	$\leq 0$
CM input range – high	$\geq 0.6V$	$\geq 1.1V$
Differential output swing	0.6Vpk-to-pk	1.2Vpk-to-pk
Load	1pF	1pF
DC Loop gain	50dB	60dB
Closed loop bandwidth	10MHz	10MHz

we will use a PMOS as input pair and tail current source mosfets and NMOS as active current mirror load mosfets and one PMOS and one NMOS mosfets for cascode for each branch.

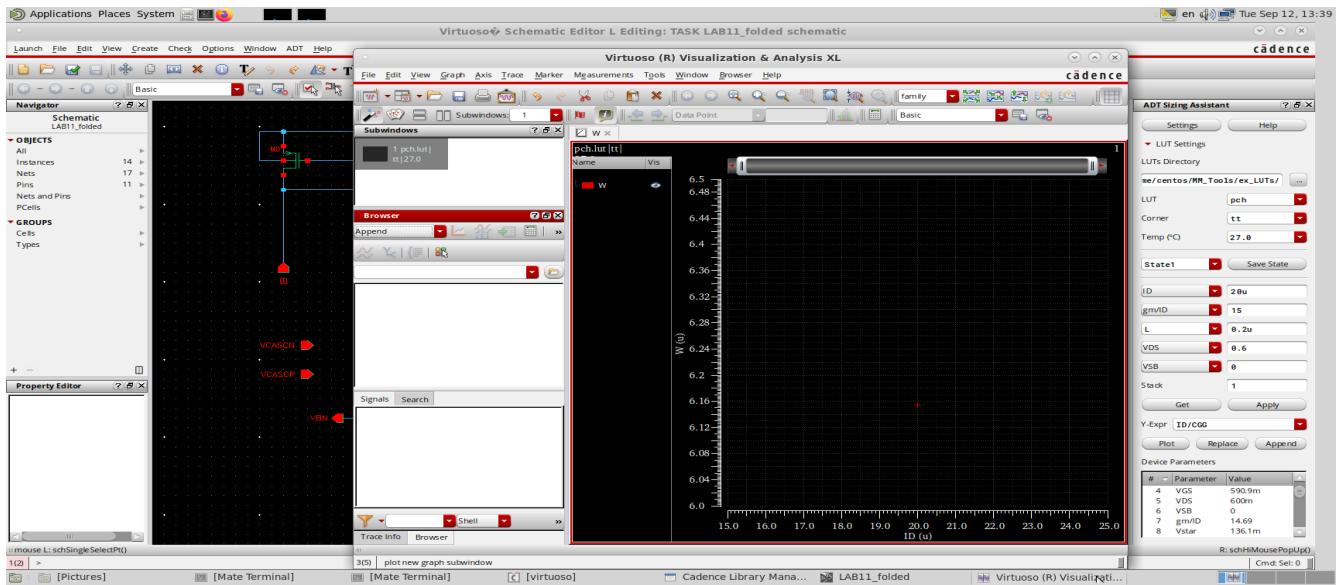
we assume VDS=0.6V and VSB=0V

### 2.Input pair design :

#### assumptions and givens:

$$L = 0.2\mu m \quad \text{and} \quad gm/id = 15 \quad \text{and} \quad ID = 20\mu A$$

## simulation results:



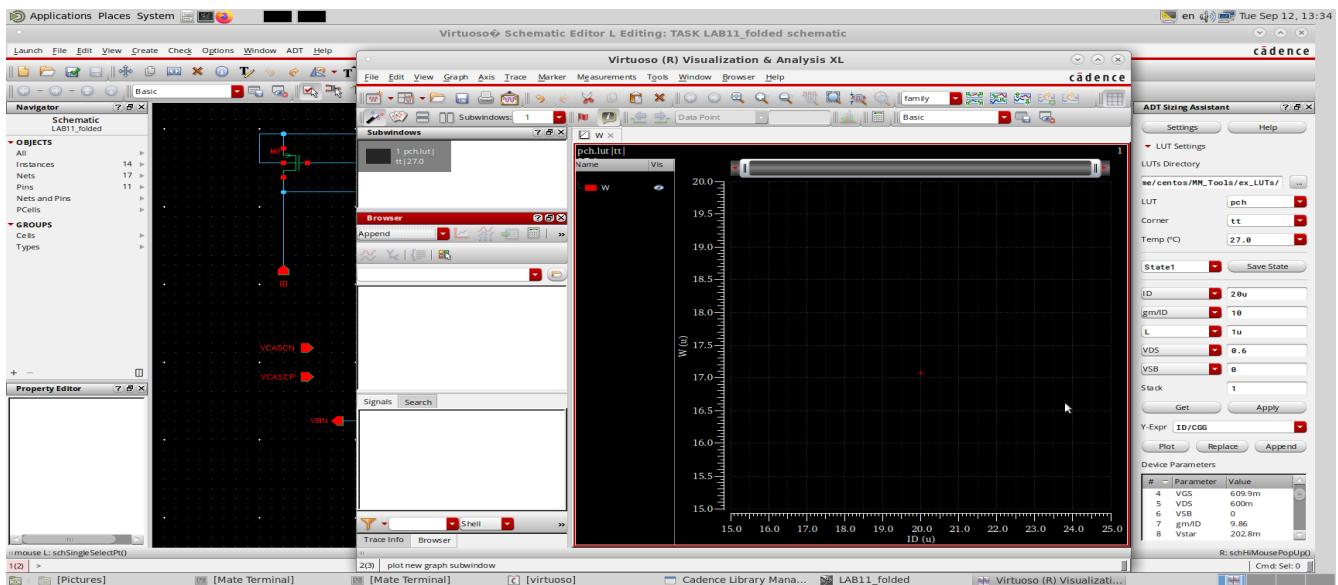
$W = 6.36\mu m$     $L = 0.2\mu m$     $VGS = 590.9mV$     $Vstar = 136.1mV$

## 3. current sources design :

### assumptions and givens:

$$L = 1\mu m \quad \text{and} \quad gm/id = 10 \quad \text{and} \quad ID = 20\mu A$$

## simulation results:



$W = 17.33\mu m$     $L = 0.2\mu m$     $VGS = 609.9mV$     $Vstar = 202.8mV$

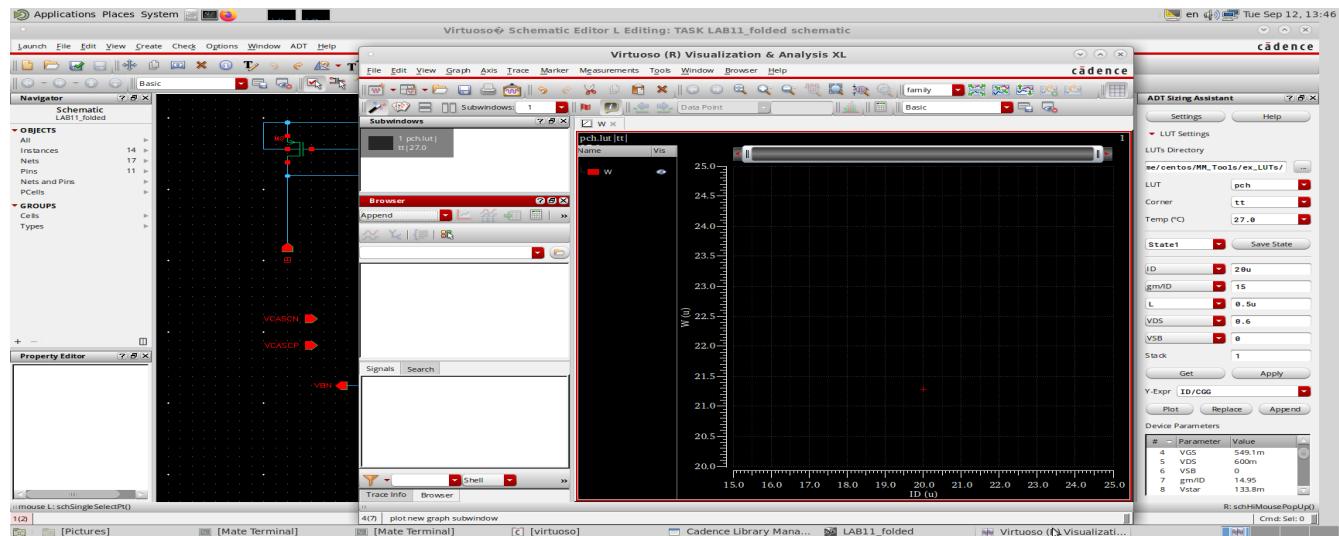
## 4.Casecode design :

### assumptions and givens:

$$L = 0.5\mu m \quad \text{and} \quad gm/id = 15 \quad \text{and} \quad ID = 20\mu A$$

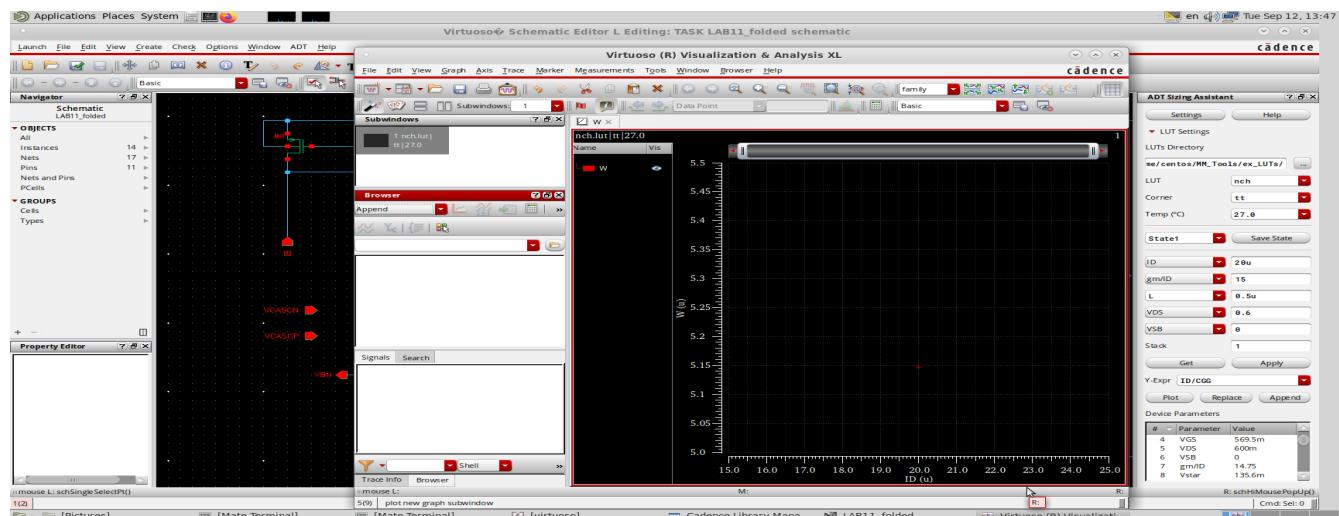
### simulation results:

#### 1.PMOS:



$W = 21.73\mu m$     $L = 0.5\mu m$     $VGS = 549.1mV$     $Vstar = 133.8mV$

#### 2.NMOS:



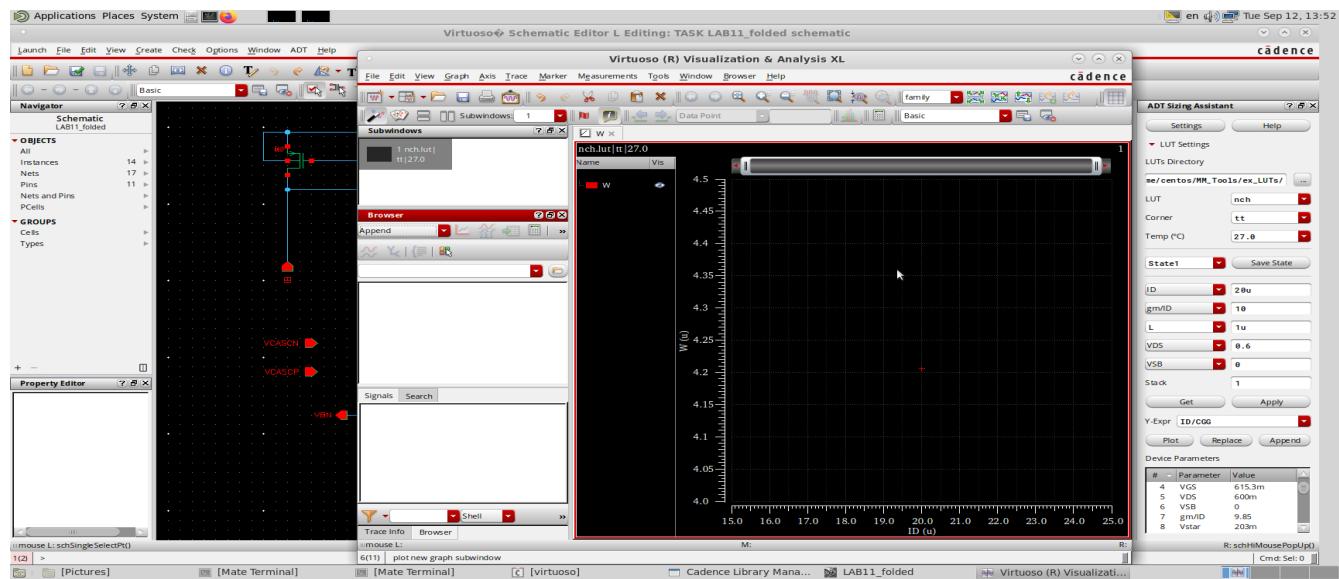
$W = 5.28\mu m$   $L = 0.5\mu m$   $VGS = 569.5mV$   $Vstar = 133.8mV$

## 5.Active load design :

### assumptions and givens:

$$L = 1\mu m \quad \text{and} \quad gm/id = 10 \quad \text{and} \quad ID = 20\mu A$$

### simulation results:



$W = 4.27\mu m$   $L = 1\mu m$   $VGS = 615.3mV$   $Vstar = 203mV$

## 6.Calculations for VCASCN and VCASCP :

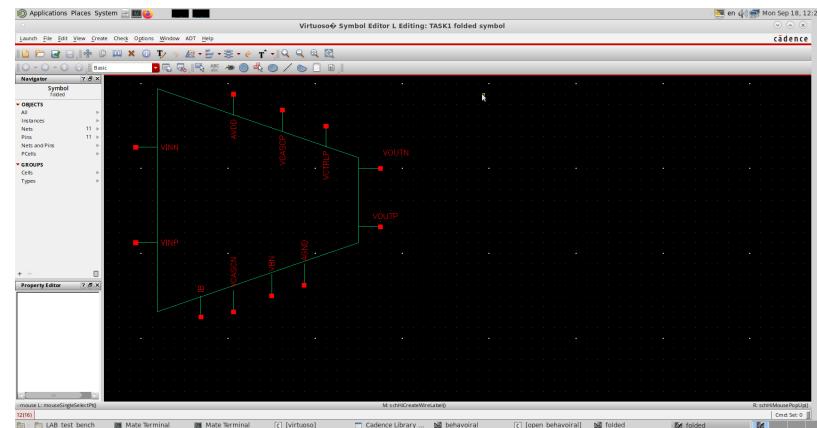
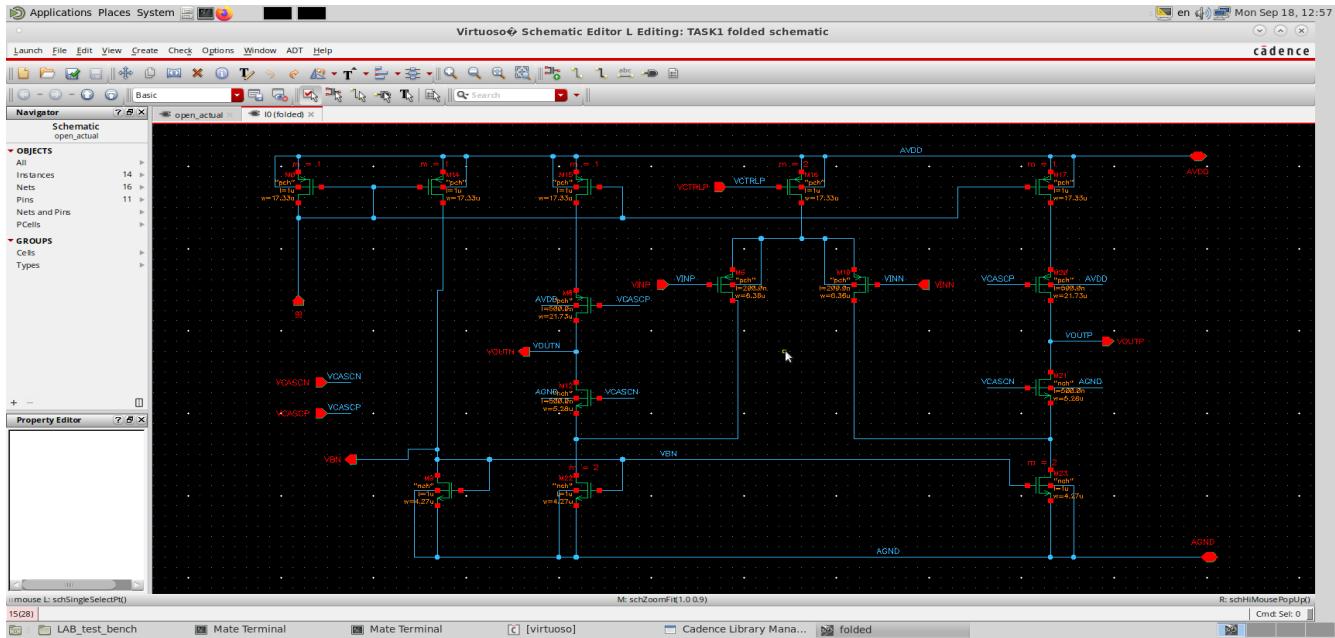
Handwritten calculations:

$$V^* = 133.6mV, VGSN = 569.5mV, VGSp = 590.9mV$$

$$VCASCP \approx VGSN + V^* = 569.5 \times 10^{-3} + 133.6 \times 10^{-3} = 805 \times 10^{-3} \text{ mV}$$

$$VCASCN \approx VDS - |VGSp| - V^* = 1.8 - 590 \times 10^{-3} - 133.6 \times 10^{-3} \approx 1.07 \text{ mV}$$

## Schematic:

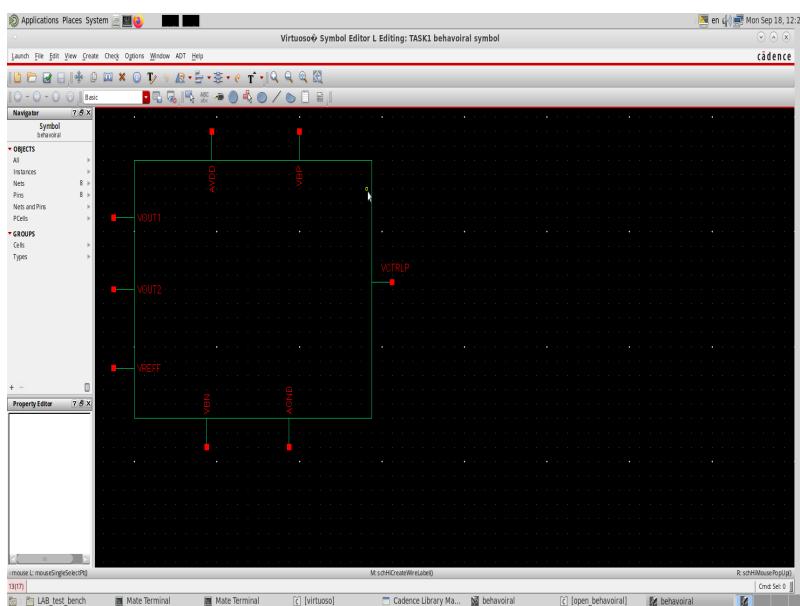
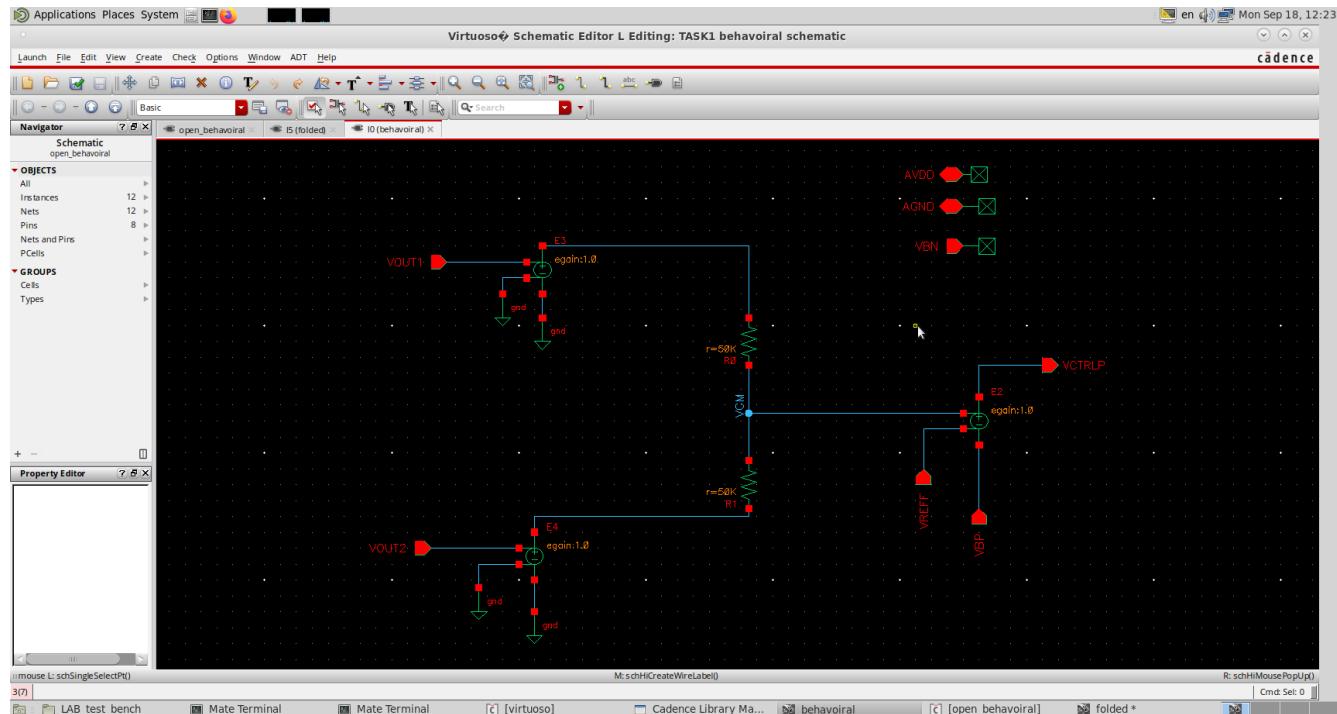


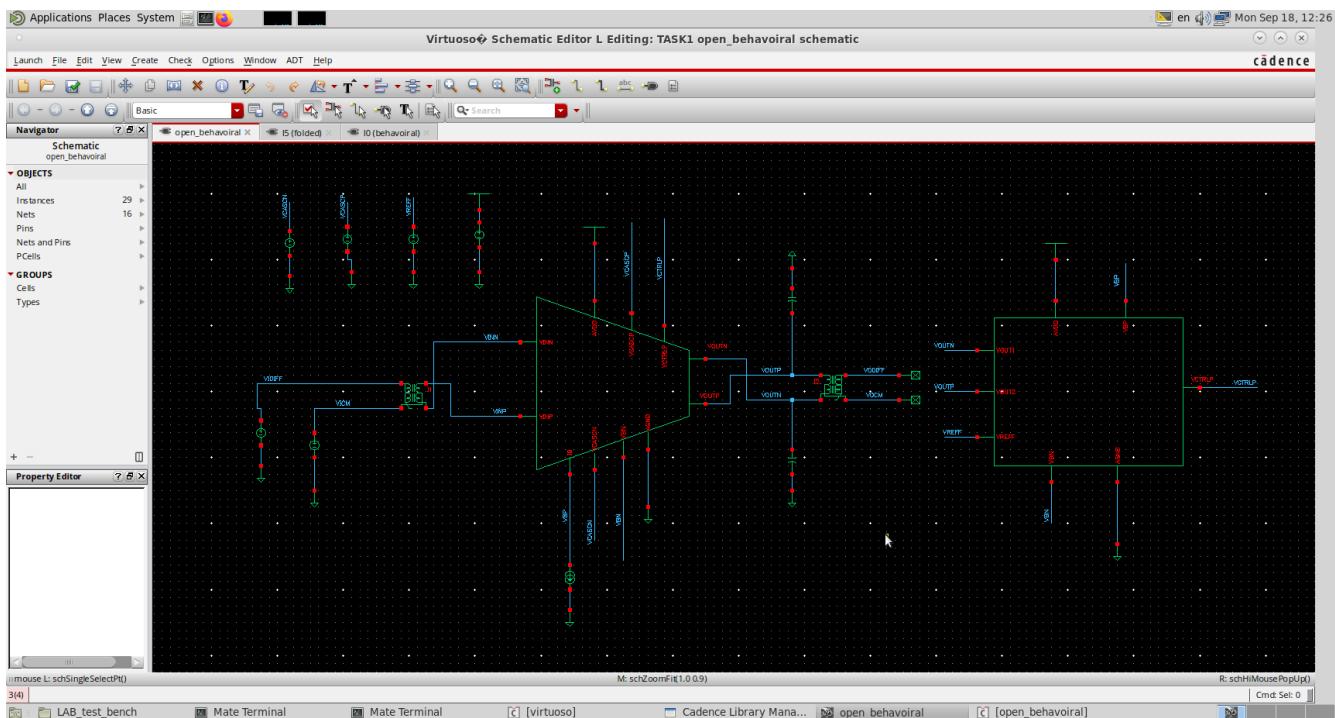
## Conclusion:

	W	L	ID	gm/ID	V*	gm
Input pair	6.36u	0.2u	20u	15	136.1m	300us
Current sources	17.33u	1u	20u	10	202.8m	200us
Active loads	4.27u	1u	20u	10	203m	200us
Cascode NMOS	5.28u	0.5u	20u	15	133.8m	300us
Cascode PMOS	21.73u	0.5u	20u	15	133.8m	300us

## Part 3(Open loop OTA simulation (Behavoiral CMFB)):

### Schematic:





The best selection is 0.9 V to maximize output swing.

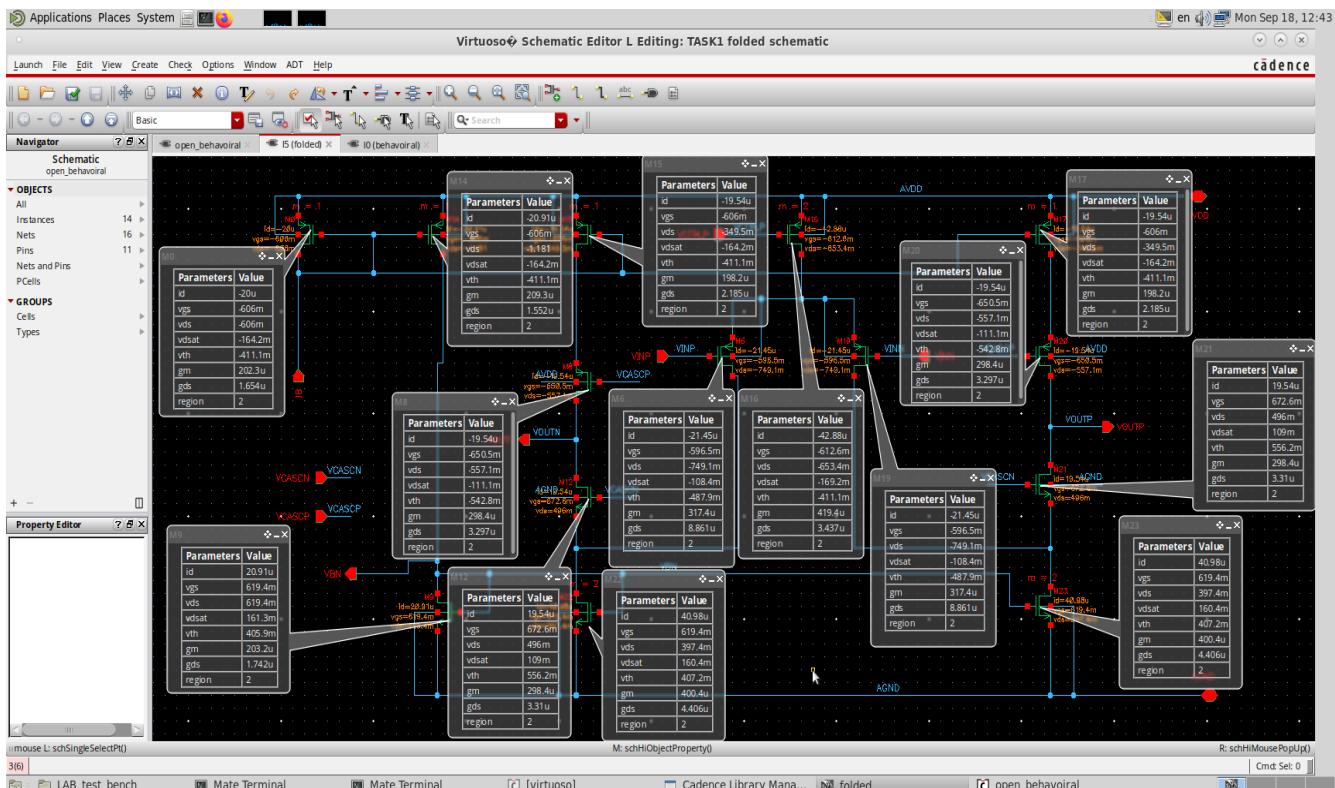
$$V_{outcm} = 0.9002V$$

The relation between output and input voltage of the error amplifier is  $V_{OUT} = V_{IN} \cdot A_v$

	Name	Value
1	/VOUTCM	900.2E-3
2	/VOUTDIF	22.78E-15
3	/VOUTN	900.2E-3
4	/VOUTP	900.2E-3
5	/VREF	900.0E-3
6	/VBP	1.194
7	/VBN	618.8E-3

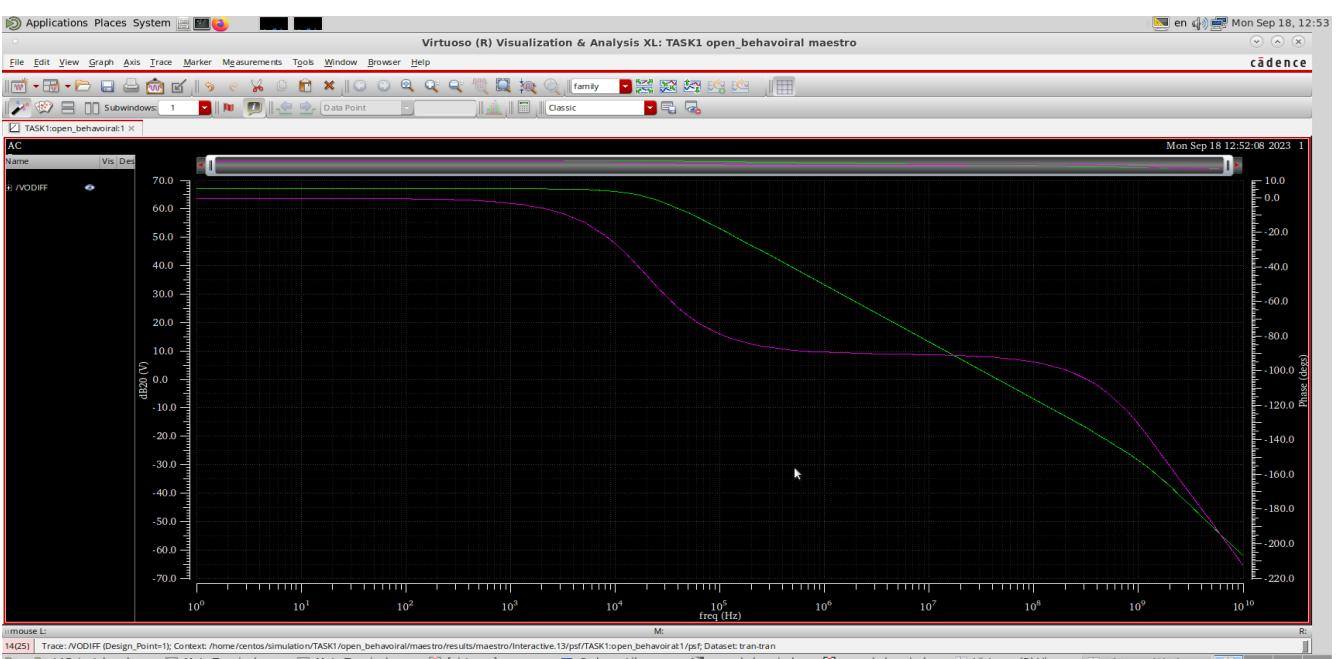
Name	Type	Details	Value
diff_out	expr	(v"/VCTRLP" ?result "dcOp") - v"/VBP" ?result "dcOp"))	195.3u
diff_in	expr	(v"/VOUTCM" ?result "dcOp") - v"/VREF" ?result "dcOp"))	195.3u

## 1. DC OP :

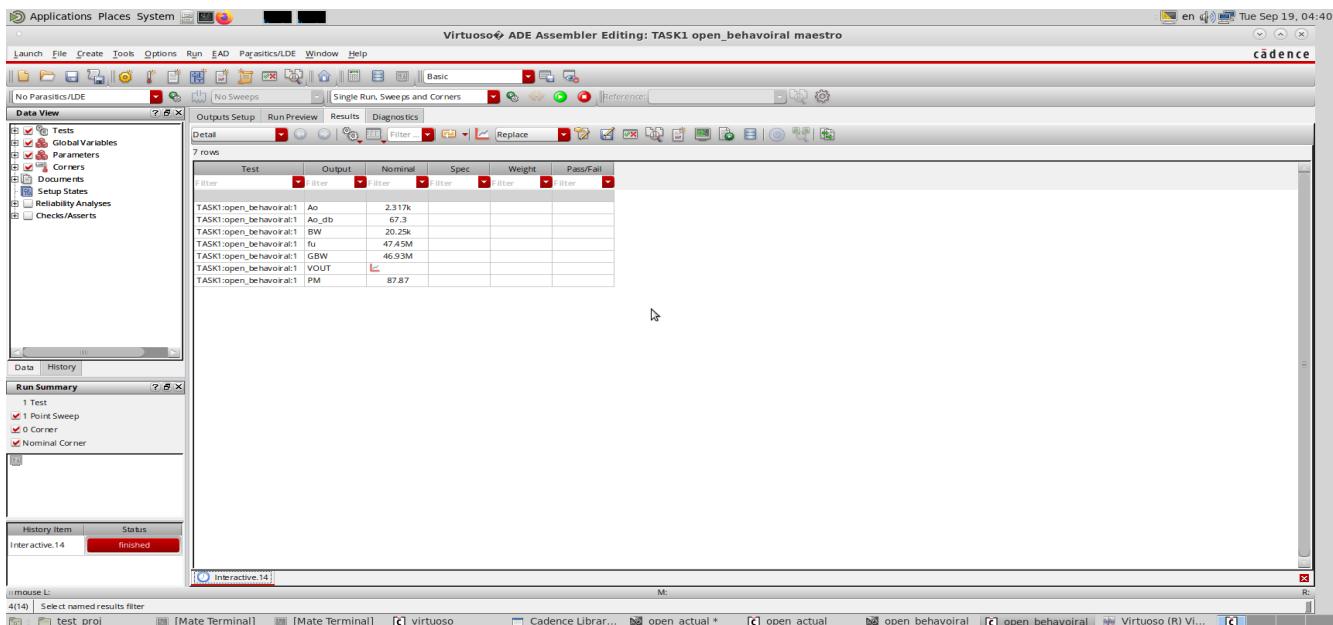


## 2. diff small signal ccs:

Diff gain in db(magnitude, phase) VS frequency :



## Calculations:



compare:

Simulation results	Hand analysis results
Avdiff= 2.317k	$R_{out} = R_{ocp} \left[ 1 + (g_{mcop} + g_{mbcp}) R_{load} \right]$ $\approx 41.72 \times 10^6 \parallel 6.34 \times 10^6$ $= 5503 K\Omega$
BW=20K	
GBW=46.9MHz	$A_{OL} = 317.8 \times 10^{-6} \times 5.5 \times 10^6 = 1746.69$ $BW = \frac{1}{2\pi \times R_{out} \times C_L} = 30 \text{ kHz}$ $GBW = BW \cdot A_{OL} = 50.5 \text{ MHz}$

## Part 4(Open loop OTA simulation (Actual CMFB)):

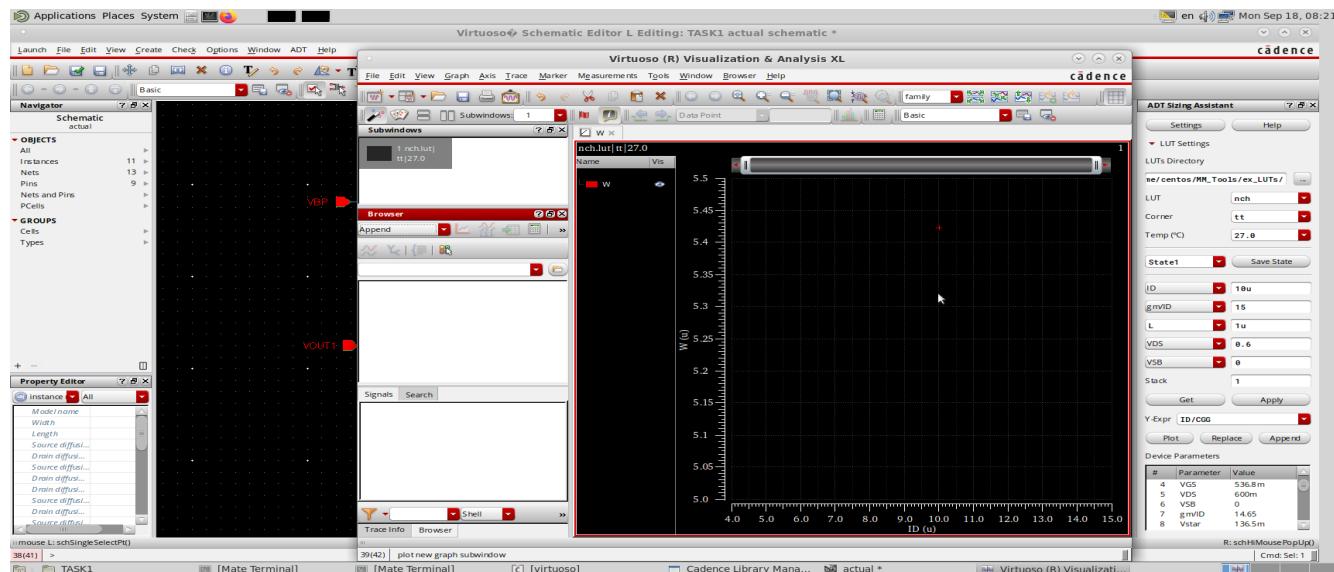
### Design of the CMFB:

#### 1. NMOS :

##### assumptions and givens:

$$L = 1\text{um} \quad \text{and} \quad gm/id = 15 \quad \text{and} \quad ID = 10\mu\text{A}$$

##### simulation results:



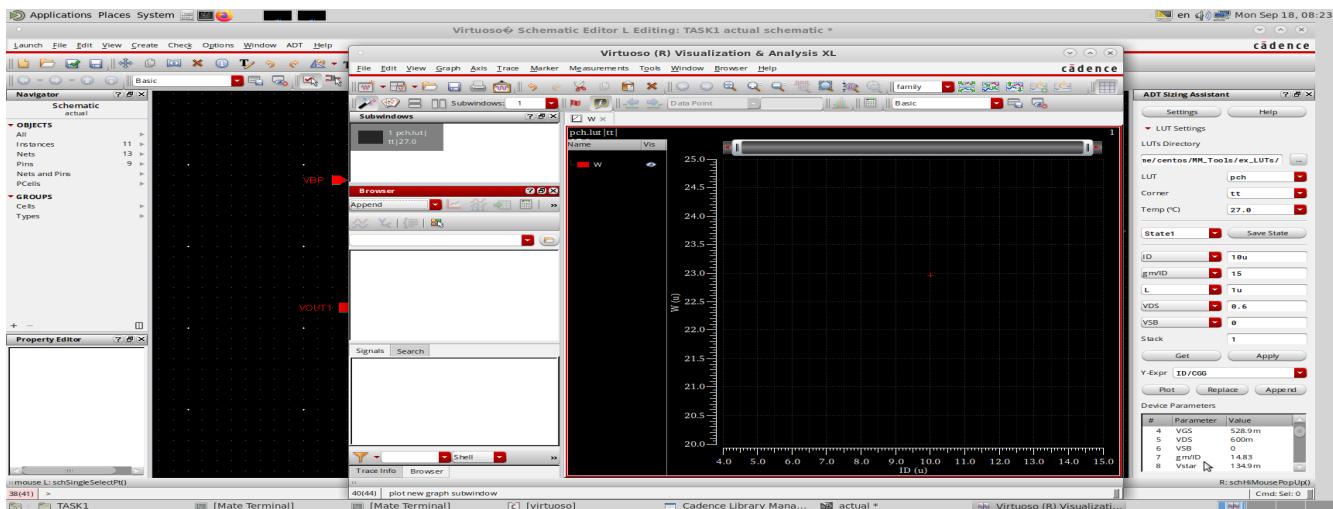
$$W = 5.61\text{um} \quad L = 1\text{um} \quad VGS = 536.8\text{mV} \quad Vstar = 136.5\text{mV}$$

#### 2. PMOS :

##### assumptions and givens:

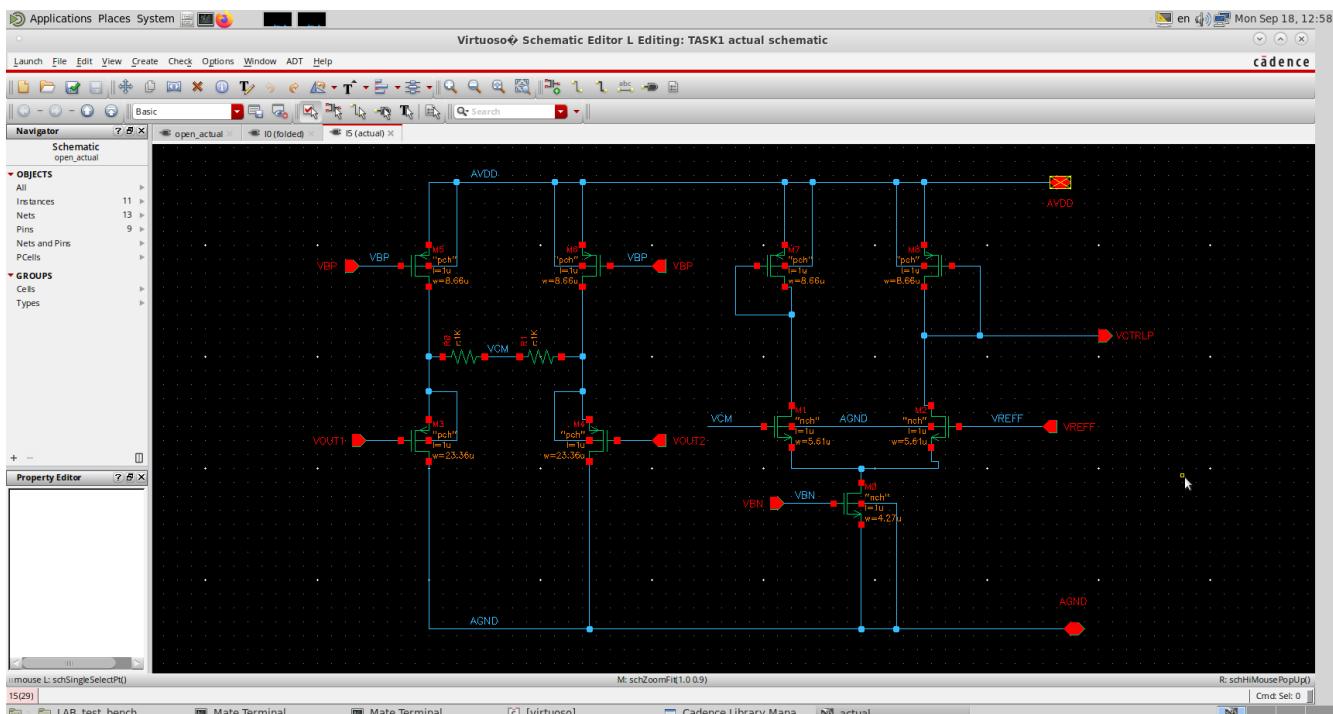
$$L = 1\text{um} \quad \text{and} \quad gm/id = 15 \quad \text{and} \quad ID = 10\mu\text{A}$$

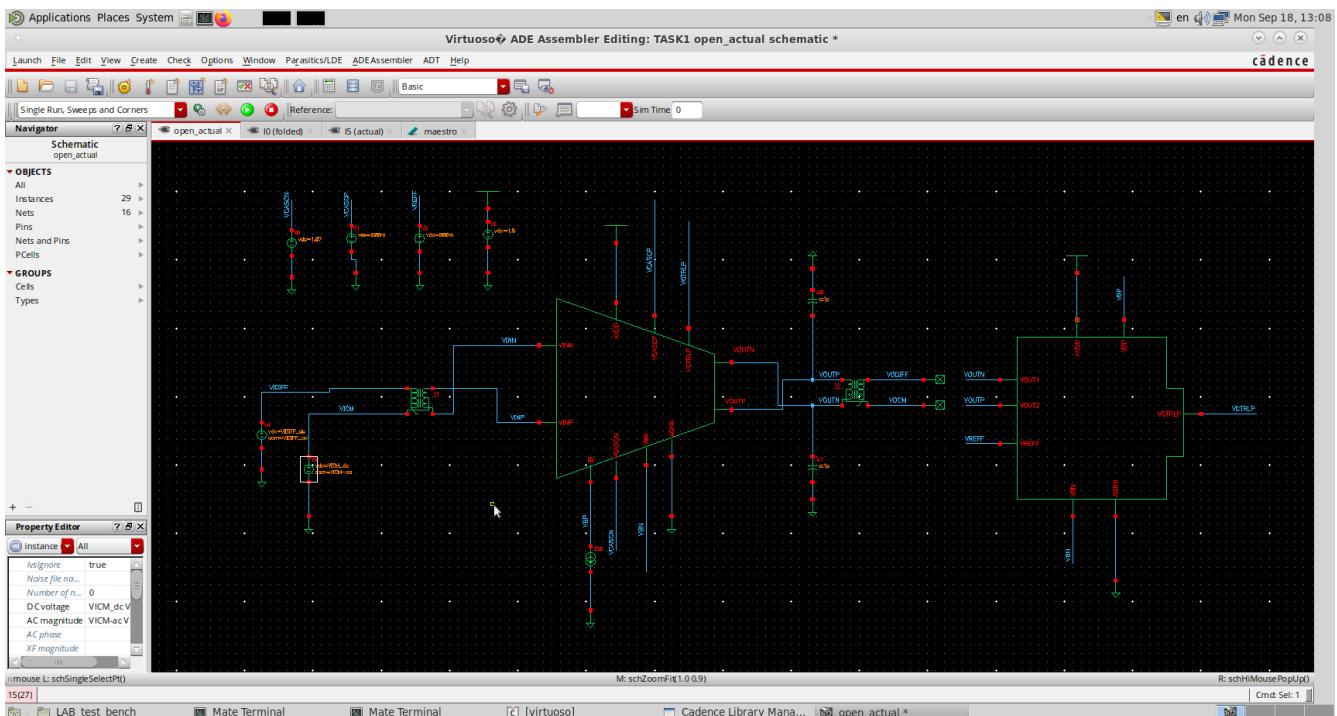
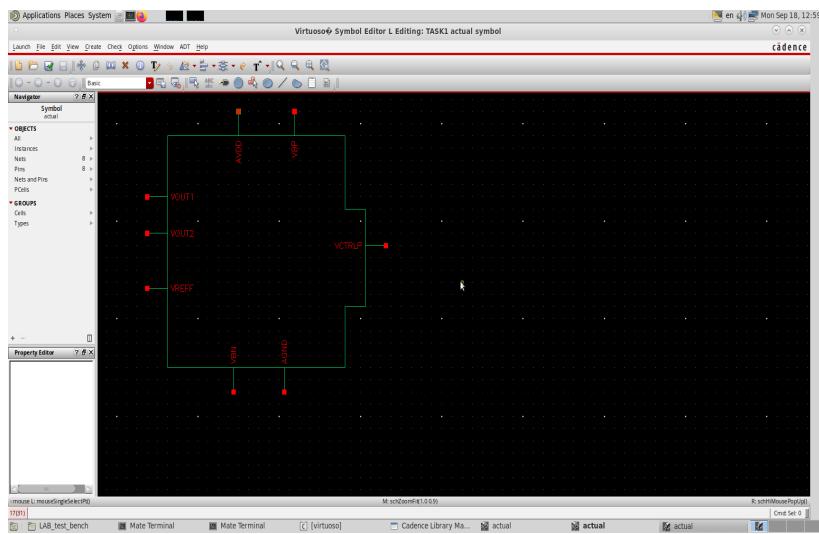
## simulation results:



$W = 23.36\mu m$   $L = 1\mu m$   $VGS = 528.9mV$   $Vstar = 134.9mV$

## Schematic:





$V_{ICM} = 0.55V$  in the middle of the CMIR.

$V_{REF}$  should be  $1.1V$

$V_{CM}$  output =  $1V$  To maximize output swing

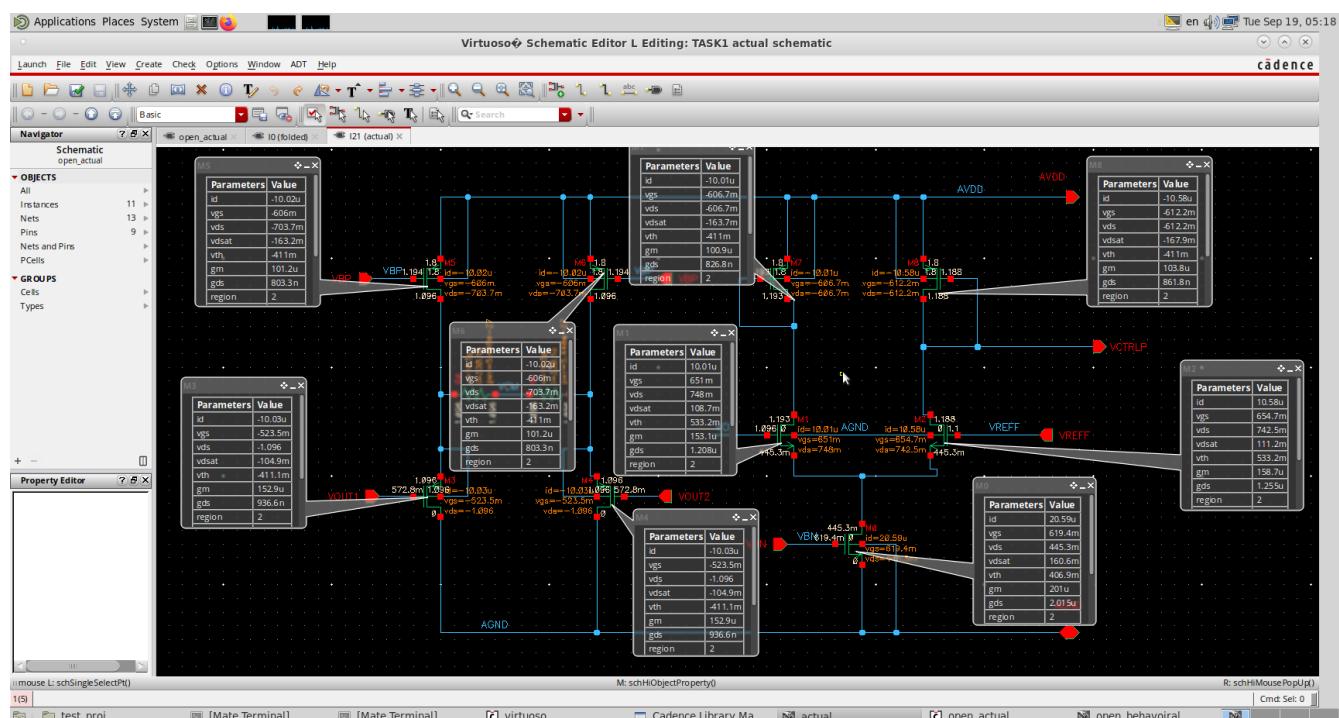
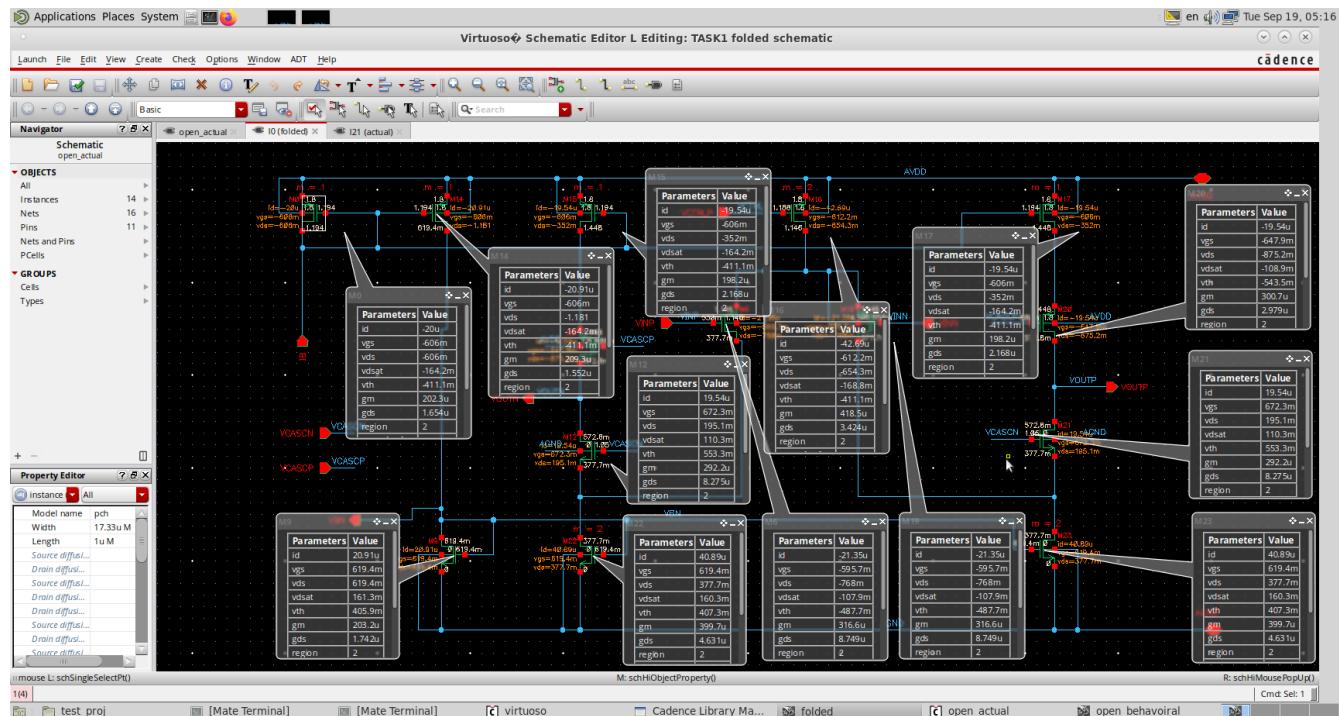
Diff output =  $\Delta V_{out} = V_{CTRLP} - V_{BP} = 1.188 - 1.194 = -6mV$

Diff input =  $\Delta V_{in} = V_{outCM} - V_{REF} = 7.3mV - 7.15mV = 2mV$

$\Delta V_{out} = \Delta V_{in} \times A_v$

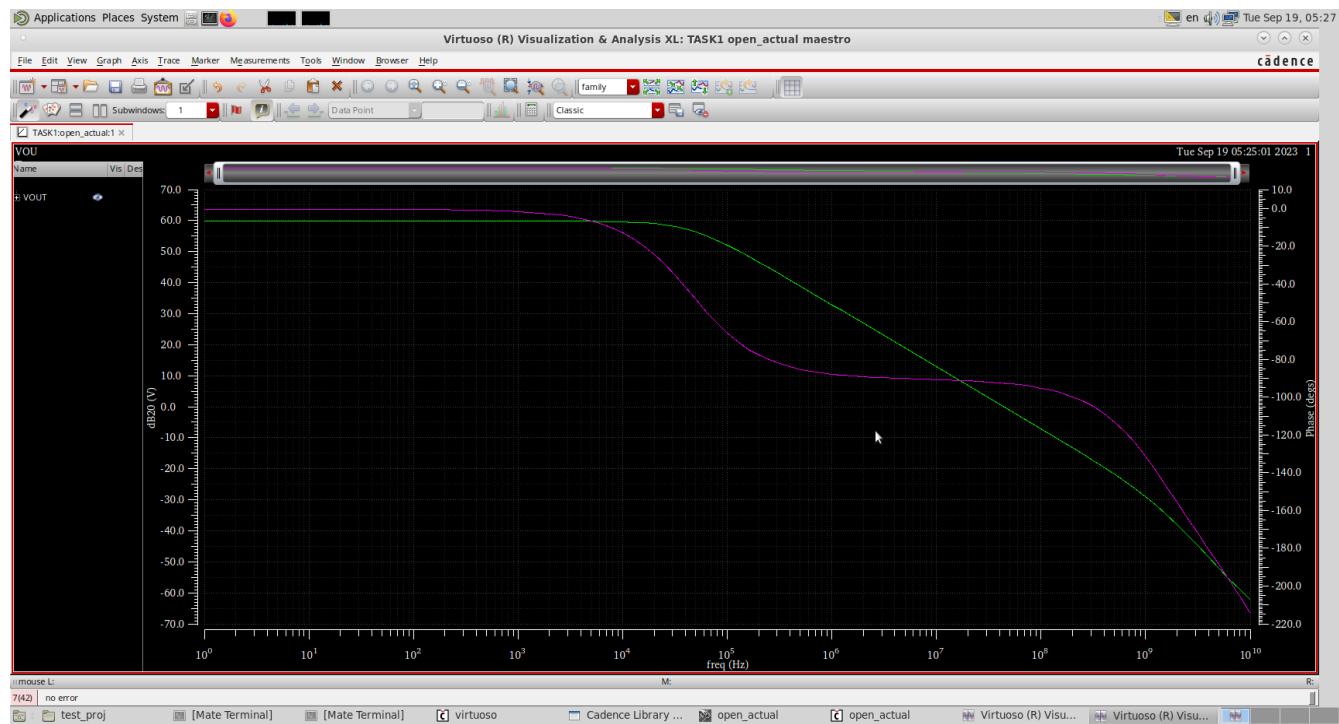
$$A_v = \frac{\Delta V_{out}}{\Delta V_{in}} \times 0.5 = \frac{1.58 \cdot 9}{103.6} \times 0.5 = 0.766$$

### 3.DC OP:

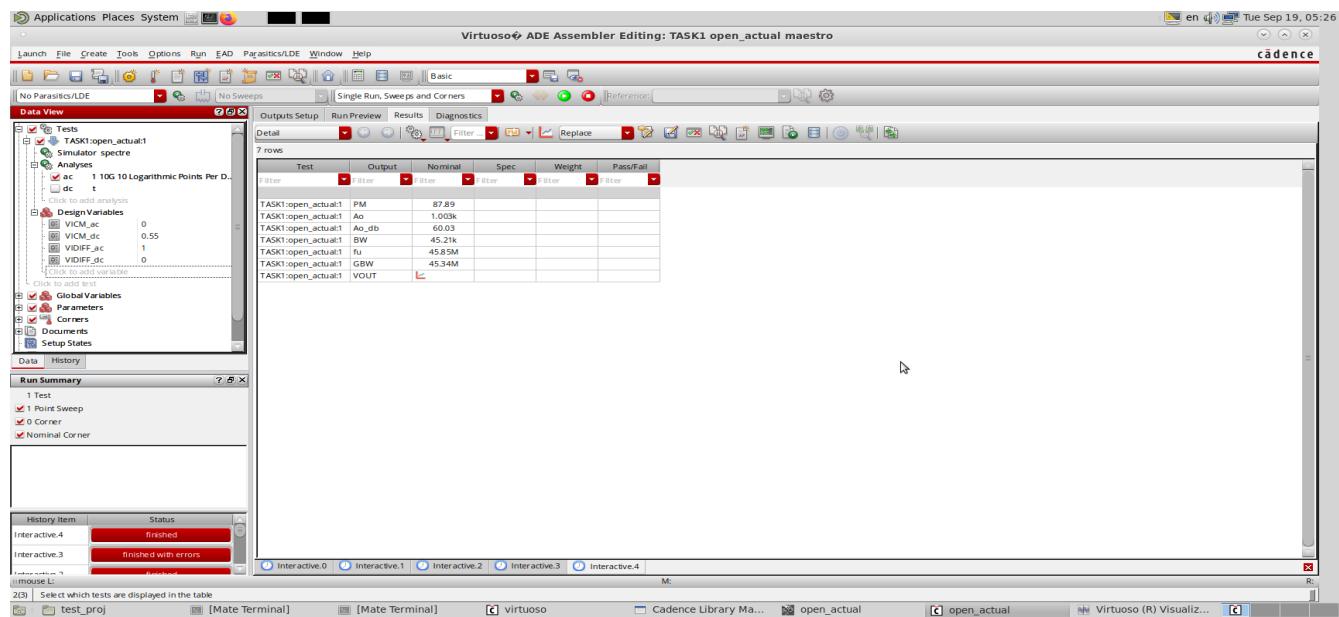


## 4.diff small signal ccs:

Diff gain in db(magnitude, phase) VS frequency :



## Calculations:

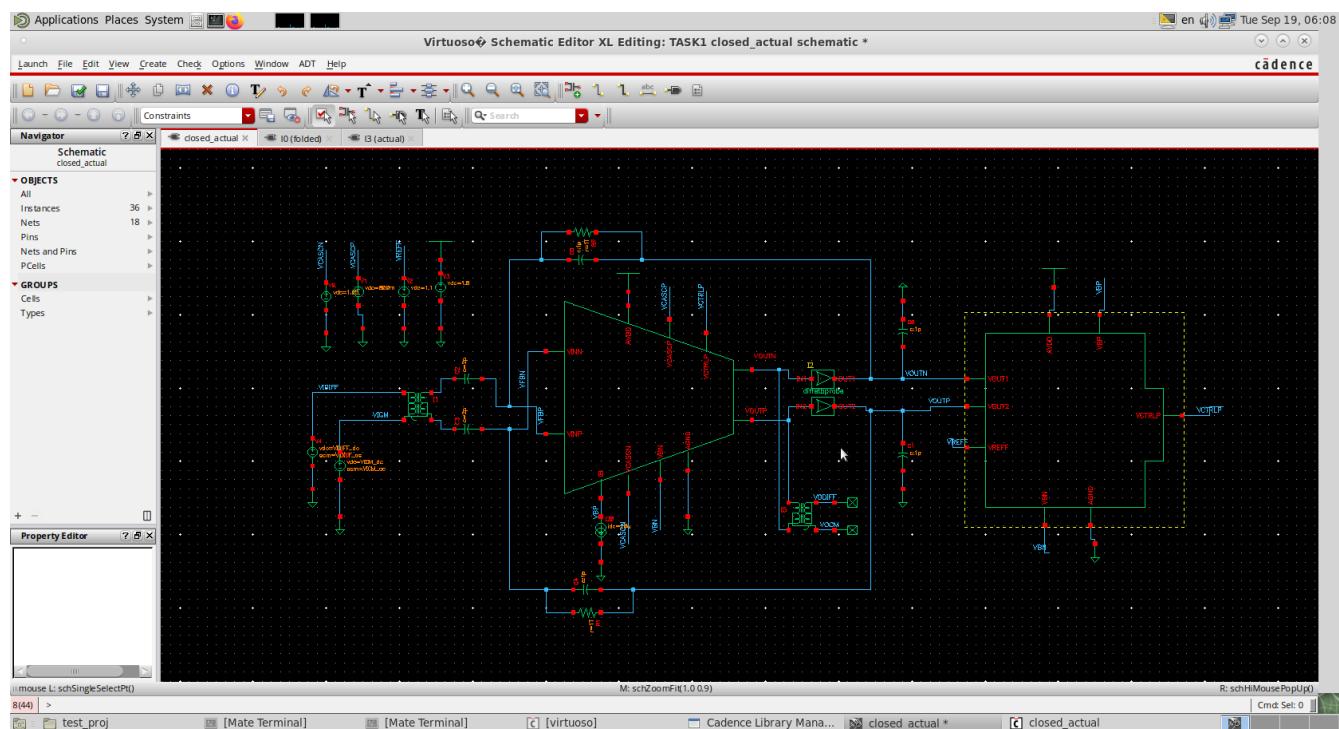


## compare:

Simulation results in actual	Simulation results in behavioral
Avdiff= 1k	Avdiff= 2.317k
BW=45.21K	BW=20K
GBW=45.34M	GBW=46.9MHz

## Part 5 (Closed loop simulation (AC and STB analysis)):

## Schematic:

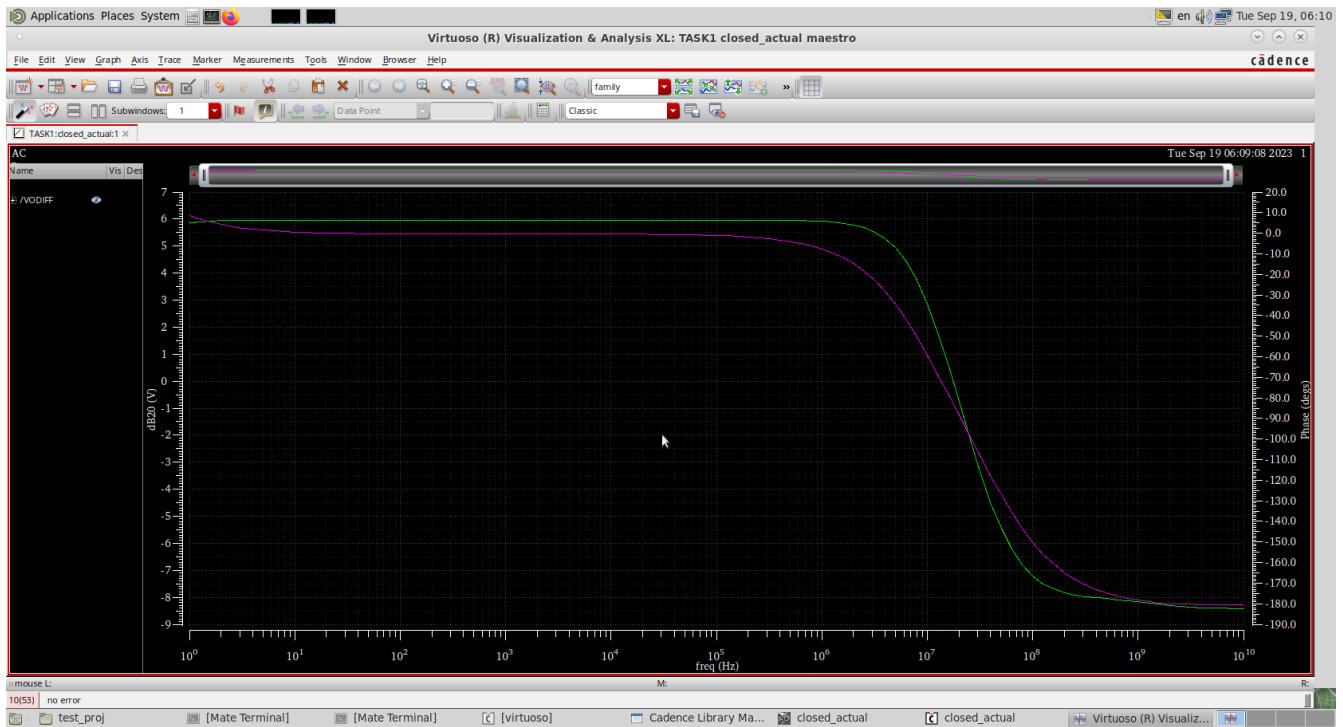


VCMOUT = 1.096V

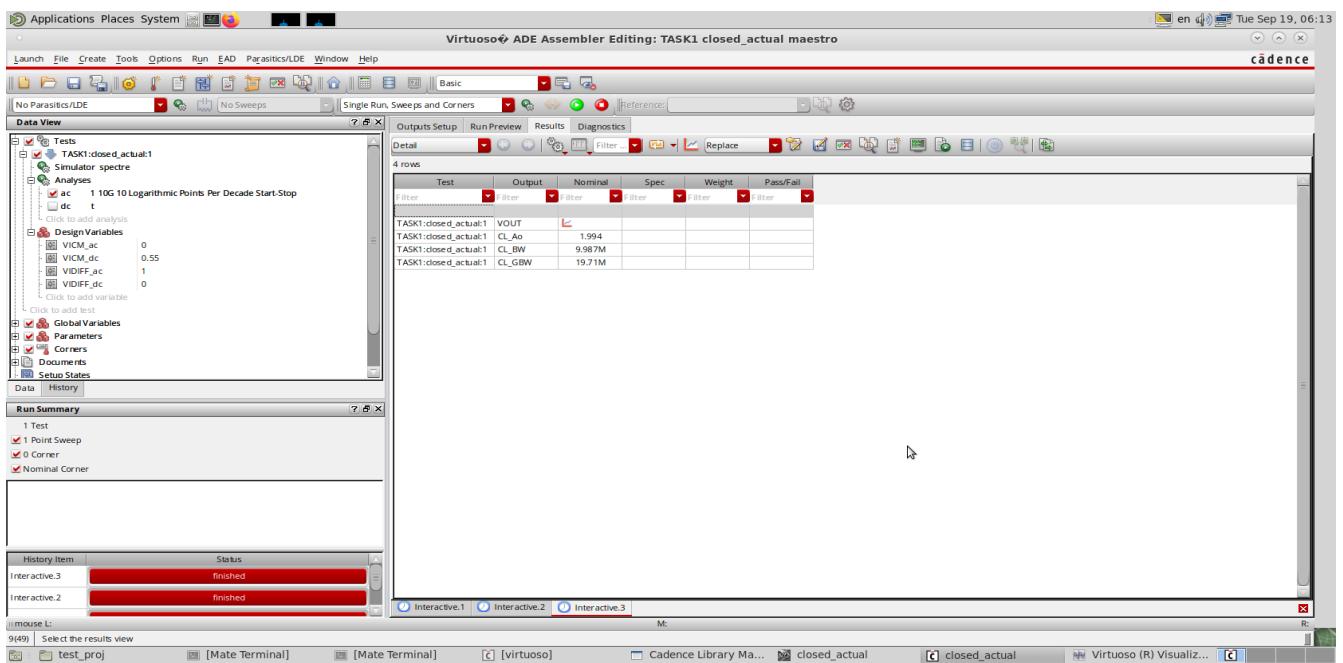
$$V_{REF} = 1.1V \quad V_{err} = 4mV$$

# 1.closed loop response:

VODIFF db(magnitude, phase) vs Frequency :

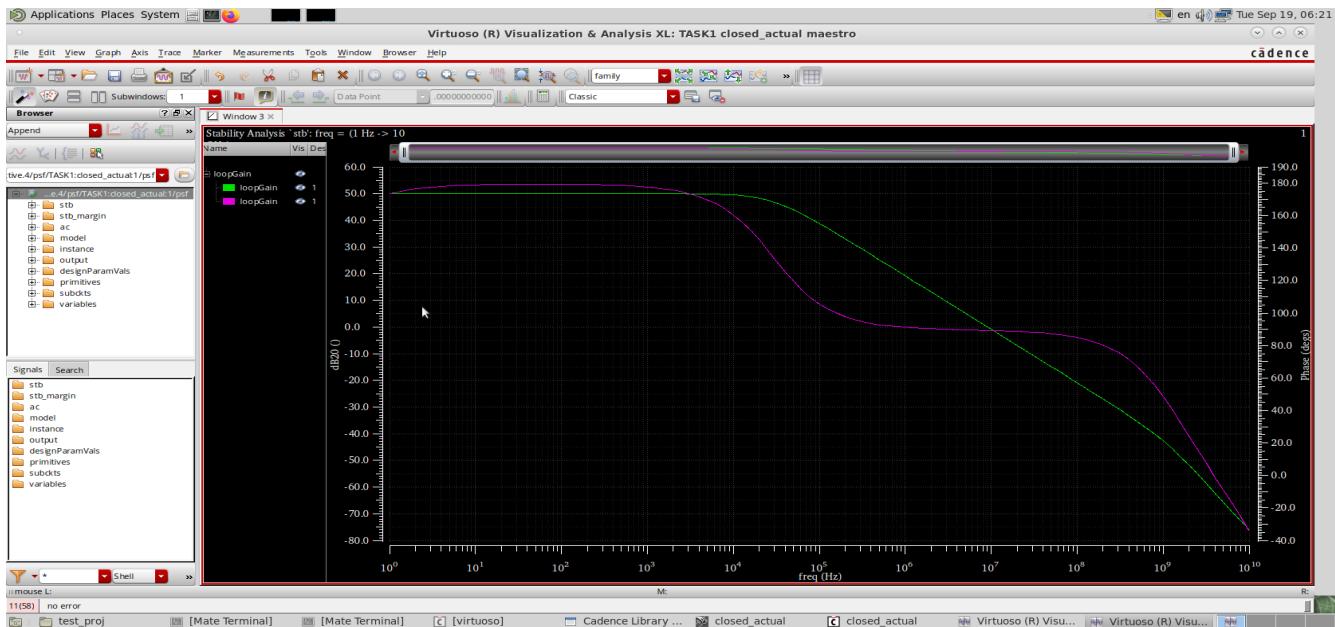


## Measures:

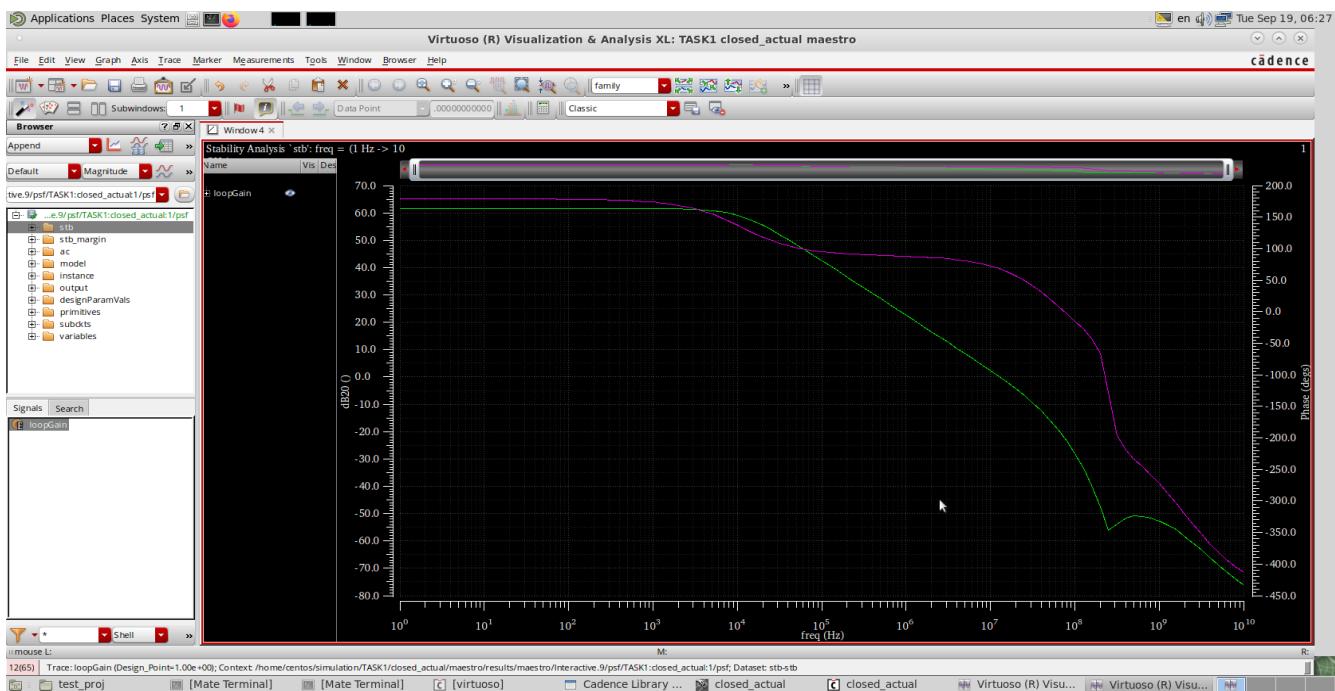


## 2.differential and CMFB loops stability:

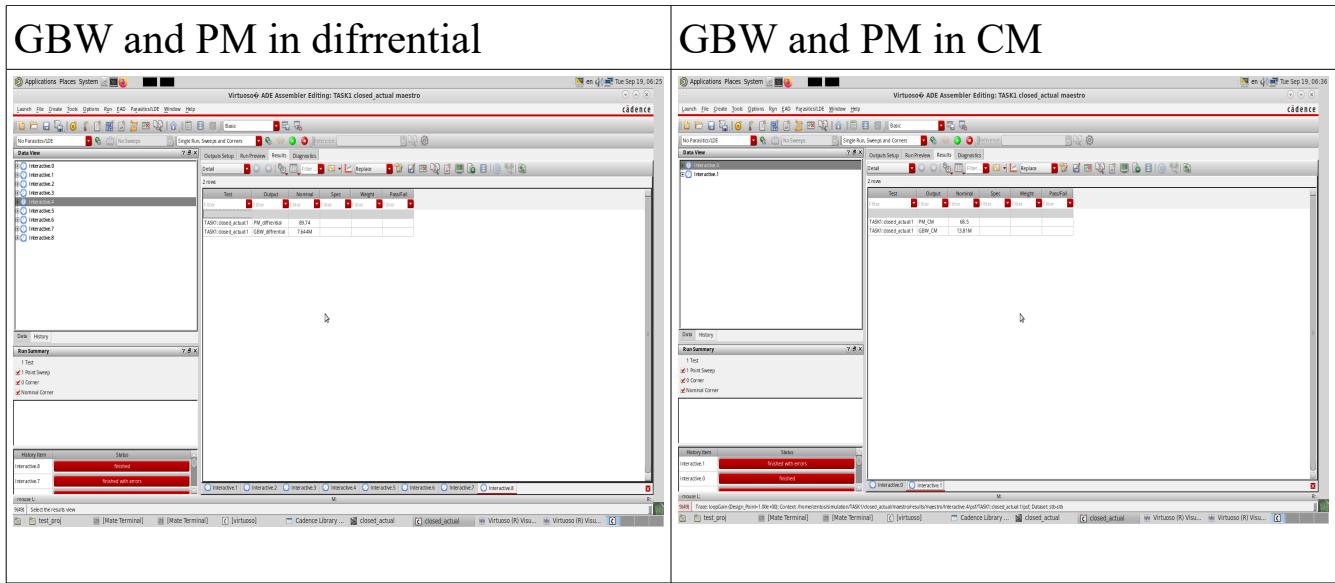
loop gain in db(magnitude, phase) VS frequency(differential loop) :



loop gain in db(magnitude, phase) VS frequency(CM loop) :



## compare:



CM and DIFF phase margin meets the spec (PM>70) but CMLOOP is slower (PM=99) due to the high due to the transistor with VCTRLP as an input which have high cap  
GBW\_diff is higher which means faster system.

## Compare:

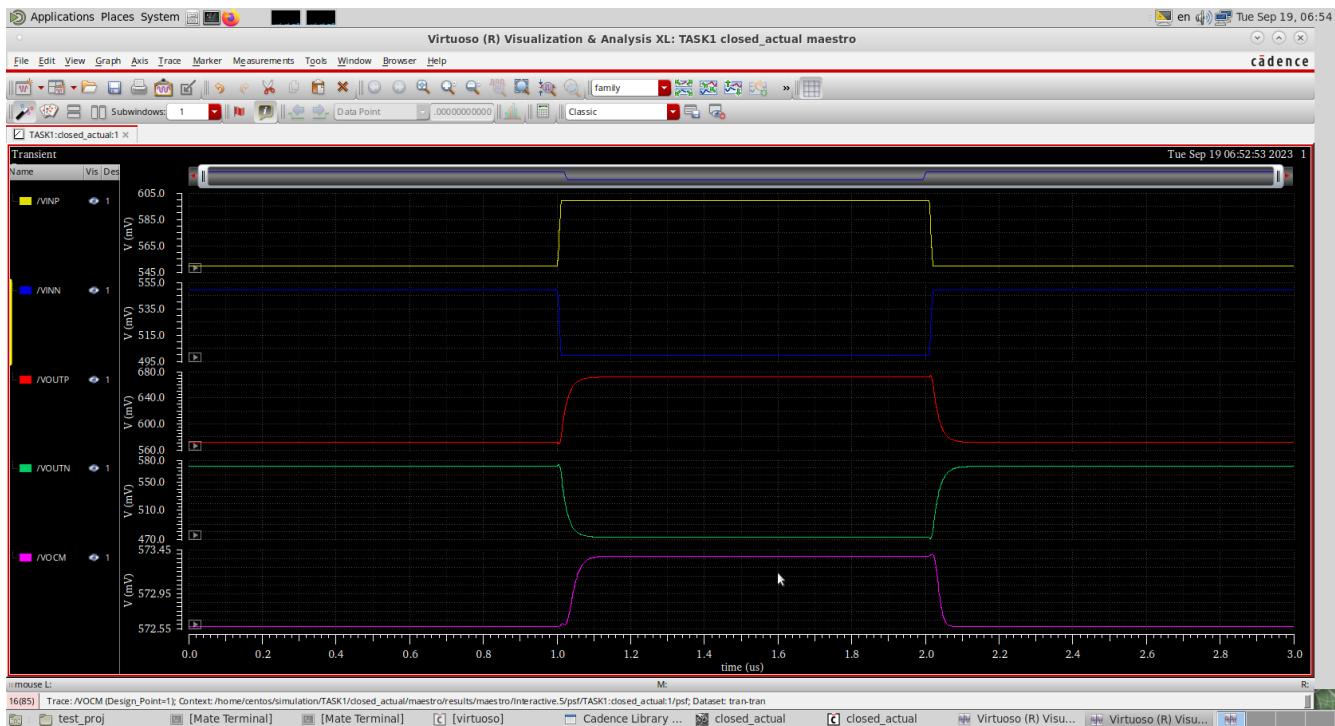
Open loop results	Closed loop results
DC LG = 1k	DC LG = 1.9K
GBW = 45.34M	GBW = 13.81M

LG decreased due to beta effect ( $\simeq 1/3$ ) , GBW decreased as the gain decreased.

## Part 6 (Closed loop simulation ( Transient analysis)):

### 1.differential and CMFB loops stability:

Plot ( **VINP** , **VINN** , **VOUTP** , **VOUTN** , **VOCM** ) vs time (differential loop):



No ringing

Both loops are staple, but over damped as Phase Margin is around 92°

## Plot ( VINP , VINN , VOUTP , VOUTN , VOCM ) vs time (CMFB loop):

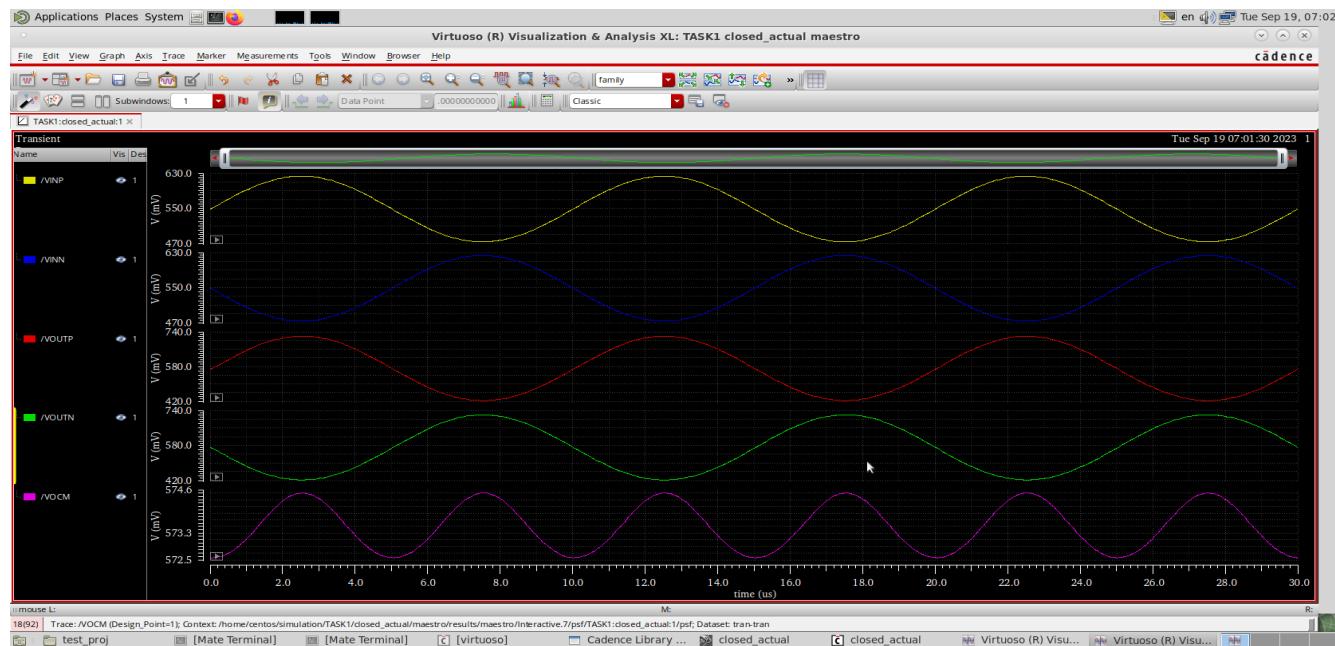


No ringing as phase margin is  $> 70^\circ$

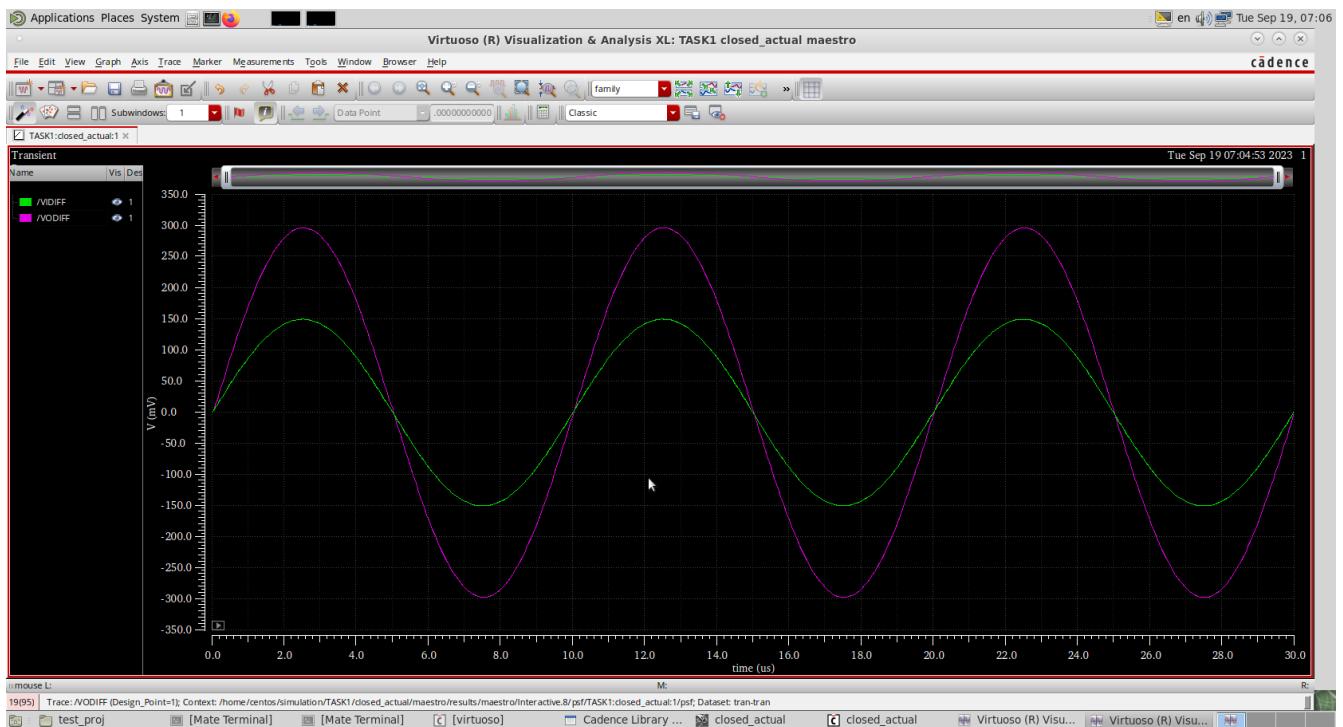
Both are stable, but over damped

## 2. Output swing:

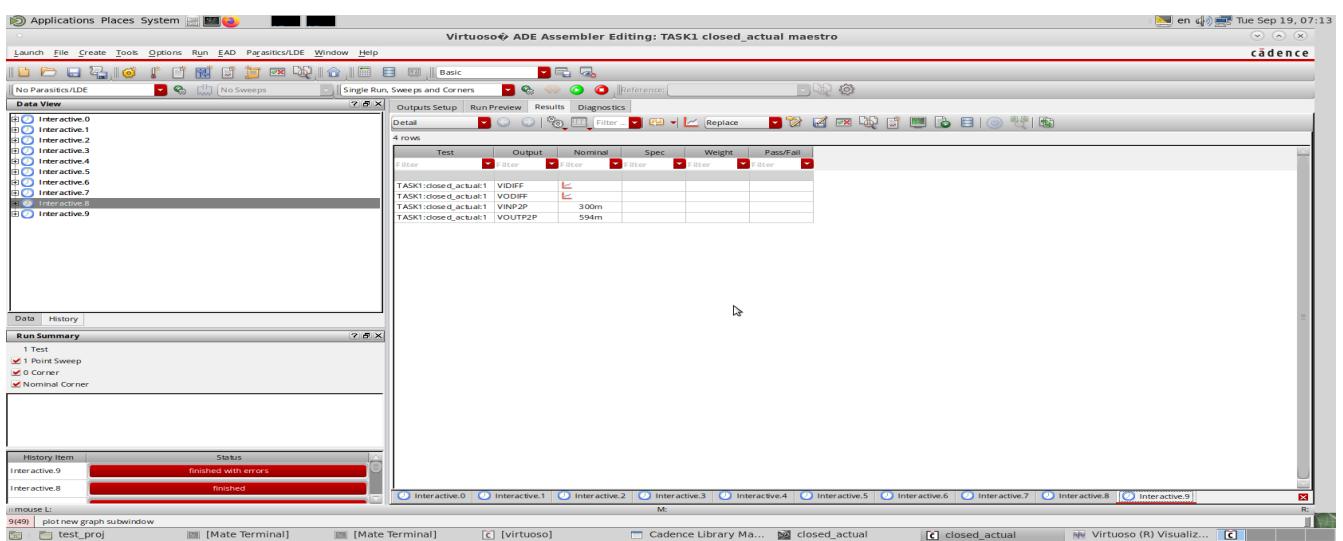
### Plot ( VINP , VINN , VOUTP , VOUTN , VOCM ) vs time :



## Plot (VIDIFF , VODIFF) vs time :



## calculations:



$$ACL = VOUTP2P / VINP2P = 594m / 300m = 1.98$$