



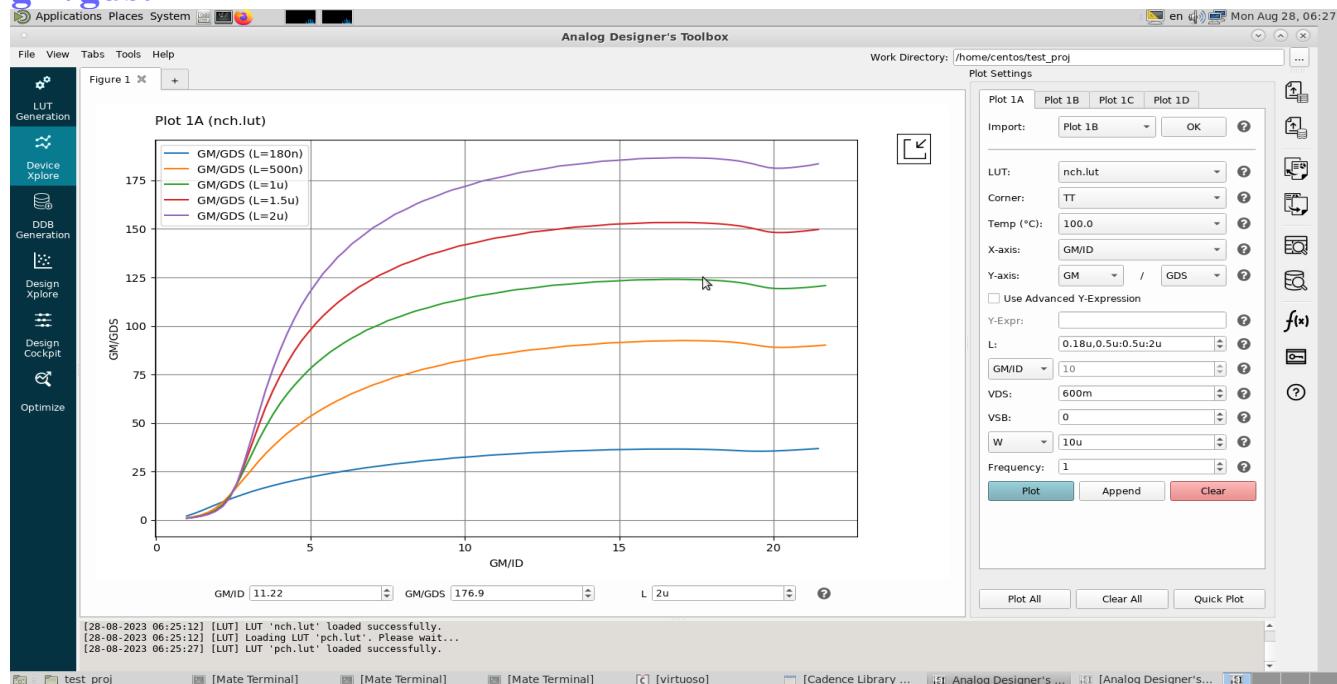
ANALOG IC DESIGN

LAB NO.9

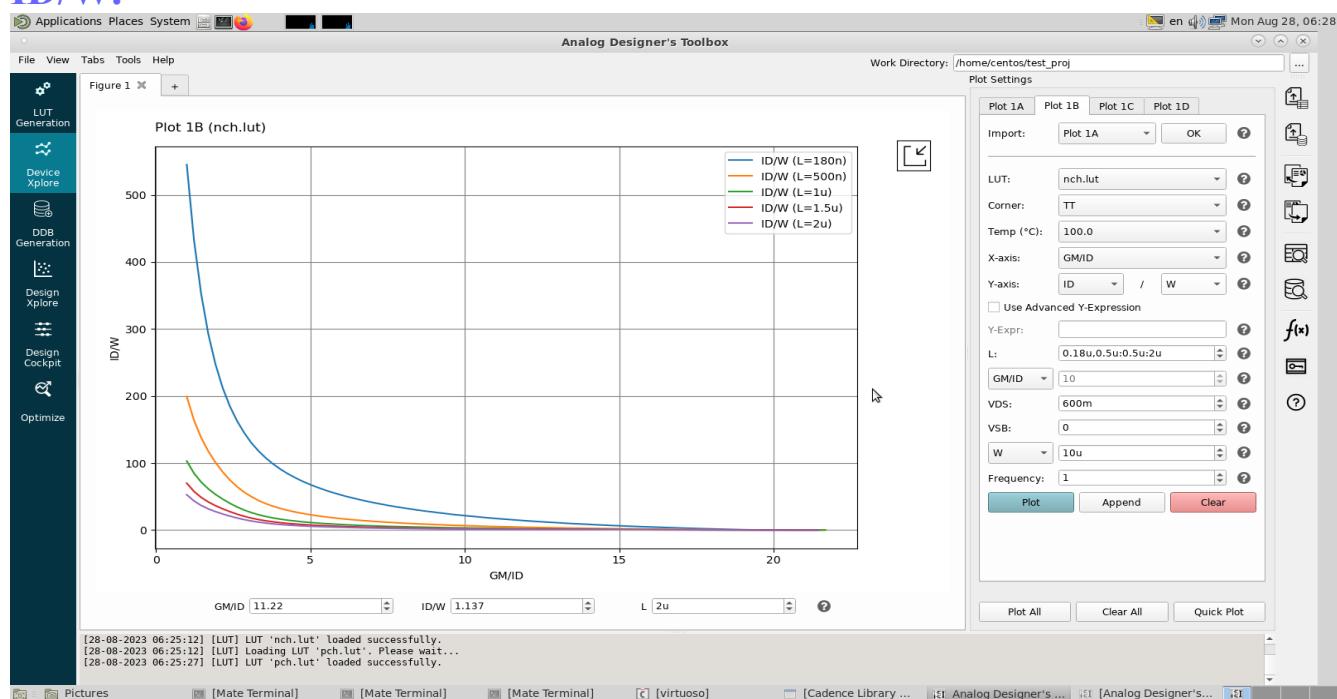
Part 1(gm/id design charts):

1.NMOS:

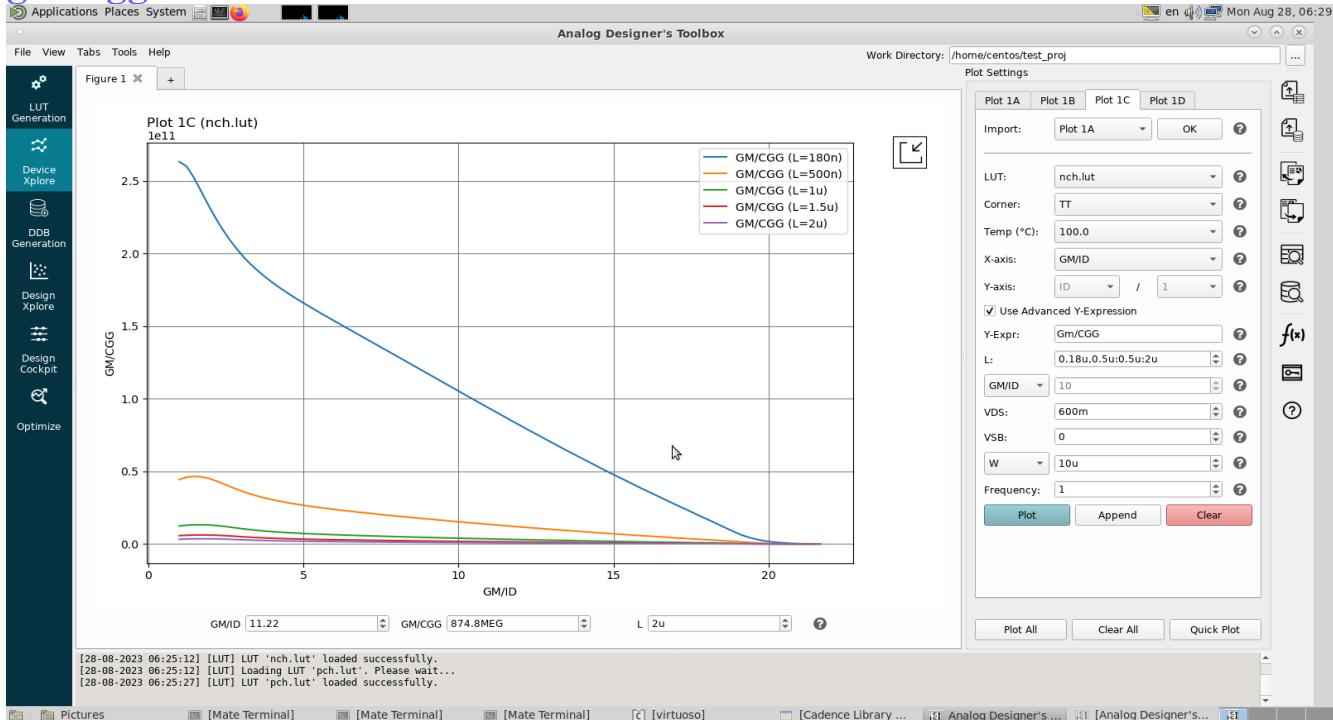
gm/gds:



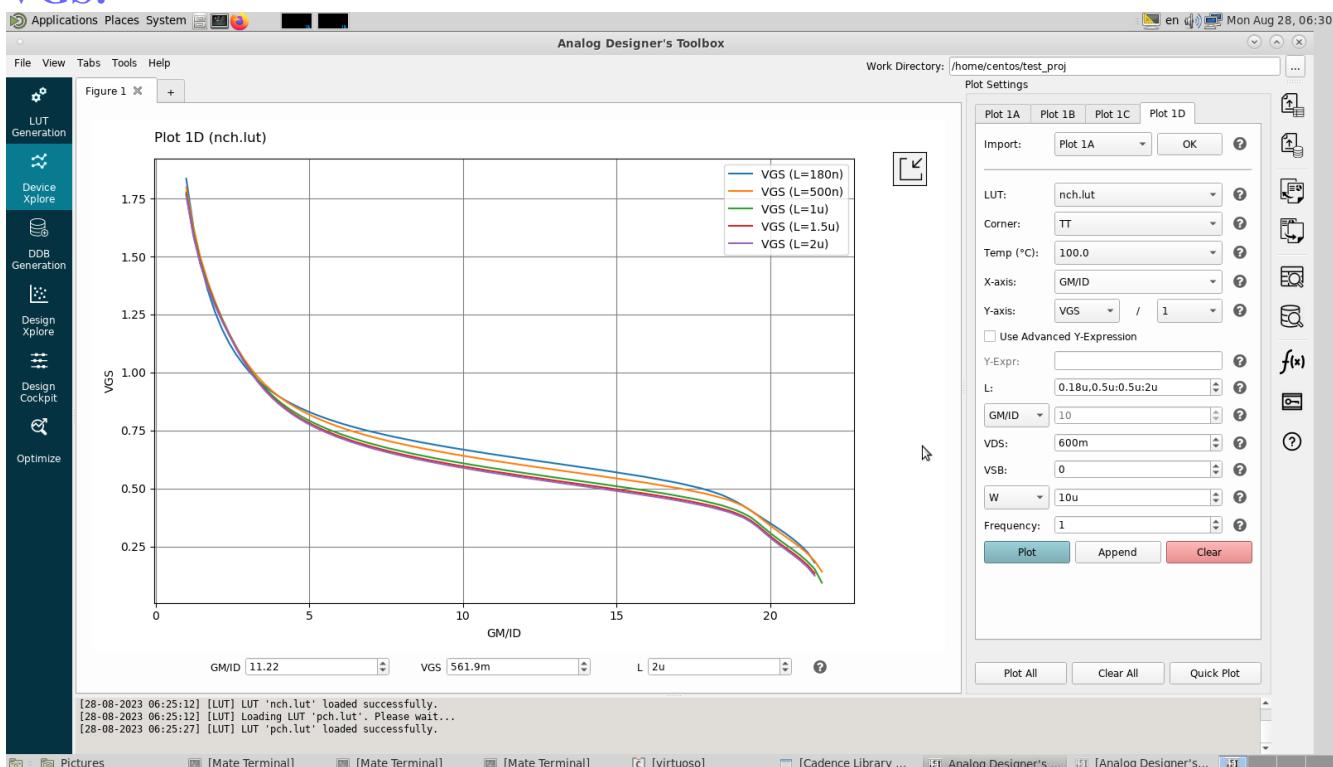
ID/W:



gm/Cgg:

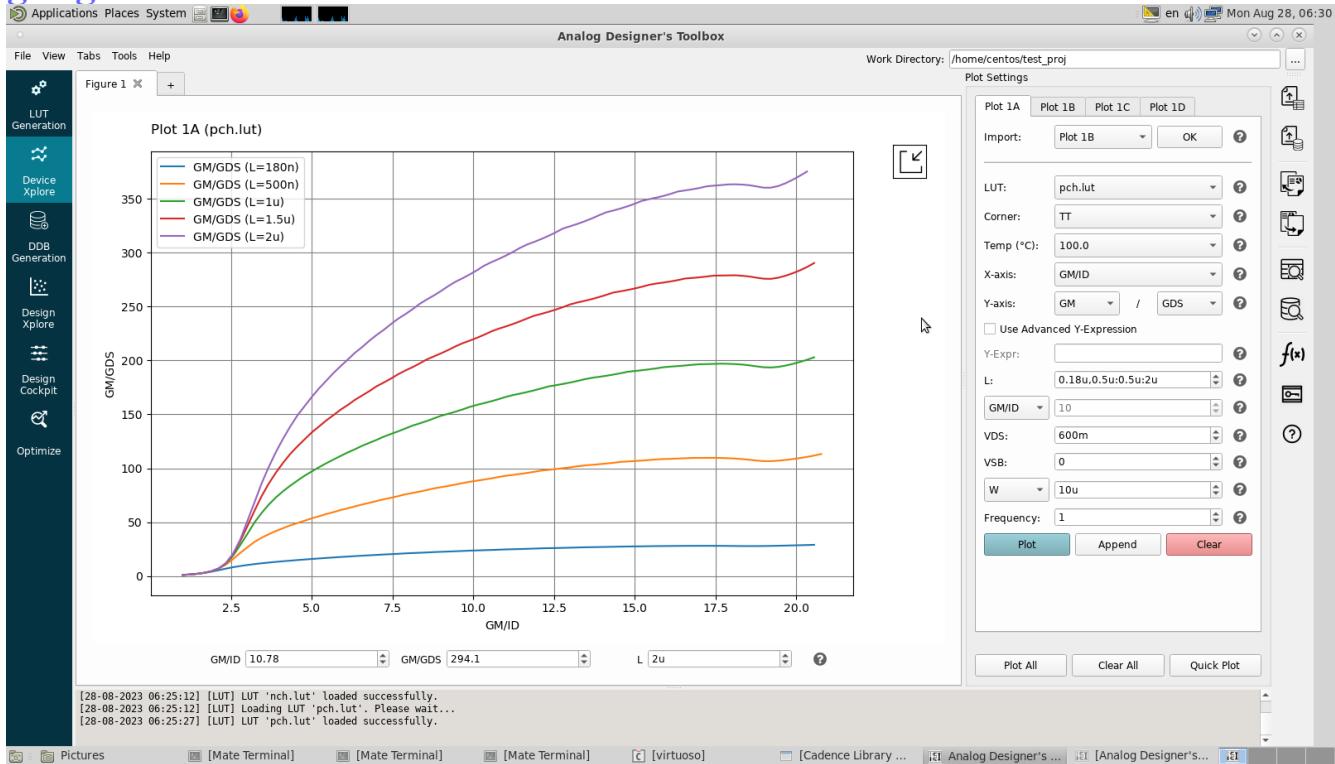


VGS:

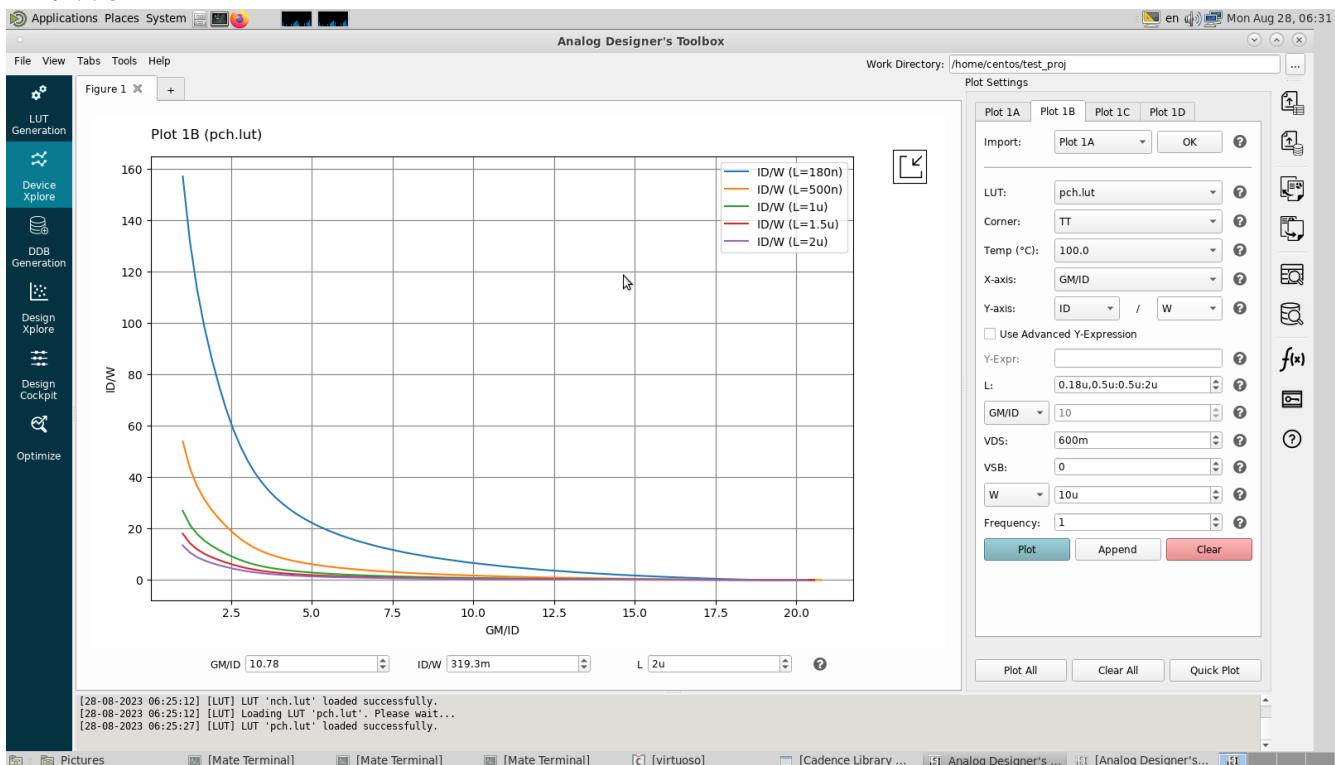


1.PMOS:

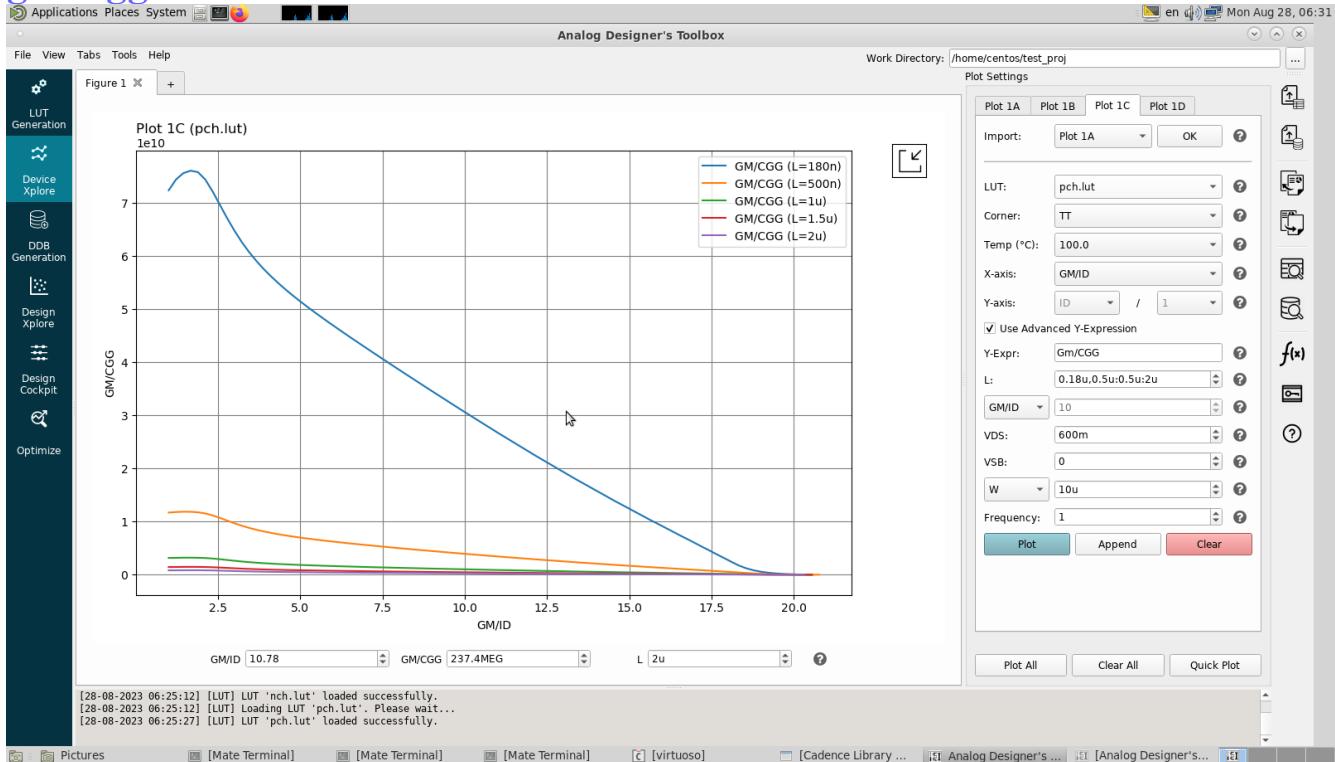
gm/gds:



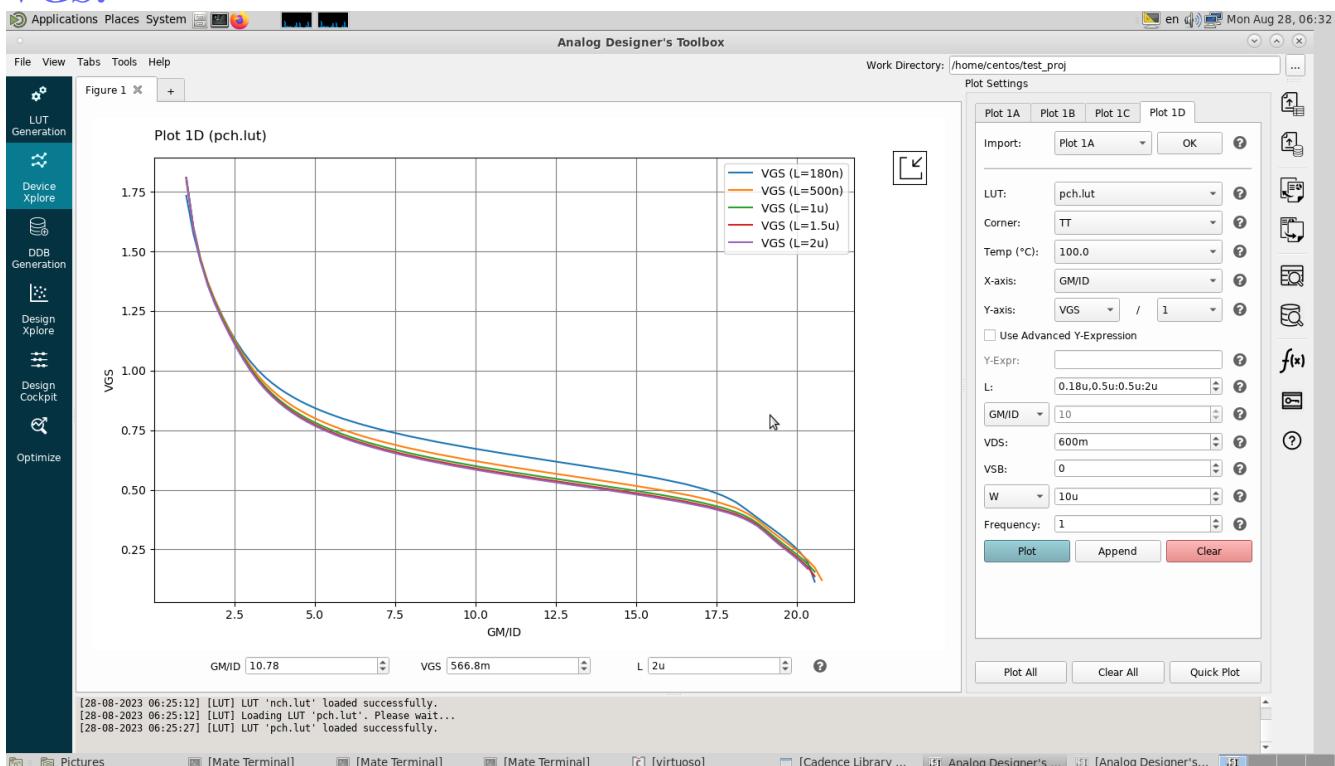
ID/W:



gm/Cgg:



VGS:



Part 2(OTA design):

1. SPECS required ,topolgy selection , givens and assumptions:

The desirable specs are :

Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Static gain error	<= 0.05%	<= 0.05%
CMRR @ DC	>= 74dB	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	<= 60uA	<= 60uA
CMIR – high	>= 0.6V	>= 1V
CMIR – low	<= 0.2V	<= 0.2V
Output swing	0.2 – 1V	0.2 – 1.6V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	<= 70ns
Slew rate (SR)	5V/μs	5V/μs

we will use a PMOS as input pair and tail current source mosfets in the first stage and NMOS as active current mirror load mosfets in the first stage and as input for the second stage

we assume VDS=0.6V in the first stage and VDS=0.9V in the second stage and VSB=0V

and we assume that the gain of the first stage is double the gain of the second stage

and some conclusions from the specs that $\beta=1$, $GBW=BW_{C1}$ and gm of 2nd stage =8 * gm of 1st stage

and some givens that $trise=2.2t$, $C_c=9.5CL$, $SR=IB_1/C_c$

2. Input pair for the first stage design :

hand analysis:

- ① $t_{rise} = 2.2 T = 2.2 \times \frac{1}{2\pi \times B_{Wd}} \leq 7 \text{ ns}$ $\Rightarrow B_{Wd} = 0.1 \times 10^6 \text{ Hz}$ $\Rightarrow B_{Wd} = 0.1 \times 10^6 \text{ Hz}$
- ② $G_B W = B_{Wd}$
 $\frac{g_{m1}}{2\pi C_c} = 5 \text{ MHz}$ $\Rightarrow g_{m1} = 5 \times 10^6 \text{ A/V}$
 $g_{m1} = 78.5 \times 10^{-6} \text{ A/V}$ $\Rightarrow g_{m1} = 78.5 \times 10^{-6} \text{ A/V}$ $\Rightarrow g_{m2} = 8 \times g_{m1}$
 $g_{m2} = 6.28 \times 10^{-6} \text{ A/V}$
- ③ $S.R. = \frac{I_{B1,2}}{C_c}$
 $S.V./M.S. = \frac{I_{B1}}{0.5 \times 10^{-12}}$
 $I_{B1} = 12.5 \text{ mA}$ (in every branch 6.25mA)
- ④ $\frac{g_m}{I_D} \geq \frac{78.5 \times 10^{-6}}{6.25 \times 10^{-6}} \geq 12.56 \approx 13$
- ⑤ $\frac{1}{L_s} < 0.05\% \rightarrow L_s > 2000 \mu\text{m}$
 $1^{\text{st}} \text{ stage gain} > 63$ \times $2^{\text{nd}} \text{ stage gain} > 31.5$
- ⑥ $\frac{g_m}{2g_{ds}} > 63$
 $\frac{g_m}{g_{ds}} > 126 \approx 130$
- ⑦ From I_D , $\frac{g_m}{I_D}$, $\frac{g_m}{g_{ds}}$, V_{DS} , V_{SB} we
get (W) , L and N_{GS} from SA

simulation results:



$W=8.82\mu$ $L=910n$ $VGS=560.9mV$

3. second stage input design :

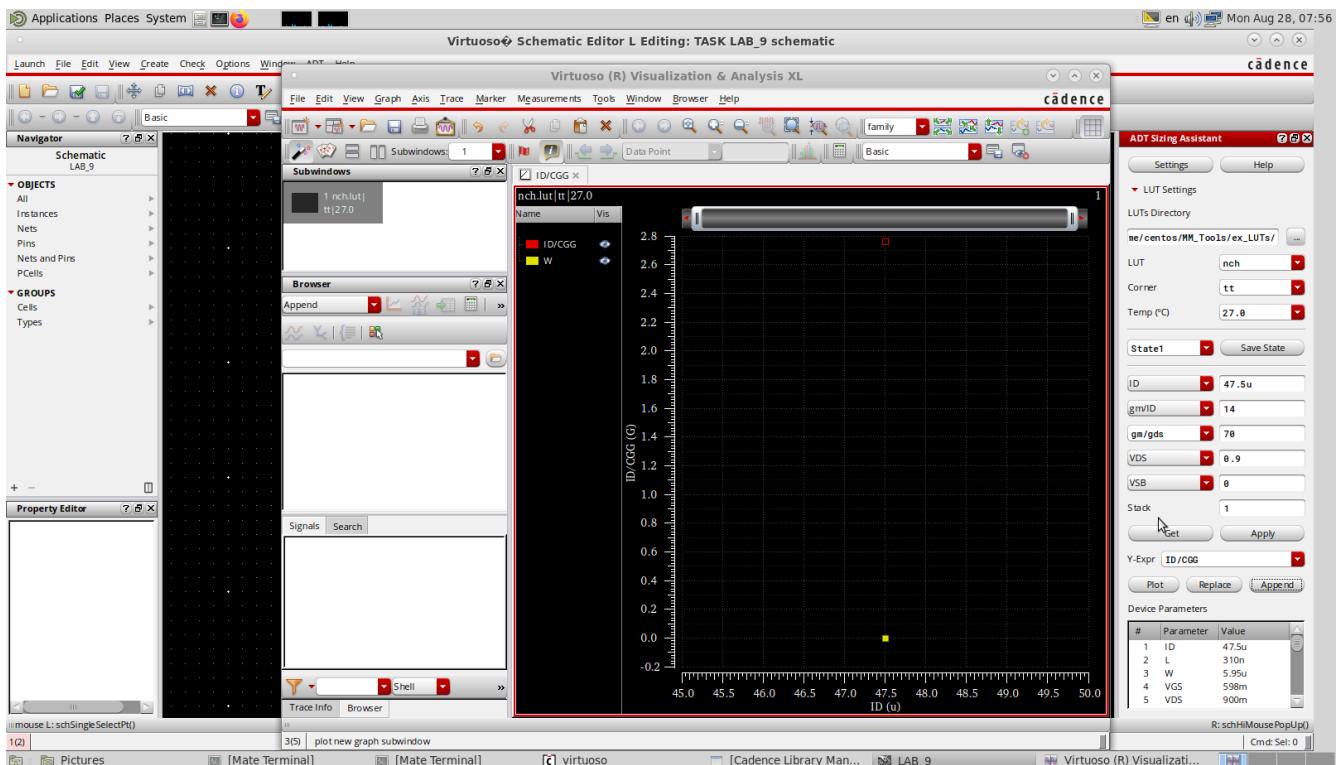
hand analysis:

① $\frac{gm}{2} \geq 6.28 \times 10^{-4}$ $\Rightarrow \frac{gm}{ID} = 13.22$ $\Rightarrow \frac{gm}{ID} \geq 13.22$ $\Rightarrow [14] \times [8]$

② $\frac{gm}{2gds} \geq 31.5$ $\Rightarrow \frac{gm}{gds} \geq 63$ $\Rightarrow \frac{gm}{gds} = 70.3$ $\Rightarrow \frac{gm}{gds} \geq 70.3$

③ From ID , $\frac{gm}{ID}$, $\frac{gm}{gds}$, VDS , VSB we get (W) , (L) and (VGS) from SA

simulation results:



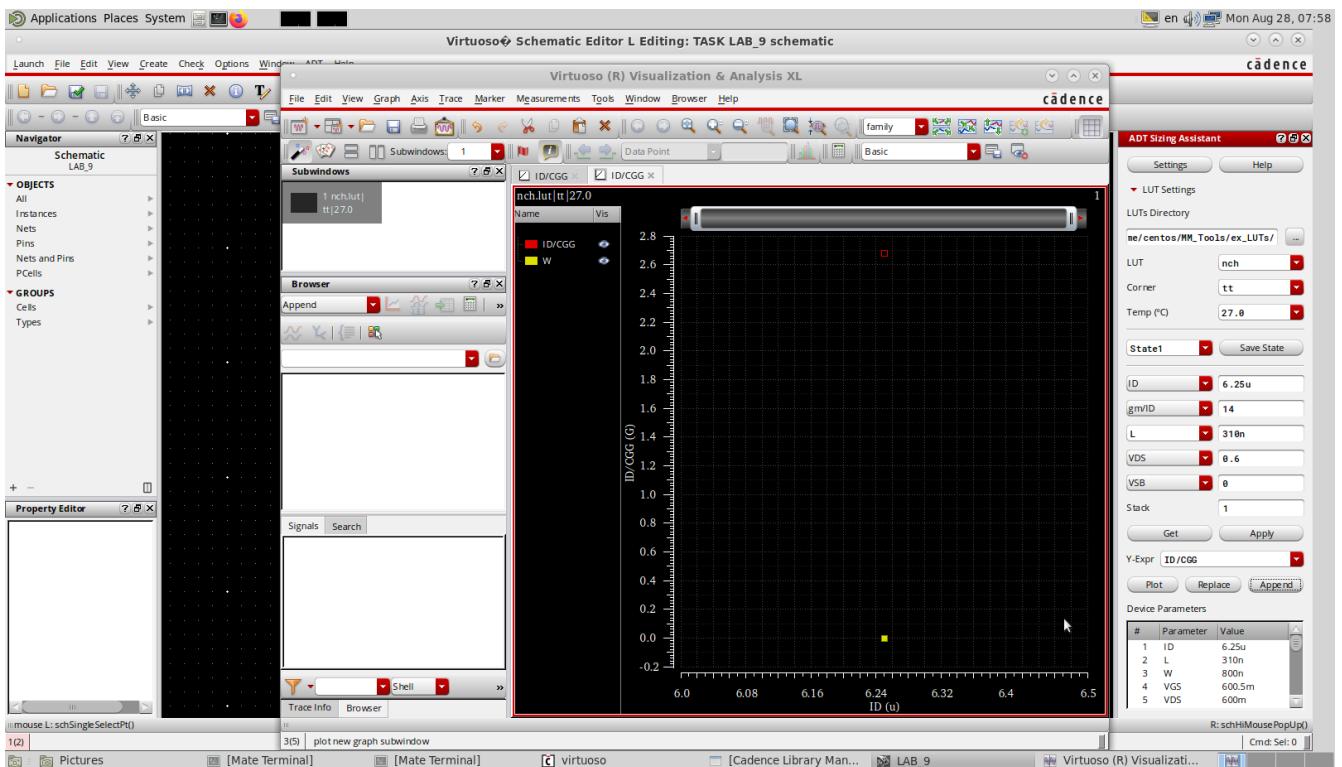
$W=5.9\mu$ $L=310n$ $VGS=900mV$

4. first stage active load design :

hand analysis:

- ① The first Stage active load must have the same L and $\frac{gm}{ID}$ of the input transistor of the second stage to make Systematic offset equal to zero
- ② by $L=310n$, $\frac{gm}{ID}=14$, $ID=6.25mA$ and VDS , V_{SB} we get W and V_{GS} from SA

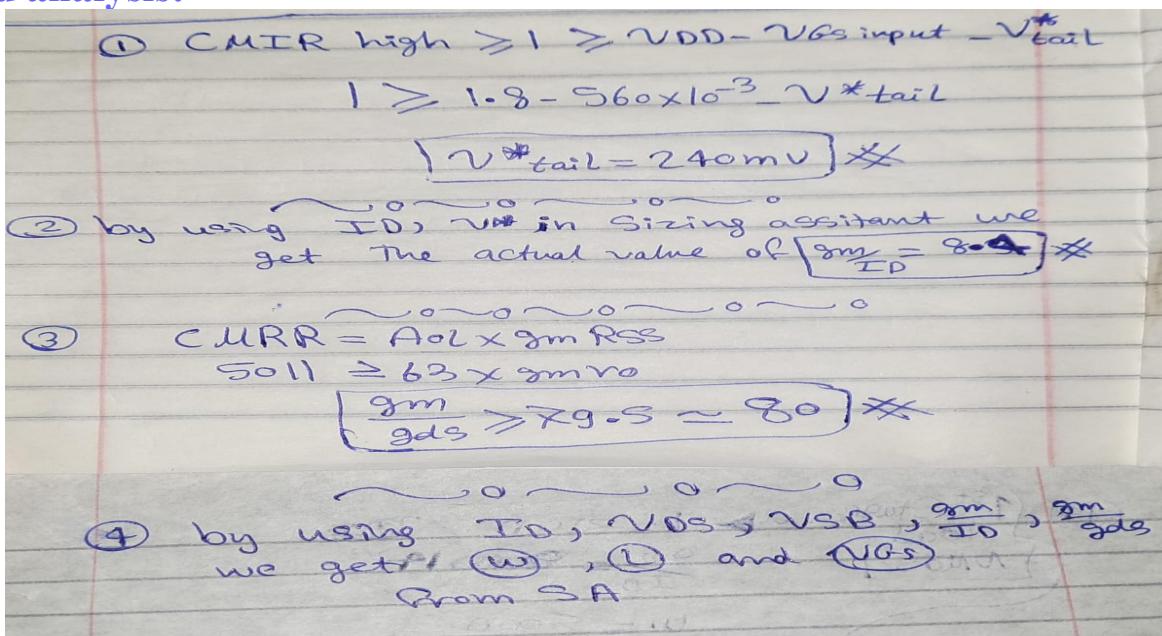
simulation results:



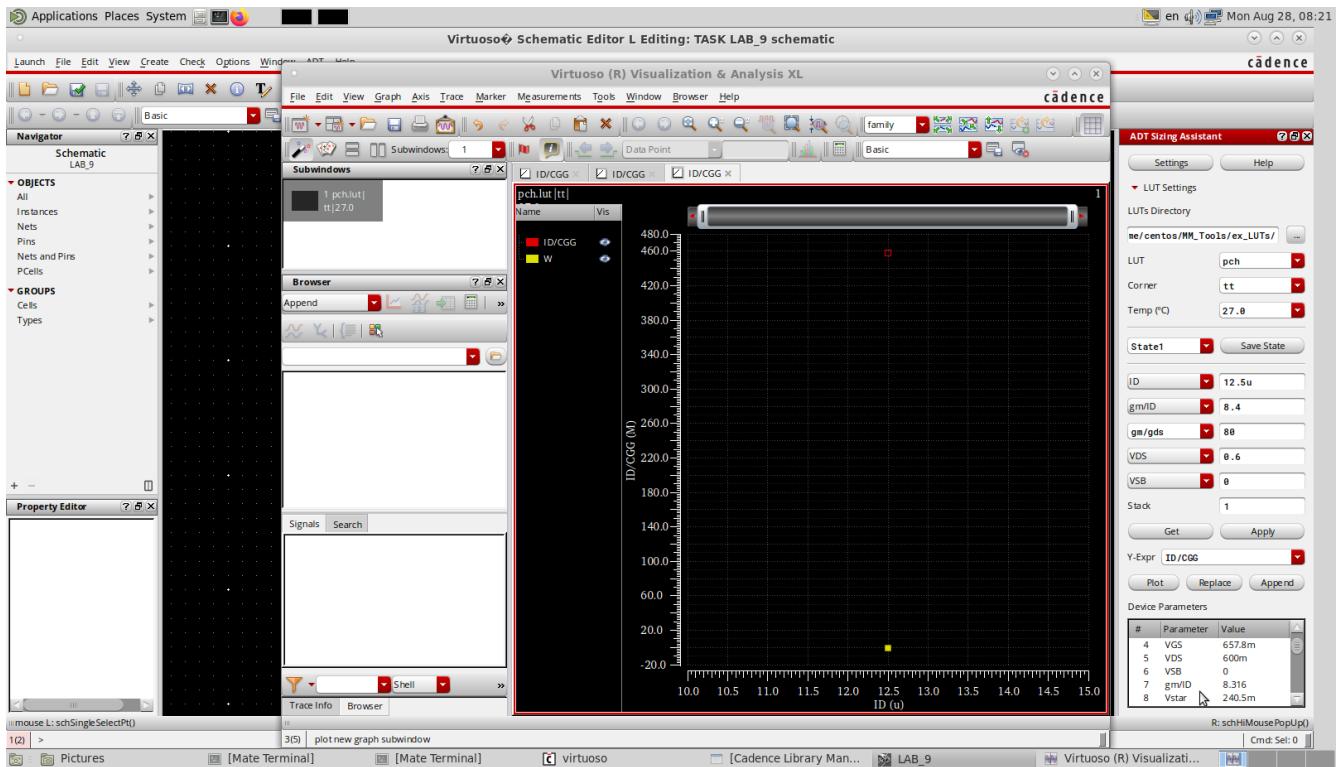
W=800n L=310n VGS=600mV

5. first and second stages tail current sources design :

hand analysis:



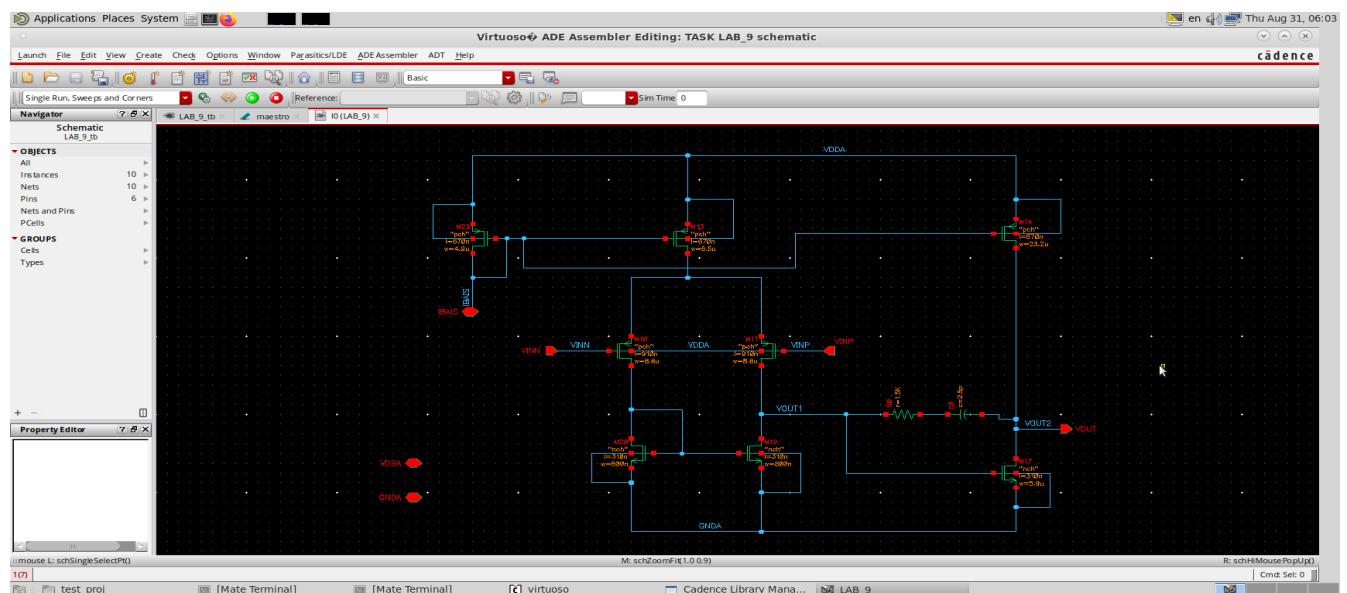
simulation results:

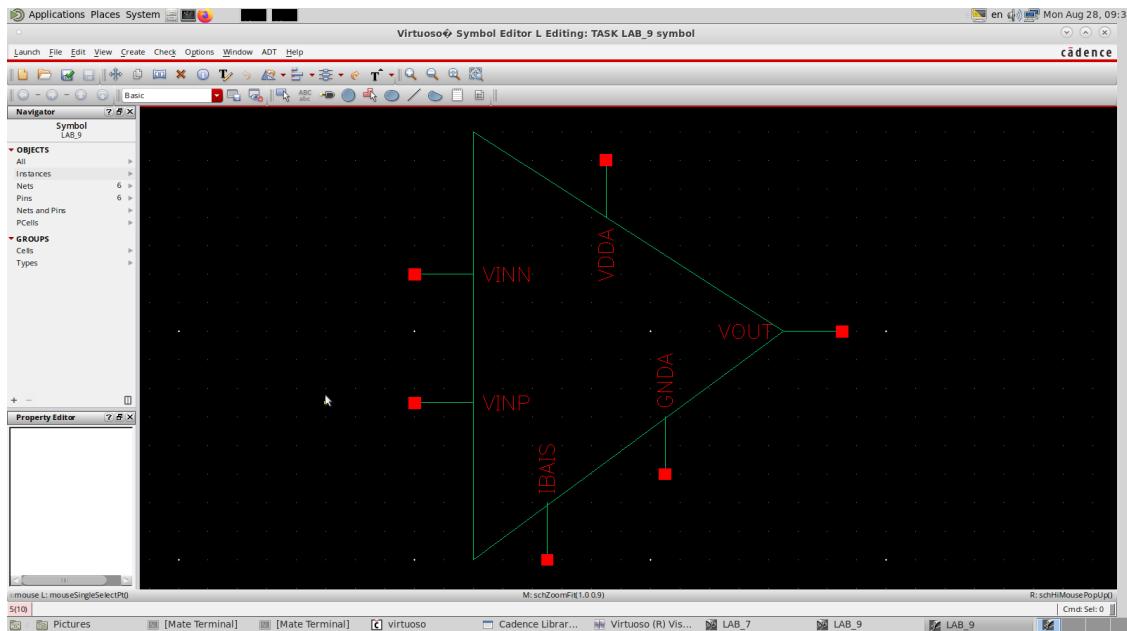


W= will get a different width for each one of the three tail current sources depending on the current flow in it with ID/W ratio by using SA and there sizing will be clear in the schematic. And some tuning will be made on them to get the desirable slew rate.

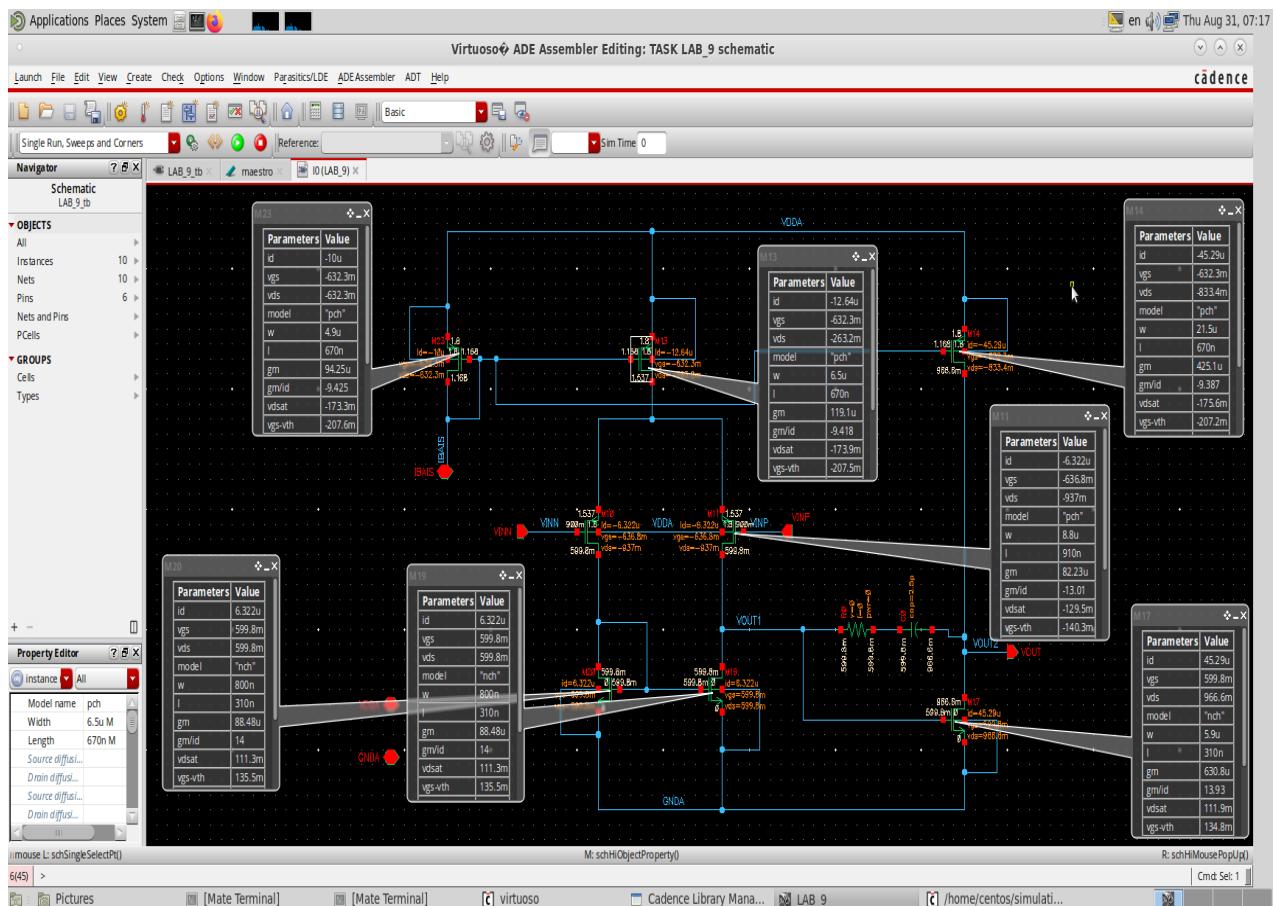
L=670n VGS=657.8mV

Schematic:





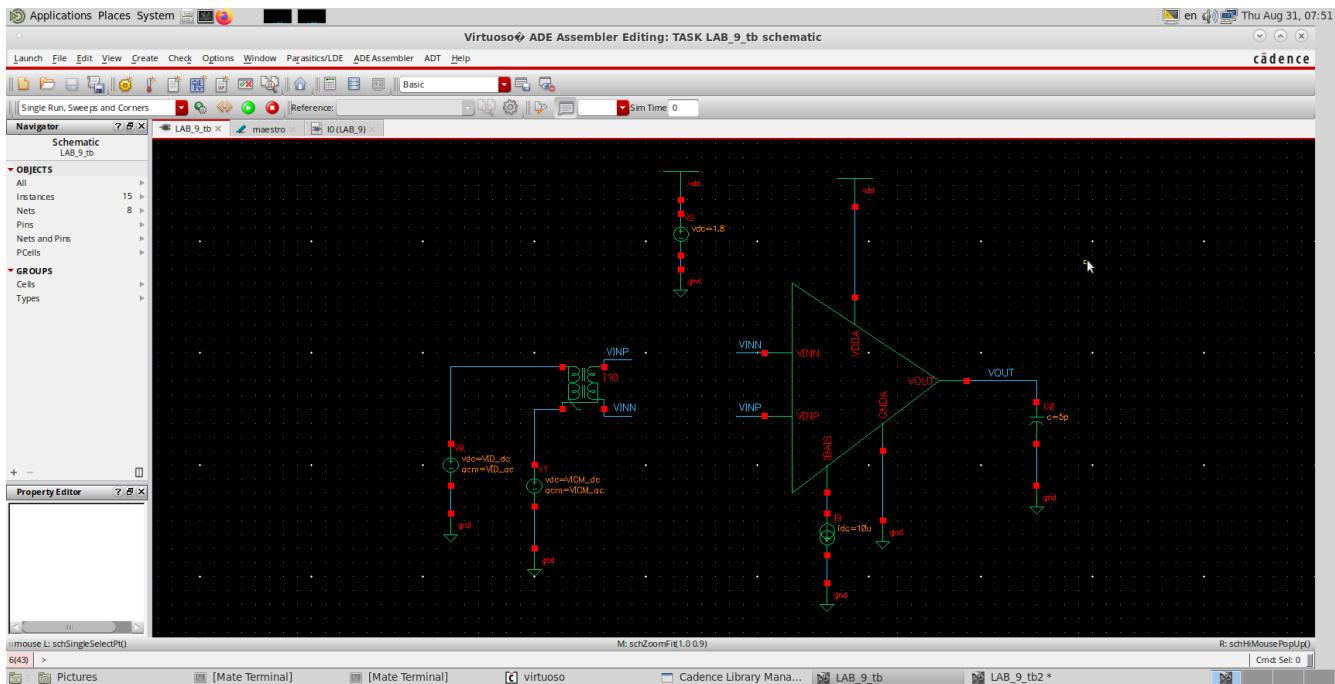
Conclusion:



	W	L	ID	gm/ID	Vdsat	Vov	V*
Positive input transistor	8.8u	910n	6.32u	13.01	129.5m	140.3m	153.7m
Negative input transistor	8.8u	910n	6.32u	13.01	129.5m	140.3m	153.7m
Right active load transistor	800n	310n	6.32u	14	111.3m	135.5m	142.8m
Left active load transistor	800n	310n	6.32u	14	111.3m	135.5m	142.8m
The main current mirror source transistor	4.9u	670n	10u	9.4	173.3m	207.6m	212.2m
The tail current source of 1 st stage transistor	6.5u	670n	12.64u	9.418	173.9m	207.5m	212.2m
The tail current current source of the 2 nd stage transistor	21.5u	670n	45.29u	9.387	175.6m	207.2m	213m
Input for 2 nd stage tarsistor	5.9u	310n	45.29u	13.9	111.9m	134.8m	143.6m

Part 3(open loop OTA simulation):

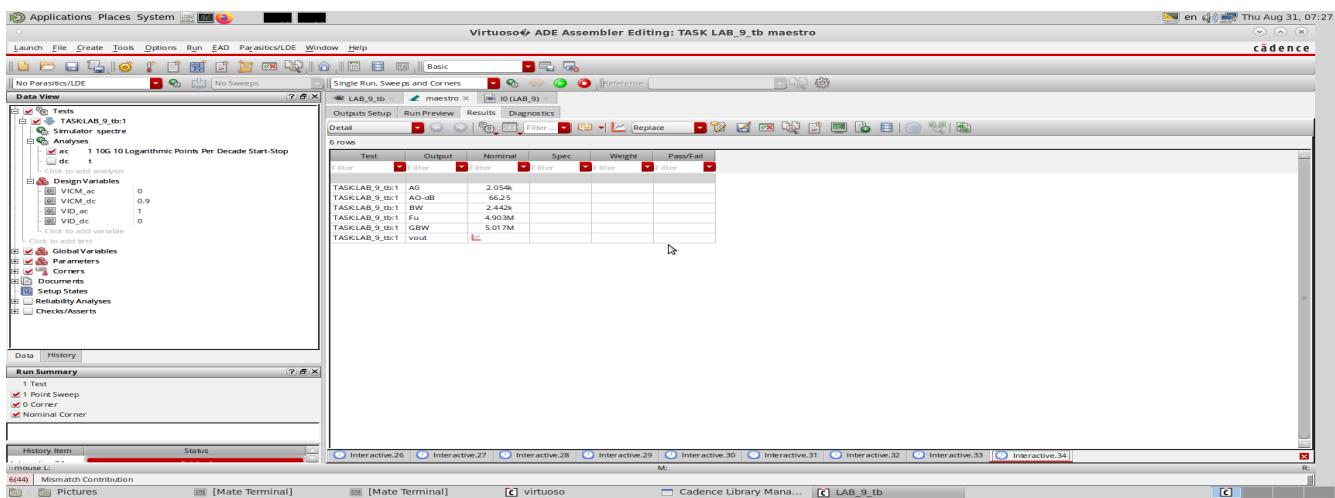
Schematic:



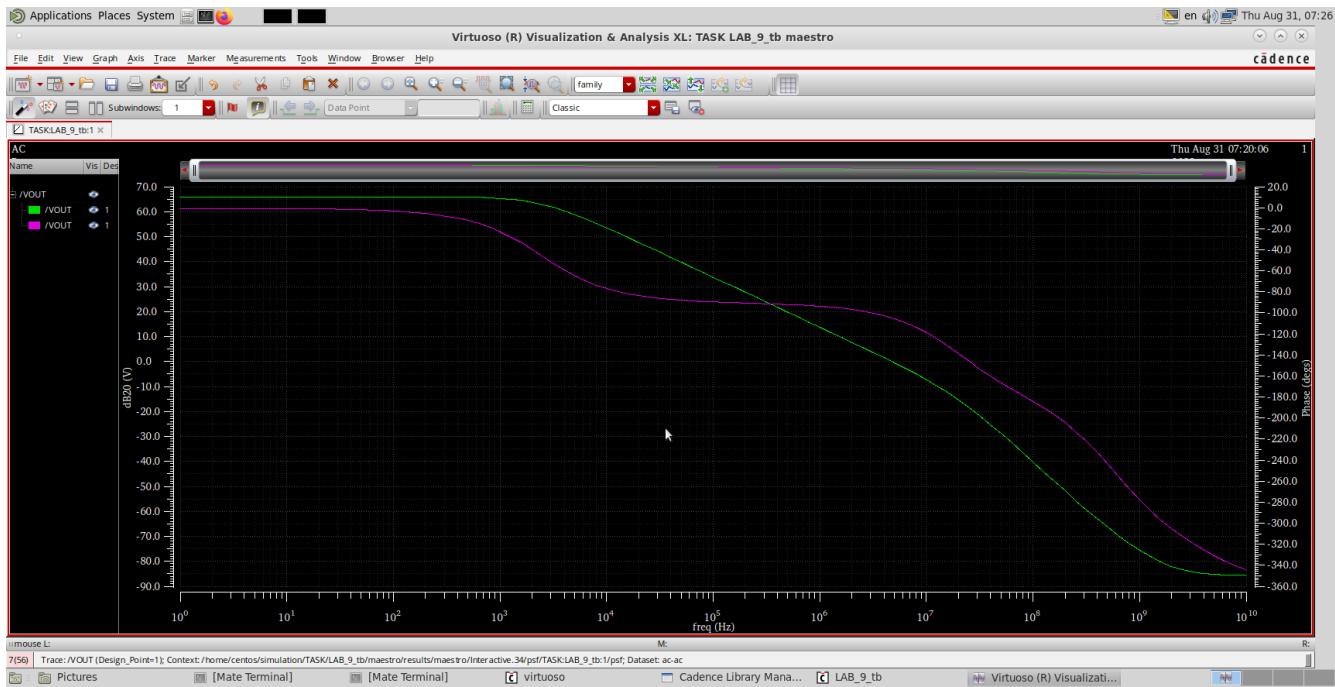
The current and gm in the input pair exactly equal as we have no mismatch
VOUT of 1st stage = 599.98mV as Vout folloe VF
VOUT if 2nd stage = 966.6mV as it is the middle of the output swing

1.diff small signal ccs:

Calculations:



Diff gain in db(magnitude, phase) VS frequency :



compare:

Simulation results	Hand analysis results
Avdiff= 66.25dB	$g_{m1st} = 81.25 \times 10^{-6}$ $\rightarrow g_{m2nd} = 66.5 \times 10^{-6}$
BW=2.442K	$r_{o, input} = \frac{1}{g_{ds, input}} = 1.6 \times 10^6$
GBW=5.01M	$r_{o, input \oplus} = \frac{1}{g_{ds, input \oplus}} = 105.3 \times 10^3$

$$\begin{aligned}
 r_{o, active \oplus} &= \frac{1}{g_{ds, active \oplus}} = 80.4 \times 10^3 \\
 r_{o, tail \oplus} &= \frac{1}{g_{ds, tail \oplus}} = 984.6 \times 10^3 \\
 r_{o, tail \ominus} &= \frac{1}{g_{ds, tail \ominus}} = 120 \times 10^3
 \end{aligned}$$

~~~~~ o ~~~~~ o ~~~~~ o ~~~~~ o

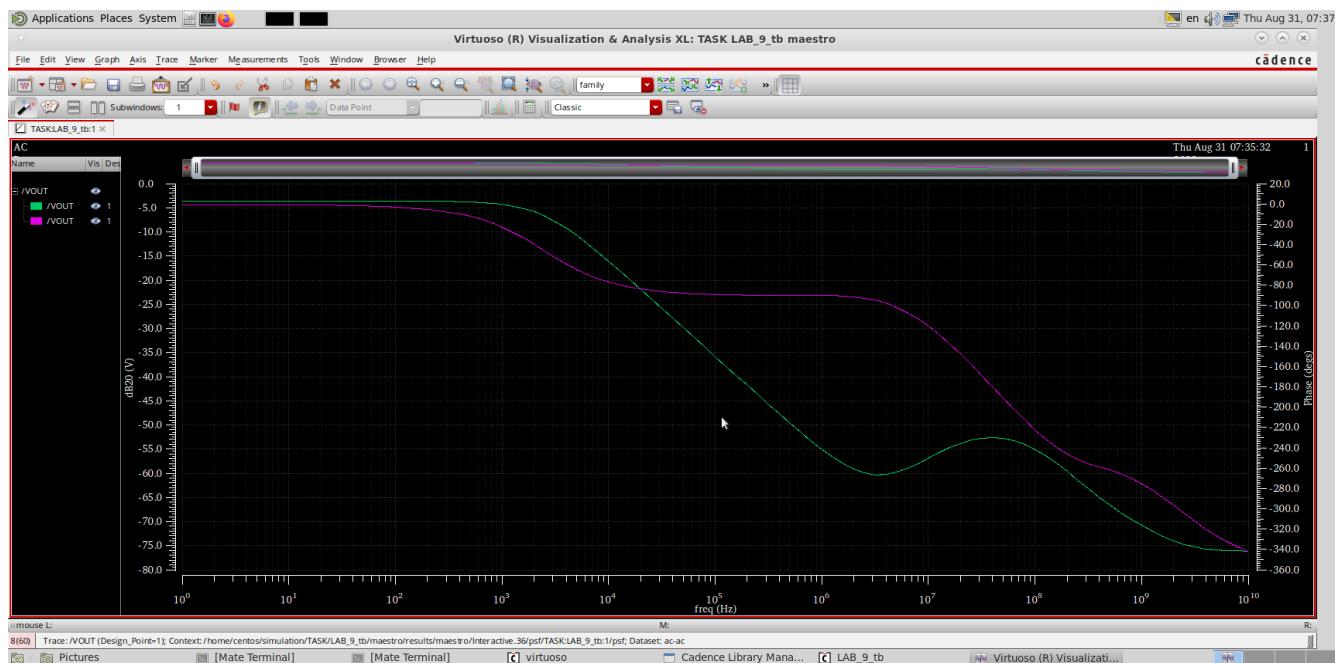
$$\textcircled{1} \text{ AV} = \left[ g_{m1st} \left( \frac{r_{o, input}}{r_{o, input \oplus}} \parallel r_{o, active \oplus} \right) \right] \times \left[ g_{m2nd} \left( \frac{r_{o, input}}{r_{o, input \oplus}} \parallel r_{o, tail \oplus} \right) \right] = 2200 \rightarrow 67 \text{ dB}$$

$$\textcircled{2} \text{ BW} = \frac{1}{2\pi g_{m2nd} (r_{o, input} \parallel r_{o, active}) \times (r_{o, input} \parallel r_{o, tail}) \times \alpha} = 2 \text{ kHz}$$

$$\textcircled{3} \text{ GBW} = A \times \text{BW} = 2200 \times 2 \text{ kHz} = 4.4 \text{ MHz}$$

## 2.CM small signal ccs:

CM gain in db(magnitude, phase) VS frequency :



compare :

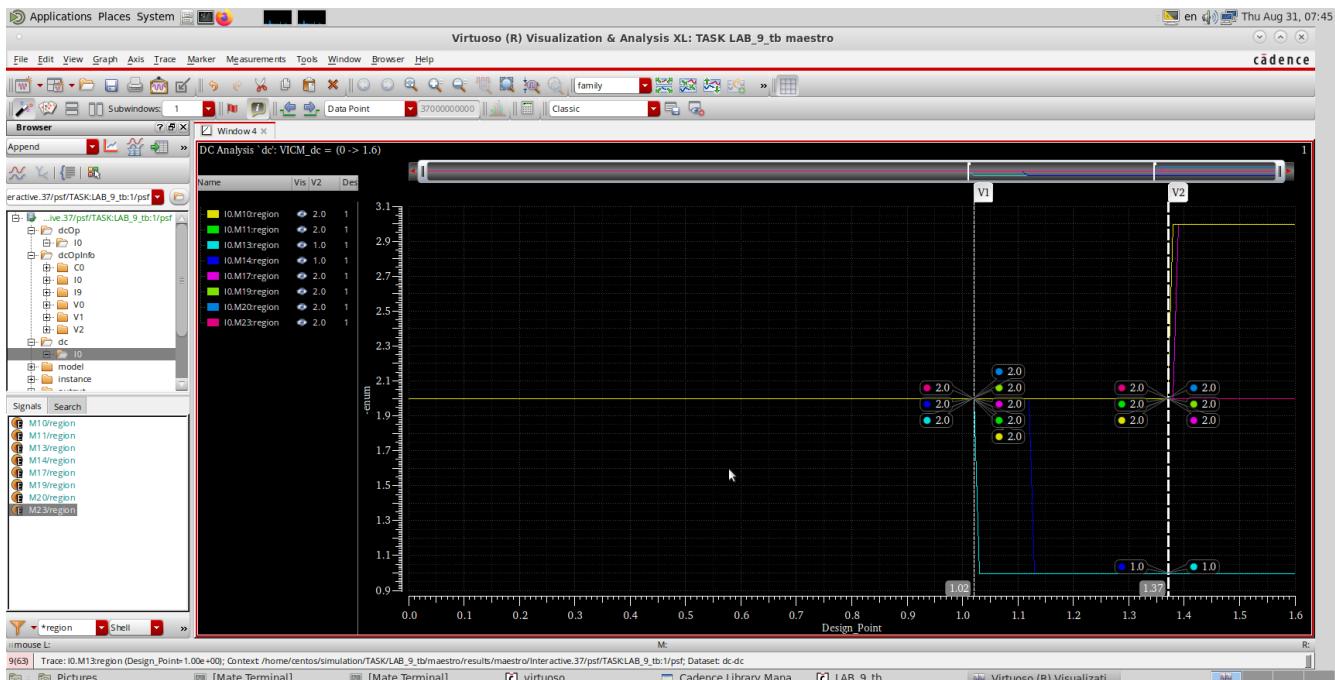
| Simulation results | Hand analysis results                                                                        |
|--------------------|----------------------------------------------------------------------------------------------|
| Avcm = -5dB        | $AVCM = \frac{g_{m2nd}/g_{m1st}}{1 + 2 \times g_{m1st} \times R_{load}}$ $= -5.8 \text{ dB}$ |

### 3.CM large signal ccs (region vs VICM):

#### region vs VICM:



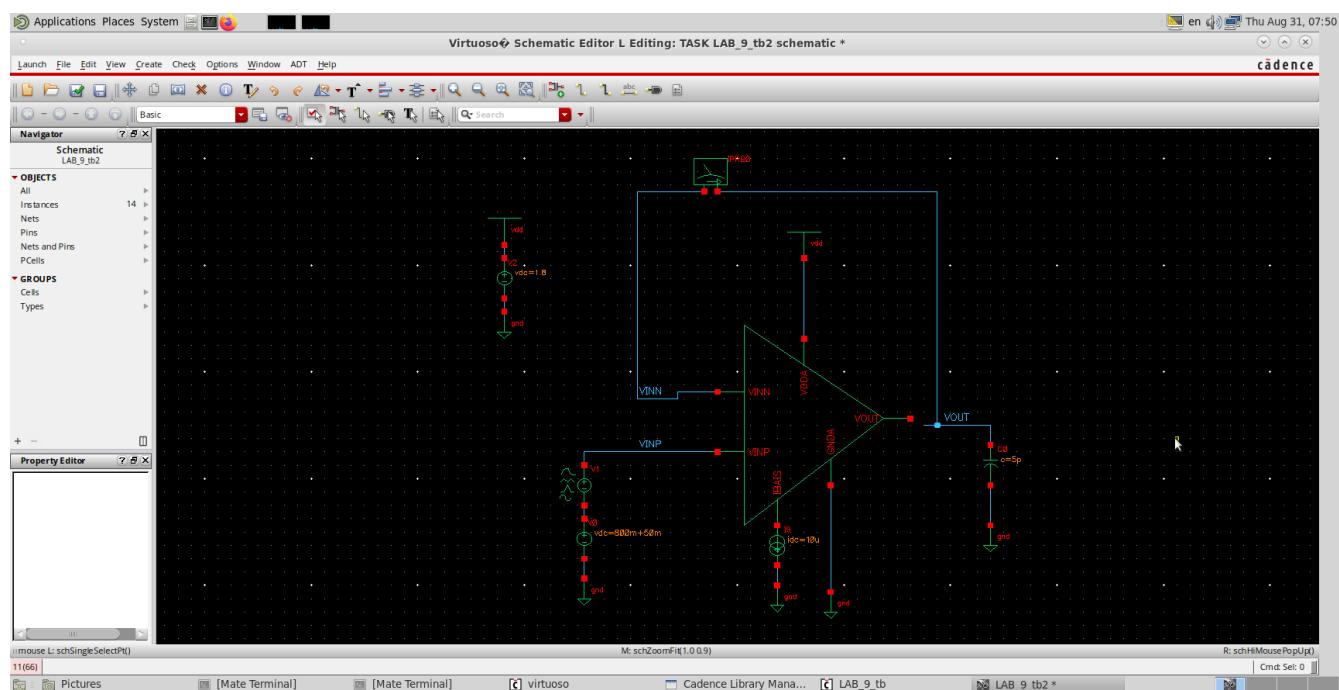
compare :



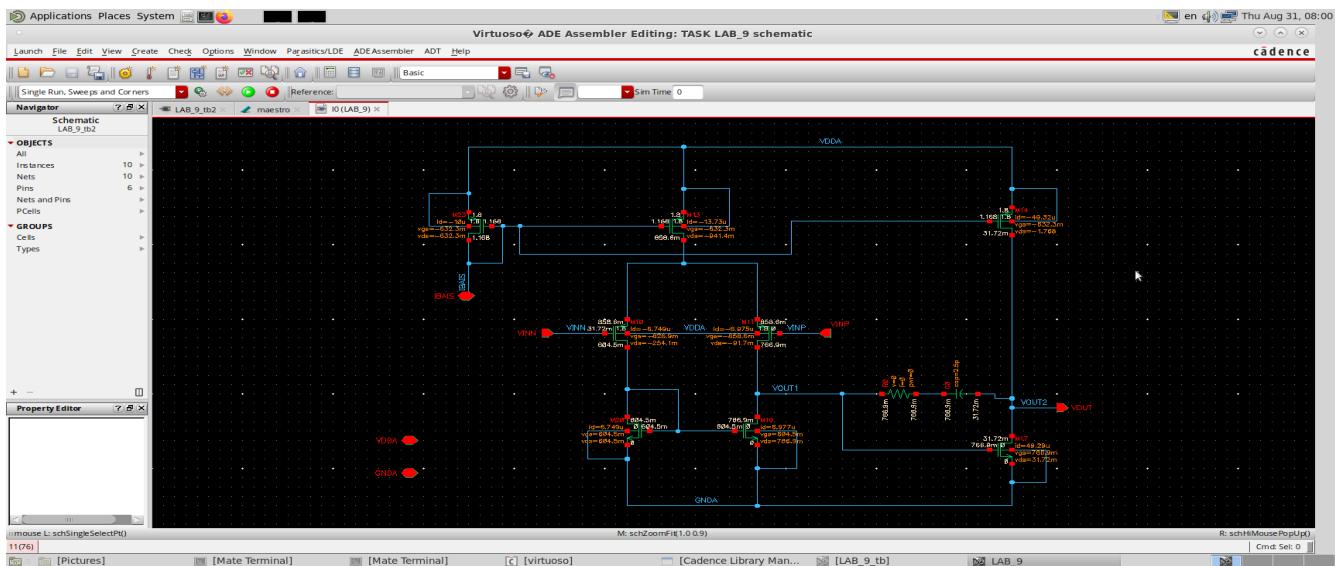
| Simulation results     | Hand analysis results                                                                                                                                                                                  |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CMIR=1.37-->1.02=0.35V | <p>CMIR: <math>\left[ V_{th_{input}} + V_{out\,input} + V_{out\,tail} \right] \rightarrow</math></p> $\left[ V_{DD} - V_{thp} - V_{out\,input} + V_{thn} \right]$ $1.1 \rightarrow 1.35 = 0.25 \times$ |

## Part 4(closed loop OTA simulation):

### Schematic:



## 1. DC op :



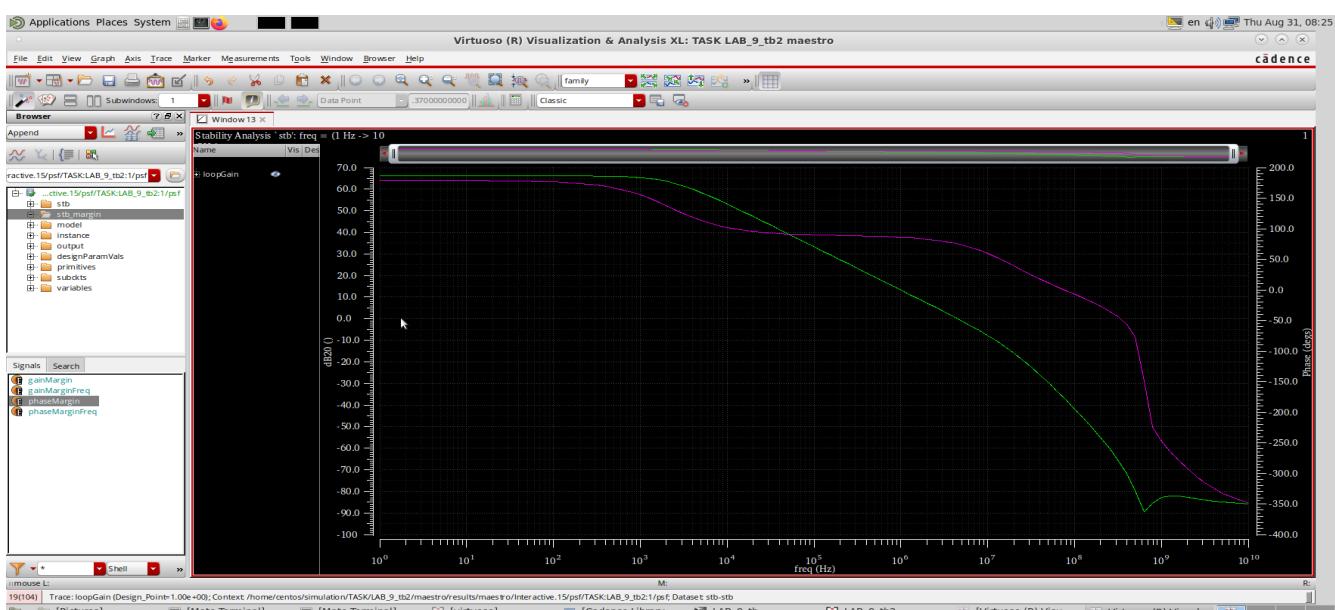
The DC voltages at the input terminals of the op-amp is not equal because feedback network

VOUT of 1<sup>st</sup> stage = 766.9mV not equal to the open loop simulation due to mismatch  
VOUT if 2<sup>nd</sup> stage = 31.72mV

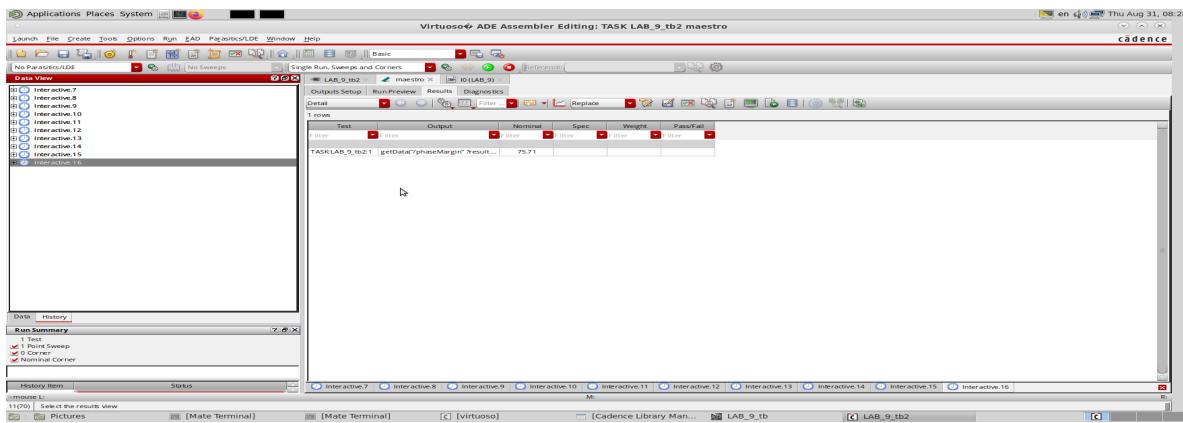
The current and gm in the input pair are not exactly equal due feedback

## 2. loop gain:

loop gain (magnitude and phase) VS frequency :



## Phase margin calculations:



## compare of PM simulation result with hand analysis results:

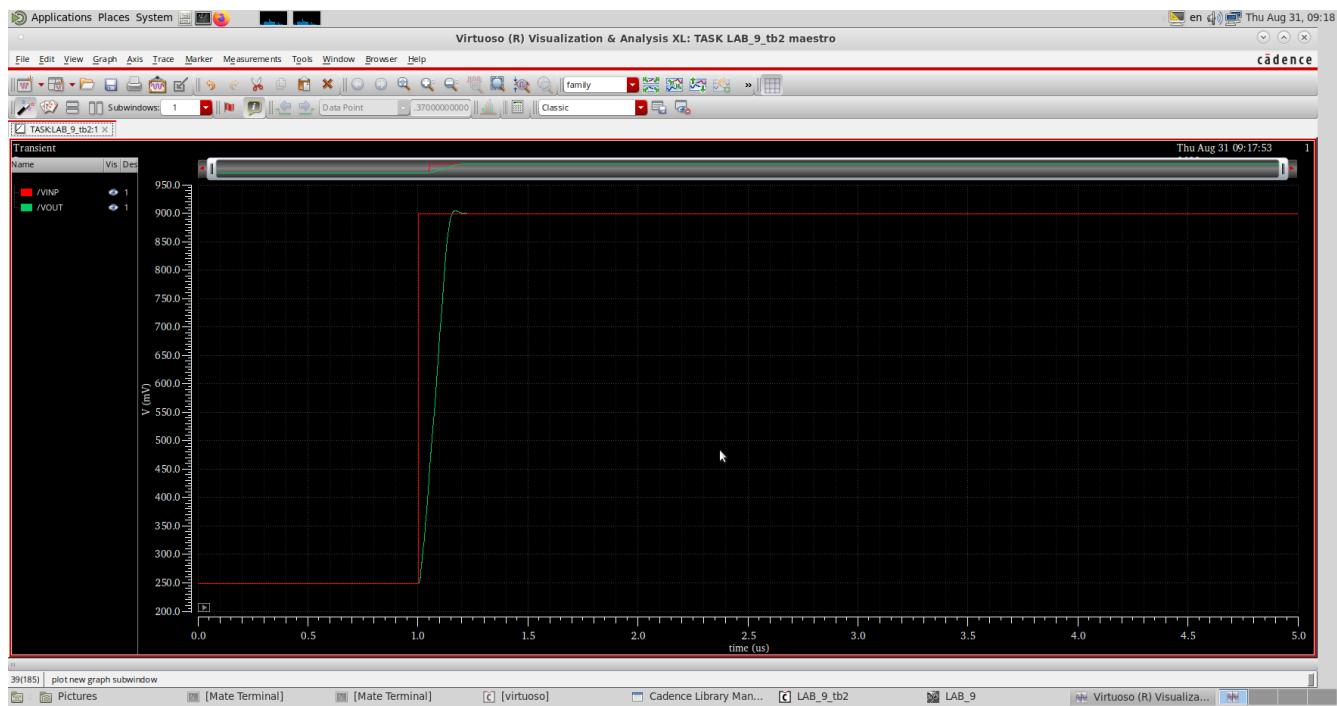
| Simulation results | Hand analysis results                                                                                                                                                                                                           |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 75.7               | <p>Handwritten notes on lined paper:</p> $wp_2 = \frac{g_m^{2nd}}{a} = 118.12$ $wp_1 = \frac{g_m^{1st}}{a} = 3.63$ $\frac{wp_2}{wp_1} = 3.25 \rightarrow \mu = 73^\circ$ <p><del><math>\sqrt{m_o A_s} = 118.12</math></del></p> |

## compare dc gain and GBW in closed loop and open loop :

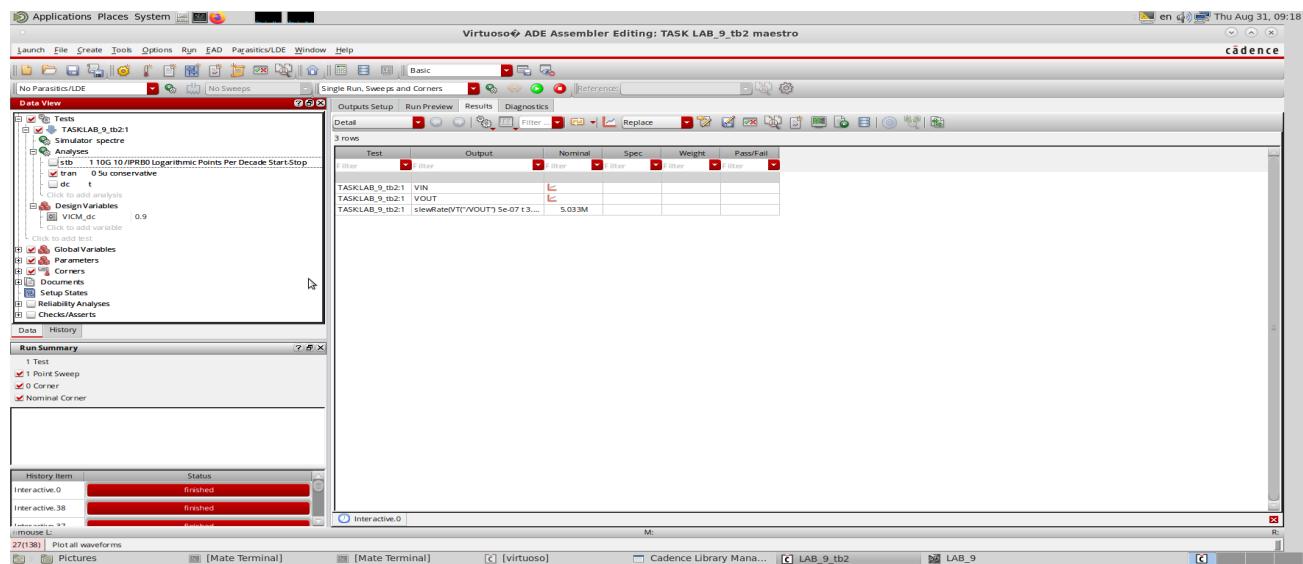
| Cloosed loop   | Open loop       |
|----------------|-----------------|
| Avdiff= 66.5dB | Avdiff= 65.75dB |
| GBW=5.01M      | GBW=5.01M       |

### 3.Slew rate:

#### VIN vs VOUT:



#### Slew rate calculations:



**compare :**

| Simulation results | Hand analysis results                                                                              |
|--------------------|----------------------------------------------------------------------------------------------------|
| SR=5.03M           | $SR = \frac{I_{B1}}{CC} = \frac{12.5 \times 10^{-6}}{0.5 \times 5 \times 10^{-12}} = 54 \text{ M}$ |

## 4.Settling time:

### Settling time calculations:



settling time is  $1.11956\mu - 992.12n = 127.4\text{ns}$

**compare :**

| Simulation results      | Hand analysis results                                                                                                                |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| settling time = 127.4ns | $\begin{aligned} \text{Settling time} &= 2 \cdot 2 \tau = 2 \cdot 2 \times \frac{1}{2\pi Bw_a} \\ &= 127.4 \text{ ns} \end{aligned}$ |