



# **ECE413: ASIC Design**

## **Project 2– MIPS16 PnR**

### **Team Members:**

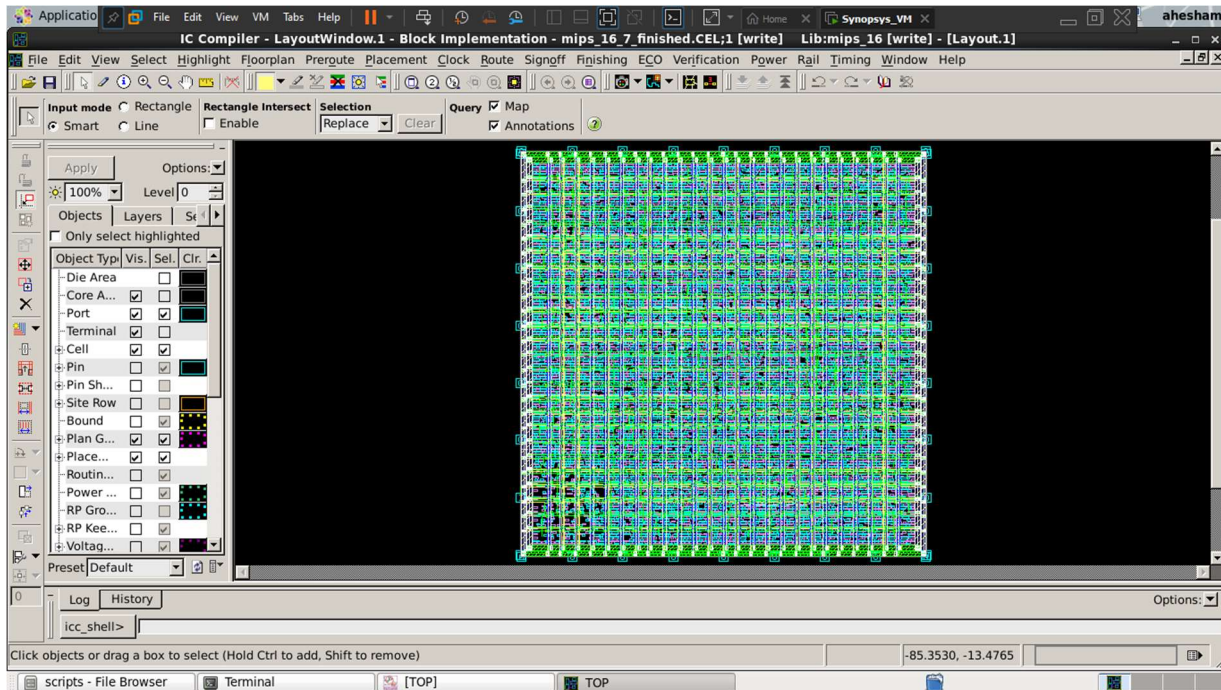
Amira Bahey Eldin Mahmoud	2000067
Rahaf Abdullah Atef Abdullah	2000099
Asmaa Abdelmotlb Yousseff	2000051
Abdallah Karim Motwea	2000993

### **Contribution:**

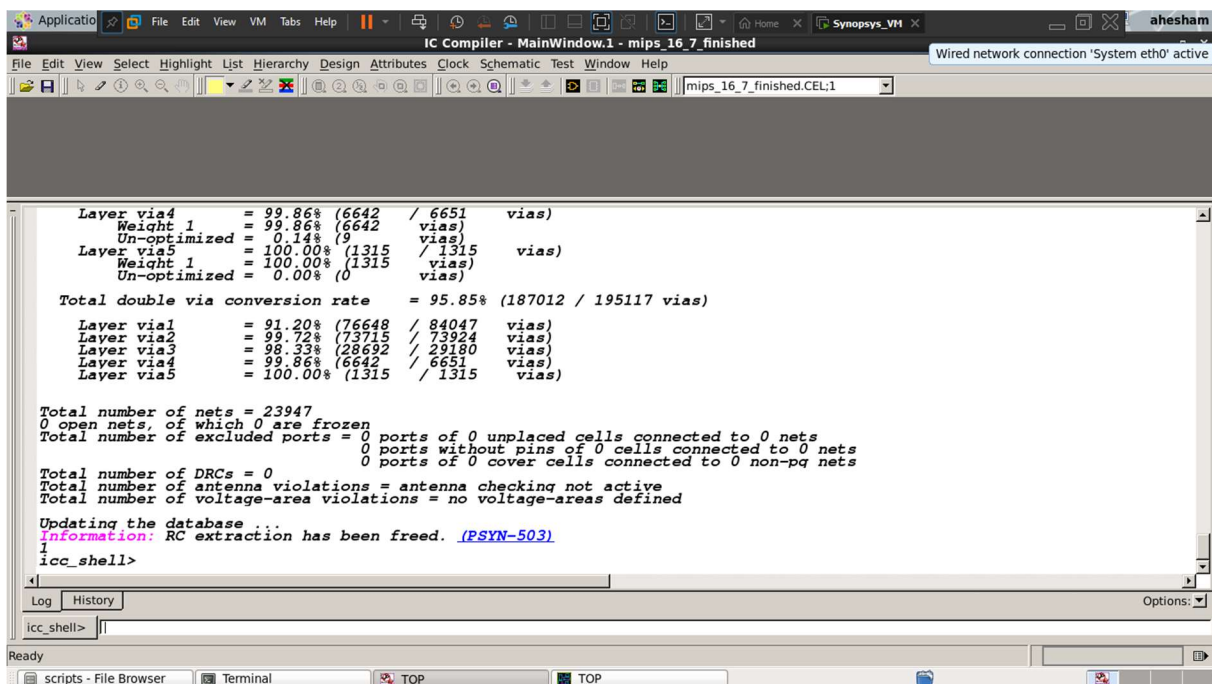
We all contributed in backend flow of the project.

# Results

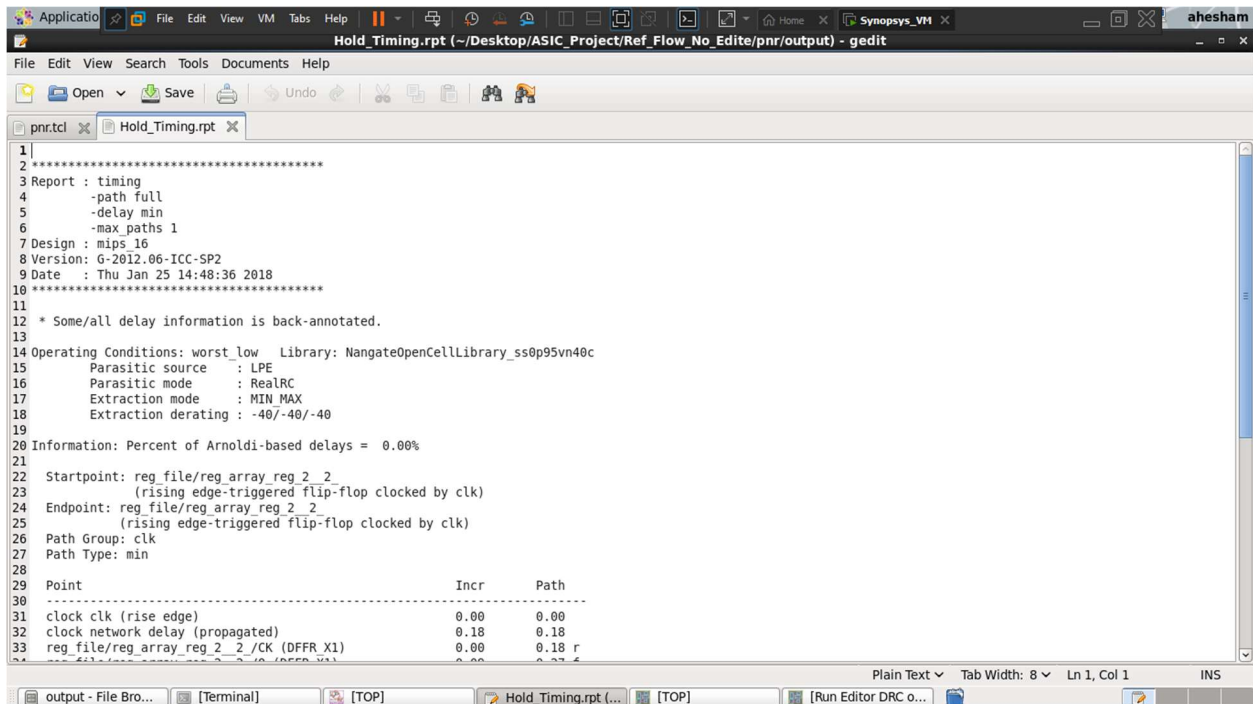
## 1. Final layout



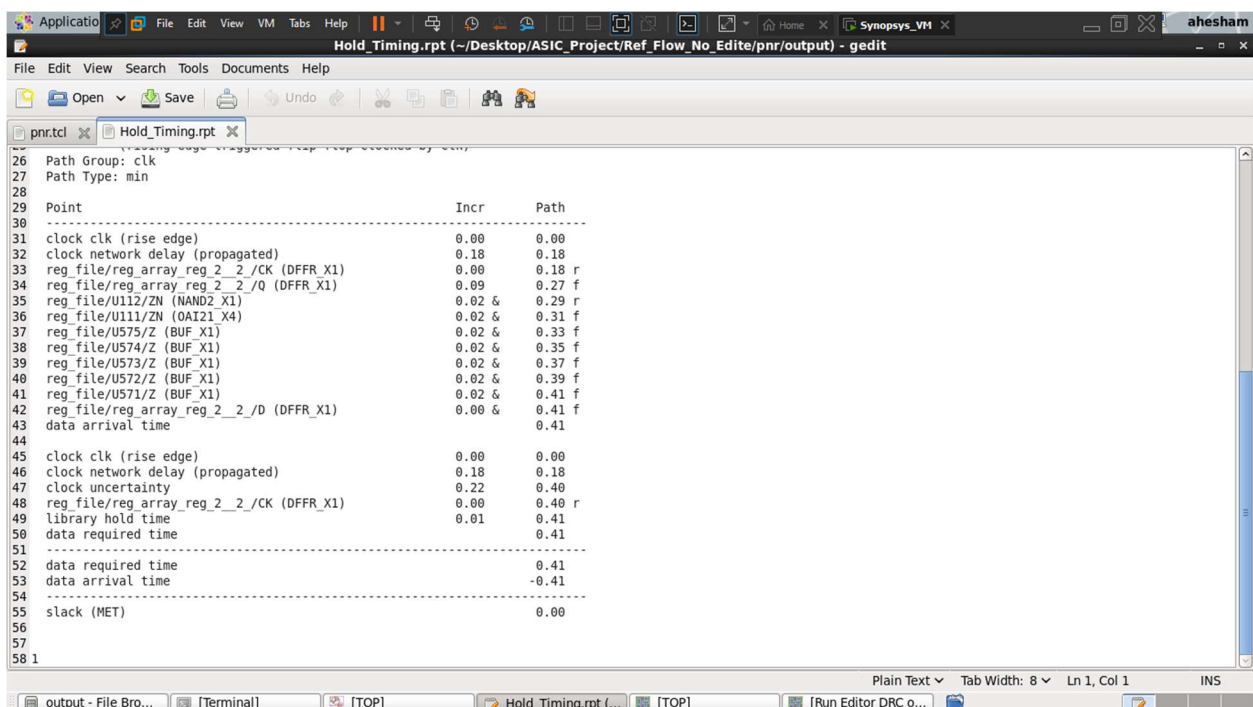
## 2. No DRCs



### 3. Hold report

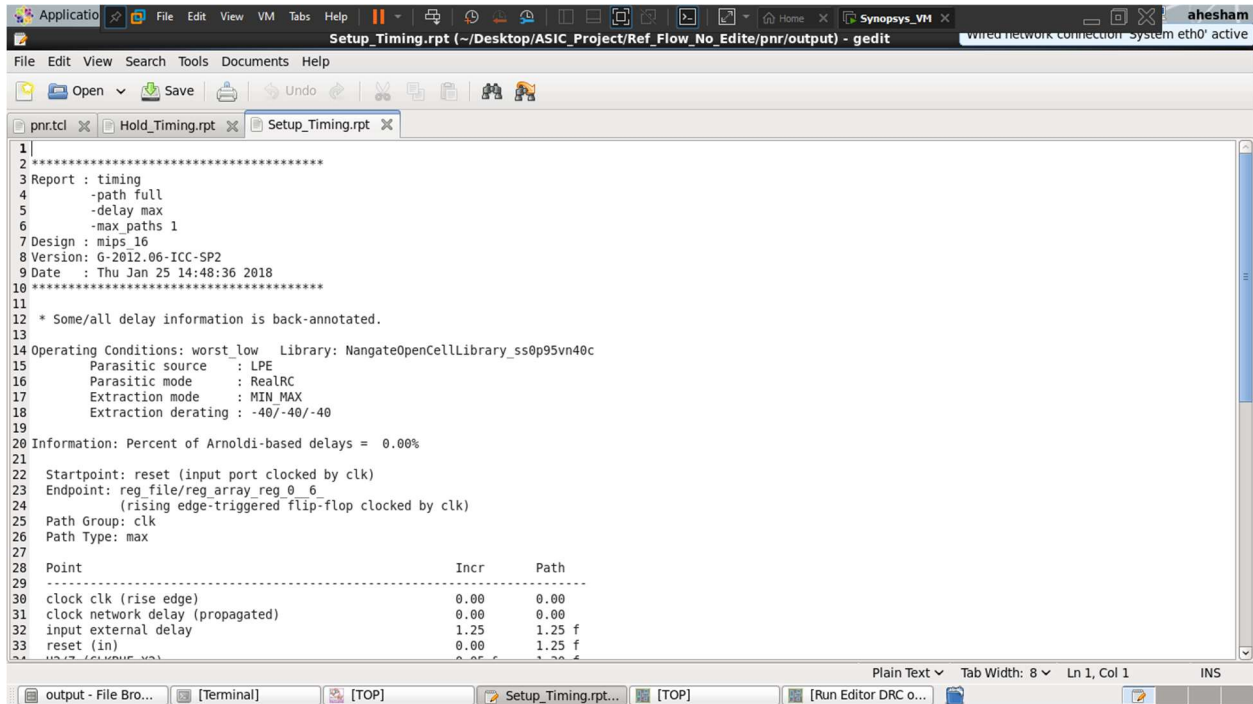


```
1
2 *****
3 Report : timing
4 -path full
5 -delay min
6 -max_paths 1
7 Design : mips_16
8 Version: G-2012.06-ICC-SP2
9 Date : Thu Jan 25 14:48:36 2018
10 *****
11
12 * Some/all delay information is back-annotated.
13
14 Operating Conditions: worst_low Library: NangateOpenCellLibrary_ss0p95vn40c
15 Parasitic source : LPE
16 Parasitic mode : RealRC
17 Extraction mode : MIN MAX
18 Extraction derating : -40/-40/-40
19
20 Information: Percent of Arnoldi-based delays = 0.00%
21
22 Startpoint: reg_file/reg_array_reg_2_2
23 (rising edge-triggered flip-flop clocked by clk)
24 Endpoint: reg_file/reg_array_reg_2_2
25 (rising edge-triggered flip-flop clocked by clk)
26 Path Group: clk
27 Path Type: min
28
29 Point Incr Path
30 -----
31 clock clk (rise edge) 0.00 0.00
32 clock network delay (propagated) 0.18 0.18
33 reg_file/reg_array_reg_2_2 /CK (DFFR_X1) 0.00 0.18 r
34
```

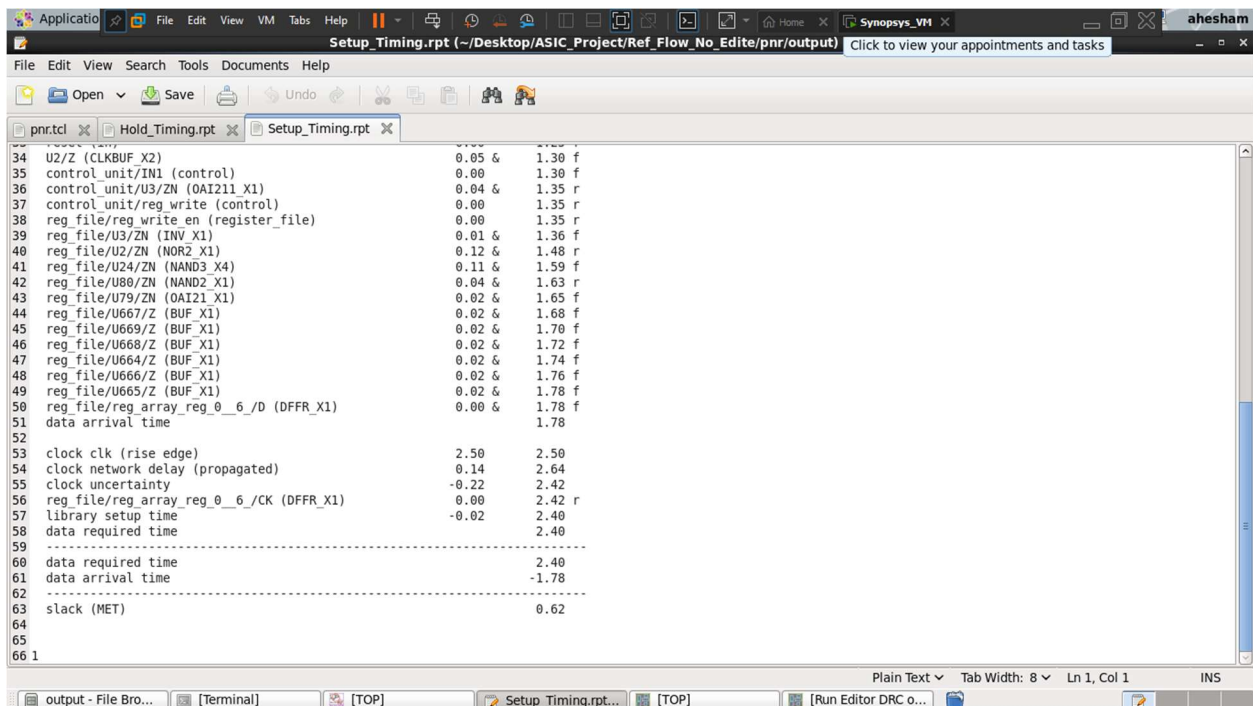


```
26 Path Group: clk
27 Path Type: min
28
29 Point Incr Path
30 -----
31 clock clk (rise edge) 0.00 0.00
32 clock network delay (propagated) 0.18 0.18
33 reg_file/reg_array_reg_2_2 /CK (DFFR_X1) 0.00 0.18 r
34 reg_file/reg_array_reg_2_2 /Q (DFFR_X1) 0.09 0.27 f
35 reg_file/U112/ZN (NAND2_X1) 0.02 & 0.29 r
36 reg_file/U111/ZN (OAI21_X4) 0.02 & 0.31 f
37 reg_file/U575/Z (BUF_X1) 0.02 & 0.33 f
38 reg_file/U574/Z (BUF_X1) 0.02 & 0.35 f
39 reg_file/U573/Z (BUF_X1) 0.02 & 0.37 f
40 reg_file/U572/Z (BUF_X1) 0.02 & 0.39 f
41 reg_file/U571/Z (BUF_X1) 0.02 & 0.41 f
42 reg_file/reg_array_reg_2_2 /D (DFFR_X1) 0.00 & 0.41 f
43 data arrival time 0.41
44
45 clock clk (rise edge) 0.00 0.00
46 clock network delay (propagated) 0.18 0.18
47 clock uncertainty 0.22 0.40
48 reg_file/reg_array_reg_2_2 /CK (DFFR_X1) 0.00 0.40 r
49 library hold time 0.01 0.41
50 data required time 0.41
51 -----
52 data required time 0.41
53 data arrival time -0.41
54 -----
55 slack (MET) 0.00
56
57
58 1
```

## 4. Setup report

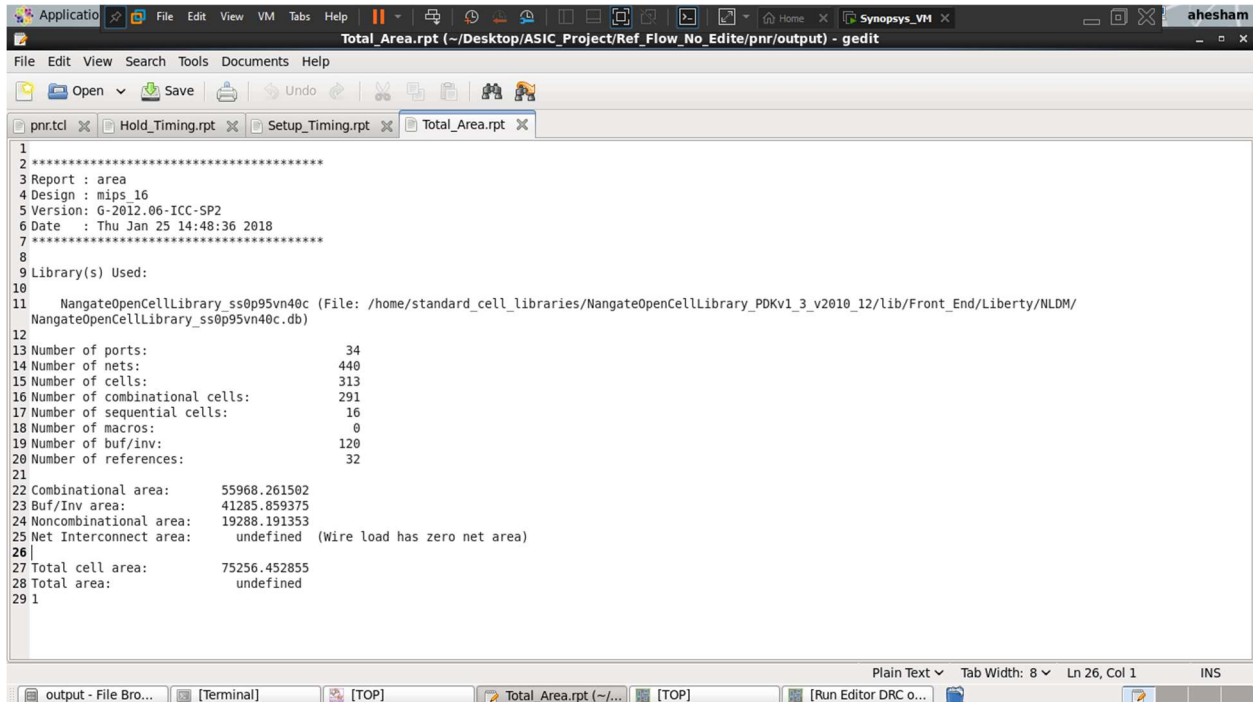


```
1
2 *****
3 Report : timing
4 -path full
5 -delay max
6 -max_paths 1
7 Design : mips_16
8 Version: G-2012.06-ICC-SP2
9 Date : Thu Jan 25 14:48:36 2018
10 *****
11
12 * Some/all delay information is back-annotated.
13
14 Operating Conditions: worst_low Library: NangateOpenCellLibrary_ss0p95vn40c
15 Parasitic source : LPE
16 Parasitic mode : RealRC
17 Extraction mode : MIN MAX
18 Extraction derating : -40/-40/-40
19
20 Information: Percent of Arnoldi-based delays = 0.00%
21
22 Startpoint: reset (input port clocked by clk)
23 Endpoint: reg_file/reg_array_reg_0_6
24 (rising edge-triggered flip-flop clocked by clk)
25 Path Group: clk
26 Path Type: max
27
28 Point Incr Path
29 -----
30 clock clk (rise edge) 0.00 0.00
31 clock network delay (propagated) 0.00 0.00
32 input external delay 1.25 1.25 f
33 reset (in) 0.00 1.25 f
34 U2/Z (CLKBUF_X2) 0.05 f 1.30 f
```



```
34 U2/Z (CLKBUF_X2) 0.05 & 1.30 f
35 control_unit/IN1 (control) 0.00 1.30 f
36 control_unit/U3/ZN (OAI211_X1) 0.04 & 1.35 r
37 control_unit/reg_write (control) 0.00 1.35 r
38 reg_file/reg_write_en (register_file) 0.00 1.35 f
39 reg_file/U3/ZN (INV_X1) 0.01 & 1.36 f
40 reg_file/U2/ZN (NOR2_X1) 0.12 & 1.48 r
41 reg_file/U24/ZN (NAND2_X4) 0.11 & 1.59 f
42 reg_file/U80/ZN (NAND2_X1) 0.04 & 1.63 r
43 reg_file/U79/ZN (OAI21_X1) 0.02 & 1.65 f
44 reg_file/U667/Z (BUF_X1) 0.02 & 1.68 f
45 reg_file/U669/Z (BUF_X1) 0.02 & 1.70 f
46 reg_file/U668/Z (BUF_X1) 0.02 & 1.72 f
47 reg_file/U664/Z (BUF_X1) 0.02 & 1.74 f
48 reg_file/U666/Z (BUF_X1) 0.02 & 1.76 f
49 reg_file/U665/Z (BUF_X1) 0.02 & 1.78 f
50 reg_file/reg_array_reg_0_6/D (DFFR_X1) 0.00 & 1.78 f
51 data arrival time 1.78
52
53 clock clk (rise edge) 2.50 2.50
54 clock network delay (propagated) 0.14 2.64
55 clock uncertainty -0.22 2.42
56 reg_file/reg_array_reg_0_6/CK (DFFR_X1) 0.00 2.42 r
57 library setup time -0.02 2.40
58 data required time 2.40
59 -----
60 data required time 2.40
61 data arrival time -1.78
62 -----
63 slack (MET) 0.62
64
65
66 1
```

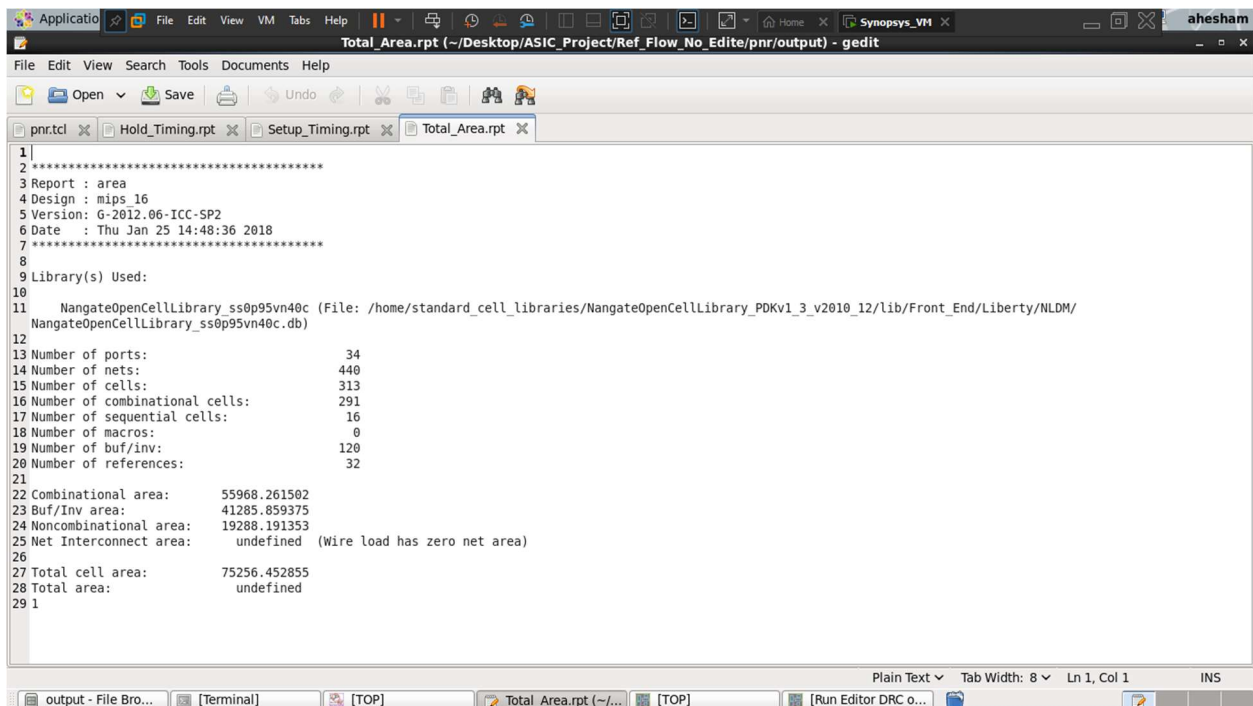
## 5. Total Area report



The screenshot shows a gedit window titled "Total\_Area.rpt (~/Desktop/ASIC\_Project/Ref\_Flow\_No\_Edite/pnr/output) - gedit". The window contains a report with the following content:

```
1
2 *****
3 Report : area
4 Design : mips 16
5 Version: G-2012.06-ICC-SP2
6 Date   : Thu Jan 25 14:48:36 2018
7 *****
8
9 Library(s) Used:
10
11 NangateOpenCellLibrary_ss0p95vn40c (File: /home/standard_cell_libraries/NangateOpenCellLibrary_PDKv1_3_v2010_12/lib/Front_End/Liberty/NLDM/
   NangateOpenCellLibrary_ss0p95vn40c.db)
12
13 Number of ports:          34
14 Number of nets:          440
15 Number of cells:         313
16 Number of combinational cells: 291
17 Number of sequential cells:  16
18 Number of macros:         0
19 Number of buf/inv:        120
20 Number of references:     32
21
22 Combinational area:      55968.261502
23 Buf/Inv area:            41285.859375
24 Noncombinational area:   19288.191353
25 Net Interconnect area:   undefined (Wire load has zero net area)
26
27 Total cell area:         75256.452855
28 Total area:              undefined
29 1
```

The status bar at the bottom indicates "Plain Text", "Tab Width: 8", "Ln 26, Col 1", and "INS".



The screenshot shows a gedit window titled "Total\_Area.rpt (~/Desktop/ASIC\_Project/Ref\_Flow\_No\_Edite/pnr/output) - gedit". The window contains a report with the following content:

```
1
2 *****
3 Report : area
4 Design : mips 16
5 Version: G-2012.06-ICC-SP2
6 Date   : Thu Jan 25 14:48:36 2018
7 *****
8
9 Library(s) Used:
10
11 NangateOpenCellLibrary_ss0p95vn40c (File: /home/standard_cell_libraries/NangateOpenCellLibrary_PDKv1_3_v2010_12/lib/Front_End/Liberty/NLDM/
   NangateOpenCellLibrary_ss0p95vn40c.db)
12
13 Number of ports:          34
14 Number of nets:          440
15 Number of cells:         313
16 Number of combinational cells: 291
17 Number of sequential cells:  16
18 Number of macros:         0
19 Number of buf/inv:        120
20 Number of references:     32
21
22 Combinational area:      55968.261502
23 Buf/Inv area:            41285.859375
24 Noncombinational area:   19288.191353
25 Net Interconnect area:   undefined (Wire load has zero net area)
26
27 Total cell area:         75256.452855
28 Total area:              undefined
29 1
```

The status bar at the bottom indicates "Plain Text", "Tab Width: 8", "Ln 1, Col 1", and "INS".