

DIGITAL ICS DESIGN

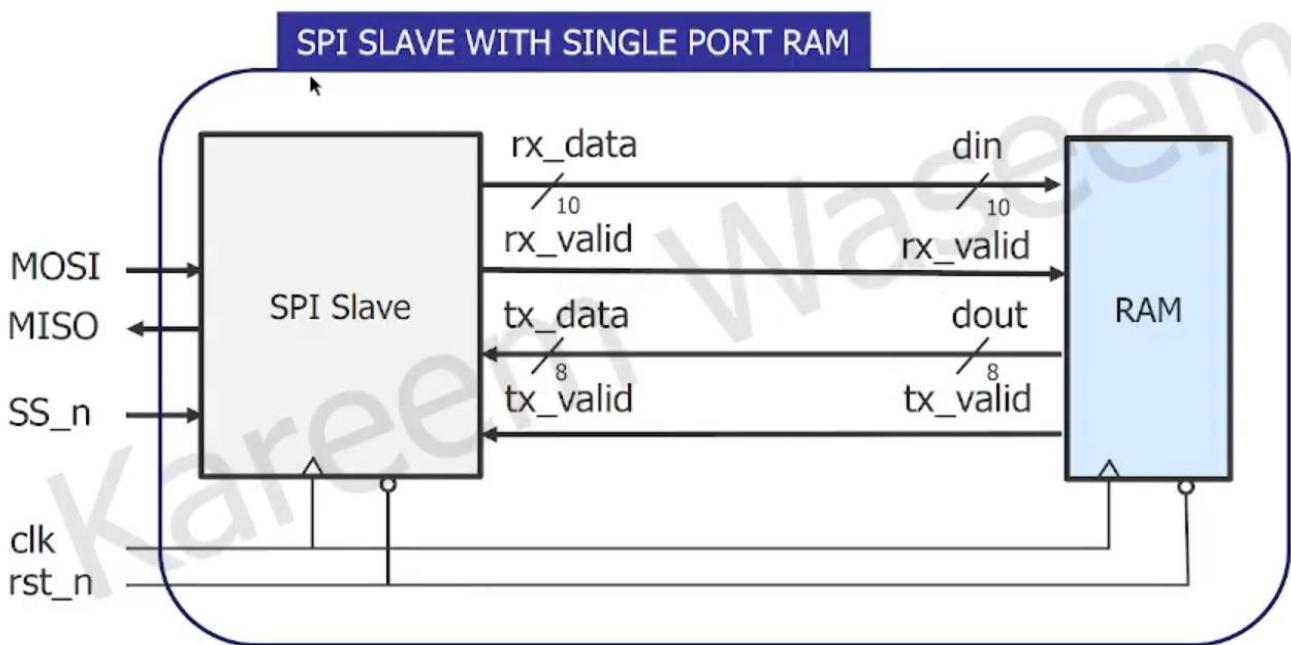
SPI SLAVE WITH SIGNAL PORT RAM



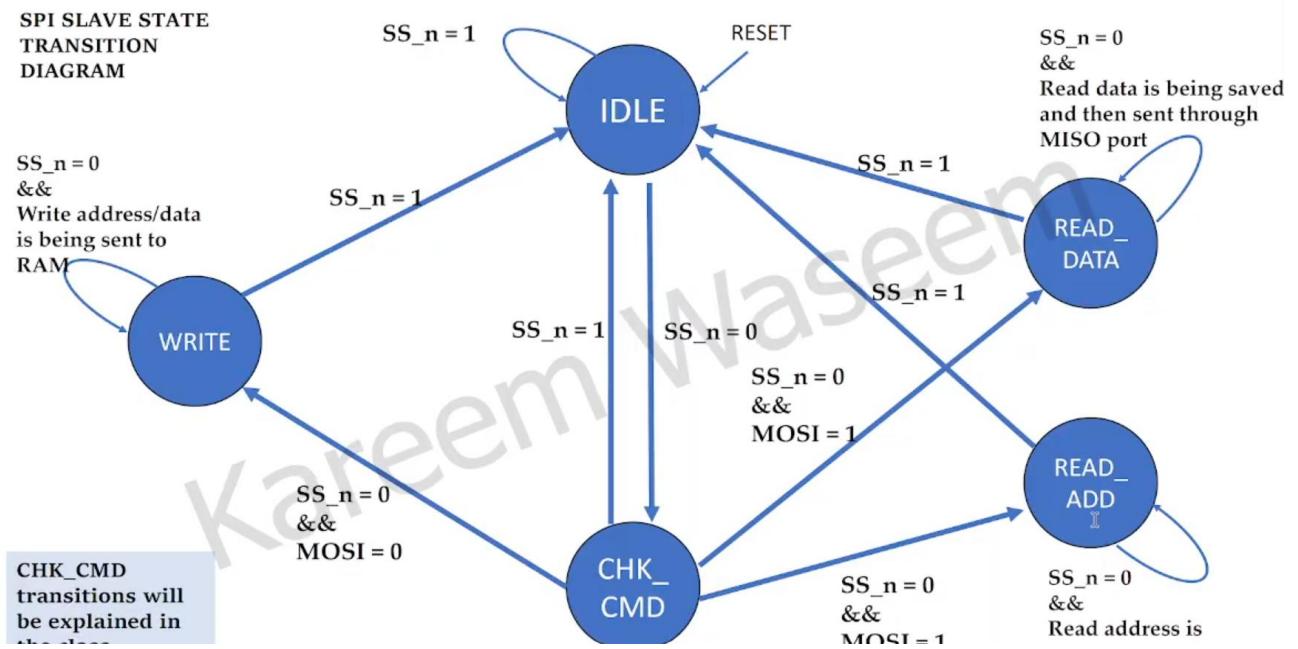
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Submitted to: Eng. Kareem Waseem & Eng. Mai Sherif

SPI SLAVE WITH SINGLE PORT RAM



SPI SLAVE STATE TRANSITION DIAGRAM



Code

```
1 /*----- RAM -----*/
2 module spr_sync(din,clk,rst_n,rx_valid,dout,tx_valid);
3 //parameter
4 parameter MEM_DEPTH = 256 , ADDR_SIZE = 8 ;
5 // input
6 input [9:0] din ;
7 //output
8 output reg[7:0] dout ;
9 output reg tx_valid ;
10 //wire address
11 reg [ADDR_SIZE-1:0] address ;
12 // memory array
13 reg [7:0] mem [MEM_DEPTH-1:0] ;
14 //behavioral modeling
15 always @(posedge clk) begin
16     if(~rst_n) begin
17         dout<=0;
18         address<=0;
19         tx_valid<=0;
20     end
21     else begin
22         if(rx_valid)begin
23             //write
24             if(~din[9])begin
25                 if(~din[8])begin
26                     address <=din[7:0];
27                     tx_valid<=0;
28                 end
29                 else begin
30                     mem[address]<=din[7:0];
31                     tx_valid<=0;
32                 end
33             end
34             //read
35             else begin
36                 if(~din[8])begin
37                     address <=din[7:0];
38                     tx_valid<=0;
39                 end
40                 else begin
41                     dout<=mem[address];
42                     tx_valid <= 1;
43                 end
44             end
45         end
46     end
47 end
48 end
49 endmodule
```

```

50  /*----- SPI SLAVE-----*/
51
52  module SPI(clk,rst_n,ss_n,MOSI,tx_data,tx_valid,rx_data,rx_valid,MISO);
53
54  //parameter
55  parameter IDEL =3'b000 , CHK_CMD = 3'b001 , WRITE = 3'b010, READ_ADD=3'b011,READ_DATA=3'b100;
56  //input
57  input clk ,rst_n,ss_n,tx_valid,MOSI;
58  input [7:0] tx_data;
59  //output
60  output reg [9:0] rx_data;
61  output reg rx_valid,MISO;
62  // current state (cs)and next stat (ns)
63  (*fsm_encoding = "gray" *) reg [2:0] cs,ns ;
64  //wire
65  reg control_read_add;
66  reg [3:0]count;//tx_count;
67  //state memory
68  always @(posedge clk ) begin
69    if(~rst_n) begin
70      cs<=IDEL;
71    end
72    else
73      cs<=ns ;
74  end
75  //next state
76  always @(*) begin
77    case (cs)
78      IDEL:
79        begin
80          if(~ss_n)
81            ns = CHK_CMD ;
82          else
83            ns = IDEL ;
84        end
85      CHK_CMD :
86        begin
87          if(ss_n)
88            ns = IDEL;
89          else if(~ss_n && ~MOSI)
90            ns = WRITE ;
91          else begin
92            if(~ss_n && MOSI)begin
93              if(~control_read_add)
94                ns = READ_ADD ;
95              else
96                ns = READ_DATA ;
97            end
98          end
99        end
...

```

```

100      WRITE :
101          begin
102              if(~ss_n)
103                  ns = WRITE ;
104              else
105                  ns = IDEL ;
106          end
107      READ_ADD :
108          begin
109              if(~ss_n)
110                  ns = READ_ADD ;
111              else
112                  ns = IDEL ;
113          end
114      READ_DATA :
115          begin
116              if(~ss_n)
117                  ns = READ_DATA ;
118              else
119                  ns = IDEL;
120          end
121
122      default: ns=IDEL;
123  endcase
124
125 end
126 //output logic.
127 always @(posedge clk) begin
128     if(~rst_n) begin
129         control_read_addr<=0;
130         count<=0;
131         rx_data<=0;
132         rx_valid<=0;
133         MISO<=0;
134         //tx_count<=0;
135     end
136     else begin
137         case (cs)
138             IDEL:
139                 begin
140                     rx_valid<=0;
141                 end
142             CHK_CMD:
143                 begin
144                     rx_valid <=0 ;
145                     count <= 0 ;
146                 end

```

```

148     WRITE :
149         begin
150             if(count <= 9 ) begin
151                 rx_valid <=0;
152                 rx_data <={rx_data[8:0],MOSI};
153                 count<=count+1;
154             end
155             else
156                 rx_valid <=1;
157         end
158     READ_AOO:
159         begin
160             if(count <= 9)begin
161                 rx_valid<=0;
162                 rx_data={rx_data[8:0],MOSI};
163                 count<=count+1;
164
165             end
166             else begin
167                 rx_valid<=1;
168                 control_read_add <=1;
169             end
170         end
171     READ_DATA :
172         begin
173             if(tx_valid)begin
174                 if(count<=7) begin
175                     MISO <= tx_data[7-count];
176                     count<=count+1;
177                 end
178                 else
179                     control_read_add <=1;
180             end
181             else begin
182                 if(count<=9) begin
183                     rx_valid<=0;
184                     rx_data ={rx_data[8:0],MOSI};
185                     count <=count+1;
186
187                 end
188                 else begin
189                     rx_valid<= 1 ;
190                 end
191             end
192         end
193         default:ns <= IDEL;
194     endcase
195 end
196 end
197 endmodule
198 /*-----SPI_Wrapper-----*/
199 module SPI_Wrapper(MOSI_wrapper,SS_n_wrapper,clk_wrapper,rst_n_wrapper,MISO_wrapper);
200 // input
201 input MOSI_wrapper,SS_n_wrapper,clk_wrapper,rst_n_wrapper ;
202 // output
203 output MISO_wrapper;
204 (* fsm_encoding="gray" *)
205 //wire
206 wire [9:0] rx_data_wrapper ;
207 wire rx_valid_wrapper,tx_valid_wrapper;
208 wire [7:0]tx_data_wrapper ;
209 //instantiation module
210 SPI_slave(.clk(clk_wrapper),.rst_n(rst_n_wrapper),.ss_n(SS_n_wrapper),
211 .MOSI(MOSI_wrapper),.MISO(MISO_wrapper),.rx_data(rx_data_wrapper),
212 .rx_valid(rx_valid_wrapper),.tx_data(tx_data_wrapper),.tx_valid(tx_valid_wrapper));
213 spr_sync RAM(.clk(clk_wrapper),.rst_n(rst_n_wrapper),.din(rx_data_wrapper),.rx_valid(rx_valid_wrapper),.dout(tx_data_wrapper),.tx_valid(tx_valid_wrapper));
214 endmodule
...

```

Testbench

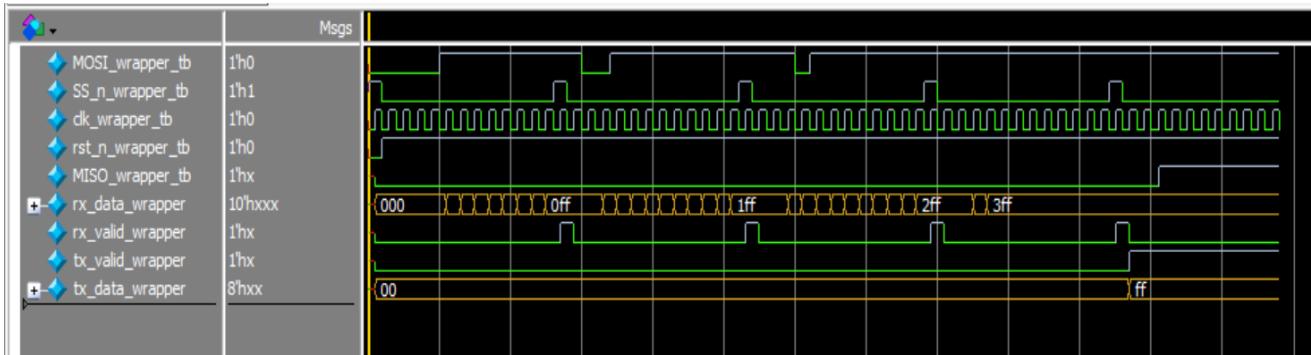
```
1 module SPI_Wrapper_tb();
2 reg MOSI_wrapper_tb,SS_n_wrapper_tb,clk_wrapper_tb,rst_n_wrapper_tb ;
3 wire MISO_wrapper_tb;
4 SPI_Wrapper dut(MOSI_wrapper_tb,SS_n_wrapper_tb,clk_wrapper_tb,rst_n_wrapper_tb,MISO_wrapper_tb);
5 initial begin
6     clk_wrapper_tb = 0;
7     forever
8     #1 clk_wrapper_tb=~clk_wrapper_tb;
9 end
10 initial begin
11     $readmemh("mem.dat",dut.RAM.mem);
12     //rst IDEL
13     rst_n_wrapper_tb = 0 ;SS_n_wrapper_tb = 1;MOSI_wrapper_tb = 0;
14     @(negedge clk_wrapper_tb );
15     //CHK_CMD
16     rst_n_wrapper_tb = 1; SS_n_wrapper_tb =0;
17     @(negedge clk_wrapper_tb );
18     //WRITE address
19     MOSI_wrapper_tb =0;SS_n_wrapper_tb =0;
20     @(negedge clk_wrapper_tb );
21     MOSI_wrapper_tb = 0;@(negedge clk_wrapper_tb );
22     MOSI_wrapper_tb = 0;@(negedge clk_wrapper_tb );
23     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
24     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
25     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
26     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
27     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
28     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
29     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
30     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
31     //IDEL
32     SS_n_wrapper_tb=1;@(negedge clk_wrapper_tb );
33     //CHK_CMD
34     SS_n_wrapper_tb =0;@(negedge clk_wrapper_tb );
35     //WRITE data
36     MOSI_wrapper_tb =0;SS_n_wrapper_tb =0;
37     @(negedge clk_wrapper_tb );
38     MOSI_wrapper_tb = 0;@(negedge clk_wrapper_tb );
39     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
40     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
41     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
42     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
43     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
44     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
45     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
46     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
47     MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb );
```

```

48      //IDEL
49      SS_n_wrapper_tb=1;@(negedge clk_wrapper_tb);
50      //CHK_CMD
51      SS_n_wrapper_tb =0;@(negedge clk_wrapper_tb);
52      //READ address
53      MOSI_wrapper_tb =1;SS_n_wrapper_tb =0;
54      @(negedge clk_wrapper_tb);
55      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
56      MOSI_wrapper_tb = 0;@(negedge clk_wrapper_tb);
57      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
58      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
59      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
60      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
61      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
62      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
63      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
64      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
65      //IDEL
66      SS_n_wrapper_tb=1;@(negedge clk_wrapper_tb);
67      //CHK_CMD
68      SS_n_wrapper_tb =0;@(negedge clk_wrapper_tb);
69      //READ data.
70      MOSI_wrapper_tb =1;SS_n_wrapper_tb =0;
71      @(negedge clk_wrapper_tb);
72      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
73      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
74      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
75      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
76      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
77      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
78      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
79      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
80      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
81      MOSI_wrapper_tb = 1;@(negedge clk_wrapper_tb);
82      //IDEL
83      SS_n_wrapper_tb=1;@(negedge clk_wrapper_tb);
84      //CHK_CMD
85      SS_n_wrapper_tb =0;@(negedge clk_wrapper_tb);
86      repeat(10)
87      @(negedge clk_wrapper_tb);
88      $stop;
89 end
90 endmodule

```

Wave:



➤ DO FILE

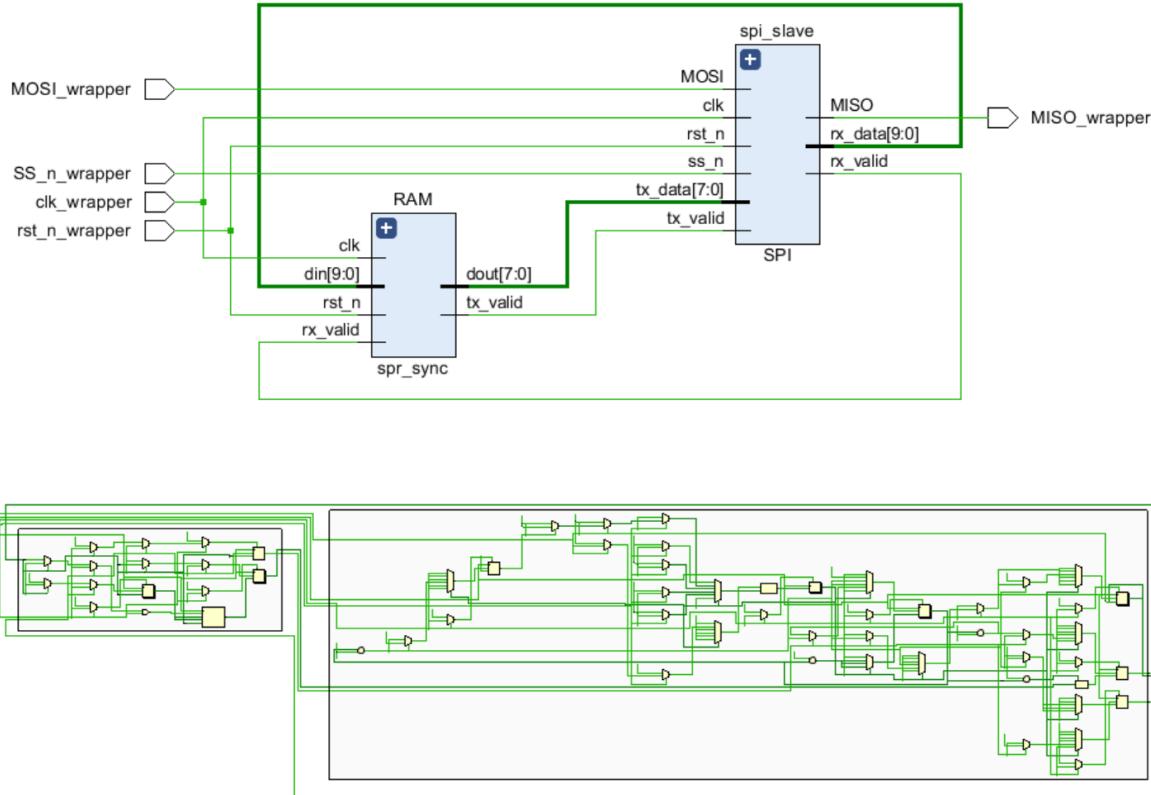
```
run_code - Notepad
File Edit Format View Help
vlib work
vlog code.v testbench.v
vsim -voptargs=+acc work.SPI_Wrapper_tb
add wave *
add wave -position insertpoint \
sim:/SPI_Wrapper_tb/dut/rx_data_wrapper \
sim:/SPI_Wrapper_tb/dut/rx_valid_wrapper \
sim:/SPI_Wrapper_tb/dut/tx_valid_wrapper \
sim:/SPI_Wrapper_tb/dut/tx_data_wrapper
run -all
#quit -sim
```

Constrain file:

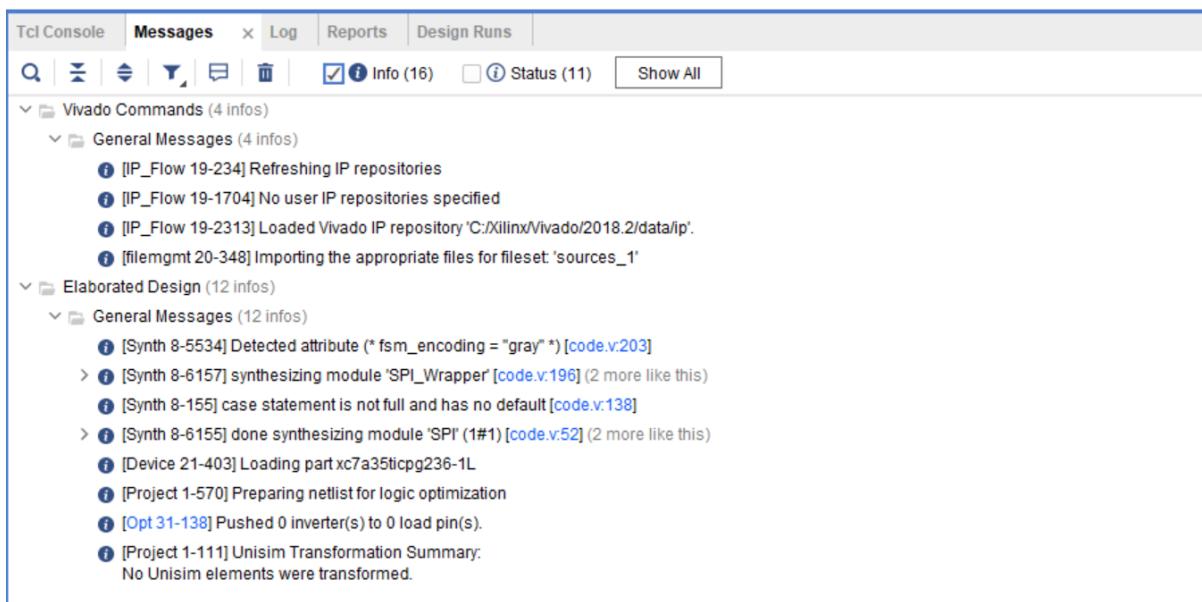
```
## Clock signal
set_property -dict {PACKAGE_PIN W5 IO_STANDARD LVCMOS33} [get_ports clk_wrapper]
create_clock -period 10.000 -name sys_clk_pin -waveform {0.000 5.000} -add [get_ports clk_wrapper]
## Switches
set_property -dict {PACKAGE_PIN V17 IO_STANDARD LVCMOS33} [get_ports rst_n_wrapper]
set_property -dict {PACKAGE_PIN V16 IO_STANDARD LVCMOS33} [get_ports SS_n_wrapper]
set_property -dict {PACKAGE_PIN W16 IO_STANDARD LVCMOS33} [get_ports MOSI_wrapper]
## LEDs
set_property -dict {PACKAGE_PIN U16 IO_STANDARD LVCMOS33} [get_ports MISO_wrapper]
## Configuration options, can be used for all designs
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
## SPI configuration mode options for QSPI boot, can be used for all designs
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.CONFIGURE 33 [current_design]
set_property CONFIG_MODE SPIx4 [current_design]
create_debug_core u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/clk]
connect_debug_port u_ila_0/clk [get_nets [list clk_wrapper_IBUF_BUFG]]
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
set_property port_width 1 [get_debug_ports u_ila_0/probe0]
connect_debug_port u_ila_0/probe0 [get_nets [list clk_wrapper_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 1 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list MISO_wrapper_OBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 1 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list MOSI_wrapper_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 1 [get_debug_ports u_ila_0/probe3]
connect_debug_port u_ila_0/probe3 [get_nets [list rst_n_wrapper_IBUF]]
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 1 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list SS_n_wrapper_IBUF]]
set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
connect_debug_port dbg_hub/clk [get_nets clk_wrapper_IBUF_BUFG]
```

Sequential encoding:

1-Schematic Elaboration:

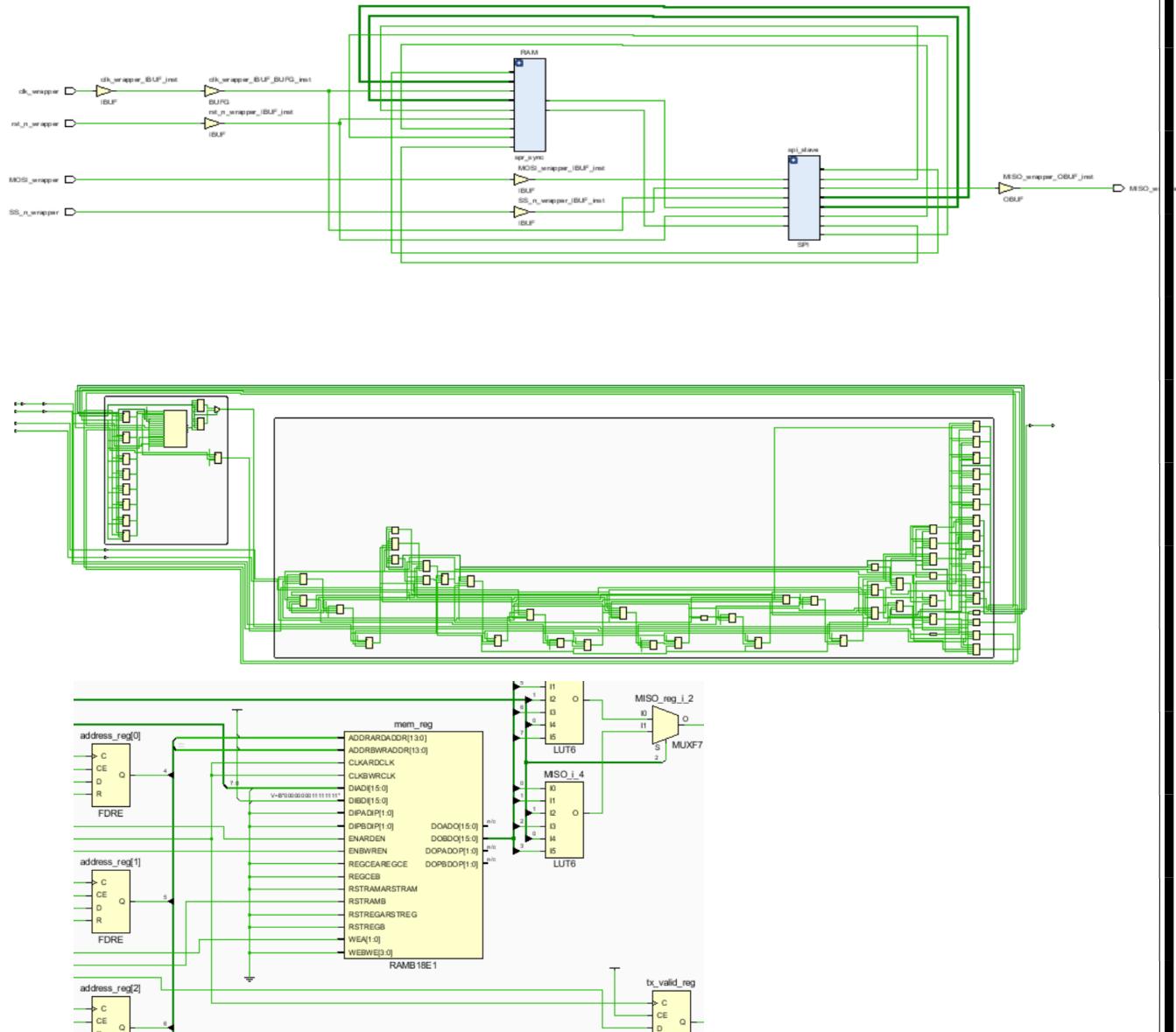


➤ Messages:



2-Synthesis

➤ Schematic:



➤ Timing:

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.146 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 84	Total Number of Endpoints: 84	Total Number of Endpoints: 34

All user specified timing constraints are met.

➤ Utilization:

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Wrapper		29	29	0.5	5	1
I RAM (spr_sync)		3	9	0.5	0	0
I spi_slave (SPI)		26	20	0	0	0

➤ Messages:

Q H D T M B Show All		Warning (1)	Info (39)	Status (17)
V Vivado Commands (4 infos)				
> G General Messages (4 infos)				
V Synthesis (1 warning, 29 infos)				
i [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'				
> i [Synth 8-6157] synthesizing module 'SPI_Wrapper' [code.v:205] (2 more like this)				
> i [Synth 8-6155] done synthesizing module 'SPI' (1#1) [code.v:52] (2 more like this)				
i [Device 21-403] Loading part xc7a35ticpg236-1L				
i [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/Vivado_session/project_10/project_10.srccs/constrs_1/im constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [Xil/SPI_Wrapper_propImpl.xdc]. Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_elaboration/synthesis.				
i [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'				
> i [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (3 more like this)				
i [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'				
> i [Synth 8-4480] The timing for the instance i_0/RAM/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could b may help in improving timing. (1 more like this)				
i [Project 1-571] Translating synthesized netlist				
i [Netlist 29-17] Analyzing 5 Unisim elements for replacement				
i [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds				
> i [Project 1-570] Preparing netlist for logic optimization (1 more like this)				
i [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).				
> i [Project 1-111] Unisim Transformation Summary: No Unisim elements were transformed. (1 more like this)				
i [Common 17-83] Releasing license: Synthesis				
Y [Constraints 18-5210] No constraint will be written out.				
i [Common 17-1381] The checkpoint 'E:/Vivado_session/project_10/project_10.runs/synth_1/SPI_Wrapper.dcp' has been generated.				
i [runcl-4] Executing : report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb				
i [Common 17-206] Exiting Vivado at Fri Aug 1 18:13:46 2025...				

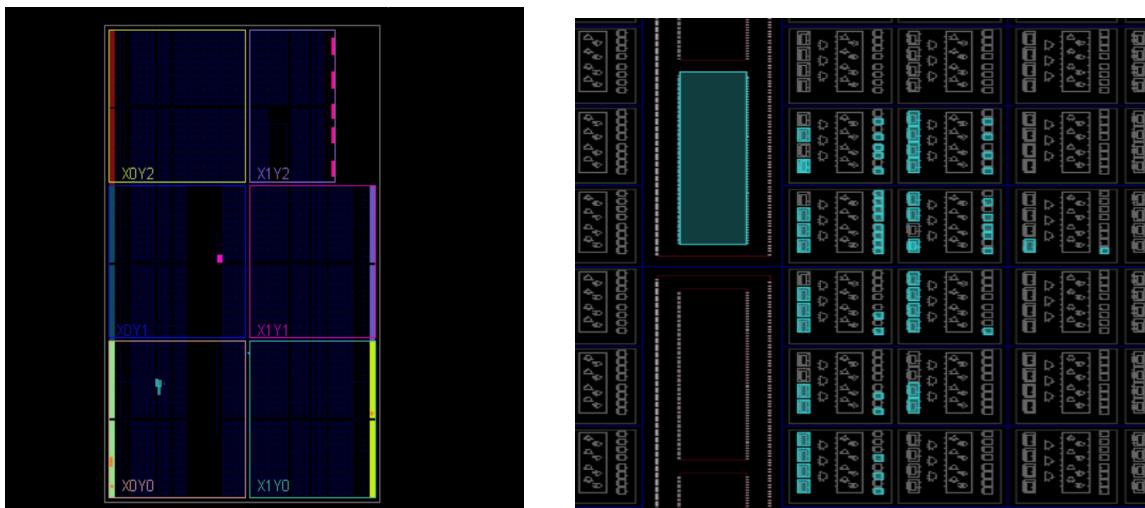
➤ Encoding:

State	New Encoding	Previous Encoding
IDEL	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI'

2-Implementation:

➤ Device:



➤ Timing:

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.401 ns	Worst Hold Slack (WHS): 0.043 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 84	Total Number of Endpoints: 84	Total Number of Endpoints: 34

All user specified timing constraints are met.

➤ Utilization:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
spi_wrapper	27	29	11	27	11	0.5	5	1
RAM (spr_sync)	4	9	5	4	0	0.5	0	0
spi_slave (SPI)	23	20	11	23	9	0	0	0

➤ Messages:

Messages

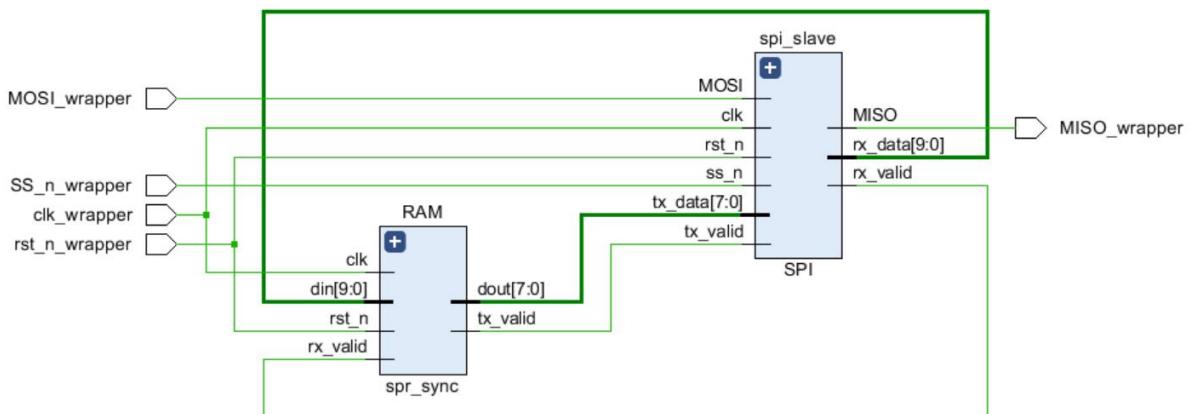
Hide All

-  Warning (1)
-  Info (242)
-  Status (481)

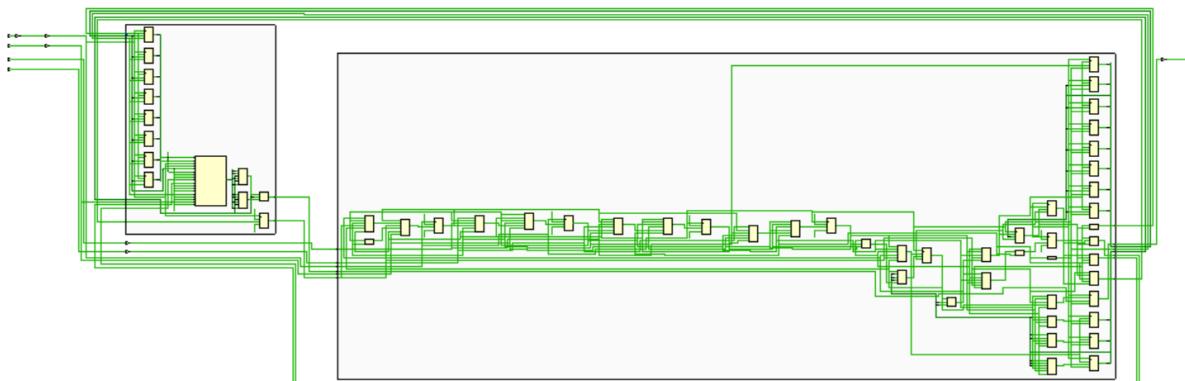
- ▼  **Vivado Commands** (4 infos, 4 status messages)
 - ▼  **General Messages** (4 infos, 4 status messages)
 -  [IP_Flow 19-234] Refreshing IP repositories
 -  [IP_Flow 19-1704] No user IP repositories specified
 -  [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
 -  [filemgmt 20-348] Importing the appropriate files for fileset: 'sources_1'
- >  **Synthesis** (1 warning, 30 infos, 11 status messages)
- >  **Synthesized Design** (9 infos, 3 status messages)
- ▼  **Implementation** (95 infos, 228 status messages)
 - >  **Design Initialization** (7 infos, 7 status messages)
 - >  **Opt Design** (31 infos, 54 status messages)
 - >  **Place Design** (23 infos, 90 status messages)
 - >  **Route Design** (34 infos, 77 status messages)
- >  **Implemented Design** (9 infos, 7 status messages)

Gray encoding

1. Elaboration schematic:



2. Synthesis schematic:



3. Encoding:

State	New Encoding	Previous Encoding
IDEL	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'

4. Synthesis timing report:

Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:	0
Total Number of Endpoints: 77	Total Number of Endpoints: 77	Total Number of Endpoints:	32

All user specified timing constraints are met.

5. Synthesis utilization report:

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_Wrapper		26	29	0.5	5	1
I RAM (spr_sync)		3	9	0.5	0	0
I spi_slave (SPI)		23	20	0	0	0

6. Implementation timing report:

Design Timing Summary

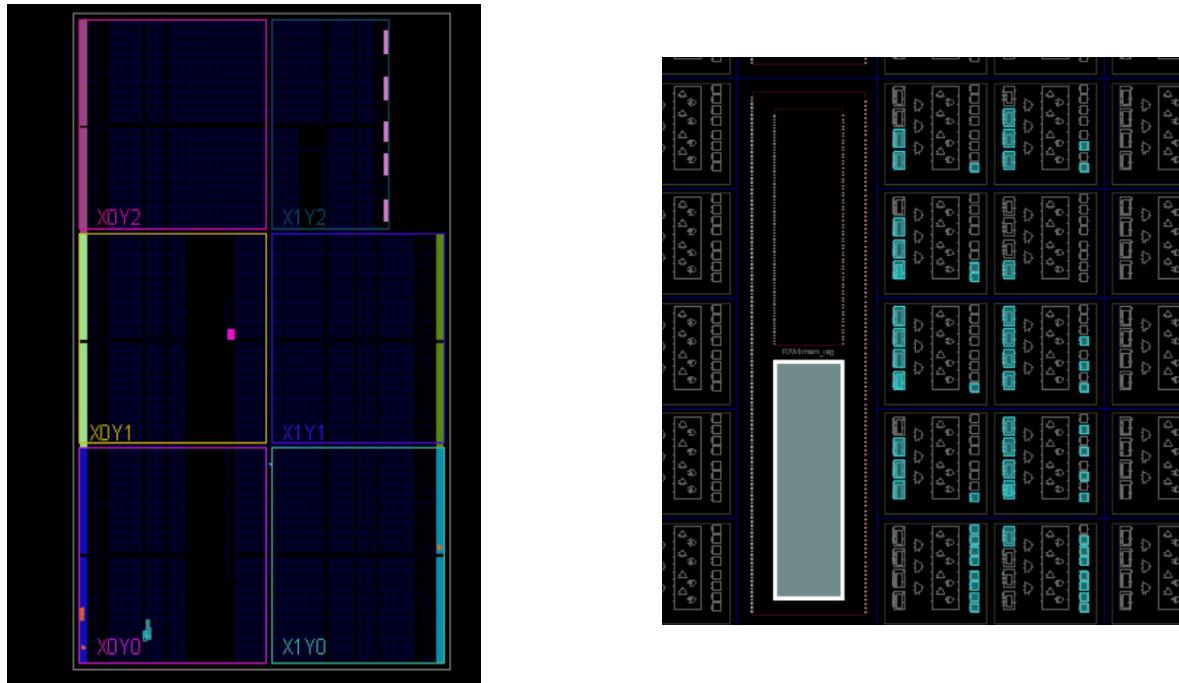
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.671 ns	Worst Hold Slack (WHS): 0.048 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 77	Total Number of Endpoints: 77	Total Number of Endpoints: 32

All user specified timing constraints are met.

7. Implementation utilization report:

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	
N SPI_Wrapper		25	29	10	25		12	0.5	5	1
I RAM (spr_sync)		4	9	4	4		0	0.5	0	0
I spi_slave (SPI)		21	20	9	21		9	0	0	0

8. Implementation device:



10. Elaboration messages:

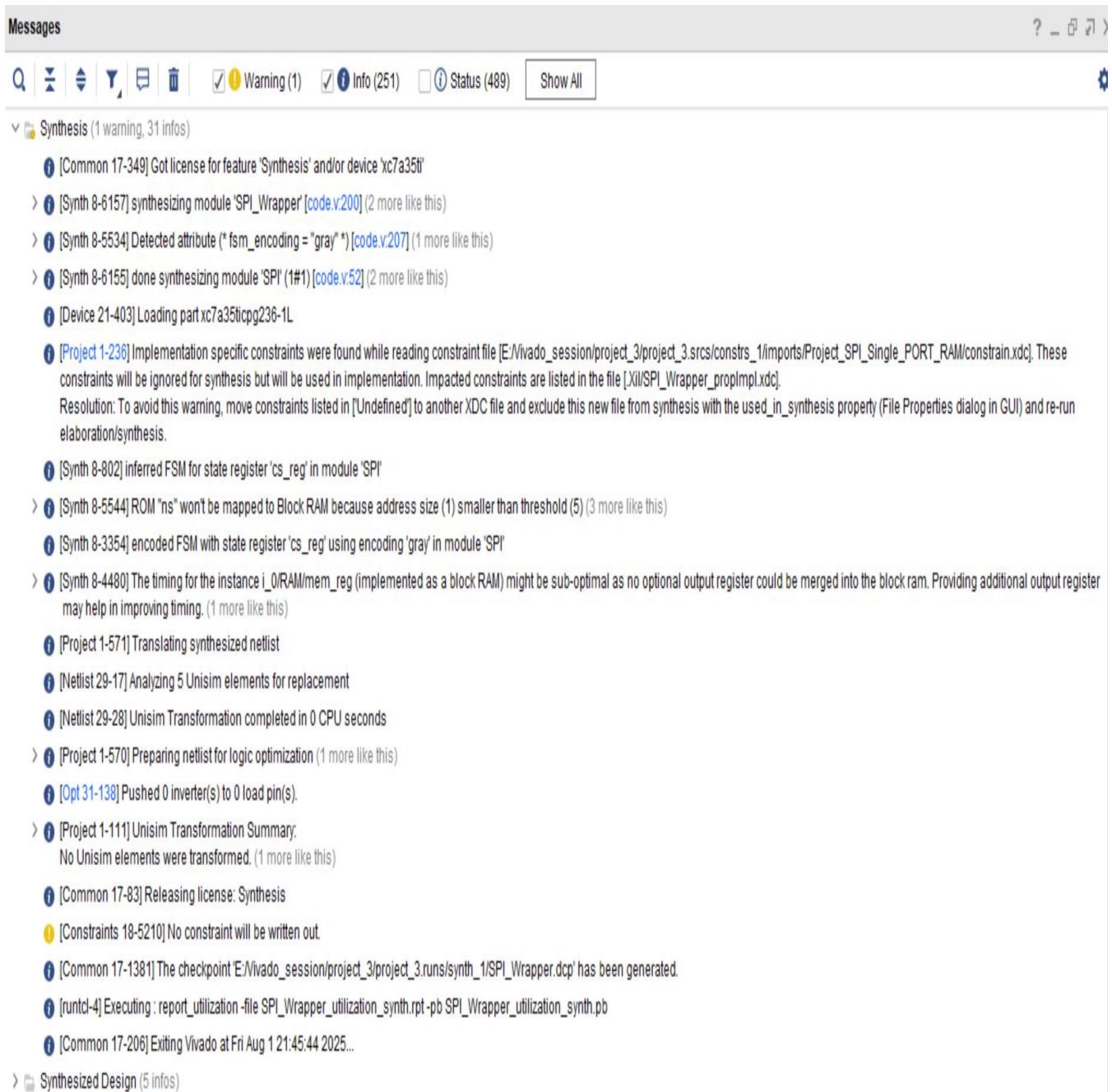


The screenshot shows the Vivado Tcl Console interface with the 'Messages' tab selected. The message list is filtered to show 4 infos under 'Vivado Commands' and 11 infos under 'Elaborated Design'. The 'Elaborated Design' section includes several synthesis-related messages, such as module synthesis, fsm_encoding detection, and project preparation.

```
Vivado Commands (4 infos)
  General Messages (4 infos)
    [IP_Flow 19-234] Refreshing IP repositories
    [IP_Flow 19-1704] No user IP repositories specified
    [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
    [filemgmt 20-348] Importing the appropriate files for fileset: 'sources_1'

Elaborated Design (11 infos)
  General Messages (11 infos)
    [Synth 8-6157] synthesizing module 'SPI_Wrapper' [code.v.200] (2 more like this)
    [Synth 8-5534] Detected attribute (* fsm_encoding = "gray"*) [code.v.207] (1 more like this)
    [Synth 8-6155] done synthesizing module 'SPI' (#1) [code.v.52] (2 more like this)
    [Project 1-570] Preparing netlist for logic optimization
    [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
    [Project 1-111] Unisim Transformation Summary:
      No Unisim elements were transformed.
```

11. Synthesis messages:



The screenshot shows the Vivado Tcl Console interface with the 'Messages' tab selected. The message list is filtered to show 1 warning and 31 infos under 'Synthesis'. The 'Synthesis' section contains numerous synthesis-related messages, including license acquisition, module synthesis, fsm_encoding detection, timing reports, and resource usage analysis. A specific note about XDC constraints is present, indicating they will be ignored for synthesis but used for implementation.

```
Synthesis (1 warning, 31 infos)

  [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
  > [Synth 8-6157] synthesizing module 'SPI_Wrapper' [code.v.200] (2 more like this)
  > [Synth 8-5534] Detected attribute (* fsm_encoding = "gray"*) [code.v.207] (1 more like this)
  > [Synth 8-6155] done synthesizing module 'SPI' (#1) [code.v.52] (2 more like this)
  [Device 21-403] Loading part xc7a35tcpg236-1L
  [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/Vivado_session/project_3/project_3.srcs/constrs_1/imports/Project_SPI_Single_PORT_RAM/constrain.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [xil/SPI_Wrapper_propImpl.xdc].
  Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

  [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'
  > [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (3 more like this)
  [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'
  > [Synth 8-4480] The timing for the instance i_0/RAM/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
  [Project 1-571] Translating synthesized netlist
  [Netlist 29-17] Analyzing 5 Unisim elements for replacement
  [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
  > [Project 1-570] Preparing netlist for logic optimization (1 more like this)
  [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
  > [Project 1-111] Unisim Transformation Summary:
    No Unisim elements were transformed. (1 more like this)
  [Common 17-83] Releasing license: Synthesis
  [Constraints 18-5210] No constraint will be written out.
  [Common 17-1381] The checkpoint 'E:/Vivado_session/project_3/project_3.runs/synth_1/SPI_Wrapper.dcp' has been generated.
  [runcl-4] Executing :report_utilization -file SPI_Wrapper_utilization_synth.rpt -pb SPI_Wrapper_utilization_synth.pb
  [Common 17-206] Exiting Vivado at Fri Aug 1 21:45:44 2025...

  Synthesized Design (5 infos)
```

12. Implementation messages:

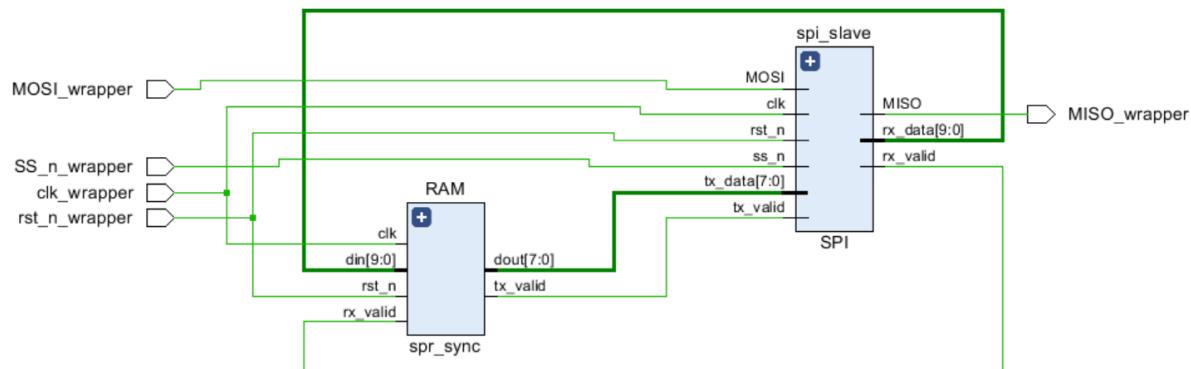
Messages

Implementation (95 infos)

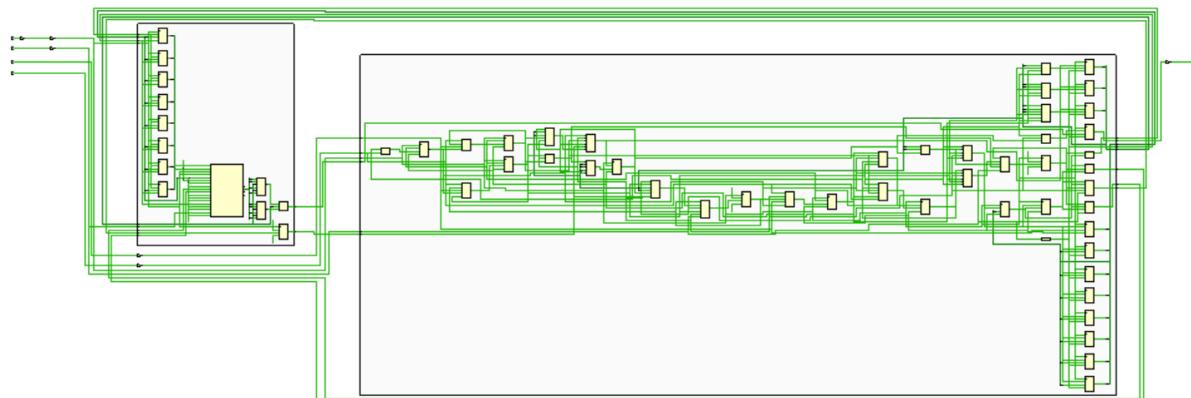
- Design Initialization (7 infos)
 - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 1 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Device 21-403] Loading part xc7a35tfg236-1L
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.
- Opt Design (31 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35tI'
 - [Project 1-461] DRC finished with 0 Errors
 - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
 - [Opt 31-49] Retargeted 0 cell(s).
 - [Opt 31-138] Pushed 1 inverter(s) to 1 load pin(s). (1 more like this)
 - [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
 - [Opt 31-662] Phase BUFQ optimization created 0 cells of which 0 are BUFQs and removed 0 cells.
 - [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
 - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [Pwropt 34-9] Applying IDT optimizations ...
 - [Pwropt 34-10] Applying ODC optimizations ...
 - [Physopt 32-619] Estimated Timing Summary | WNS=5.898 | TNS=0.000 |
 - [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
 - [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-1381] The checkpoint 'E:/vivado_session/project_3/project_3.runs/impl_1/SPI_Wrapper_opt.dcp' has been generated.
- IP_Flow (19-234) Refreshing IP repositories
- IP_Flow (19-1704) No user IP repositories specified
- IP_Flow (19-2313) Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Corecl 2-168] The results of DRC are in file SPI_Wrapper_drc_opted.rpt.
- Place Design (23 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35tI'
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
 - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
 - [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [Physopt 32-65] No nets found for high-fanout optimization.
 - [Physopt 32-232] Optimized 0 net. Created 0 new instance.
 - [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
 - [Place 46-31] BUFQ insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
 - [Place 30-746] Post Placement Timing Summary WNS=5.621. For the most accurate timing information please run report_timing.
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-1381] The checkpoint 'E:/vivado_session/project_3/project_3.runs/impl_1/SPI_Wrapper_placed.dcp' has been generated.
 - [runcl-4] Executing : report_io -file SPI_Wrapper_io_placed.rpt (2 more like this)
- Route Design (34 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35tI'
 - [Vivado_Tcl 4-198] DRC finished with 0 Errors
 - Route Design (34 infos)
 - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35tI'
 - [Vivado_Tcl 4-198] DRC finished with 0 Errors
 - [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
 - [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
 - [Route 35-416] Intermediate Timing Summary | WNS=5.527 | TNS=0.000 | WHS=-0.217 | THS=-3.657 | (2 more like this)
 - [Route 35-57] Estimated Timing Summary | WNS=5.670 | TNS=0.000 | WHS=0.046 | THS=0.000 |
 - [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
 - [Route 35-16] Router Completed Successfully
 - [Common 17-83] Releasing license: Implementation
 - [Timing 38-480] Writing timing data to binary archive.
 - [Common 17-1381] The checkpoint 'E:/vivado_session/project_3/project_3.runs/impl_1/SPI_Wrapper_routed.dcp' has been generated.
 - [DRC 23-27] Running DRC with 2 threads (1 more like this)
 - [Corecl 2-168] The results of DRC are in file SPI_Wrapper_drc_routed.rpt.
 - [runcl-4] Executing : report_drc -file SPI_Wrapper_drc_routed.rpt -pb SPI_Wrapper_drc_routed.pb -rpx SPI_Wrapper_drc_routed.rpx (7 more like this)
 - [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
 - [DRC 23-133] Running Methodology with 2 threads
 - [Corecl 2-1520] The results of Report Methodology are in file SPI_Wrapper_methodology_drc_routed.rpt.
 - [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
 - [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
 - [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)
 - Implemented Design (10 infos)
 - General Messages (10 infos)
 - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization

One hot encoding

1. Elaboration schematic:



2. Synthesis schematic:



3. Encoding:

State	New Encoding	Previous Encoding
IDEL	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'

4. Synthesis timing report:

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.898 ns	Worst Hold Slack (WHS): 0.149 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Falling Endpoints: 0	Number of Falling Endpoints: 0	Number of Falling Endpoints: 0
Total Number of Endpoints: 84	Total Number of Endpoints: 84	Total Number of Endpoints: 34

All user specified timing constraints are met.

5. Synthesis utilization report:

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▀ N SPI_Wrapper		26	31	0.5	5	1
▀ RAM (spr_sync)		3	9	0.5	0	0
▀ spi_slave (SPI)		23	22	0	0	0

6. Implementation timing report:

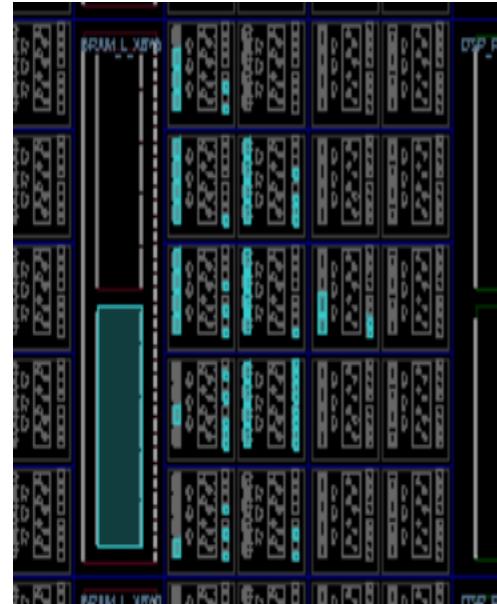
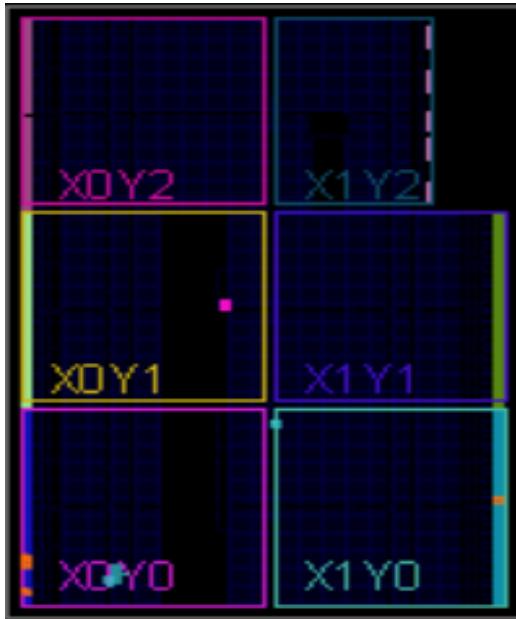
Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.276 ns	Worst Hold Slack (WHS): 0.047 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 84	Total Number of Endpoints: 84	Total Number of Endpoints: 34

All user specified timing constraints are met.

7. Implementation utilization report:

Name	1	Slice LUTs (20800)	Slice Registers (41600)	Slice (815 0)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
▀ N SPI_Wrapper		27	31	10	27	15	0.5	5	1
▀ RAM (spr_sync)		4	9	5	4	0	0.5	0	0
▀ spi_slave (SPI)		23	22	8	23	13	0	0	0

8. Implementation device:



9. Elaboration messages:

The screenshot shows the Vivado Messages window with the following details:

- Tab bar: Tcl Console, Messages (selected), Log, Reports, Design Runs, Power, Methodology, Timing.
- Toolbar: Search, Filter, Show All.
- Message list:
 - Vivado Commands (4 infos):
 - General Messages (4 infos):
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2018.2/data/ip'.
 - [filemgmt 20-348] Importing the appropriate files for fileset: 'sources_1'
 - Elaborated Design (11 infos):
 - General Messages (11 infos):
 - > [Synth 8-6157] synthesizing module 'SPI_Wrapper' [code.v:200] (2 more like this)
 - > [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [code.v:207] (1 more like this)
 - > [Synth 8-6155] done synthesizing module 'SPI' (1#1) [code.v:52] (2 more like this)
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

10. Synthesis messages:

The screenshot shows the Vivado Messages window with the following details:

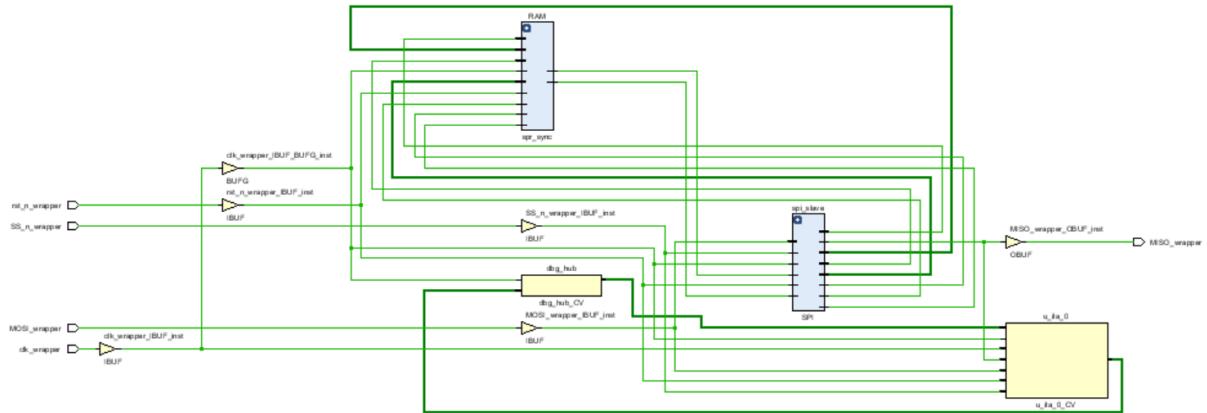
- Tab bar: Utilization, Messages (selected), Log, Reports, Design Runs, Power, Methodology, Timing.
- Toolbar: Search, Filter, Show All.
- Message list:
 - Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
 - > [Synth 8-6157] synthesizing module 'SPI_Wrapper' [code.v:200] (2 more like this)
 - > [Synth 8-5534] Detected attribute (* fsm_encoding = "gray" *) [code.v:207] (1 more like this)
 - > [Synth 8-6155] done synthesizing module 'SPI' (1#1) [code.v:52] (2 more like this)
 - [Device 21-403] Loading part xc7a35tclcp236-1L
 - [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/Vivado_session/project_3/project_3.srcs/constrs_1/imports/Project_SPI_Single_PORT_RAM/constrain.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [XILISP_Vwrapper_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [Undefined] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
 - [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'SPI'
 - > [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5) (3 more like this)
 - [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'
 - > [Synth 8-4480] The timing for the instance I_0/RAM/mem_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing. (1 more like this)
 - [Project 1-571] Translating synthesized netlist
 - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - > [Project 1-570] Preparing netlist for logic optimization (1 more like this)
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - > [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed. (1 more like this)
 - [Common 17-83] Releasing license: Synthesis
 - [Constraints 18-5210] No constraint will be written out.
 - [Common 17-1381] The checkpoint E:/Vivado_session/project_3/project_3.rpt/synth_1/SPI_Wrapper.dcp has been generated.
 - [runrtl-4] Executing : report_utilization -file SPI_Wrapper_utilization_rpt.rpt -pb SPI_Wrapper_utilization_synth.pb
 - [Common 17-206] Exiting Vivado at Fri Aug 1 22:30:31 2025...
 - > [Synthesized Design] (13 infos)
 - > [Synthesized Design] (13 infos)
 - General Messages (13 infos):
 - [Netlist 29-17] Analyzing 5 Unisim elements for replacement
 - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
 - [Project 1-479] Netlist was created with Vivado 2018.2
 - [Project 1-570] Preparing netlist for logic optimization
 - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
 - > [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
 - > [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max. (2 more like this)
 - > [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (2 more like this)

11. Implementation messages:

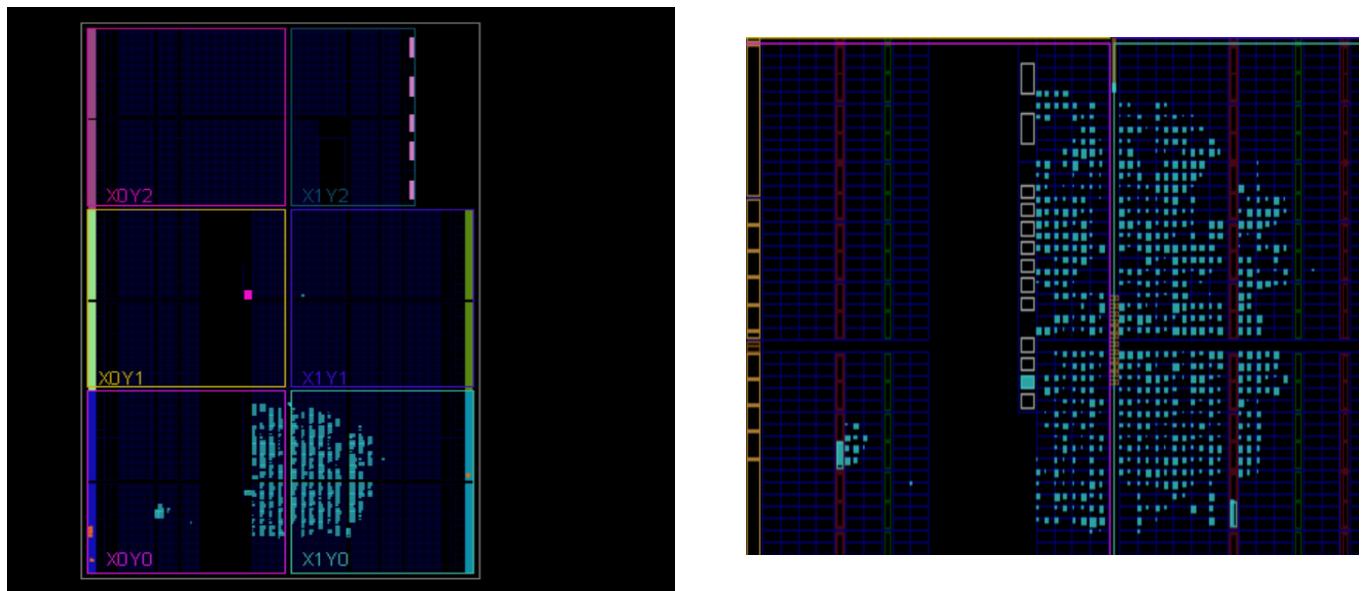


Bitstream generation:

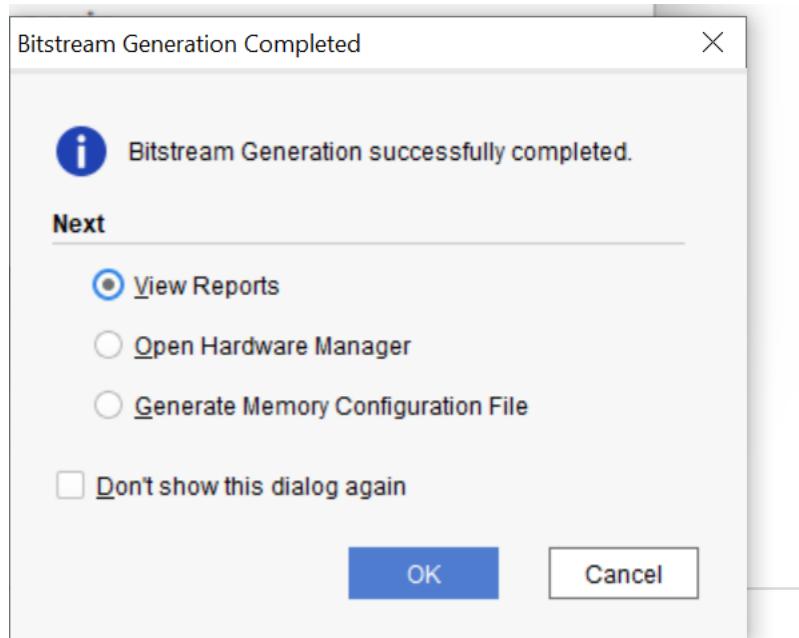
1. Synthesis schematic:



2. Device:



Message showing successful bitstream generation:



Netlist generation

A screenshot of a Verilog code editor window. The code is a Verilog netlist for a design named "Project_SPL_Single_PORT_BAM". The code includes header comments, module definitions, and various logic statements. A large portion of the right side of the screen shows a graphical schematic or simulation interface with multiple components and connections.

```
1 // code.v 2 // mm.netlist.v 3 // Settings
4 // Copyright 1999-2018 Xilinx, Inc. All Rights Reserved.
5 // Tool Version: Vivado v.2018.2 (win64) Build 2258644 Thu Jun 14 20:03:12 PDT 2018
6 // Date    : Fri Aug 12 23:51:08 PDT 2022
7 // Command : write_verilog E:/Depot_Karem/Project_SPL_Single_PORT_BAM/mm.netlist.v
8 // Design  : SPL_Mapper
9 // Purpose : This script generates a Verilog netlist of the current design or from a specific cell of the design. The output is an IEEE 1364-2008 compliant Verilog HDL file that contains netlist information obtained from the input
10 //          design files.
11 //          Device : xc7a3tftg256-1L
12 //          time scale: 1 ps / 1 ps
13
14 module SPL
15   (MISO_wrapper_IBUF,
16   S,
17   tx_valid_reg,
18   Q,
19   lcount_Reg[1:0],
20   L,
21   mem_Reg,
22   mem_Reg,
23   mem_Reg,
24   mem_Reg[1:0],
25   CLK_wrapper_IBUF,
26   tx_valid_wrapper,
27   rst_n_wrapper_IBUF,
28   D,
29   SS_n_wrapper_IBUF);
30   output MISO_wrapper_IBUF;
31   output tx_valid_wrapper;
32   output tx_valid_Reg;
33   output [7:0]Q;
34   output [2:0]lcount_Reg[1:0];
35   output mem_Reg;
36   output mem_Reg;
37   output mem_Reg[1:0];
38   output VFSH_gray_cst[0:1],L_1,n_0;
39   input clk_wrapper_IBUF_IBUF;
40   input tx_valid_wrapper;
41   input rst_n_wrapper_IBUF;
42   input [9:0]D;
43   input SS_n_wrapper_IBUF;
44   wire control_read;
45   wire control_read_d1;
46   wire [9:0]D;
47   wire [9:0]E;
48   wire VFSH_gray_cst[0:1],L_1,n_0;
49   wire VFSH_gray_cst[1:2],L_1,n_0;
50   wire VFSH_gray_cst[2:3],L_1,n_0;
51   wire VFSH_gray_cst[3:4],L_1,n_0;
52   wire MISO_wrapper_IBUF;
53   wire [7:0]Q;
54   wire tx_valid_Reg;
55   wire SS_n_wrapper_IBUF;
56   wire clk_wrapper_IBUF_IBUF;
57   wire control_read_addr;
58   wire control_read_d1_d_1_n_0;
```