2025

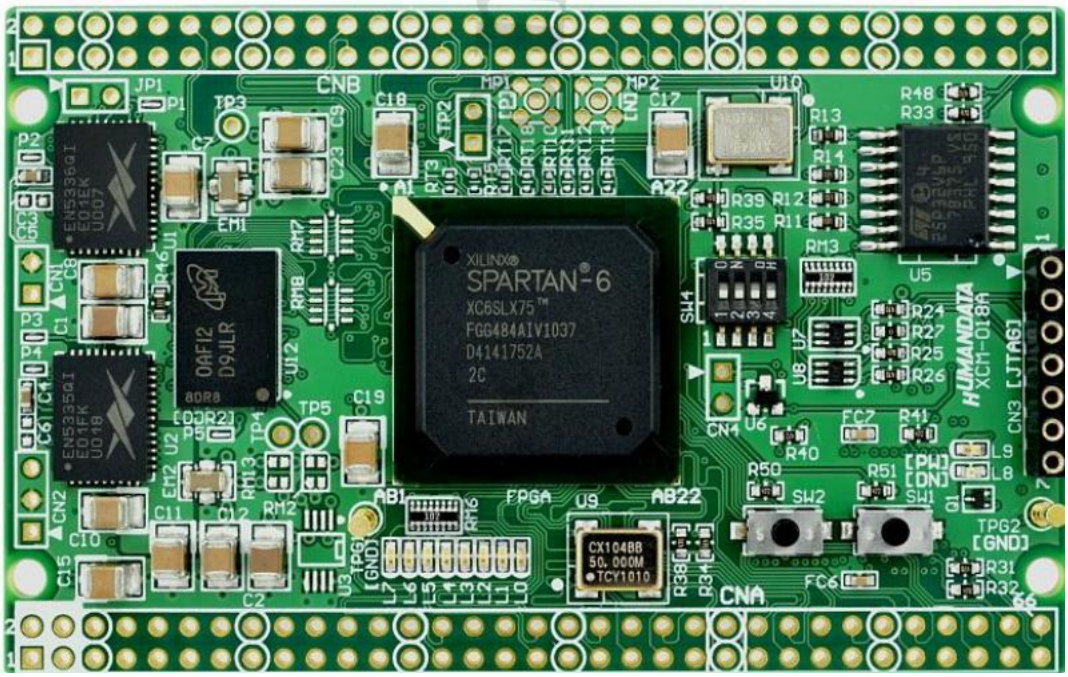
Digital IC Design

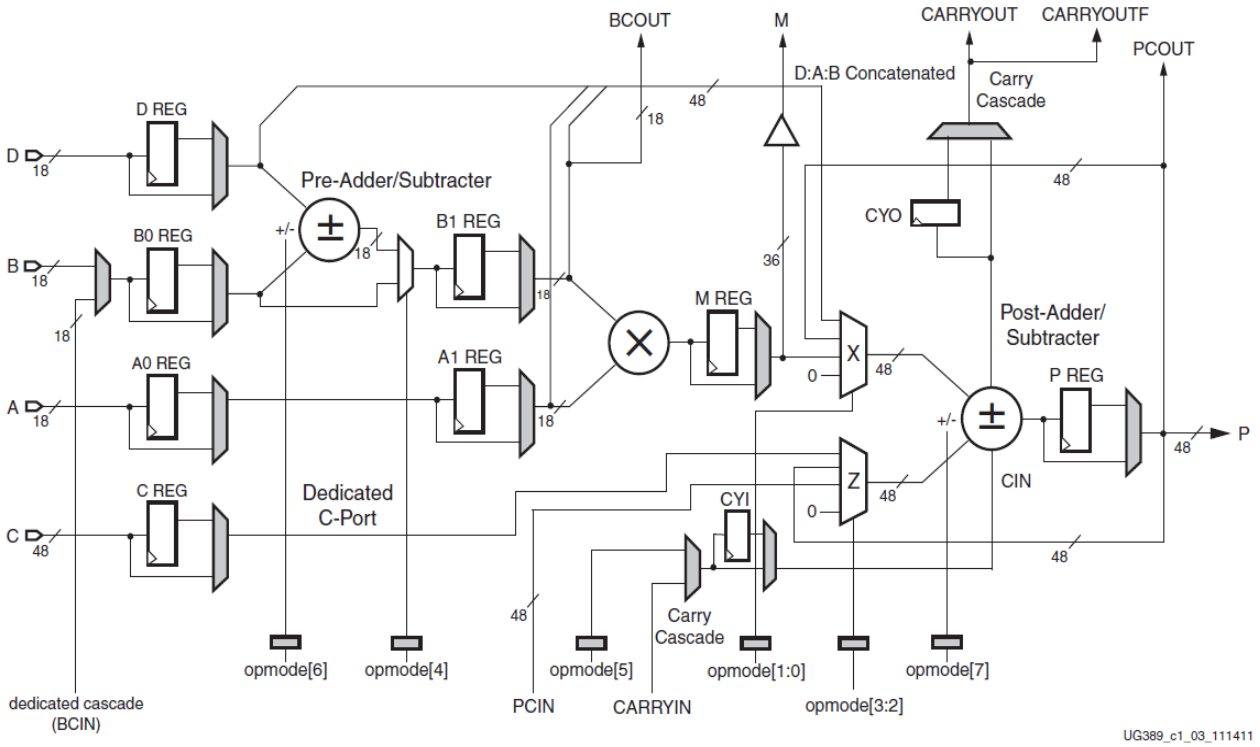
Project : DSP48A1

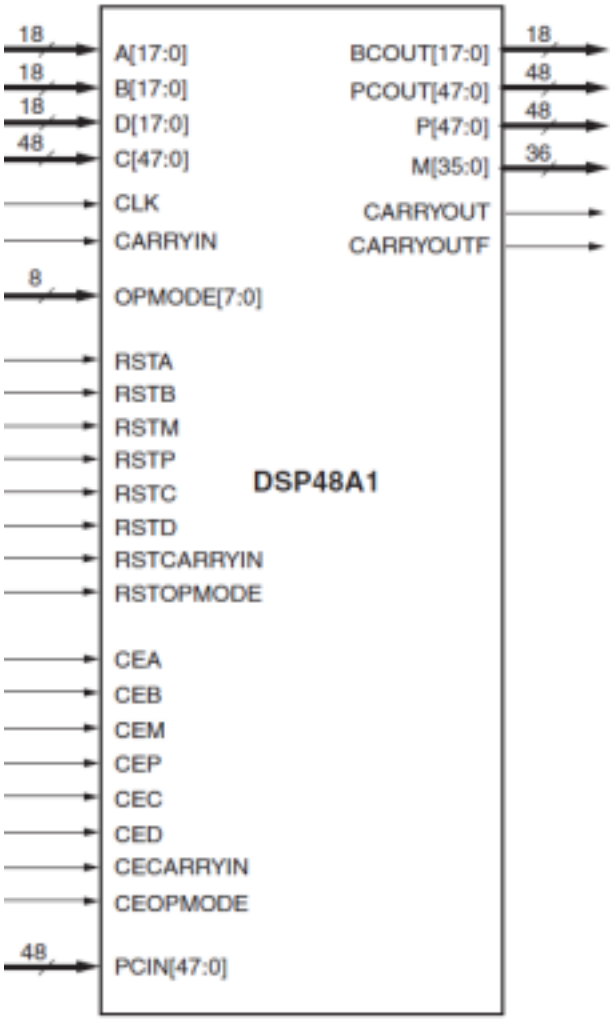
PREPARED BY: ABD ALRAHMAN ALI ELTAHER

FPGA Board Used: xc7a200tffg1156-3

Xilinx Spartan-6 FPGA Board




BCOUT
M
CARRYOUT
CARRYOUTF
PCOUT
D:A:B Concatenated
Carry Cascade
D REG
Pre-Adder/Subtracter
B1 REG
B0 REG
CYO
M REG
Post-Adder/ Subtracter
A0 REG
A1 REG
P REG
C REG
Dedicated C-Port
CYI
CIN
Carry Cascade
opmode[6]
opmode[4]
opmode[5]
opmode[1:0]
opmode[7]
dedicated cascade (BCIN)
PCIN
CARRYIN
opmode[3:2]
UG389_c1_03_111411


A[17:0]
B[17:0]
D[17:0]
C[47:0]
CLK
CARRYIN
OPMODE[7:0]
RSTA
RSTB
RSTM
RSTP
RSTC
RSTD
RSTCARRYIN
RSTOPMODE
CEA
CEB
CEM
CEP
CEC
CED
CECARRYIN
CEOPMODE
PCIN[47:0]
DSP48A1
BCOUT[17:0]
PCOUT[47:0]
P[47:0]
M[35:0]
CARRYOUT
CARRYOUTF

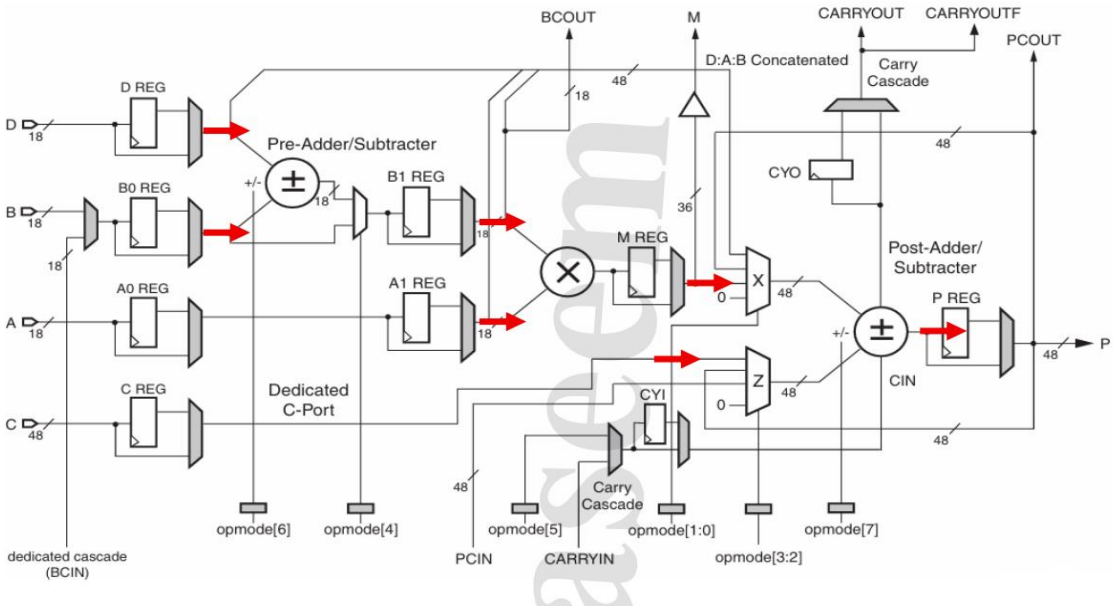
Code:

```
1   // Mux_with_dff
2   module Mux_with_dff(clk,en,rst,d,out);
3   parameter opmode = 1, RSTYPE = "SYNC",size = 18;
4   input clk,en,rst;
5   input [size-1:0] d ;
6   output reg [size-1:0]out;
7   generate
8       if(opmode)begin
9           if(RSTYPE ==  "SYNC") begin
10              always @(posedge clk) begin
11                  if(rst)
12                      out<=0;
13                  else begin
14                      if(en)
15                          out<=d;
16                  end
17              end
18          end
19          else begin
20              always @(posedge clk or posedge rst) begin
21                  if(rst)
22                      out<=0;
23                  else begin
24                      if(en)
25                          out<=d;
26                  end
27              end
28          end
29      end
30      else begin
31          always @(*) begin
32              out = d ;
33          end
34      end
35  endgenerate
36  endmodule
```

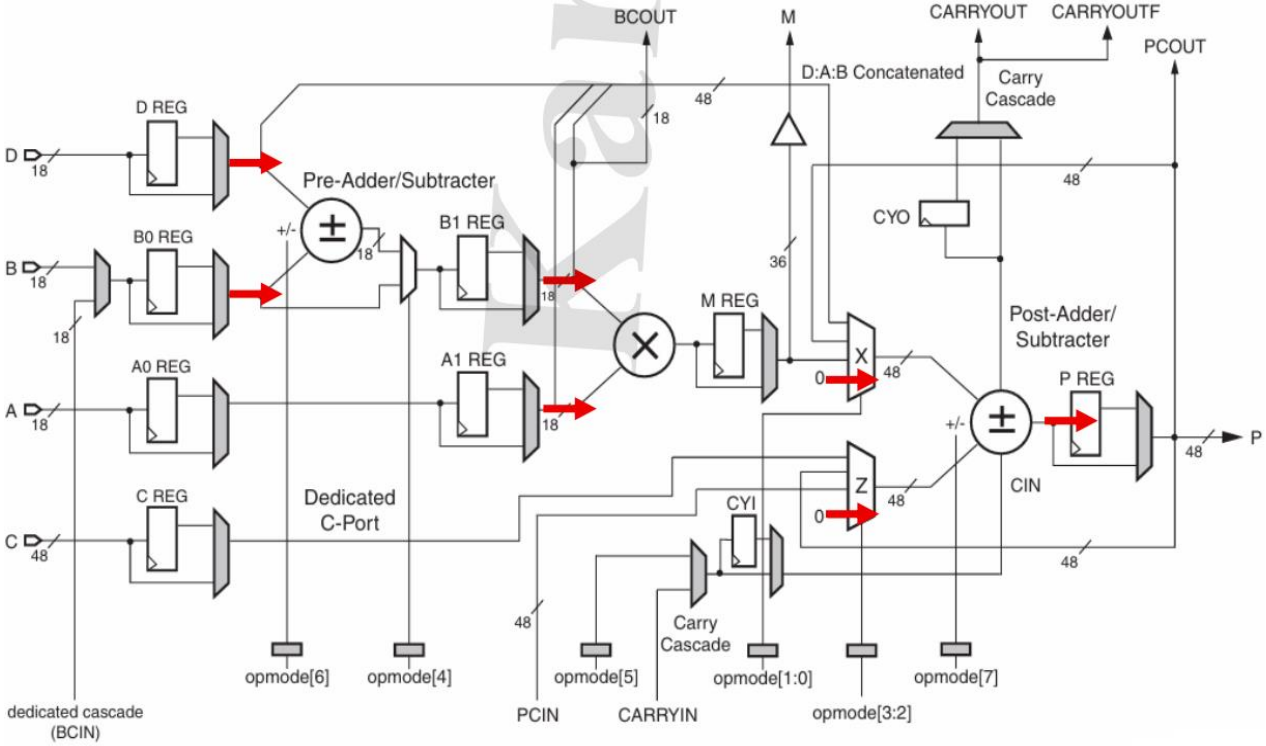
```
// DSP48A1
module DSP48A1(A,B,C,D,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
//parameter.
parameter A0REG = 0,A1REG=1,B0REG=0,B1REG=1,CREG=1,DREG=1,MREG=1,PREG=1,CARRYINREG=1,CARRYOUTREG=1,OPMODEREG = 1,CARRYINSEL="OPMODE5",B_INPUT="DIRECT",RSTTYPE="SYNC";
//input.
input [17:0]A,B,D,BCIN;
input [47:0] PCIN,C;
input [7:0]OPMODE;
input CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
//output
output [47:0] PCOUT,P;
output [17:0]BCOUT;
output [35:0] M ;
output CARRYOUT,CARRYOUTF;
//wire.
wire CYI_in,CYI_out,CYO_in;
wire [17:0]B_INPUT_WIRE,D_out,B0_out,A0_out,B1_in,B1_out,A1_out,Pre_Adder_Subtracter;
wire[47:0] post_Adder_Subtracter,C_out,concat,out_z,out_x,multipler_out_48;
wire [7:0]OPMODE_out;
wire [35:0]  multipler_in,multipler_out;
// B or BCIN or 0
assign B_INPUT_WIRE=(B_INPUT == "DIRECT")?B:(B_INPUT == "CASCADE")?BCIN:0;
//DREG ,B0_out,A0REG and CREG
Mux_with_dff #(.opmode(B0REG),.size(18),.RSTYPE(RSTTYPE))b0reg(.clk(CLK),.en(CEB),.rst(RSTB),.d(B_INPUT_WIRE),.out(B0_out));
Mux_with_dff #(.opmode(A0REG),.size(18),.RSTYPE(RSTTYPE))a0reg(.clk(CLK),.en(CEA),.rst(RSTA),.d(A),.out(A0_out));
Mux_with_dff #(.opmode(DREG),.size(18),.RSTYPE(RSTTYPE))dreg(.clk(CLK),.en(CED),.rst(RSTD),.d(D),.out(D_out));
Mux_with_dff #(.opmode(CREG),.size(48),.RSTYPE(RSTTYPE))creg(.clk(CLK),.en(CEC),.rst(RSTC),.d(C),.out(C_out));
// Pre_Adder_Subtracter
Mux_with_dff #(.opmode(OPMODEREG),.size(1),.RSTYPE(RSTTYPE))opmode6(.clk(CLK),.en(CEOPMODE),.rst(RSTOPMODE),.d(OPMODE[6]),.out(OPMODE_out[6]));
assign Pre_Adder_Subtracter =(OPMODE_out[6] == 1)? (D_out-B0_out):(D_out+B0_out);
// select Pre_Adder_Subtracter or B0_out
Mux_with_dff #(.opmode(OPMODEREG),.size(1),.RSTYPE(RSTTYPE))opmode4(.clk(CLK),.en(CEOPMODE),.rst(RSTOPMODE),.d(OPMODE[4]),.out(OPMODE_out[4]));
assign B1_in = (OPMODE_out[4]== 1)? Pre_Adder_Subtracter:B0_out;
// A1REG and B1REG
Mux_with_dff #(.opmode(B1REG),.size(18),.RSTYPE(RSTTYPE))b1reg(.clk(CLK),.en(CEB),.rst(RSTB),.d(B1_in),.out(B1_out));
Mux_with_dff #(.opmode(A1REG),.size(18),.RSTYPE(RSTTYPE))a1reg(.clk(CLK),.en(CEA),.rst(RSTA),.d(A0_out),.out(A1_out));
// multipler operation.
assign BCOUT=B1_out;
assign multipler_in = B1_out*A1_out;
//MREG
Mux_with_dff #(.opmode(MREG),.size(36),.RSTYPE(RSTTYPE))mreg(.clk(CLK),.en(CEM),.rst(RSTM),.d(multipler_in),.out(multipler_out));
//buffer M
assign M = ~(~multipler_out);
//(multipler_out_48) is 48 bit
assign multipler_out_48=multipler_out;
// concatination.
assign concat ={D_out[11:0],A1_out,B1_out};
//Mux_4_x
Mux_with_dff #(.opmode(OPMODEREG),.size(2),.RSTYPE(RSTTYPE))opcode10(.clk(CLK),.en(CEOPMODE),.rst(RSTOPMODE),.d(OPMODE[1:0]),.out(OPMODE_out[1:0]));
assign out_x =(OPMODE_out[1:0] == 2'b00)? 48'd0:(OPMODE_out[1:0] == 2'b01)? multipler_out_48:(OPMODE_out[1:0] == 2'b10)? P: concat ;
// Mux_4_z
Mux_with_dff #(.opmode(OPMODEREG),.size(2),.RSTYPE(RSTTYPE))opcode32(.clk(CLK),.en(CEOPMODE),.rst(RSTOPMODE),.d(OPMODE[3:2]),.out(OPMODE_out[3:2]));
assign out_z =(OPMODE_out[3:2] == 2'b00)? 48'd0:(OPMODE_out[3:2] == 2'b01)? PCIN:(OPMODE_out[3:2] == 2'b10)? P: C_out ;
// select OPMODE_out[5] or CARRYIN or 0 .
Mux_with_dff #(.opmode(OPMODEREG),.size(1),.RSTYPE(RSTTYPE))opmode5(.clk(CLK),.en(CEOPMODE),.rst(RSTOPMODE),.d(OPMODE[5]),.out(OPMODE_out[5]));
assign CYI_in=(CARRYINSEL == "OPMODE5")?OPMODE_out[5]:(CARRYINSEL == "CARRYIN")?CARRYIN:0;
//CYI.
Mux_with_dff #(.opmode(CARRYINREG),.size(1),.RSTYPE(RSTTYPE))cyireg(.clk(CLK),.en(CECARRYIN),.rst(RSTCARRYIN),.d(CYI_in),.out(CYI_out));
// post_Adder_Subtracter
Mux_with_dff #(.opmode(OPMODEREG),.size(1),.RSTYPE(RSTTYPE))opmode7(.clk(CLK),.en(CEOPMODE),.rst(RSTOPMODE),.d(OPMODE[7]),.out(OPMODE_out[7]));
assign {CYO_in,post_Adder_Subtracter} = (OPMODE_out[7] == 1)? (out_z-(out_x+CYI_out)):(out_z+out_x+CYI_out);
// PREG
Mux_with_dff #(.opmode(PREG),.size(48),.RSTYPE(RSTTYPE))preg(.clk(CLK),.en(CEP),.rst(RSTP),.d(post_Adder_Subtracter),.out(P));
assign PCOUT = P;
// CYO
Mux_with_dff #(.opmode(CARRYOUTREG),.size(1),.RSTYPE(RSTTYPE))cyoreg(.clk(CLK),.en(CECARRYIN),.rst(RSTCARRYIN),.d(CYO_in),.out(CARRYOUT));
assign CARRYOUTF =CARRYOUT;
endmodule
```

Testbench:

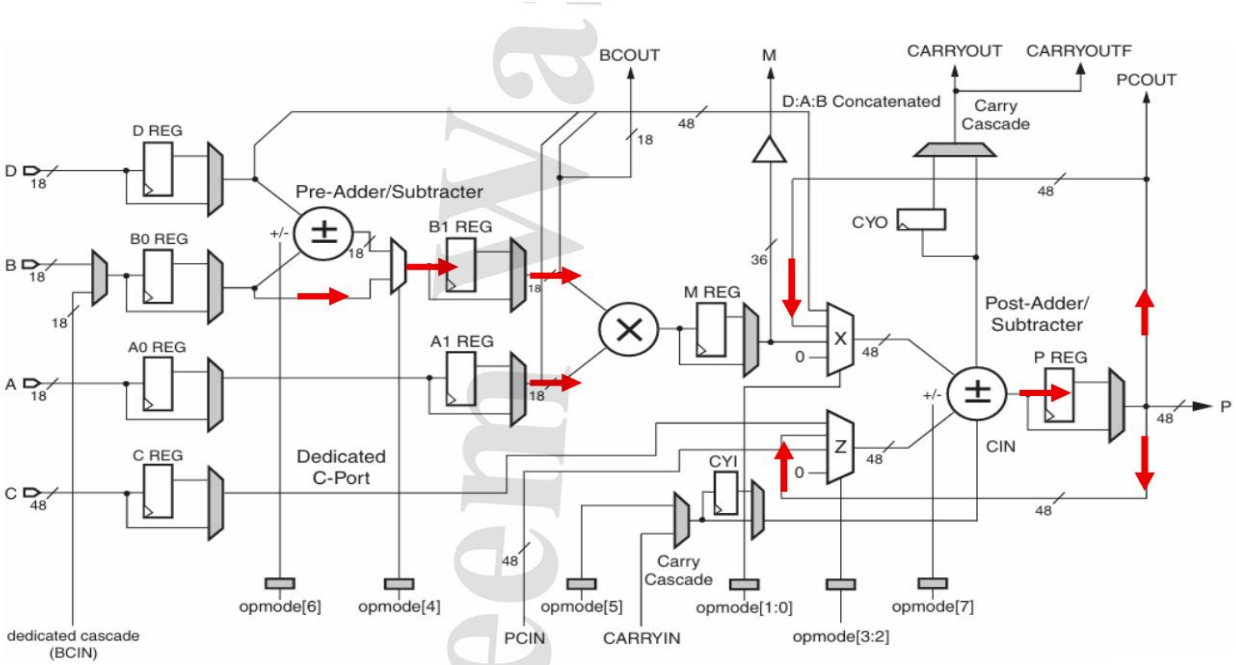
- **Path 1**



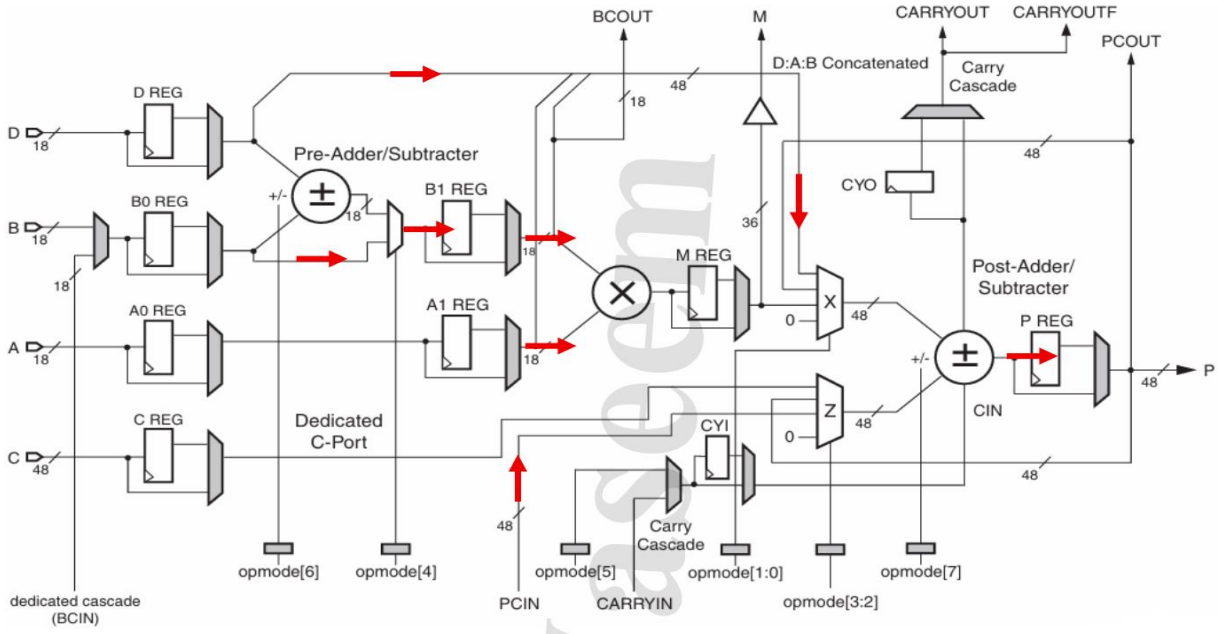
- **Path 2**



- **Path 3**


BCOUT
M
CARRYOUT
CARRYOUTF
PCOUT
D:A:B Concatenated
Carry Cascade
D REG
Pre-Adder/Subtracter
B1 REG
B0 REG
M REG
CYO
Post-Adder/ Subtracter
A0 REG
A1 REG
P REG
P
C REG
Dedicated C-Port
CYI
CIN
opmode[6]
opmode[4]
opmode[5]
opmode[1:0]
opmode[7]
opmode[3:2]
PCIN
CARRYIN
dedicated cascade (BCIN)

Path 4


BCOUT
M
CARRYOUT
CARRYOUTF
PCOUT
D:A:B Concatenated
Carry Cascade
D REG
Pre-Adder/Subtracter
B1 REG
B0 REG
M REG
CYO
Post-Adder/ Subtracter
A0 REG
A1 REG
P REG
P
C REG
Dedicated C-Port
CYI
CIN
opmode[6]
opmode[4]
opmode[5]
opmode[1:0]
opmode[7]
opmode[3:2]
PCIN
CARRYIN
dedicated cascade (BCIN)

Testbench code:

```
module DSP48A1_tb();
parameter A0REG= 0,A1REG=1,B0REG_tb=0,B1REG=1,CREG=1,DREG=1,MREG=1,PREG=1,CARRYINREG=1,CARRYOUTREG=1,OPMODEREG = 1,CARRYINSEL="OPMODE5",B_INPUT="DIRECT",RSTTYPE="SYNC";
//input
reg [17:0]A,B,D,BCIN;
reg [47:0] PCIN,C;
reg [7:0]OPMODE;
reg CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
//out dut
wire [47:0] PCOUT_dut,P_dut;
wire [17:0]BCOUT_dut;
wire [35:0] M_dut ;
wire CARRYOUT_dut,CARRYOUTF_dut;
//output expect
reg [47:0] PCOUT_expect,P_expect;
reg [17:0]BCOUT_expect;
reg [35:0] M_expect ;
reg CARRYOUT_expect,CARRYOUTF_expect;
// instantiation
DSP48A1 #( A0REG,A1REG,B0REG_tb,B1REG,CREG,DREG,MREG,PREG,CARRYINREG,CARRYOUTREG,OPMODEREG ,CARRYINSEL,B_INPUT,RSTTYPE)dut(A,B,C,D,CLK,CARRYIN,
            OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,
            CEOPMODE,PCIN,BCOUT_dut,PCOUT_dut,P_dut,M_dut,CARRYOUT_dut,CARRYOUTF_dut);
initial begin
    CLK = 0;
    forever
        #1 CLK = ~ CLK ;
end
initial begin
    //verify reset operation.
    RSTA=1;RSTB=1;RSTM=1;RSTP=1;RSTC=1;RSTD=1;RSTCARRYIN=1;RSTOPMODE=1;CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;
    A = $random;B= $random;D= $random;BCIN= $random;PCIN= $random;C= $random;OPMODE= $random;CARRYIN= $random;
    @(negedge CLK);
     PCOUT_expect=0;P_expect=0;BCOUT_expect=0;CARRYOUT_expect=0;CARRYOUTF_expect=0; M_expect =0;
    if(PCOUT_dut !=PCOUT_expect || P_dut !=P_expect || BCOUT_dut !=BCOUT_expect || M_dut !=M_expect || CARRYOUT_dut != CARRYOUT_expect || CARRYOUTF_dut != CARRYOUTF_expect)begin
        $display("error : P_dut=%h,P_expect =%h  ",P_dut,P_expect);
        $stop;
    end
    RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;
    //verify dsp path 1 .
    OPMODE = 8'b11011101;
    A = 20;B=10;C=350;D=25;
    BCIN =$random;PCIN=$random;CARRYIN=$random;
    @(negedge CLK);
    @(negedge CLK);
    @(negedge CLK);
    @(negedge CLK);
     BCOUT_expect = 'hf ;M_expect='h12c;P_expect='h32;PCOUT_expect='h32;CARRYOUT_expect=0;CARRYOUTF_expect=0;
    if(PCOUT_dut !=PCOUT_expect || P_dut !=P_expect || BCOUT_dut !=BCOUT_expect || M_dut !=M_expect || CARRYOUT_dut != CARRYOUT_expect || CARRYOUTF_dut != CARRYOUTF_expect)begin
        $display("error : P_dut=%h,P_expect =%h  ",P_dut,P_expect);
        $stop;
    end
    //verify dsp path 2 .
    OPMODE =8'b00010000;
    A = 20;B=10;C=350;D=25;
    BCIN =$random;PCIN=$random;CARRYIN=$random;
    @(negedge CLK);
    @(negedge CLK);
    @(negedge CLK);
    BCOUT_expect = 'h23; M_expect = 'h2bc; P_expect =0; PCOUT_expect =0;CARRYOUT_expect = 0; CARRYOUTF_expect = 0;
    if(PCOUT_dut !=PCOUT_expect || P_dut !=P_expect || BCOUT_dut !=BCOUT_expect || M_dut !=M_expect || CARRYOUT_dut != CARRYOUT_expect || CARRYOUTF_dut != CARRYOUTF_expect)begin
        $display("error : P_dut=%h,P_expect =%h  ",P_dut,P_expect);
        $stop;
    end
    // verify dsp path 3.
    OPMODE = 8'b00001010;
    A = 20;B=10;C=350;D=25;
    BCIN =$random;PCIN=$random;CARRYIN=$random;
    @(negedge CLK);
    @(negedge CLK);
    @(negedge CLK);
    BCOUT_expect = 'ha; M_expect = 'hc8;
    if(PCOUT_dut !=PCOUT_expect || P_dut !=P_expect || BCOUT_dut !=BCOUT_expect || M_dut !=M_expect || CARRYOUT_dut != CARRYOUT_expect || CARRYOUTF_dut != CARRYOUTF_expect)begin
        $display("error : P_dut=%h,P_expect =%h  ",P_dut,P_expect);
        $stop;
    end
    // verify dsp path 4.
     OPMODE = 8'b10100111;
    A = 5; B = 6; C = 350; D = 25; PCIN = 3000;BCIN =$random;CARRYIN=$random;
    @(negedge CLK);
    @(negedge CLK);
    @(negedge CLK);
    BCOUT_expect = 'h6; M_expect = 'h1e;P_expect = 'hfe6fffec0bb1;PCOUT_expect = 'hfe6fffec0bb1; CARRYOUT_expect = 1;CARRYOUTF_expect = 1;
    @(negedge CLK);
    if(PCOUT_dut !=PCOUT_expect || P_dut !=P_expect || BCOUT_dut !=BCOUT_expect || M_dut !=M_expect || CARRYOUT_dut != CARRYOUT_expect || CARRYOUTF_dut != CARRYOUTF_expect)begin
        $display("error : P_dut=%h,P_expect =%h  ",P_dut,P_expect);
        $stop;
    end
    //stop
    $stop;
end
endmodule
```

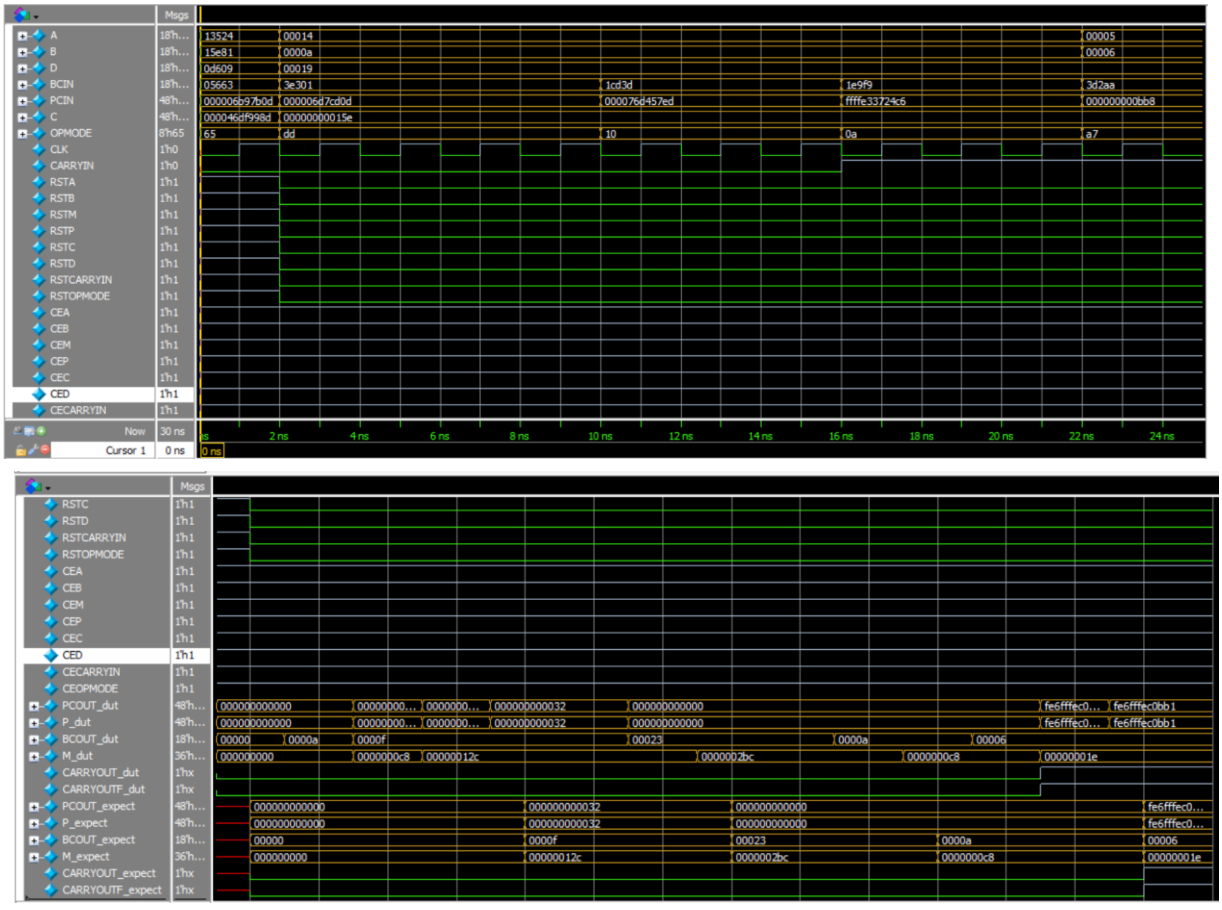
Do file:

run_project - Notepad

File Edit Format View Help

```
vlib work
vlog project_code.v project_tb.v
vsim -voptargs=+acc work.DSP48A1_tb
add wave *
run -all
#quit -sim
```

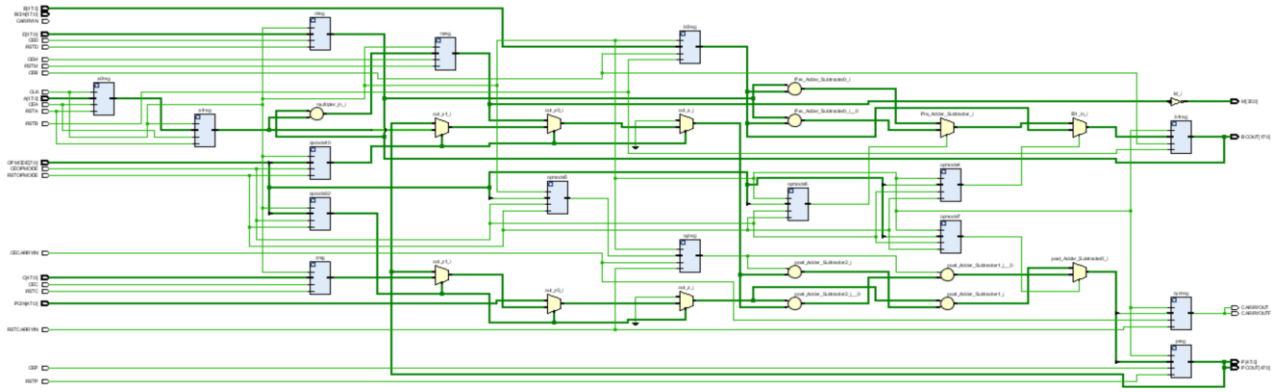
Wave:



➢ Elaboration

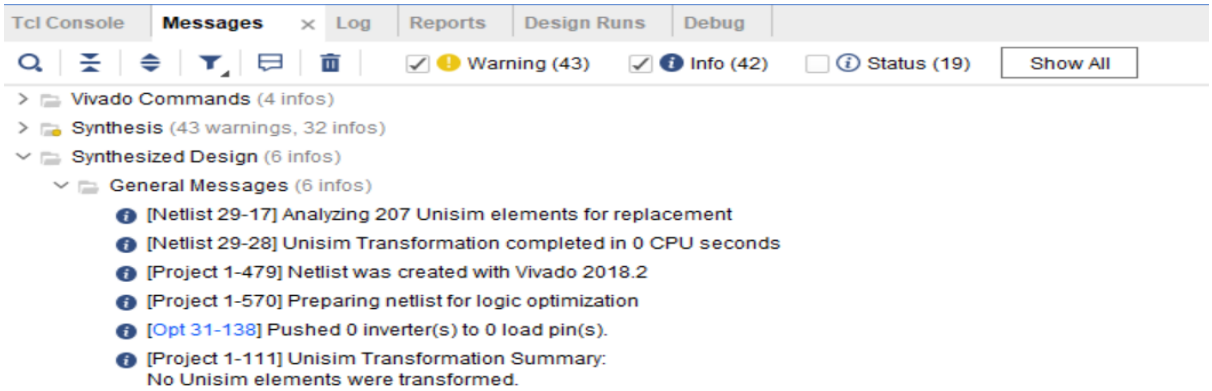
Messages:

Schematic:



➢ Synthesis:

Messages:



Utilization:

Name	Slice LUTs (134600)	Slice Registers (269200)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
N DSP48A1	309	160	1	327	1
a1reg (Mux_with_dff__...	0	18	0	0	0
b1reg (Mux_with_dff__...	0	18	0	0	0
creg (Mux_with_dff__p...	0	48	0	0	0
cyireg (Mux_with_dff__...	2	1	0	0	0
cyoreg (Mux_with_dff_...	0	1	0	0	0
dreg (Mux_with_dff__p...	0	18	0	0	0
mreg (Mux_with_dff__...	0	0	1	0	0
opcode10 (Mux_with_d...	145	2	0	0	0
opcode32 (Mux_with_d...	123	2	0	0	0
opmode4 (Mux_with_d...	18	1	0	0	0
opmode5 (Mux_with_d...	0	1	0	0	0
opmode6 (Mux_with_d...	17	1	0	0	0
opmode7 (Mux_with_d...	3	1	0	0	0
preg (Mux_with_dff__p...	0	48	0	0	0

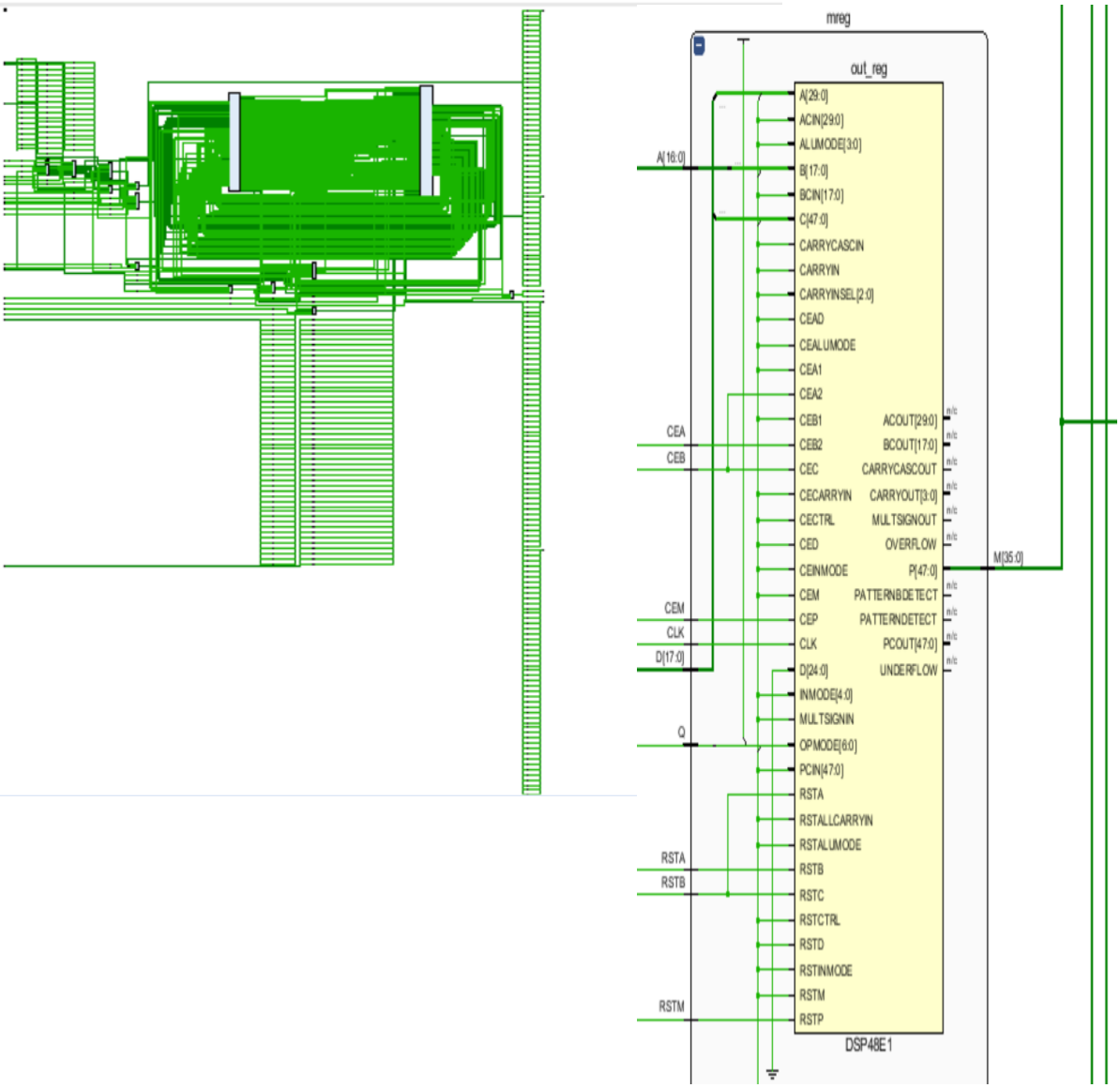
Timing:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.366 ns	Worst Hold Slack (WHS):	0.182 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	106	Total Number of Endpoints:	106	Total Number of Endpoints:	162

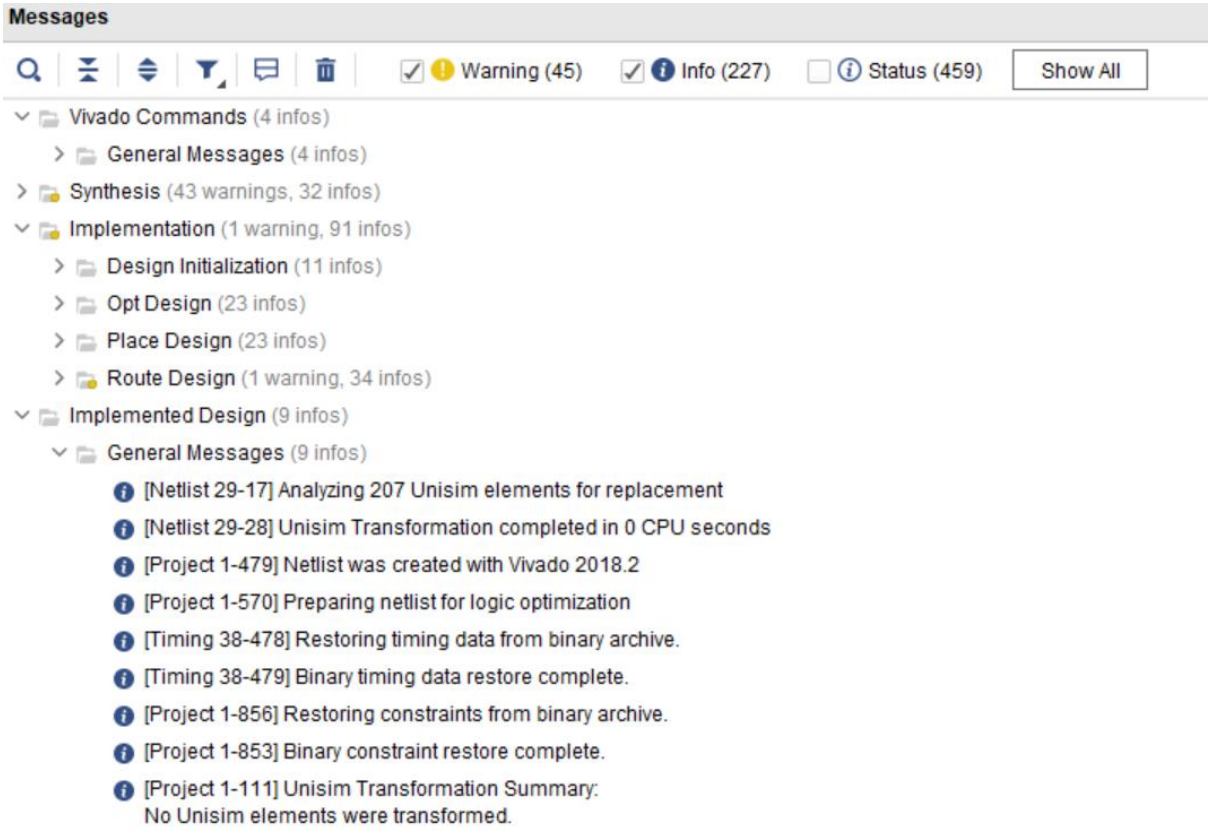
All user specified timing constraints are met.

schematic:



➢ Implementation

Messages:



Utilization

Name	Slice LUTs (133800)	Slice Registers (267600)	Slice (33450)	LUT as Logic (133800)	LUT Flip Flop Pairs (133800)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP48A1	308	179	127	308	51	1	327	1
a1reg (Mux_with_dff__...	0	18	9	0	0	0	0	0
b1reg (Mux_with_dff__...	0	36	14	0	0	0	0	0
creg (Mux_with_dff__p...	0	48	19	0	0	0	0	0
cyireg (Mux_with_dff__...	2	1	2	2	1	0	0	0
cyoreg (Mux_with_dff_...	0	2	2	0	0	0	0	0
dreg (Mux_with_dff__p...	0	18	11	0	0	0	0	0
mreg (Mux_with_dff__...	0	0	0	0	0	1	0	0
opcode10 (Mux_with_d...	145	2	66	145	0	0	0	0
opcode32 (Mux_with_d...	123	2	60	123	0	0	0	0
opmode4 (Mux_with_d...	18	1	9	18	0	0	0	0
opmode5 (Mux_with_d...	0	1	1	0	0	0	0	0
opmode6 (Mux_with_d...	17	1	6	17	0	0	0	0
opmode7 (Mux_with_d...	3	1	4	3	0	0	0	0
preg (Mux_with_dff__p...	0	48	12	0	0	0	0	0

Timing:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.054 ns	Worst Hold Slack (WHS):	0.240 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	125	Total Number of Endpoints:	125	Total Number of Endpoints:	181

All user specified timing constraints are met.

Device: