ARM AVIP

BP062 AMBA® 3 AXI™ Protocol Checker

Release Note (r0p1-00rel0)

AMBA 3 AXI Protocol Checker (BP062)

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Proprietary notice

Document confidentiality status

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Product status

The information in this document relates to the BP062-BU-01000-r0p1-00rel0 release.

Web address

http://www.arm.com

Feedback and support

ARM Limited welcomes feedback on both the product and the documentation.

Feedback on this document

If you have any comments about this document, please send email to errata@arm.com giving:

- The document title
- The document number
- The page number(s) to which your comments refer
- A concise explanation of your comments

General suggestion for additions and improvements are also welcome.

Feedback on the AMBA 3 AXI Protocol Checker

If you have any comments or suggestions about this product, please contact your supplier giving:

- The product name
- A concise explanation of your comments.

Alternatively you can email support-axi@arm.com.

Change history

Issue	Date	Change
1.0	09 July 2009	Release information for r0p1-00rel0

Contents

1 Deliverables

Introduction

The BP062 AMBA 3 AXI Protocol Checker is a verification and validation product designed to work with a range of different user environments and usage scenarios. The underlying goal is to provide coverage points for the AMBA 3 AXI protocol.

Disk space required

The BP062 deliverables require approximately 1 MB of disk space when installed.

Deliverables

This release note refers to the installation of the bundle BP062-BU-01000-r0p1-00rel0 obtained through ARM's IP delivery server. The deliverables are supplied as a single UNIX compressed tar file which has been gzipped. The download filename will be of the form:

```
<download_name>.tgz
```

where `<download_name>` is typically of the form `arm-download-<transaction_id>` and where `<transaction_id>` is a unique 6 digit number identifying the specific download.

This tar file contains a number of parts bundled together in a single design directory structure to form the release. Table 1-1 lists the part numbers and their descriptions.

Table 1-1: Parts included in bundle BP062-BU-01000-r0p1-00rel0

Part Number	Description
Documentation	
BP062-DC-06002-r0p1-00rel0	AMBA 3 AXI Protocol Checker Release Note
BP062-DC-08001-r0p1-00rel0	AMBA 3 AXI Protocol Checker User Guide
Other parts	
BP062- VL-70002-r0p1-00rel0	Verilog OVL Assertions
BP062- VL-70004-r0p1-00rel0	System Verilog Assertions (SVA)
BP148- MN-22001-r0p0-00rel0	AXI Protocol Support Synthesizable Verilog

NOTE: These deliverable part numbers do not exist in the installed directory structure as distinguishable parts and are defined for contractual purposes only.

2 Installation

Unpacking files

Relocate the `tgz` file to an appropriate installation location and unpack the *.tgz file using the GNU tar utility as follows:

```
gtar –zxvf <download_name>.tgz
```

NOTE: Use GNU tar version 1.13.25 (or later) to unpack the deliverables as other versions of tar have problems dealing with very long path names. To find the version of gtar being used type `gtar –-version`

This extracts the deliverables into a directory named the same as the bundle number BP062-BU-01000-r0p1-00rel0.

Figure 2-1 shows the top-level directory structure created after unpacking the tar file:

```
BP062-BU-01000-r0p1-00rel0/
|-- docs
|   |-- BP062-RLNC-000288-r0p1-00rel0_amba_axi_pc_release_note.pdf
|   `-- DUI0305C_amba_axi_pc_ug.pdf
|-- sva
|   `-- AxiPC.sv
`-- verilog
    |-- Axi.v
    `-- AxiPC.v
```

Figure 2-1: Top-level directory structure after unpacking the bundle

BP062 Usage

For details on how to use the BP062 AMBA 3 AXI Protocol Checker please refer to the BP062 AXI Protocol Assertions User Guide (ARM DUI 0305).

To use the Verilog OVL version of the AMBA™ 3 AXI™ Protocol Checker, you must install the OVL assertion library *.vlib and *.h components and you must configure your simulator as described in the User Guide.

The OVL assertion library can be downloaded via the downloads section of www.eda.org/ovl.

Product documents supplied

The following documents are supplied with BP062 AMBA 3 AXI Protocol Assertions:

- BP062 AXI Protocol Assertions User Guide (ARM DUI 0305)
- BP062 AXI Protocol Assertions Release Note (BP062-RLNC-000288)

The documents are located in the following directory:

```
BP062-BU-01000-r0p1-00rel0/docs
```

The User Guide defines the features, interfaces and programmers model of the product.

3 Tools

This release of BP062 has been developed and tested with tool versions listed below.

Verilog OVL v2.3

SystemVerilog version 3.1a.

Cadence Incisive 8.10.007

Mentor ModelSim SE 6.3g

Synopsys VCS 2006.06-SP1-7

Users may experience problems with v2006.06-SP1-7 VCS when running simulations with the AxiPC under Solaris. In these cases using VCS v2006.06-SP2-5 solves the problem.

4 Third-party IP Requirements

The following library will need to be downloaded and installed separately before using the AMBA 3 AXI Protocol Checker:

- Accellera OVL assertion library v2.3

This library is required to run any simulation which is to include the AXI protocol checker and can be downloaded from http://www.accellera.org.

NOTE: If OVL assertions are never enabled then you are not required to install the Accellera OVL library.

5 Product Status

EAC Quality Definition

Early Access release status has a particular meaning to ARM of which the recipient must be aware. A deliverable so designated has satisfactorily achieved all criteria for its promotion to a Mature Release status. It may be delivered in accordance with the contract and be expected to perform as described in the data-sheet. However, there remain some elements of uncertainty, which cannot finally be validated until the deliverable has been successfully deployed by customers. Accordingly, the recipient of a deliverable with Early Access-Release status may be directly contributing to the final stage of approval of that deliverable.

In due course, after the Early Access-Release the product status will change to Mature. It should be noted that Support for the Early Access release of the deliverable will only be provided by ARM to a recipient who has a current support and maintenance contract for the deliverable.

Limitations or known issues in this release

- To synthesis the AMBA 3 AXI Protocol Checker on to an emulation box the internal signals `i_RecommendOn` and `i_RecMaxWaitOn` may need to be statically defined as 0 or 1 outside of the initial statement.
- Some simulators can have timing issues, but these can be worked around by using the AXI_*_CLK macro to clock the assertions on the negedge (but the auxiliary logic on the posedge). See user guide for details.
- The SVA version of AxiPC deliberately does not use the *_PropertyType parameters. The reason is that assume in System Verilog does not allow an action block – so you will not see an error report in simulation (unlike the Verilog OVL version). The advantage with this approach is that simulations will check that any assumptions used for formal verification are sound (just like the OVL version). The disadvantage is that you cannot ignore SV assertions (aside from recommended rules),
- If users have difficulty fitting the design onto an emulation box the design can be constrained by reducing parameters such as MAXRBURSTS and MAXWBURSTS.

Standards compliance

AXI interface is tested to:

AMBA® 3 AXI Protocol v1.0 Specification (ARM IHI 0022)

6 Differences between prior releases and r0p1-00rel0

The following changes have been implemented in this version of the product.

Enhancements

- Parameter EXMON_WIDTH was added to control the number of exclusive access monitors. In the r0p0 version the exclusive access monitor logic was linked to the ID_WIDTH parameter. As ID_WIDTH increases the size of the monitor logic would grow exponentially. It is now possible to use larger values for ID_WIDTH without exceeding the capacity of the simulator tool.
- Added assertion AXI_AUXM_EXCL_OVERFLOW to warn that the EXMON_WIDTH parameter needs to be increased as there are more exclusive access sequences in progress than the monitor can track.
- The MAXWBURSTS parameter can now be set to 1.
- Added assertion AXI_RECS_BRESP to warn that a slave should not give a write response before the write address.
- Extended assertion AXI_ERRM_WDATA_NUM to cover cases where the number of beats in a write burst is exceeded by leading write data beats that have completed before the write address has been issued.
- Added assertion AXI_ERRS_RDATA_X to detect X values in valid read data byte lanes.
- Modified assertion AXI_ERRS_RDATA_STABLE to only monitor valid read data byte lanes.
- Extended assertions AXI_ERRM_AWLOCK_START, AXI_ERRM_AWLOCK_LAST, AXI_ERRM_AWLOCK_END, AXI_ERRM_ARLOCK_START, AXI_ERRM_ARLOCK_LAST and AXI_ERRM_ARLOCK_END to cover transactions with leading write data.
- Extended assertions AXI_ERRM_AWLOCK_CTRL and AXI_ERRM_ARLOCK_CTRL to cover cases where a locked read and a locked write are issued simultaneously.
- Extended assertion AXI_ERRM_WSTRB to cover cases where the write response leads the write address.
- Extended assertion AXI_RECM_EXCL_PAIR to cover cases where a non-exclusive read of the same ID as an exclusive sequence starts between the exclusive read and completes in the same cycle as the exclusive write address.

OVL Specific

- Updated to the Accellera standard v2.* versions
- DATA_WIDTH parameter check assertion changed to avoid triggering on X at time 0 of a simulation.

7 Support and maintenance

Please contact support-axi@arm.com regarding any issues with the installation, content or use of this release and a member of the ARM Product Support Group will log your query in the support database and respond as soon as possible. Note that Support for this release of the product is only provided by ARM to a recipient who has a current support and maintenance contract for the product.

Any issues that arise subsequent to this release are to be documented in a BP062 Errata Notice document and re-issued as required.