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Basic Static Timing Analysis

Course Version 1.2

Lab Manual **Revision 1.0**

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Module 9: Setting Timing Constraints

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Lab 9-1 Setting Up the Database

Objective: To download and set up the course database.

Software Requirements

You can use any synthesis tool to load the constraints and run the synthesis and analyze the results.

The manner in which this lab was setup, it uses the following software:

- SSV162 (Tempus™ Timing Signoff Solution 16.2 version software)

Linux Instructions for the Database

The software for the course runs only on Linux, so there are no PC or UNIX instructions for the database.

1. After downloading the database file, you must uncompress it using the following commands:

   ```
   gunzip BSTA_1_2.tar.gz
   tar xvf BSTA_1_2.tar
   ```

   These commands create a directory called *bsta_labs*.

   Make sure that you read the *README* file in the *bsta_labs* directory concerning any specific sub-versions of the software to use with these labs.

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Lab 9-2 Setting Timing Constraints

Objective: To write your constraints for a design in a Manual format.

In this lab, you edit a *constraints.sdc* file and add constraints according to a design specification. After editing the file, you compare it with the provided solution.

Setting Constraints

1. Change to the *work* directory.

```
cd bsta_labs/work
```

2. Use the following specification to write your constraints into the *constraints.sdc* file:

   Note: Use your own favorite text editor to edit the *constraints.sdc* file.

   - Use the slow operating conditions from the *slow* library.
   - Use wire-load mode *top*.
   - Use wire-load model *custom_high* from the library *wireloadlib*.
   - All input ports have a drive strength of 0.3ns per pF.
   - All output ports will have a capacitive load of 300 femtofarads (notice the units – SDC you specify in picofarads).
   - Continue the constraints creation using the following table:

Port	Specification
xxin_ORSCLK	Clock Name: ORSCLK
	Period: 5ns
	Waveform: {0 2.5} (50% duty cycle)
FtiCoreClk	Clock Name: CORECLK
	Period: 2.5ns
	Waveform: {0 2.5} (50% duty cycle)
All inputs	Input delay: 1ns
	Related clock: CORECLK
Reset,	Input delay: 0ns
xxin_ORSCLK,	
and FtiCoreClk,	
All outputs	Output delay: 1ns
	Related clock: CORECLK
xxin_ORSCLK,	Skew: 100ps
and FtiCoreClk	Clock jitter: 0ns

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3. Add an additional constraint to the *constraints.sdc*:

```
set_dont_touch fticustomc
```

4. Save the *constraints.sdc* file.

Summary

This exercise gives you a good idea of what you need to do to write your constraints.

Compare the constraints you have created with the ones in the *solutions* folder.

Note: The constraints you have written do not have to match exactly one-on-one with all the constraints in the solutions folder. There are a few extras in the solutions that were used to create the netlist for use in the next lab.

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Module 11: Analyzing a Timing Report

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Lab 11-1 Analyzing the Timing in a Design

Objective: To analyze timing using the timing reports.

In this lab, you use the information in a timing report to debug a design that is not meeting timing.

Generating Timing Reports

In this section, you run Tempus™ software to generate the necessary timing reports for analysis.

1. Change to the *work* directory.

   ```
   cd bsta_labs/work
   ```

2. Run the following command to start Tempus Timing Signoff Solution and load the necessary reports for timing:

   ```
   tempus -files run_tempus.tcl
   ```

   Note: The *run_tempus.tcl* file has commands to run the software. Take a look at the file in a separate window.

   Important: Make sure that Tempus software is installed and is in your path. Also, make sure the software is licensed.

Analyzing a Timing Report

1. Generate a timing report to see whether your design meets timing by entering:

   ```
   report_timing
   ```

   Note: By default, only one worst/most critical path is reported.

   To report additional paths, you can use the *-max_paths <integer>* option.

   Note: You can redirect this report into a file using “>”and look at the file instead.

2. Analyze the timing report.

   What is the slack of this reported worst/most critical path?

   Answer: _____ ps

   Did you meet timing?

   Answer: Yes/No_____

   What do you see? Does anything stand out as a problem?

   Answer: _____

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3. Continue analyzing the report by answering these questions:

   What is the amount of slack reported?

   Answer: _____

   What is the start point of this critical path?

   Answer: _____

   What is the end point of this critical path?

   Answer: _____

   What type of path is this? (Reg-Reg, Input-Reg, Reg-Out)

   Answer: _____

   What clocks drive the start point and the end point?

   Answer: _____

   Locate where the input drive or output load reported. Did you find it?

   Answer: Yes/No_____

   Answer: It should be under slack time calculation.

   Locate where the insertion delay reported. Did you find it?

   Answer: Yes/No_____

   Note: It should also be under slack time calculation.

   Are there any cells with a large delay?

   Answer: _____

   Answer: It should be under arrival time calculation in the table.

4. To find out whether any other paths are violating, enter:

   ```
   resume
   start_gui // if needed.
   ```

   Then, in the graphical interface, click on the  and open the **Analysis** tab.

   How many other paths violate timing?

   Answer: _____

   Do all these paths have the same end point?

   Answer: Yes/No_____

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Verifying Multicycle Paths

After the session resumes and completes, the *tempus*> command prompt returns and you should see there are multicycle path constraints reported in the report.

1. View the report at the *tempus* prompt.

   This report shows multicycle paths that are from the *GlCOreSoftResetSynR00C* port.

   What is the slack reported?

   Answer: _____

2. Edit the *DESIGN/top._default_constraint_mode_.sdc* file.

   a. Look for *set_multicycle_path* commands in the file.

   b. Remove the comments on the hold muticycle path from the file.

   c. **Save** the file.

3. Reset the timing and regenerate timing reports by entering:

   ```
   resume
   ```

   Note: This command does the steps after the *suspend* command. It resets the SDC that was previously read in, and then read the SDC file again (the one you updated and saved).

   Did the timing of the path get any better?

   Answer: _____

Additional Steps (Optional)

1. Look at the following timing report:

   ```
   report_timing -to U_fticustomc
   ```

   Is there time borrowing in this report?

   Answer: _____

   Note: Look at the appendix section of the lecture for information on what *latches* are and what *time borrowing* is.

2. Feel free to modify the constraints and see the effects of the changes in the tool and run reports.

3. Exit the software by entering:

   ```
   quit
   ```

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Summary

In this lab, we looked at how to look at different timing reports in Tempus software and also the effects of the constraints on timing closure.

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