Clock Tree Synthesis

How to Synchronize your own chip

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Design Status, Start of CTS Phase

- Placement - completed
- Power and ground nets – prerouted
- Estimated congestion - acceptable
- Estimated timing - acceptable (0ns slack)
- Estimated max cap/transition – no violations
- High fanout nets:
  1. Reset, Scan Enable synthesized with buffers
  2. Clocks are still not buffered

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Question

Why are there no buffers on clock nets?

CTS Problem

- CTS is the process of distributing clock signals to clock pins based on physical/layout information
- After placement of cells the tree of synchronization is synthesized
- Balanced clock tree is synchronized with the addition of buffers
- After routing CT optimization is made

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  2. Floorplan and Technology constraints
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- **Inputs:**
  1. Netlist of gates and wires.
  2. Floorplan and Technology constraints
- **Outputs:**
  1. All cells located in the floorplan.
- **Goals:**
  1. Provide legal location of entire netlist
  2. Enable detailed route of all nets
  3. Meet timing, area, and power targets

Global and Detailed Placement

- In general, most tools partition the placement task into two stages:

Global Placement

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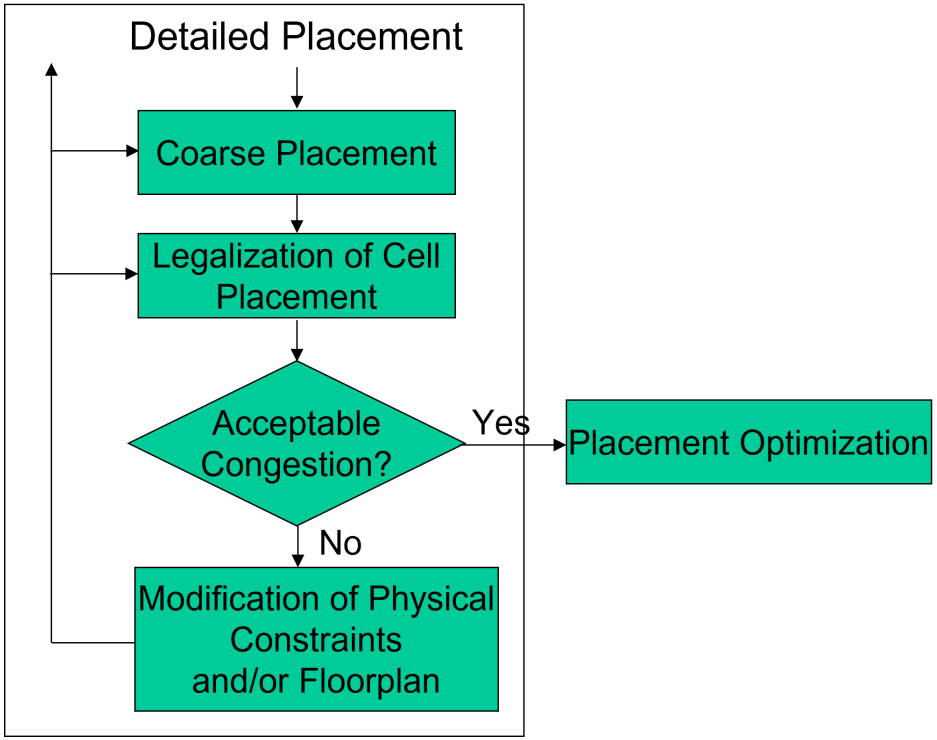
- This issue is solved through circuit partitioning
- As a basic criterion, the minimum is taken among group connections

Detailed Placement



- As a rule, detailed placemen is solved in two stages:
  1. Coarse placement
  2. Legalization of cell placement

Coarse placement

- In a coarse placement all the cells are placed in the approximate locations but they are not legally placed.
- Cells overlap and are not on-grid.
- Large cells (e.g. RAMs) form large placement blockages for other smaller leaf cells.
- Power routing forms routing layer blockages that will also be checked and avoided if specified.

Legalize Cell Placement

- Provide a legal placement for each instance with no overlap
- Try and minimize wirelength (or other cost metrics)
- Try to finish with uncongested design

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Timing-Driven Placement (1)

- All steps including placement are timing-driven
- Timing-driven placement tries to place critical path cells close together to reduce net RCs and to meet setup timing
- RCs are based on Virtual Route (VR)

Timing-Driven Placement (2)

- Timing-driven placement based on Virtual Route
  - Tries to place cells along timing-critical paths close together to reduce net RCs and meet setup timing
  - Net RCs are based on Virtual Routing (VR) estimates

Timing-Driven Placement (3)

- Standard cells are placed in "placement rows"
- Cells in a timing-critical path are placed close together to reduce routing-related delays $\rightarrow$ Timing-Driven Placement

TDP: Estimating Rnet and Cnet Before Placement

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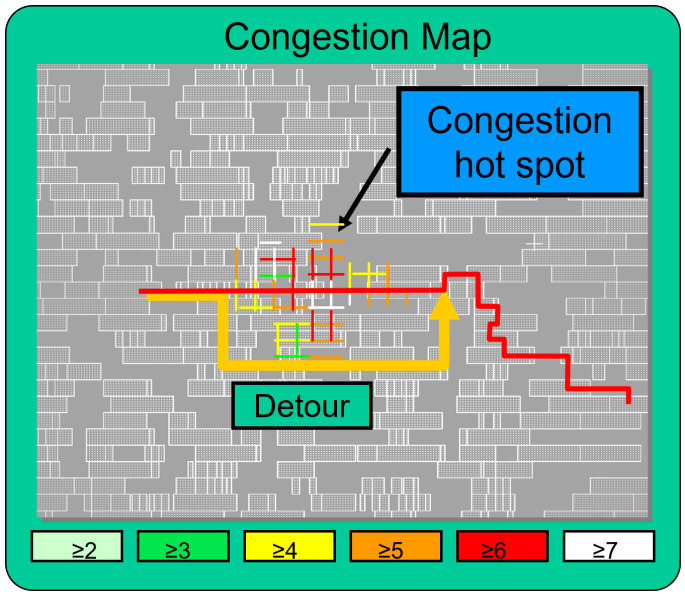
Congestion

- Congestion occurs when the number of required routing tracks exceeds the number of available tracks.
  - Congestion can be estimated from the results of a quick global route.
  - Global bins with routing overflow can be identified

Congestion Driven Placement: Routing resource

Placement Issues with Congestion

- If congestion is not too severe, the actual route can be detoured around the congested area
- The detoured nets will have worse RC delay compared to the VR estimates



congested

In highly congested areas, delay estimates during placement will be optimistic.

Non Routable on Severely Congested Design

- It is important to minimize or eliminate congestion before continuing
- Severe congestion can cause a design to be un-routable

Congestion Calculation

Congestion-driven Placement

- It is important to minimize or eliminate congestion before continuing
- Severe congestion can cause a design to be un-routable

Congestion-driven Placement

- Congestion Reduction
  - The tool tries to evaluate congestion hotspots and spread the cells (lower utilization) in the area to reduce congestion.
  - The tool can also choose cell location based on congestion, rather than wire-length.

Congestion vs. Timing-Driven Placement

Global Route (GR) for Congestion Map

Strategies to Fix Congestion

Modify the floorplan:

- Mark areas for low utilization.
- Top-level ports
  - Changing to a different metal layer
  - Spreading them out, re-ordering or moving to other sides
- Macro location or orientation
  - Alignment of bus signal pins
  - Increase of spacing between macros
  - Add blockages and halos
- Core aspect ratio and size
  - Making block taller to add more horizontal routing resources
  - Increase of the block size to reduce overall congestion
- Power grid
  - Fixing any routed or non-preferred layers

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High Fanout Synthesis (HFS)

High Fanout Synthesis

- **What is fanout?**
  - Fanout is the number of gate inputs to which the output can be safely connected. i.e., The load that a gate output can drive.
  - The maximum fanout of an output measures it's load-driving capability. Fanout belongs to the output.
- **What are High Fanout Nets(HFN) ?**
  - High Fanout Nets are the nets which drive more number of load. We set some max fanout limit by using the command set_max_fanout
  - The nets which have greater than these limit are considered as High Fanout Nets (HFN).
  - Generally clock nets, reset, scan, enable nets are High Fanout Nets.

What is High Fanout Net Synthesis (HFNS)?

- High Fanout Net Synthesis (HFNS) is the process of buffering the High Fanout Nets to balance the load.
- To balance the load HFNS is perfomed.
- Too many load affects delay numbers and transition times, Because load is directly proportional to the delay.
- Generally at placement step HFNS performed. HFNS can also be performed at synthesis step using Design Compiler. But it's not good idea, Buffers will be removed during PD and again HFNS is performed.
- **Care that should taken during HFNS:**
  1. Make sure an appropriate fanout limit is set using set_max_fanout command
  2. Verify the SDC used for PD should not have set_ideal_network or set_dont_touch commands on High Fanout Nets.
  3. Use ideal clock network – As clock nets are synthesized separately during Clock Tree Synthesis (CTS) step, we set clock network as ideal network.

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Pre-Existing Scan Chains?

What's the Issue with Existing Scan Chains?

Placement Based Scan Chain Routing

SCANDEF Reordering

Partitioning with SCANDEF

SCANDEF generated with DFTC

Alpha-Numeric Ordering

Reordering Within Scan-Chain

Reordering Across Scan-Chains

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Optimization techniques

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No Hold Time Fixing

- By default place_opt tries to fix only setup time violations - No hold time fixing
- Hold time will be addressed during clock tree synthesis
- All timing calculations are based on ideal clocks (clock skew = 0). Therefore, it is a common practice to give more constrained timing to placement engine with:
  1. Extra uncertainty
  2. Frequency Overdrive

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