

Routing

How to Route your own chip

Ahmed Abdelazeem

Faculty of Engineering
Zagazig University

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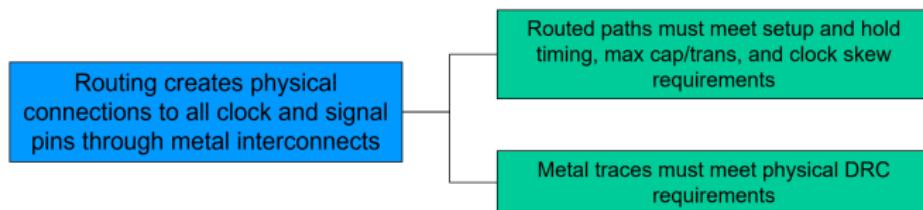
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Design Status, Start of Routing Phase

- Placement - completed
- CTS – completed
- Power and ground nets – prerouted
- Estimated congestion - acceptable
- Estimated timing - acceptable (0ns slack)
- Estimated max cap/transition – no violations

Routing Fundamentals: Goal

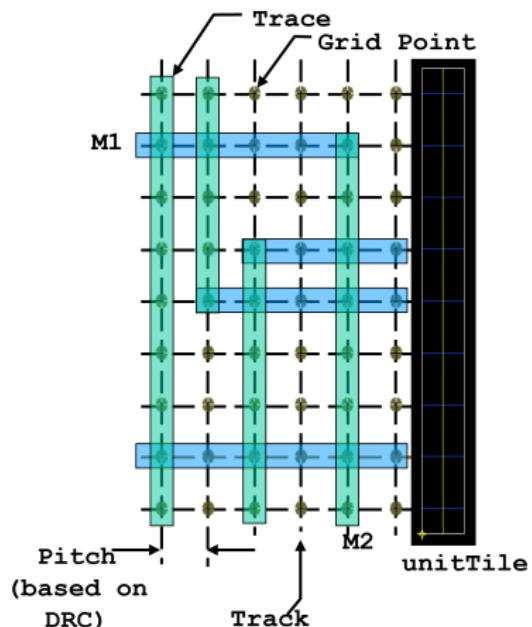


Routing creates physical connections to all clock and signal pins through metal interconnects

- Routed paths must meet setup and hold timing, max cap/trans, and clock skew requirements
- Metal traces must meet physical DRC requirements

Grid-Based Routing System

- Metal traces (routes) are built along and centered upon routing tracks based on a grid.
- Each metal layer has its own grid and preferred routing direction:
 - M1: Horizontal
 - M2: Vertical, etc...
- The tracks and preferred routing directions are defined in a "unitTile" cell in the standard cell library



Peculiarities of Grid-Based Routing System in IC Compiler

- The "unitTile" shown as a screen shot is used to define and store routing tracks and preferred directions information.
- unitTile cell is part of the standard cell library.
- The unitTile is similar to a site. It defines several things:
 - The minimum height and width a cell can occupy
 - The pitches in the preferred direction
 - Power and ground rail locations for standard cells
- The height of the unitTile is based on the metal 1 pitch (vertical) and must be a multiple of it.
- The width is based on the metal 2 pitch (horizontal) and must be a multiple of it.
- The metal 2 routing track defined in it must either be along the left side boundary or centered in the unitTile.

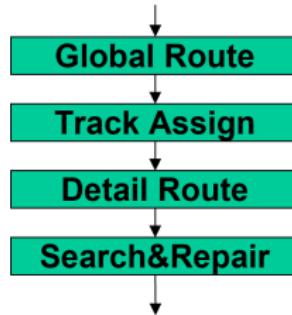
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Routing Operations

- **PnR Compiler performs:**

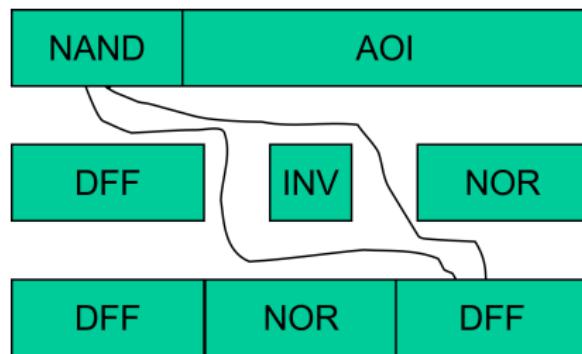
- 1 Global Routing
- 2 Track Assignment
- 3 Detail Routing
- 4 Search and Repair



- After global routing, track assignment and detail routing all clock/signal nets will be completely routed and should meet all timing, and most all DRC, requirements
- Any remaining DRC violations can be fixed by Search & Repair

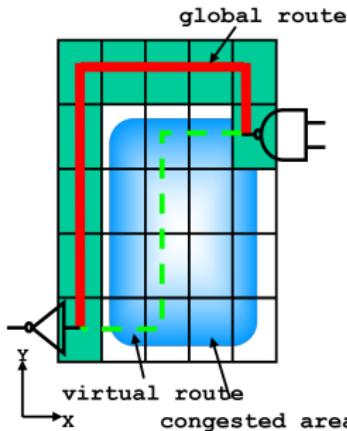
Route Operations: Global Route

- Global Route (GR) is the first step in routing
- GR gives more accurate parasitic and delay estimates compared to VR.
- The Global Route that is performed during routing will be used by the subsequent Track Assign operation
- Determining overall path of all routes
- Seeking to reduce delay, channel widths



Route Operations: Global Route

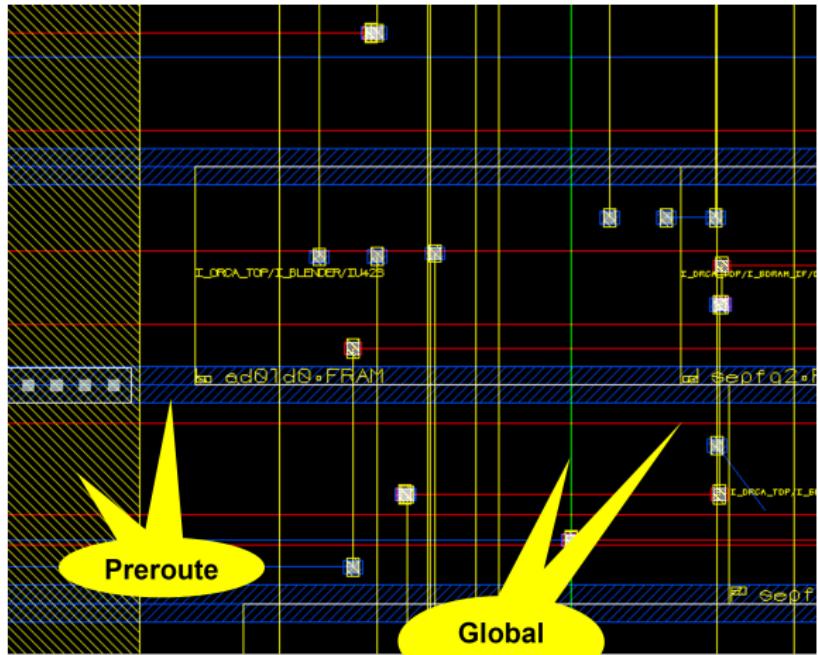
- GR assigns nets to specific metal layers and global routing cells (Gcells)
- GR tries to avoid congested Gcells while minimizing detours:
 - Congestion exists when more tracks are needed than available
 - Detours increase wire length (delay)
- GR also avoids:
 - P/G (rings/straps/rails)
 - Routing blockages



Metal traces exist after Global Route. True or False?

Route Operations: Global Route Summary

Answer: False!
GR does not lay down any metal traces.



Route Operations: Track Assignment

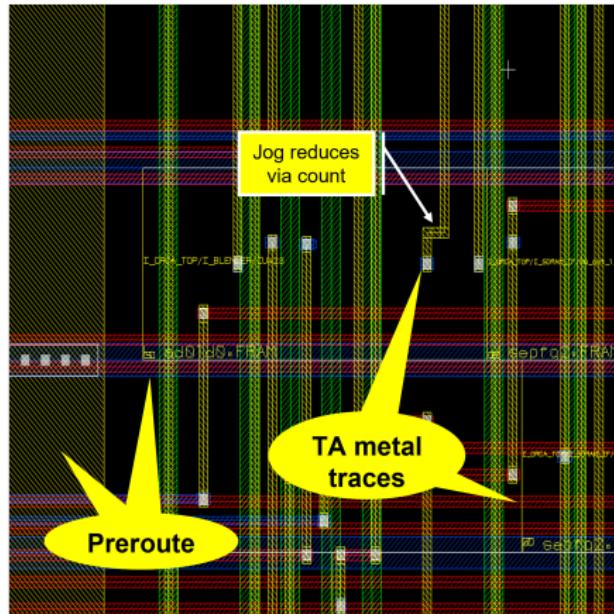
■ Track Assignment (TA):

- Assigns each net to a specific track and lays down the actual metal traces

■ It also attempts to:

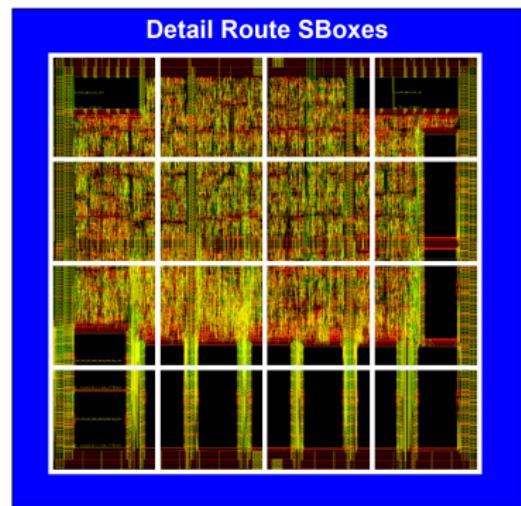
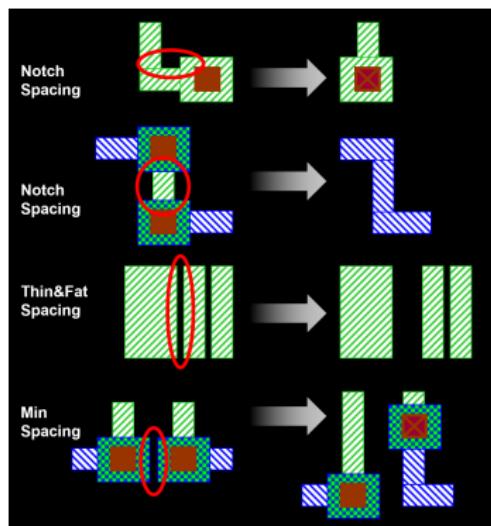
- Make long, straight traces
- Reduce the number of vias

■ TA does not check or follow physical DRC rules



Route Operations: Detail Routing

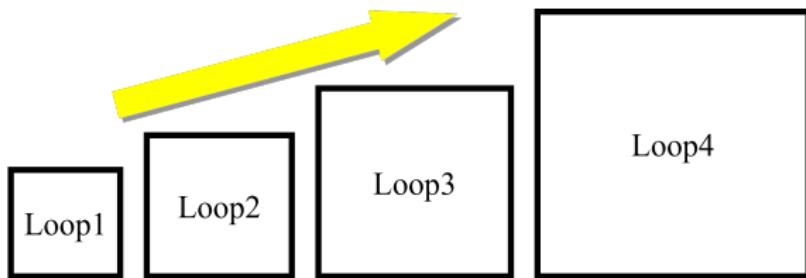
- **Detail route attempts to clear DRC violations using a fixed size Sbox**



- **Due to the fixed Sbox size, detail route may not be able to clear all DRC violations**

Route Operations: Search&Repair

- **Search&Repair fixes remaining DRC violations through multiple loops using progressively larger SBox sizes**

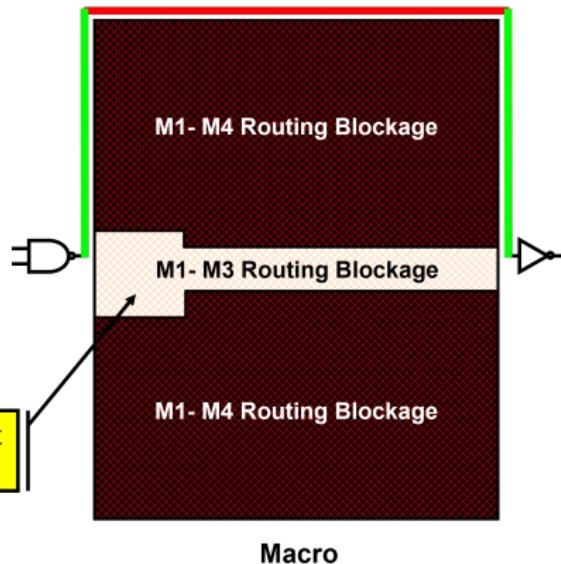


- **Note: Even if the design is DRC clean after S&R, you must still run a sign-off DRC checker (Caliber).**
 - Routing DRC rules are a subset of the complete technology DRC rules
 - IC Compiler works on the FRAM view, not the detailed transistor-level (CEL) view

Routing over Macros

■ By default IC Compiler will:

- Route over macros
- Not route where there is a routing blockage
- Not route through a narrow channel in the non-preferred routing direction



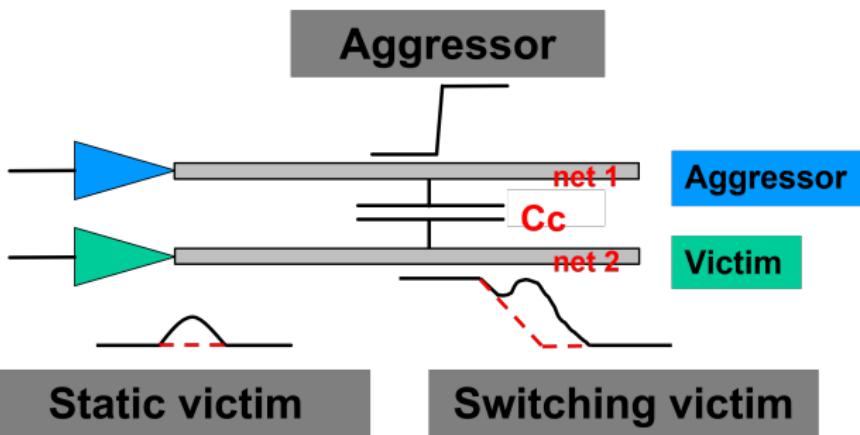
You need to change the preferred routing direction!

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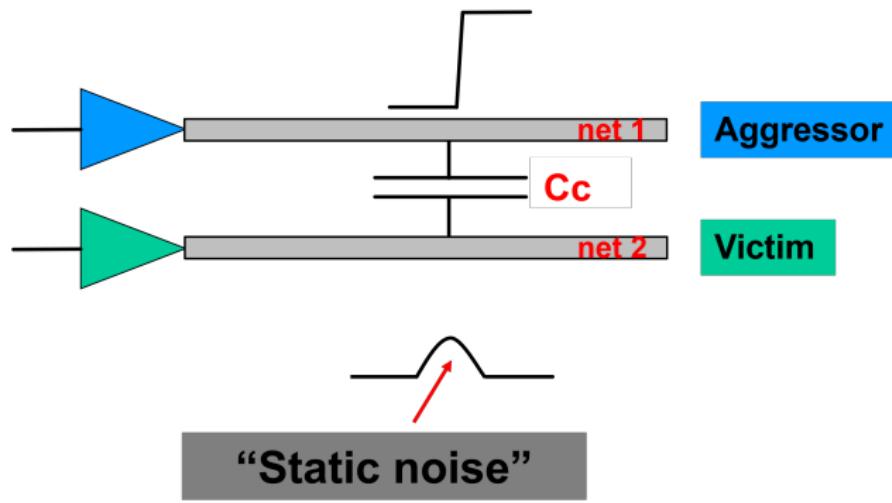
What is Crosstalk?

Crosstalk is the transfer of a voltage transition from one switching net (aggressor) to another static or switching net (victim) through a coupling capacitance (C_c)



Crosstalk-Induced Noise (aka Glitches)

Aggressor nets can create crosstalk-induced noise on static victim nets, also called as “static noise”



Crosstalk-Induced Delay

Aggressor/victim nets with overlapping timing windows can cause “crosstalk-induced delay” on victim nets.

This can lead to a speed-up or a slow-down of the victim net.

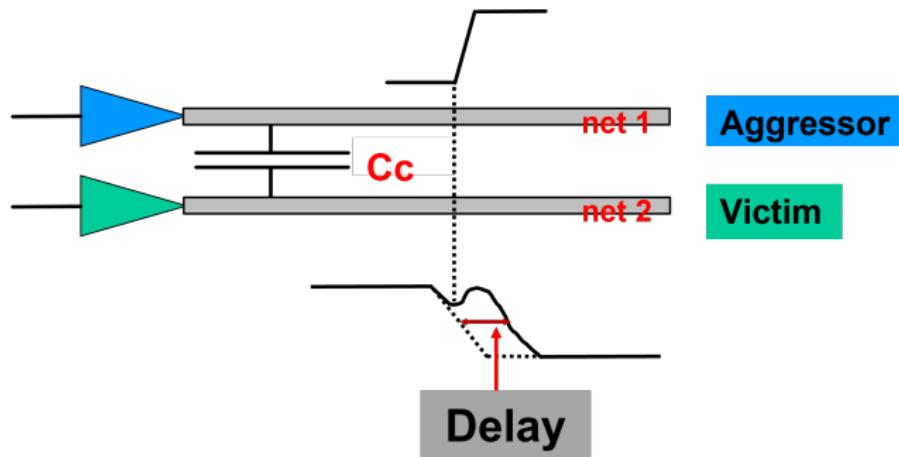
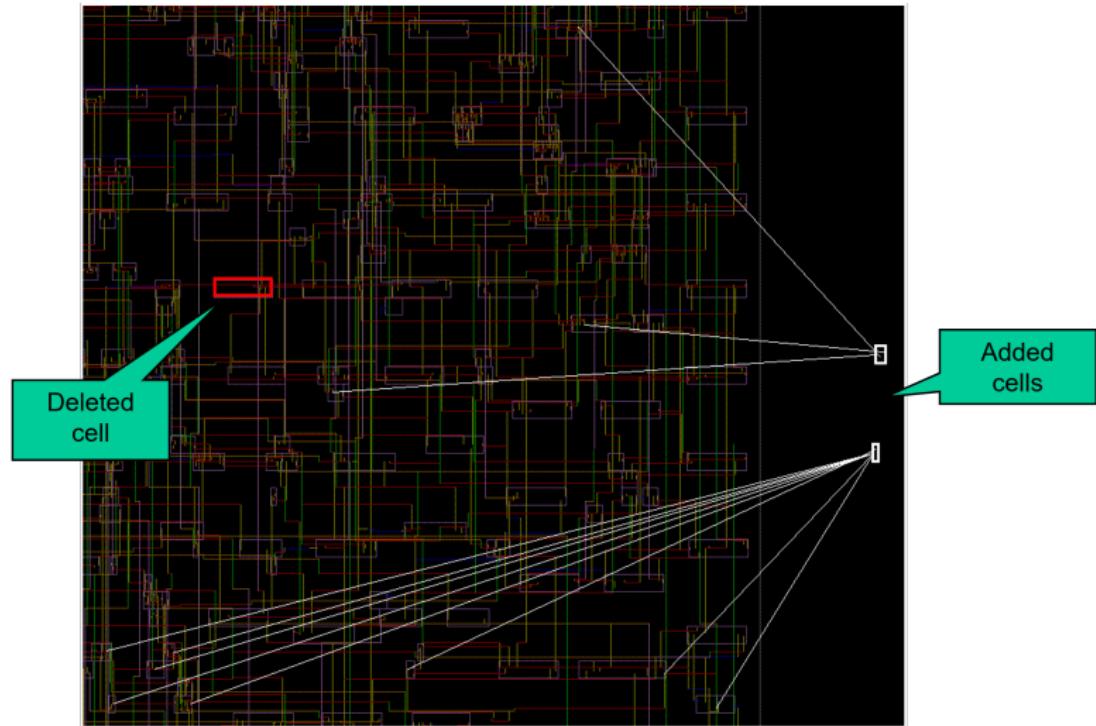


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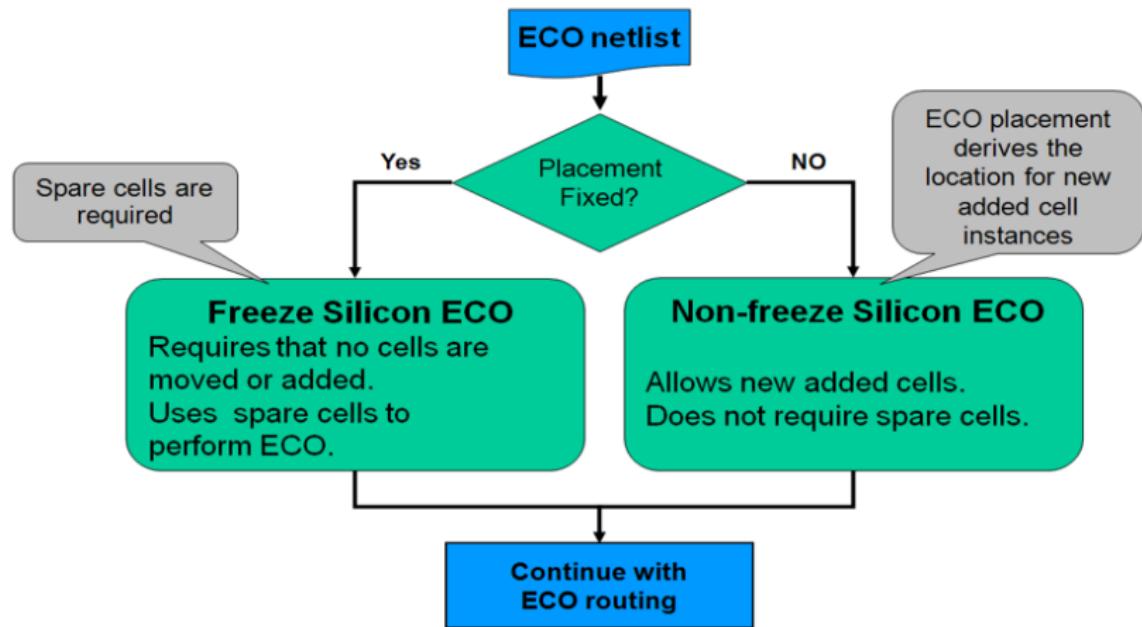
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Engineering change order



Functional changes occur late in the design cycle

Two Types of ECO Flows



Functional ECO Flows

■ Non-Freeze silicon ECO

- Pre-tapeout, no restriction on placement or routing
- Minimal disturbances to the existing layout
- ECO cells are placed close to their optimal locations

■ Freeze silicon ECO

- Post-tapeout, metal masks change only using previously inserted spare cells
- Cell placement remains unchanged
- ECO cells are mapped to spare cells that are closest to the optimal location
- Deleted cells become spare cells

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Chip Finishing Flow

- **PnR Compiler can address several issues to increase manufacturing yield:**

- Gate Oxide integrity → antenna fixing
- Via resistance and reliability → extra contacts
- Random Particle defect → Wire spreading
- Metal erosion → metal slotting
- Metal liftoff → metal slotting
- Metal Over-Etching → metal fill

Manufacturability Issues

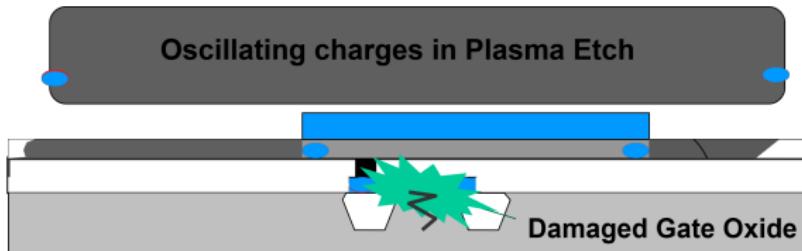
- In deep submicron VLSI, some manufacturing steps, like photo-resist exposure, development and etch and Chemical Mechanical Polishing (CMP) have detrimental effects on interconnect structures. These effects can vary based on local characteristics of the layout.
- To make these effects predictable, the layouts must be made “uniform” with respect to certain density standards across very small localized areas of the die. In the past, foundries performed the post processing needed to provide this uniformity. The techniques they used were filling (selective insertion of shapes) or slotting (selective reduction of shapes).
- In today’s processes, the design tools doing RC extraction, delay calculation, IR drop analysis, timing/noise/crosstalk analysis must be aware of these slotting/filling activities or suffer significant inaccuracy.

Manufacturability Issues

- PnR Compiler attempts to move all these into the design stage and out of the Fab post processing regime.
- To minimize the impact of the manufacturing process on device yields, foundries impose various density rules to make the layouts more uniform. For instance, the foundry may impose a density rule on an interconnect layer such that in any $10\text{ um} \times 10\text{ um}$ window, there must be at least 35 um^2 of metal features, but no greater than 70 um^2 of metal.
- Spare areas must be filled, but wide metal stripes must be slotted to meet the density rules.

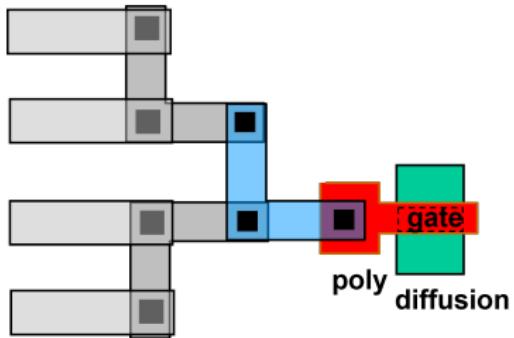
Problem: Gate Oxide Integrity

- Metal wires (antennae) placed in an EM field generate voltage gradients
- During the metal etch stage, strong EM fields are used to stimulate the plasma etchant
- Resultant voltage gradients at MOSFET gates can damage the thin oxide



Antenna Rules

- As length of wire increases during processing, the voltage stressing the gate oxide increases
- Antenna rules define acceptable length of wires

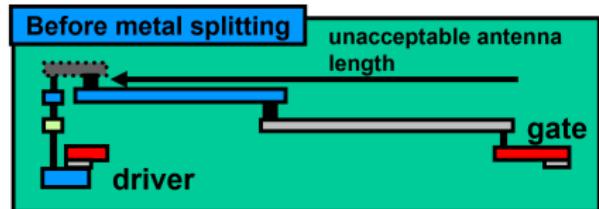


Antenna Ratios:

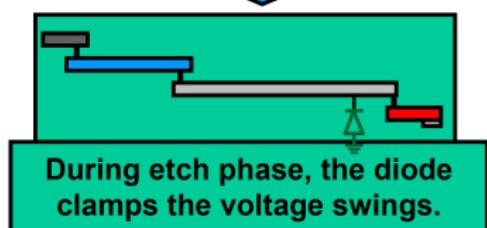
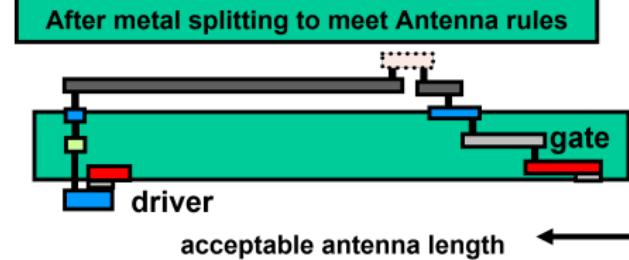
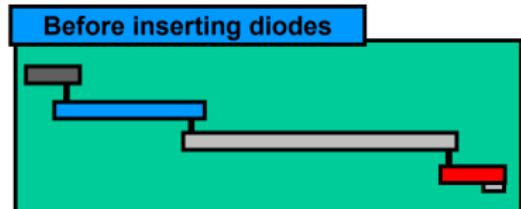
Area of Metal Connected to Gate
Combined Area of Gate
Or
Area of Metal Connected to Gate
Combined Perimeter of Gate

Fixing Antenna Problems

Splitting Metal or Layer Jumping

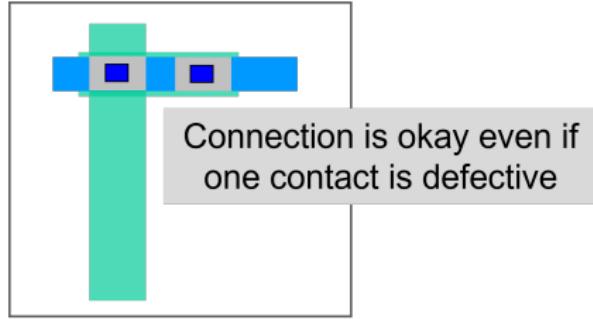
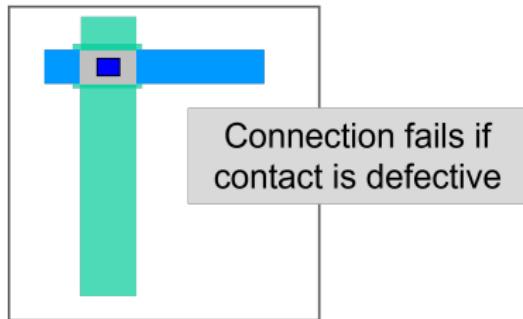


Inserting Diodes



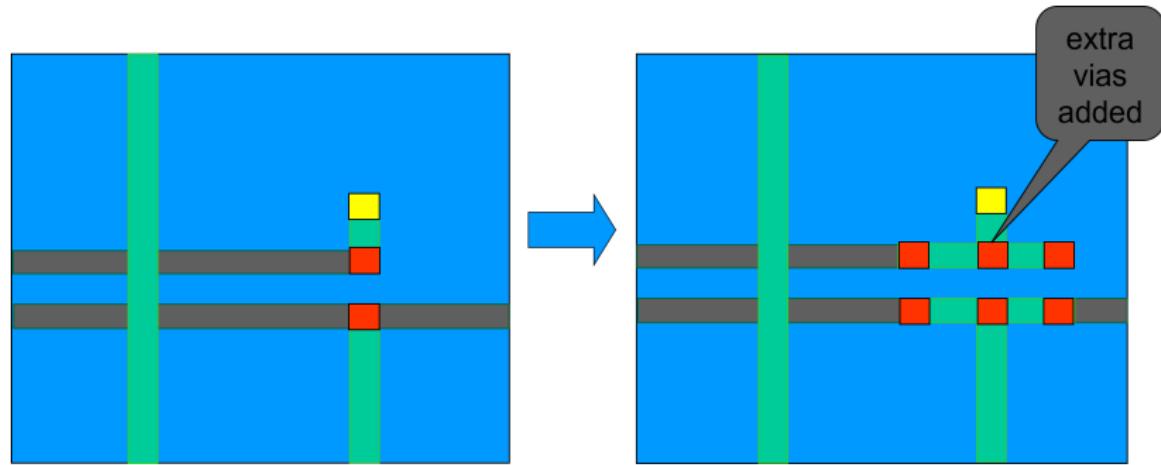
Voids in Vias During Manufacturing

- **Voids in vias is a serious issue in manufacturing**
- **Two solutions are available:**
 - Reduce via count: via optimization techniques are employed in routing stage
 - Add backup vias: known as redundant vias



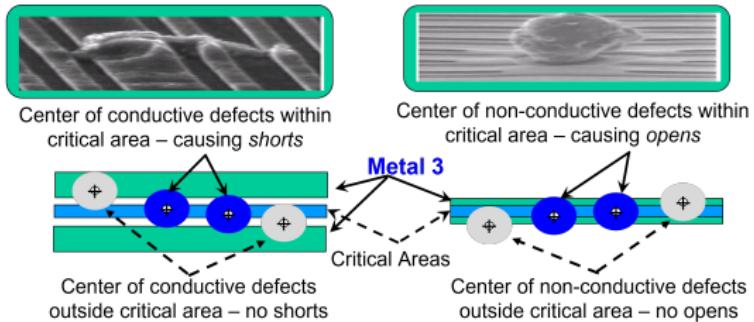
Via Resistance and Reliability

- Replacing one via with multiple vias can improve yield & timing (series R reduction)
- Inserts multiple vias without rerouting



Wire Spreading: Random Particle Defects

- Random missing or extra material causes opens or shorts during the fabrication process
 - Wires at minimum spacing are most susceptible to shorts
 - Minimum-width wires are most susceptible to opens



Filler Cell Insertion

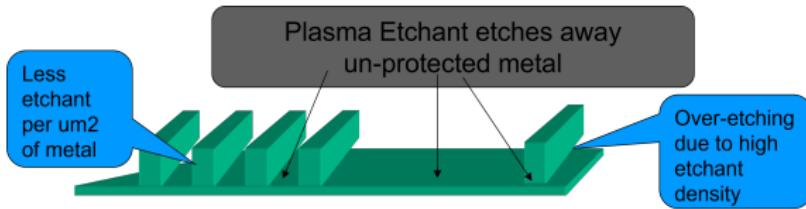
- **Metal fill insertion helps**

- To fill layers of choice including poly
- To insert floating vias
- To do area based metal fill
- To specify required width (timing driven metal fill doesn't fill wire tracks around critical nets)

- **For better yield, density of the chip needs to be uniform**
- **Some placement sites remain empty on some rows**

Problem: Metal Over-Etching

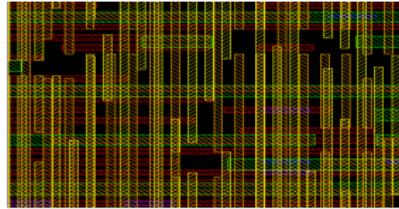
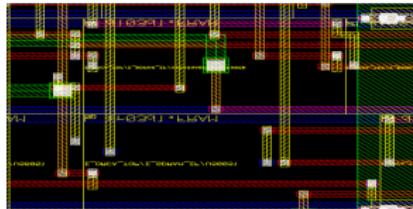
- A narrow metal wire separated from other metal receives a higher density of etchant than closely spaced wires
- The narrow metal can get over-etched
- Minimum metal density rules are used to control this



- Too much etchant in contact with too little metal → over-etched metal

Solution: Metal Fill

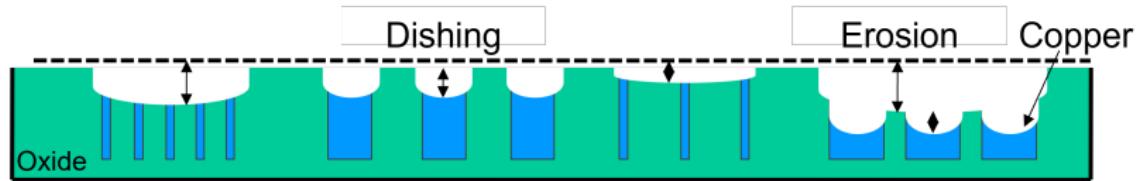
- **Fills empty tracks with metal shapes to meet the minimum metal density rules**
- **Uses up most of the remaining routing resource:**
 - No further routing or antenna fixes can be done



- **Metal filling is done to improve process planarization, which is important for processes with a large number of metal layers.**

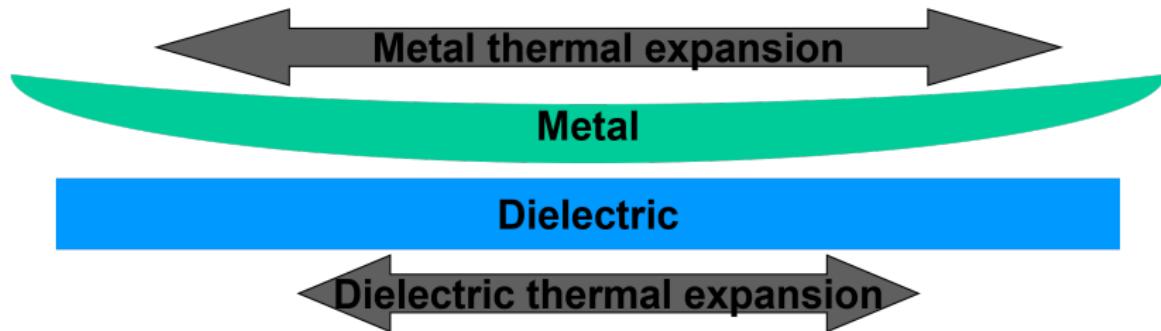
Problem: Metal Erosion

- The wafer is made flat (planarized) by a process called Chemical Mechanical Polishing (CMP)
- Metals are mechanically softer than dielectrics:
 - CMP leaves metal tops with a concave shape - **dishing**
 - The wider the metal the more pronounced the dishing
 - Wide traces with little intervening dielectric and can become quite thin – dishing this severe is called **erosion**
- Process rules specify **maximum** metal density per layer to minimize erosion



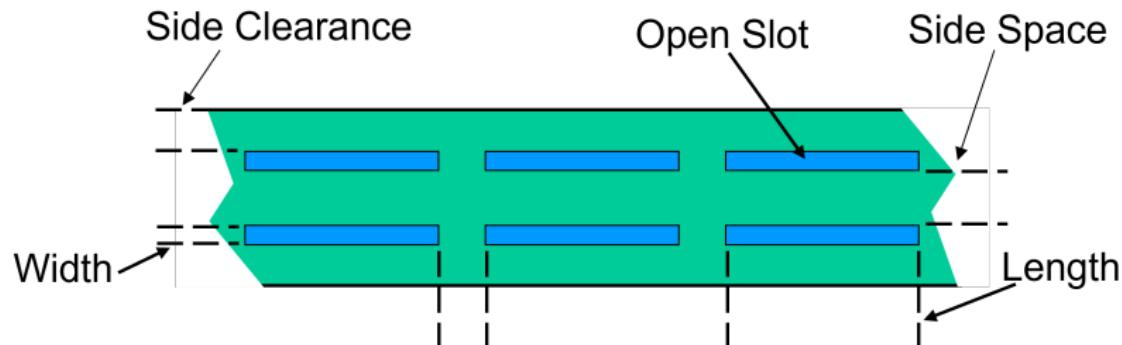
Problem: Metal Liftoff

- Conductors and Dielectrics have different coefficients of thermal expansion:
 - Stress builds up with temperature cycling
 - Metals can delaminate (lift off) with time
 - Wide metal traces are more vulnerable than narrow ones
- Maximum metal density rules also address this issue

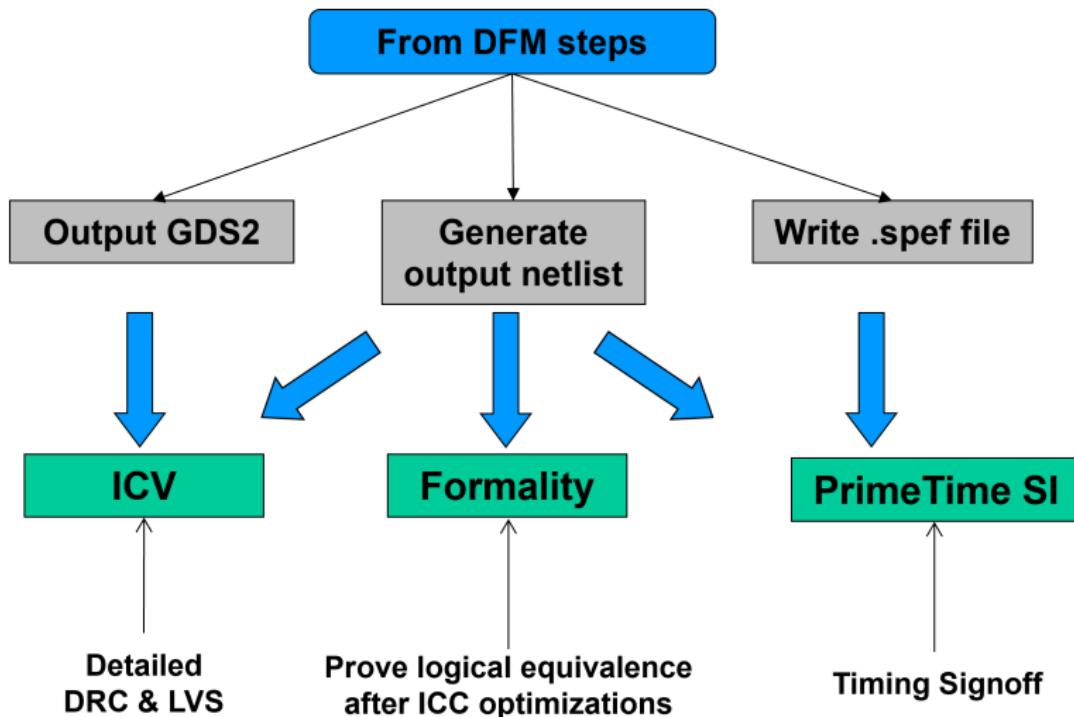


Solution: Metal Slotting

- Slotting wide wires reduces the metal density
- Slots minimize stress buildup, reducing liftoff tendency
- Primarily used on Power and Ground traces:
 - Can apply to any other net if wide enough
- Slotting parameters can be set layer by layer



Final Validation



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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ
وَمَا أُوتِيْتُ مِنَ الْعِلْمِ إِلَّا قَلِيلًا