PowerPlanning

How to Plan your own chip

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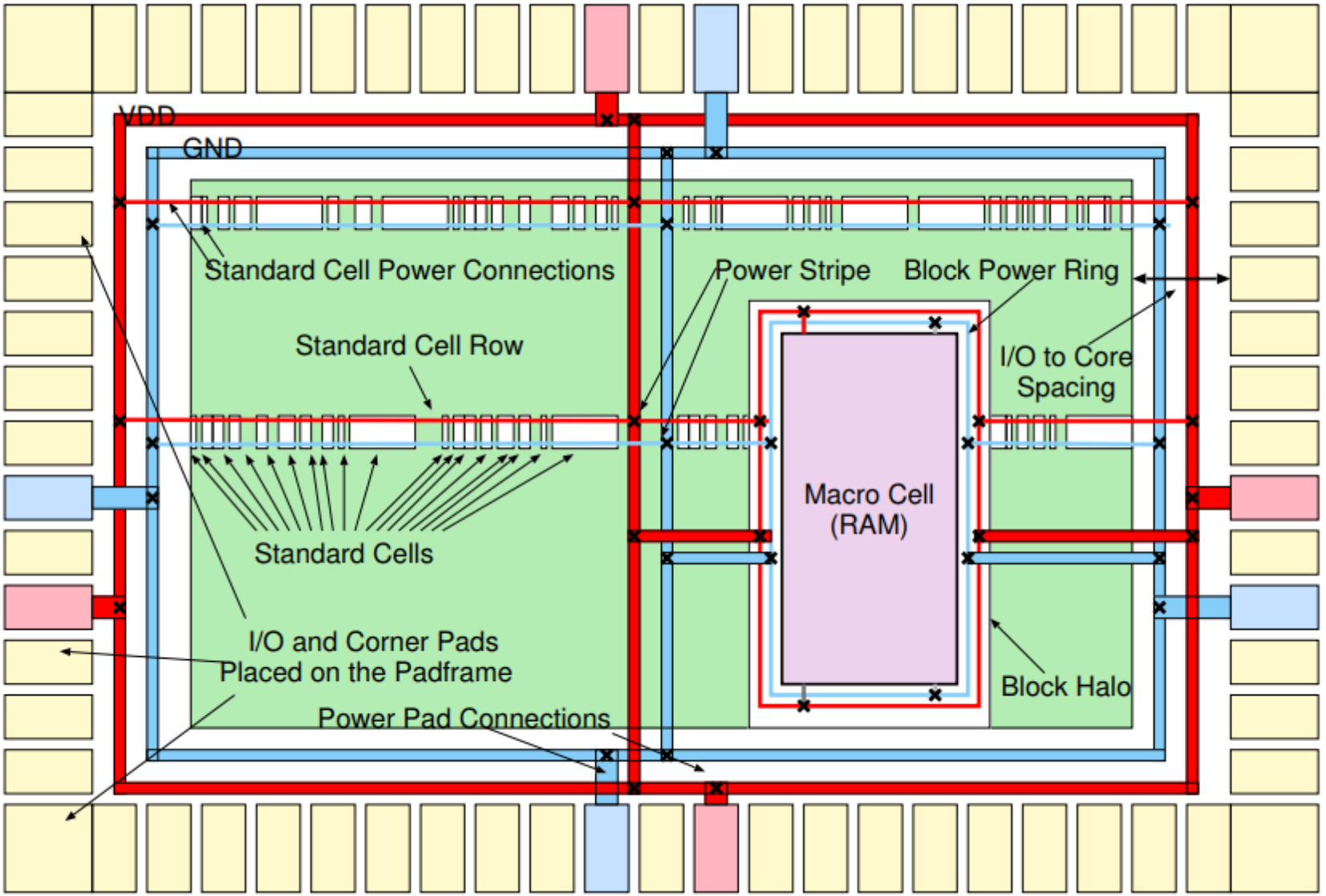


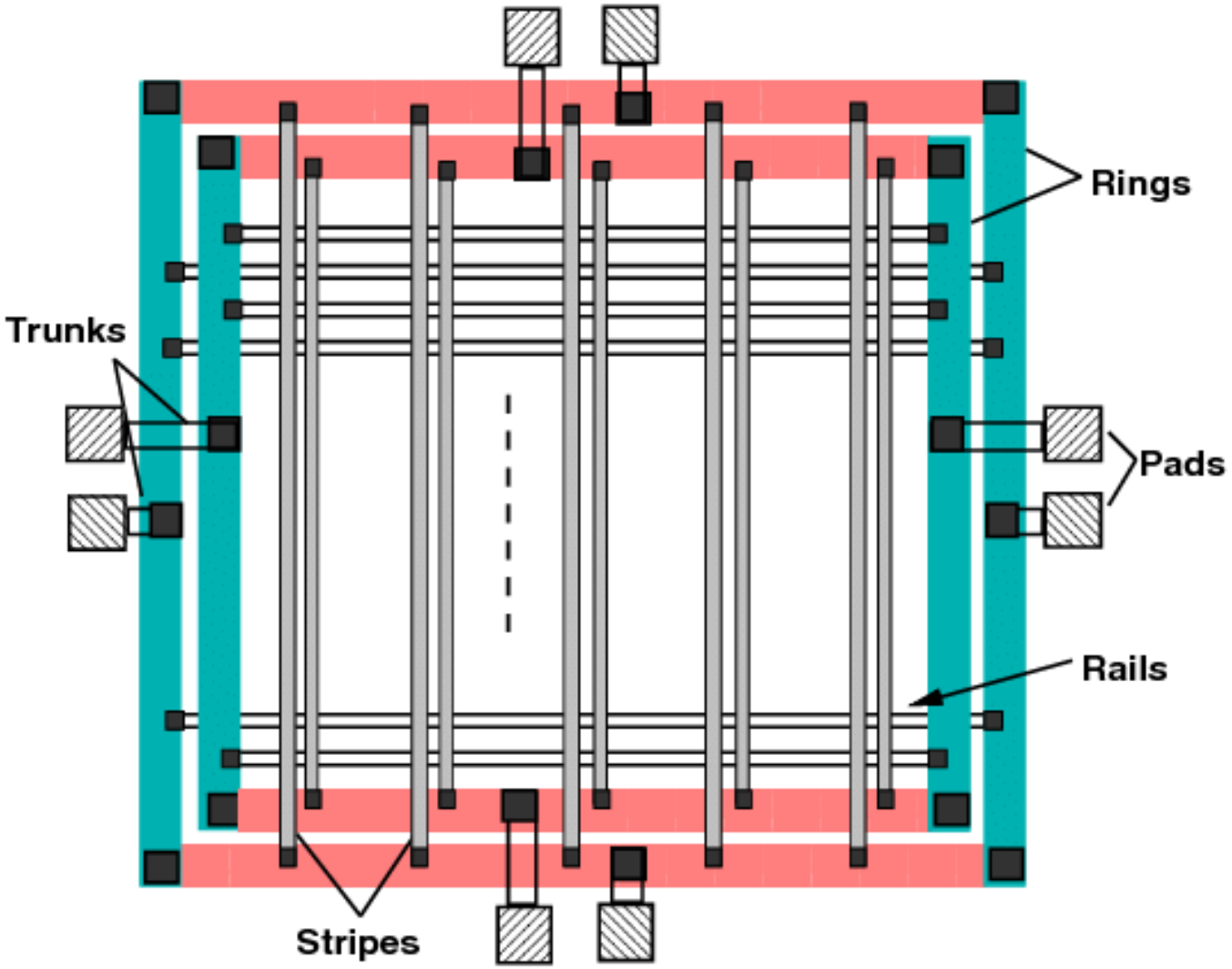
Objective of PowerPlanning

- To distribute the power from power pads to all elements in the chip.
- Unified supply of power with less voltage drop
- A proper Power design should aim at using as less routing recourse as possible.
- Power Analysis (EMIR) check should be done after power planning is completed

PowerPlanning

- Creation of the power network within a design
- Power planning is integrated with the overall design flow and must be taken into account early in the design process because:
  - # of pads may determine physical size (pad limited).
  - The power structures within the core area consume physical area.
  - The power grid topology effects top level routability, and also placement and routing within the child blocks.
  - The power structure effects functionality and reliability.

Simplified Power Distribution Architecture



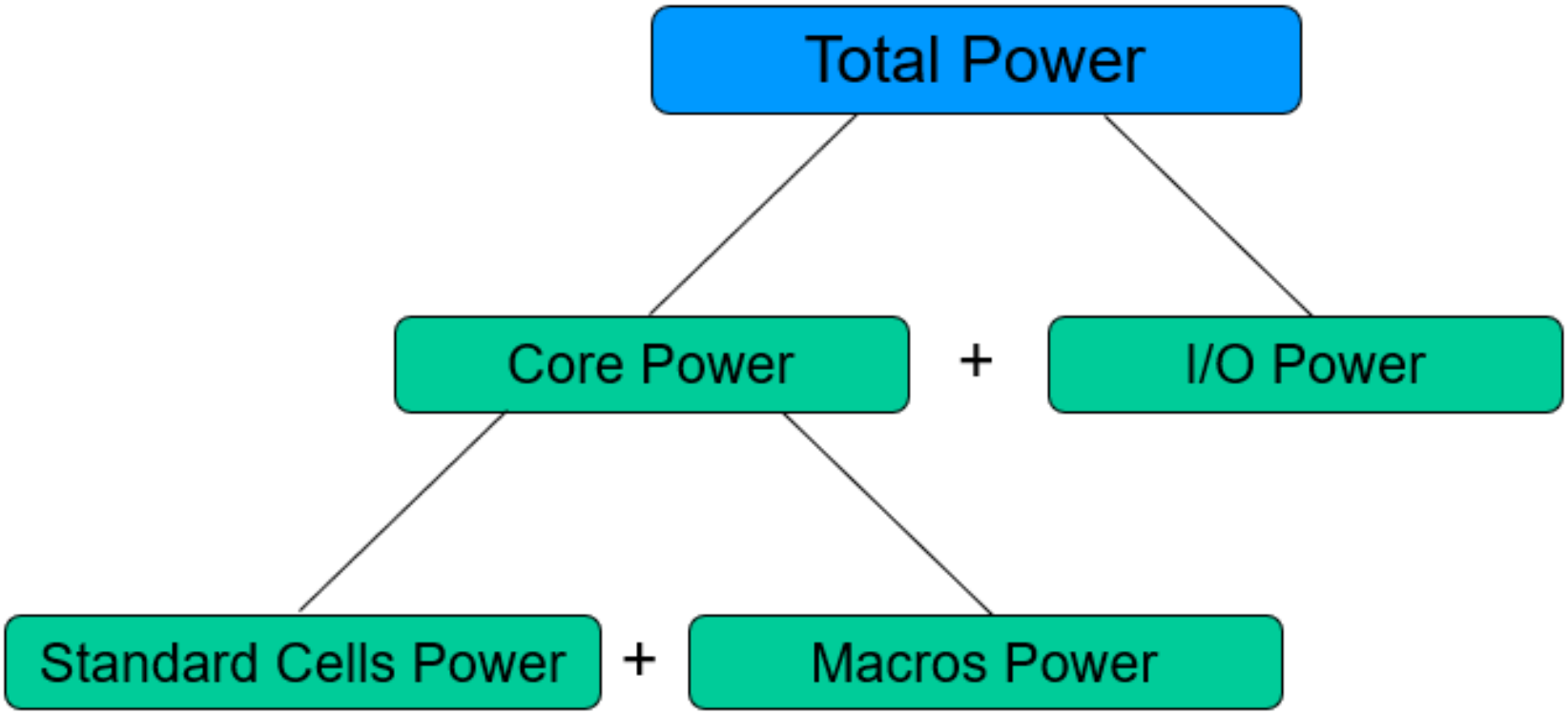
Power Network Elements

- **Power Pad**
- **Trunks**
  - Connects Ring to Power Pad
- **Power Rings**
  - Form complete rings around the periphery of the die, around individual hard macros, or inside of hierarchical blocks
  - higher-level Metal layers Power
- **Power Stripes**
  - Carries VDD and VSS from Rings across the chip
  - Horizontal and vertical metal wires placed in an array across the entire or section die
  - higher level routing layers
  - typically uniformly distributed across the die.
- **Power Rails**
  - Is used to connect the standard cell power rails together, and or power straps.
  - Low level, typically metal 1.

Power Estimations

Power Estimation is based on total power consumed by the chip:

- IO Power
- Core Power (Std. Cells +Macros)

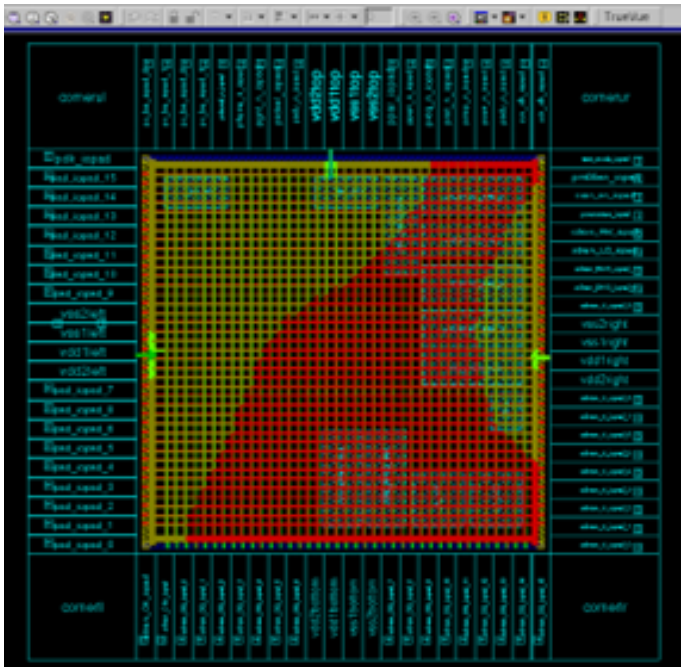


Power Planning

- Power Planning includes:
  - proper Estimation of power of chip
  - power routing the design based on the estimation.
- We create a mesh kind of structure, so that instance(s) can take direct supply from the nearest point
- We create multiple VDD and VSS lines(for each power domain)
- Hierarchical Mesh from upper metal layers to lowest(MI or M2 layers for standard cells). Connection from higher to adjacent lower metal layer is through VIAs

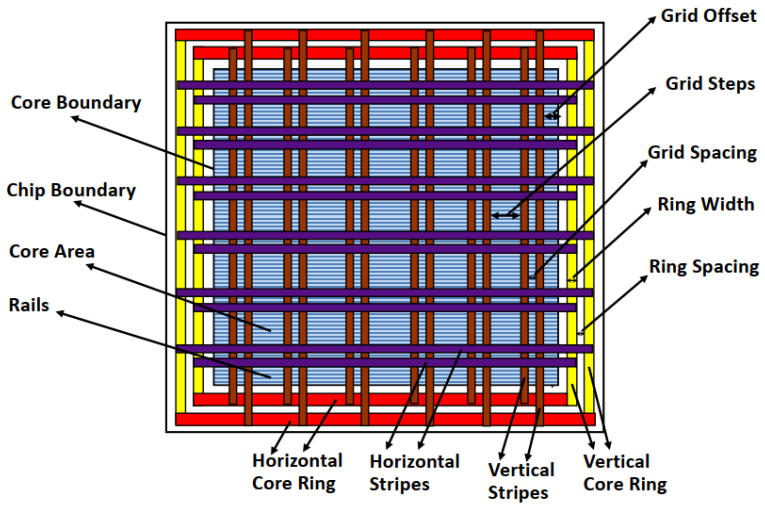
Power Mesh

- Power/Ground mesh will allow multiple paths from P/G sources to destinations
  - Hierarchical power and ground meshes from upper metal layers to lower metal layers
  - Multiple vias between layers



Why create mesh kind of structure ?

- To distribute the Power from power pads/pins to all elements of the chip.
- Provides multiple paths from PG sources to destinations (less series resistance)
- Uniformly distribute power with less voltage drop.
- To meet IR/EM targets
- For meeting timing requirements



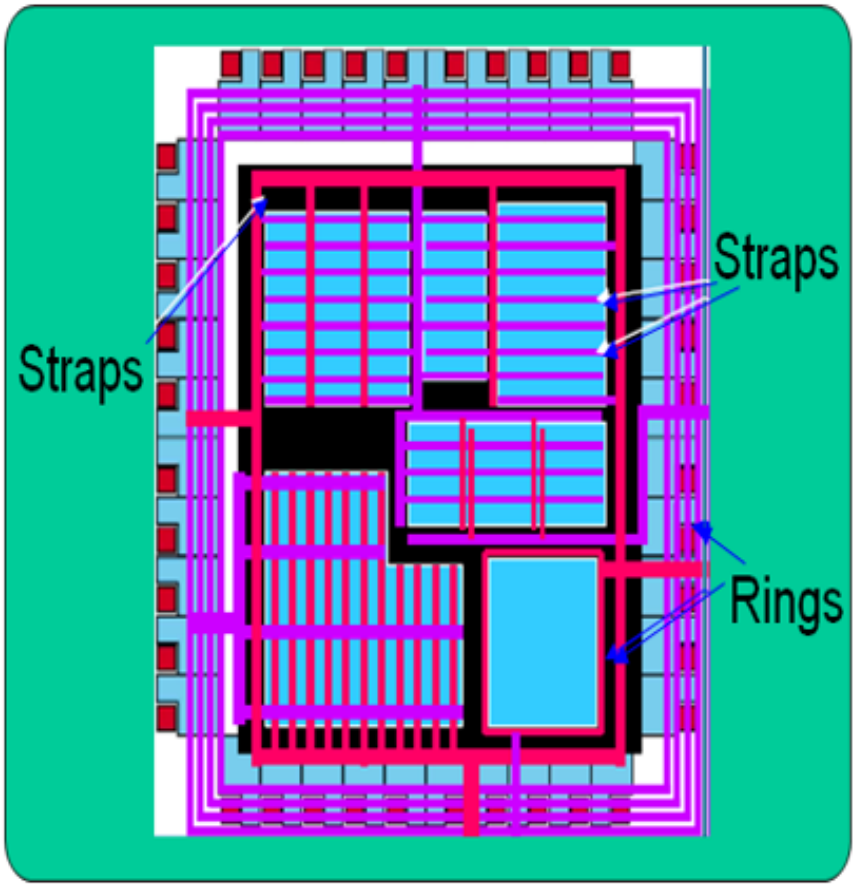
Power Planning vs. Power Routing

Power Planning

Creation of power structures like rings and straps

Power Routing

Dropping vias and connecting the power ports of the cells to power lines



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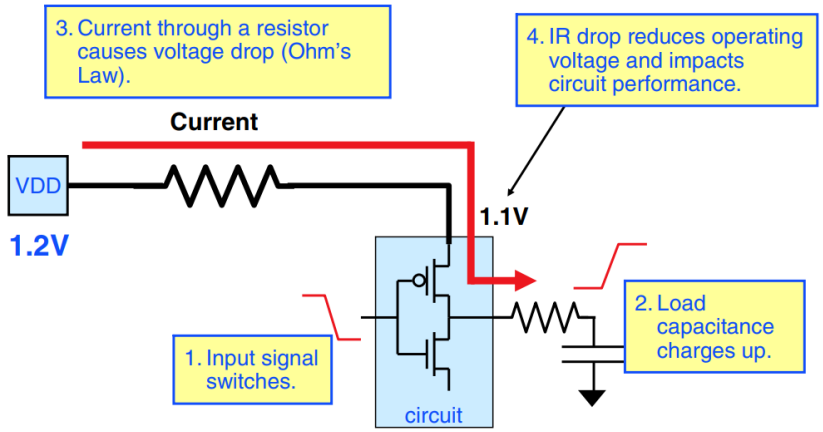
IR Drop

- Reduction in voltage that occurs on power supply networks
- IC design expects availability of ideal power supply
- In reality, localized voltage drops within the power grid
  - Increasing current/area on die
  - Narrower metal line widths (increases power grid resistance)
- Results in decreased power supply voltage at cells/transistors
- Decreases the operating voltage of the chip, resulting in timing and functional failures



Reasons of IR Drop Violations

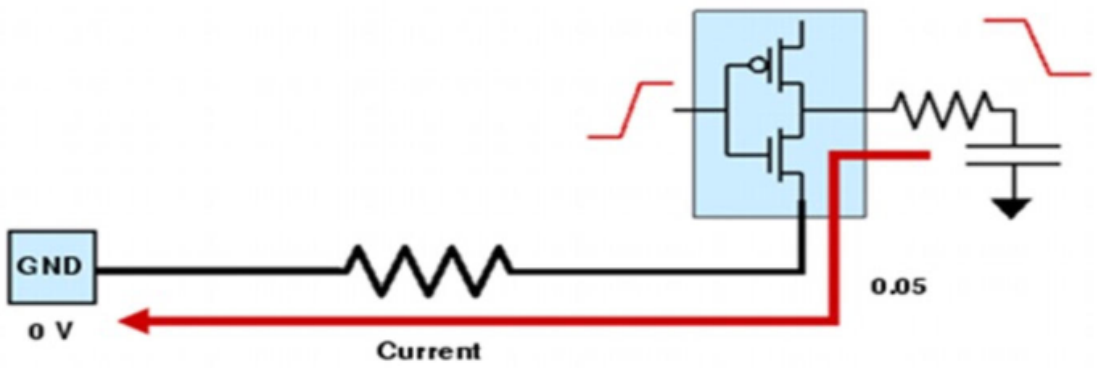
- Power structure is not proper.
- Cell density is very high.
- Instances are not get proper power because of no straps over there
- Mesh structure is proper but there is no via

How to reduce IR drop ?

- Routing should be from Top Layer.
- By adding some more Power Stripes.
- By increasing the width of the metal.
- By adding Decaps(DCAP cells).
- By using some Low Power Techniques

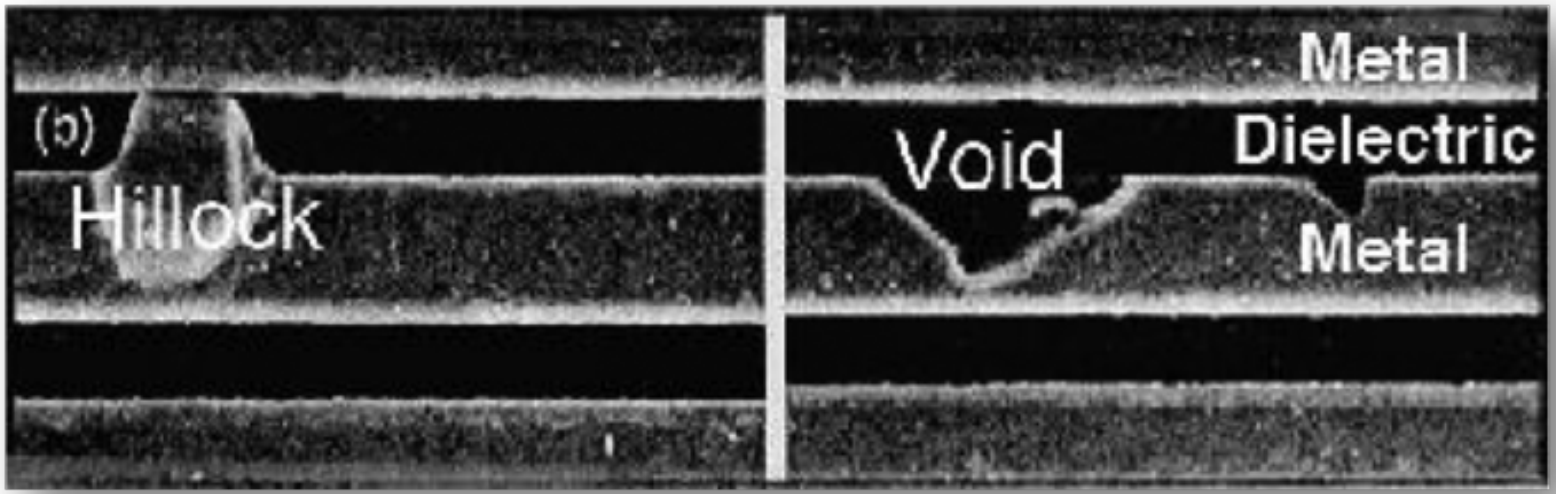
Ground Bounce

- Increase in voltage that occurs on ground networks (VSS or GND) in integrated circuits
- Increase in ground voltage decreases the operating voltage of the chip, resulting in timing and functional problems



Electromigration

- Electromigration is the movement of atoms based on the flow of current through a material.
- If the current density is high enough, the heat dissipated within the material will repeatedly break atoms from the structure and move them.
- Results of EM in ICs: The VOIDs and HILLOCKS gets created and potentially causing open and short circuits.



EM violations : Reasons of EM violation

- High Fanout Net (multiple fanout cells switch simultaneously, draws larger current from driver)
- Higher Driver Strength Cells(delivers large current unnecessarily, heating up the wire)
- Higher frequency(quick transitions)
- Narrow metal width
- Metal slotting (resulting into narrower widths)
- Long Nets (because of larger resistance, higher localized temperature)

Solutions of EM violations

- Decrease Driver's drive Strength.
- NonDefault (wider) rule based routing.
- Insert buffer on long nets.
- Route with higher metal layers(lessresistive, higher tolerance (current carrying capabilities)
- Use multi-Cut Via
- Break the fanout (have lesser fanouts)
- Use wider metals (more width)

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Power Plan Checks

- There should be no open connection
- All the Macros should be hooked up with Power/Ground.
- IR/EM target should be met.
- Missing Vias should be taken care
- There should be no Hot Spots (during IR-Drop Analysis)

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