IR drop and Electromigration

Errors Can Break Your ASIC!

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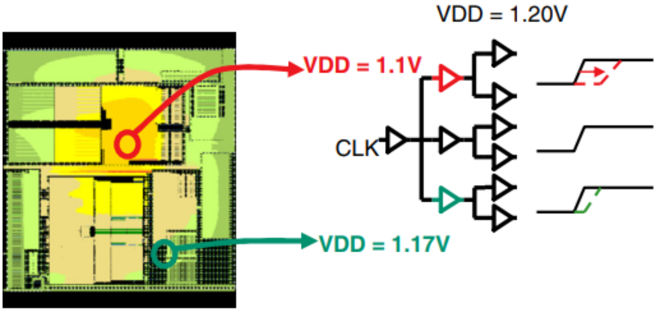
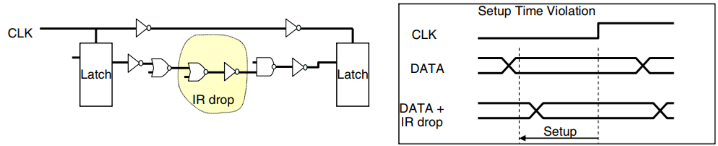
Introduction

- **IR drop:** Voltage drops caused by current flowing from the power source through the resistive power network to the on-chip devices is called IR drop.
- **Ground bounce:** Voltage spikes caused by current flowing from on-chip devices though the resistive ground network to the ground pins (or bumps)
- IR drop and ground bounce combine to impact silicon performance.

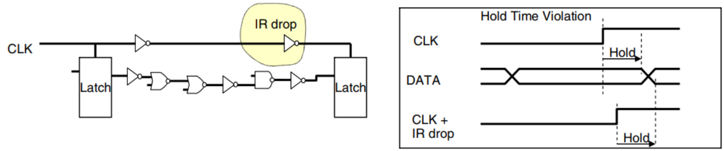


IR Drop Impacts on Setup and Hold Time

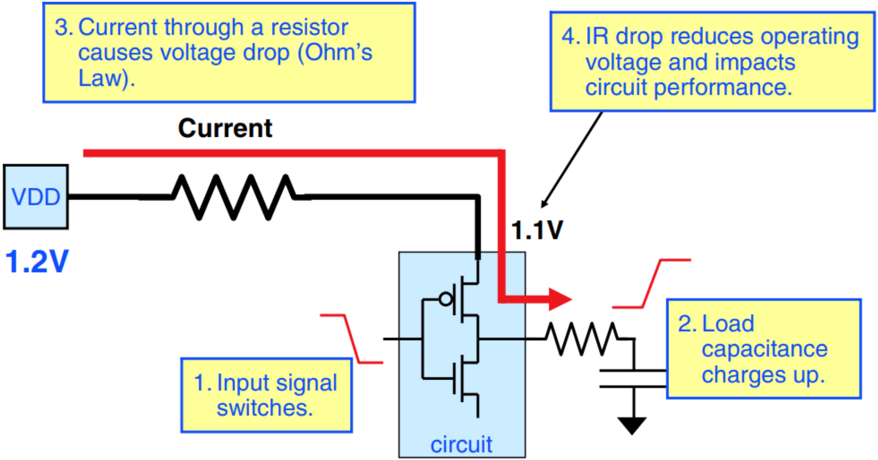
- In the case where the IR drop occurs within the signal path, the signal is slowed, potentially causing setup time violations for this signal path



- In the case where IR drop occurs on a clock buffer, the clock signal beyond this buffer is slowed, potentially causing hold time violations for all signals clocked by this clock branch.



How Does a Power Rail IR Drop Occur?



IR Drop Occur

- The power supply (VDD and VSS) in a chip is uniformly distributed through the metal rails and stripes which is called Power Delivery Network (PDN) or power grid.
- Each metal layers used in PDN has finite resistivity.
- When current flow through the power delivery network, a part of the applied voltage will be dropped in PDN as per the Ohm's law
- The amount of voltage drop will be $V = I.R$, which is called the IR drop.
- If the resistivity of metal wire is high or the amount of current following through the power net is high, A significant amount of voltage may be dropped in the power delivery network which will cause a lesser amount of voltage available to the standard cells than the actual amount of voltage applied.

IR Continue

- If V1 voltage is applied at the power port and current I is following in a particular net which has total resistance R, then the voltage available (V2) to the other end for the standard cell will be

$$V2 = V1 – I.R \tag{1}$$

- Standard cells or macros sometimes do not get the minimum operating voltage which is required to operate them due to IR drop in power delivery network even the application of sufficient voltage in the power port.
- Voltage drop in the power delivery network before reaching the standard cells is called IR drop.
- This drop may cause the poor performance of the chip due to the increase of delay of standard cells and may cause the functional failure of the chip due to setup/hold timing violation.

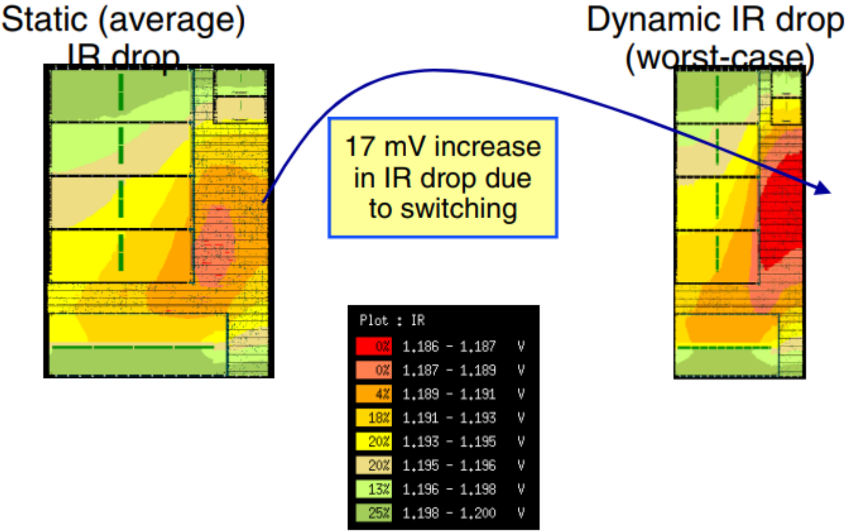
Types of IR drop

There are two types of IR drop in the ASIC design:

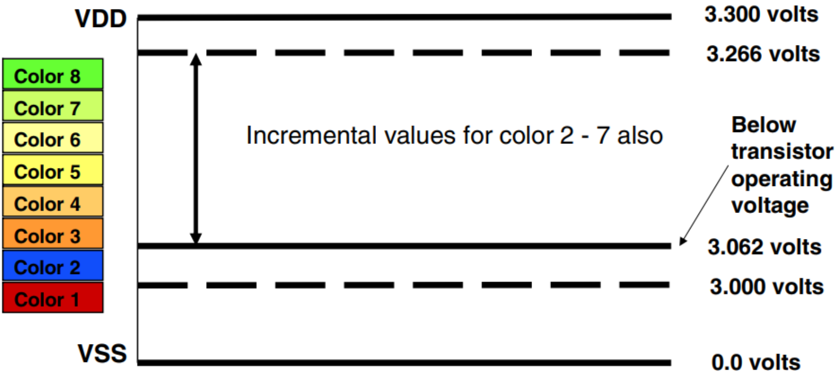
- Static IR drop
- Dynamic IR drop

- Static IR drop is the voltage drop in the power delivery network (PDN) when there are no inputs switching means the circuit is in the static stage.
- dynamic IR drop is the voltage drop in the power delivery network when the inputs are continuously switching means the circuit is in a functional state. Dynamic IR drop will depend on the switching rate of instance.
- When the inputs are switching continuously, more current would flow in the instances and also in PDN. So there will be more IR drop in the PDN. Therefore dynamic IR drop is more than the static IR drop.

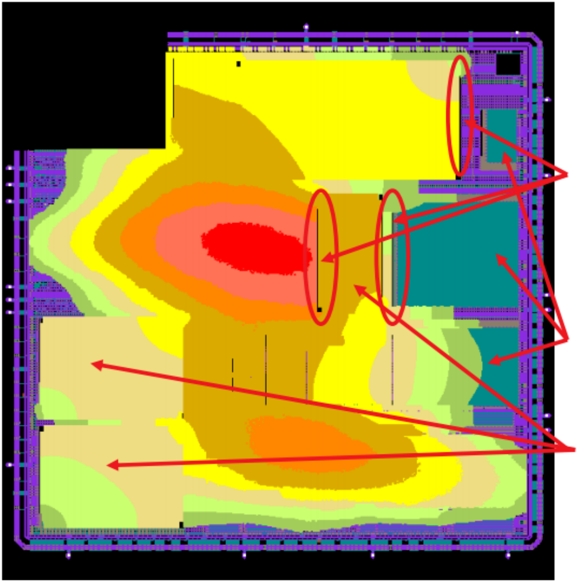
Static vs. Dynamic IR Drop Analysis



Example Colors for IR Drop



IR Drop Example for Chip



Abrupt IR drop color change shows locations where there is a discontinuity in the power grid.

These RAMs connect well to the power grid.

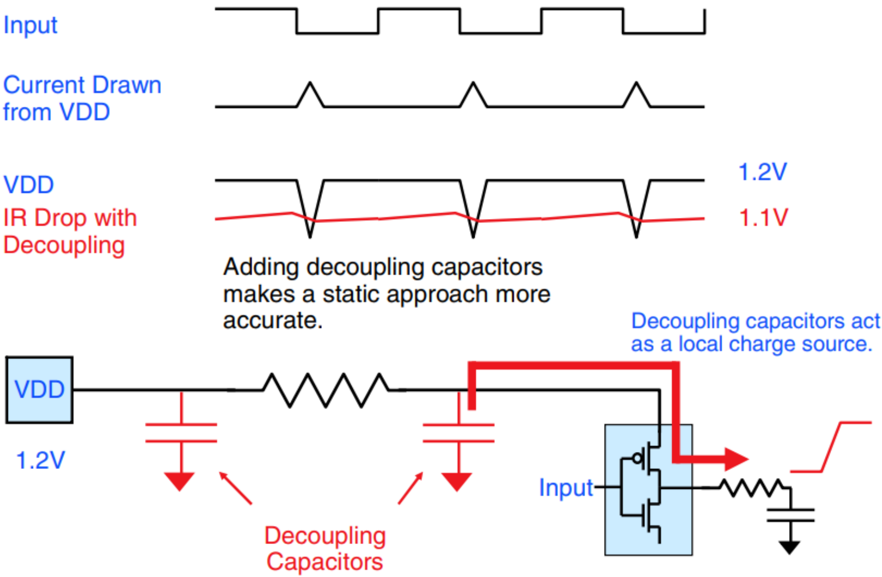
These RAMs do not connect well to the grid.

Reasons for IR drop:)

IR drop could occur due to various reasons but some main reasons are as bellow.

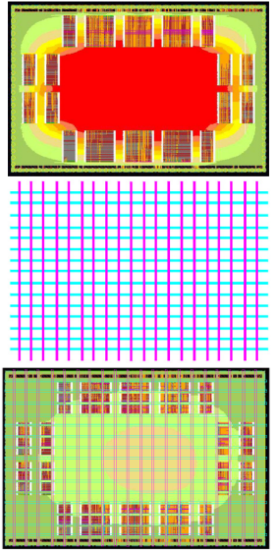
- Poor design of power delivery network (lesser metal width and more separation in the power stripes)
- inadequate via in power delivery network
- Inadequate number of decap cells availability
- High cell density and high switching in a particular region
- High impedance of the power delivery network
- Rush current
- Insufficient number of voltage sources
- High RC value of the metal layer used to create the power delivery network

Method of Reducing Dynamic IR Drop



Method of Reducing Static IR Drop

- The red area means a voltage drop of more than 10% of the nominal supply voltage. The solution is to use wider power stripes or use more metal on higher levels.
- Additional power stripes are added to the design and are marked in cyan and magenta.
- This IR drop plot is made after an increase of the number of power stripes.
- This plot shows a very low voltage drop, which is required for a functional chip.



Methods to improve IR drop

Methods to improve static IR drop

- We can go for higher layers if available
- Increase the width of the straps.
- Increase the number of wires.
- Check if any via is missing then add more via.

Methods to improve dynamic IR drop

- Use de-cap cells.
- Increase the number of straps

Tools used for IR drop analysis

- RedHawk of Ansys.
- Voltus of Cadence Design System.

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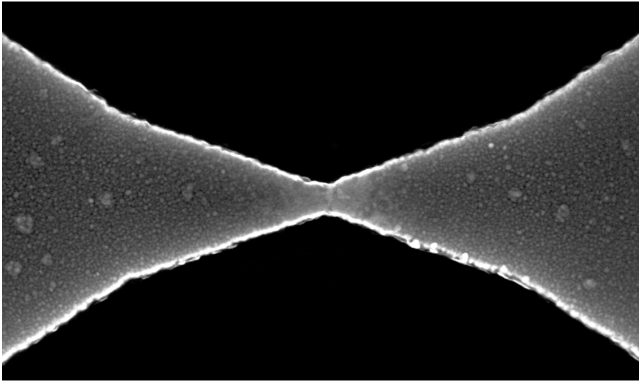
What is Electromigration?

Definition

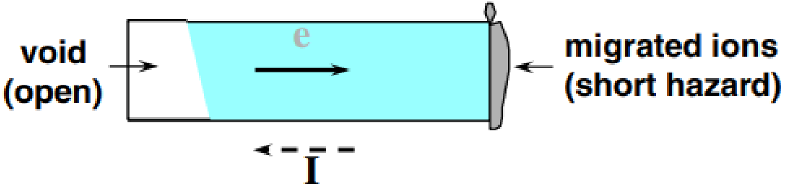
is the gradual displacement of metal atoms in a semiconductor. It happens when the current density is high enough to cause the drift of metal ions in the direction of the electron flow.



What is Electromigration?

Electromigration is a wear-out mechanism of metal wires.

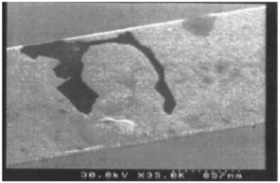
- Metal atoms migrate over a period of time, causing open circuits, shorts circuits, or unacceptable increases in resistance.
- There are two main causes of electromigration failure:
  1. High (DC) current densities
  2. Joule heating, which is caused by high alternating currents
- These wear-out mechanisms can take extended periods of time



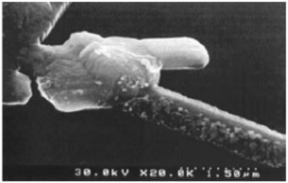
Causes of Electromigration

- Electromigration is mechanical failure in the wire caused by frequently varying thermal conditions.
- As pulses go through the wire, the power dissipated by the wire causes it to heat above oxide temperature
- The difference in the thermal constants between the oxide and the wire causes mechanical stress, and the wire can eventually fail resulting in chip failure in the field.

EM failures as seen though a scanning electron microscope (SEM)



FESEM micrograph of aluminum lines exhibiting classic

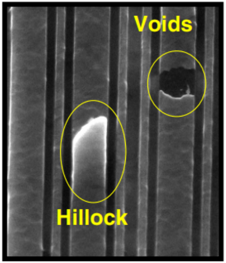


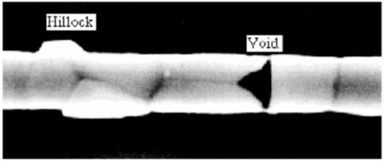
Hillocks formed in a Cu line during electromigration test.

Electromigration Damages

Effects of EM

- Depletion of atoms (Voids): Slow reduction of connectivity; Interconnect failure
- Deposition of atoms (Hillocks): Shorts





http://www-mse.stanford.edu/faculty/nix/research/interconnect/interconnect.html, IC Interconnect Reliability, 11/22/98

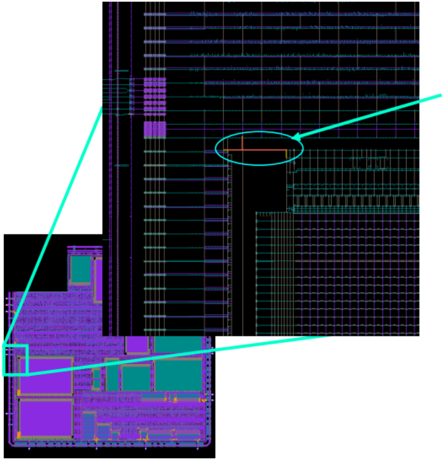
High (DC) Current Densities

- Physical migration of metal atoms due to “electron wind” can eventually create a break in a wire.
  - (MTTF) is an indication of the life span of an integrated circuit. MTTF is calculated using Black’s equation as bellow.

$$MTTF = \frac{A}{J^n} exp(\frac{Ea}{KT}) \tag{2}$$

  - Current density must not exceed specification
  - Specified as $mA/\ \mu\mathrm{m}$ wire width (e.g., $1\ \mathrm{mA}/\mu\mathrm{m}$) or mA per via cut
- EM occurs both in signal (AC=bidirectional) and power wires (DC = unidirectional)
  - Much worse for DC than AC; DC occurs inside cells and in power buses

Example: Current Density



There is a high current density due to a narrow *metal3* power grid strap connecting to the internal RAM.

A failure here is catastrophic.

Reasons of Electromigration

Reasons of EM Violation:

- High Fanout Net(Multiple fanout cells switch simultaneously, draws larger current from driver)
- Higher Driver strength Cells (delivers large current unnecessarily, heating up the wire)
- Higher Frequency (quick tarnsitions)
- Narrow Metal Width.
- Metal slotting (resulting into narrower widths)
- Long Nets (because of larger resistance, higher localized temperature)

Prevention techniques for EM:

During the physical design, the following techniques could be used to prevent the EM issue.

Solutions of EM Violation:

- Decrease Drive's drive Strength.
- Insert Buffer on long nets.
- Increase the width of wire
- Adding more vias (Multi-Cut Vias)
- Break the fanout (have lessar fanout)
- Switch the net to higher metal layers.

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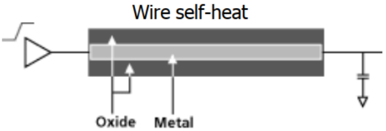
What Is Joule Heating?

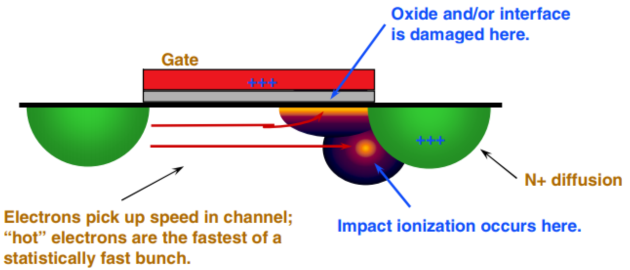
Wire Self-Heat (WSH)

- May also be called signal wire electromigration, or Joule heating, since it is related to the power that is dissipated into the interconnect.
- WSH is the rise in temperature due to the electron movement within a conductor.
- Depends on metal composition, signal frequency, wire sizes, slew rates, and amount of capacitance driven
- Self-heating = More EM
  - Since SH increases temperature, self-heating on a metal line can aggravate EM effects.
  - SH on a line can also increase EM effects on neighboring lines.
- Because self-heating contributes to electromigration, failures are typically labeled as EM, not SH.

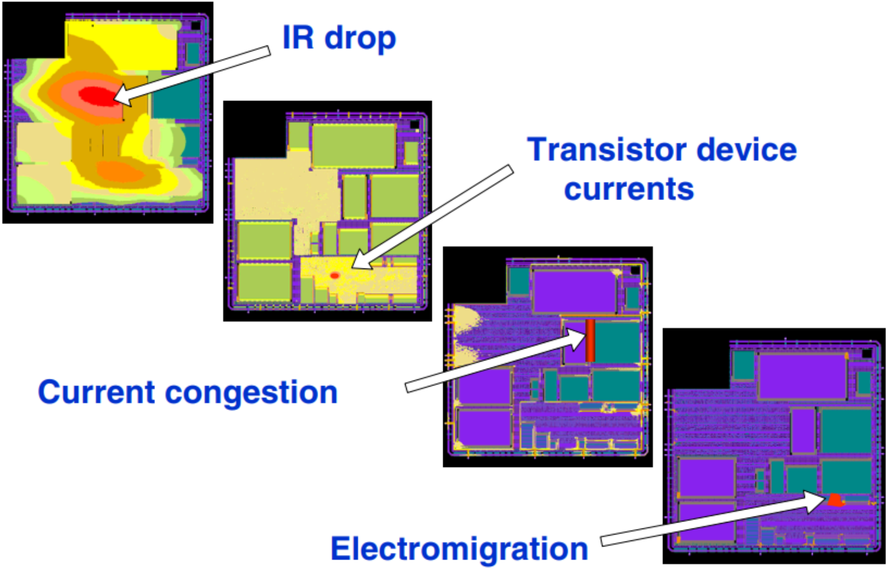


Hot Electron Effect (Short Channel Effect)

- Caused by extremely high electric fields between source and drain
  - Occurs when voltages are not scaled as fast as dimensions
- Electrons pick up speed in the channel
- Fastest electrons damage the oxide and interface near the drain
- Transistor threshold and mobility change over the life of the part, i.e., threshold eventually moves to a point where the device no longer meets specifications



Analysis Output from Power Grid Analysis



Wrap up

بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ
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