Standard Cells, and Physical Only Cells
in ASIC Design

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Table of Contents

1. Standard Cells
2. Physical Only Cells

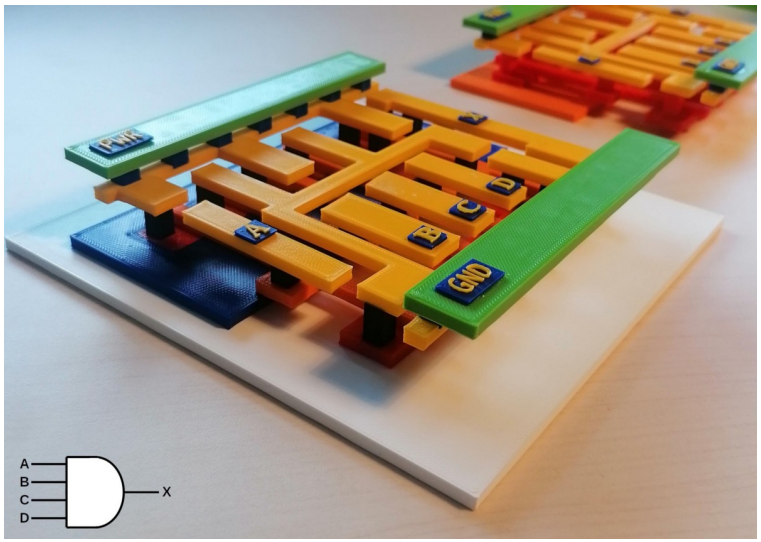
Table of Contents

1 Standard Cells

2 Physical Only Cells

Introduction

- **Standard cells** are a collection of well-defined and pre-characterized cells with multi-drive strength and multi-threshold voltage cells in the form of a predefined standard cell layout.
- It also contains a number of physical only cells and a set of library files required by Place and Route (PnR) tool for automatic placement and routing.
- Standards cells are highly reusable as it is save lots of ASIC design time.



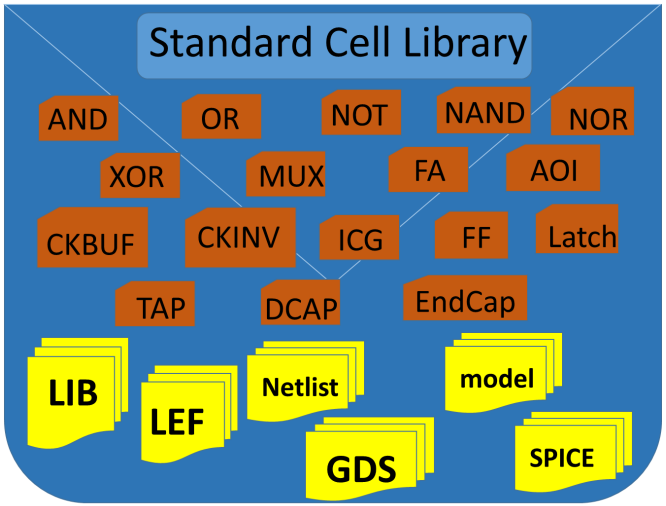
Introduction

- **Pre-characterization:** cells are gone through schematic design, simulations followed by Symbol creation, layout design, physical verifications, abstraction, extraction and characterization.
- **Multi-drive strength cells:**drive strength of a standard cell increases when we increase the size (W/L) of its transistors.
  - cells labeled as "1X", "2X", eg (BUF_1X, BUF_2X, and etc...)
  - low drive strength cell will require less power and area but having more delay and more transition time
  - high drive strength cell can drive a larger number of cells and having a fast transition.
- **Multi-Vt cells:** Multiple threshold voltage techniques use both Low Vt and High Vt cells.
  - **LVT:** Low-Vt cells have a lowered threshold voltage. i.e. it has a faster operation, but leakage currents are more.
  - **HVT** High-Vt cells have the highest threshold voltage for device operation in this group. The cells are slower, but due to the higher threshold, leakage is also lower.

Cell Collections

In general, a standard cell library contains the following types of cell:

- All basic and universal gates (like AND, OR, NOT, NAND, NOR, XOR etc)
- Complex gates (like MUX, HA, FA, Comparators, AOI, OAI etc)
- Clock tree cells (like Clock buffers, clock inverters, ICG cells etc)
- Flip flops and latches
- Delay cells: used to fix hold with huge magnitude of violations
- Physical only cells
- Scannable Flip flops



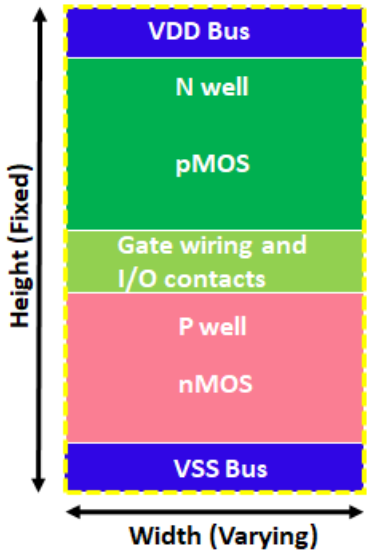
File Collections

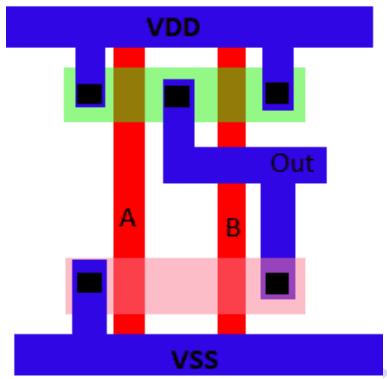
Apart from the standard cells, the Standard cell library is delivered with a collection of files which contains all the information required to auto place and route. These files are mainly:

- LIB files(.lib): Library files contain cell delay, power and area information
- LEF files(.lef): LEF file contains the information of cell boundary, Pins inside the cell, location, direction, and metal layer of each pin.
- Netlist file(.v): Netlist file is a Verilog file of the standard cell which defines the functionality of a cell.
- GDS file(.gds): GDS file is the layout of the standard cell.
- SPICE Netlist(.sp): SPICE netlist is the netlist of cell in SPICE format is used for simulation.
- Model file(.m): contains the various design parameters of the cell required for SPICE simulation.

Standard Cell Layout

- All the Standard cells are in equal in height and varying width.
- At the top of the standard cell, there is VDD rail and bottom there is a VSS rail.
- Both the Power rails are drawn in the Metal-1 layer.
- In between the VDD rail and VSS rail there are three main regions
  - a nwell region, a gap of nwell and pwell and pwell region.
  - nwell region is near to the VDD rail and pwell region is near the VSS rail.
  - pMOS transistors are build inside the nwell, nMOS transistors are build inside the Pwell





Standard Cells Notes

Remember

In standard cell most of the cases, the height of standard cells are constant and width varies.

Remark

There may be double height cells, triple height cell, etc. Similarly the rows also have heights accordingly.

Examples

Level Shifter "is used to shift a signal voltage from one voltage domain to another" may be twice or three times as high as a standard cell with a least height.

Exercises

- Why Multi-Vth Cells are required in Standard cell Library?
- If you have "HVT, SVT, and LVT" Cells Which cells would you use:
  - in order to fix setup violations.
  - in order to fix hold violations.
  - in Low Power Design (Power Density)
- How to implement various drive strength standard cells in fixed height?
- Compare the following cells in terms of: speed, area, and leakage power
  - svt_x2_buf, svt_x8_buf, svt_x16_buf
  - svt_x2_buf, lvt_x2_buf

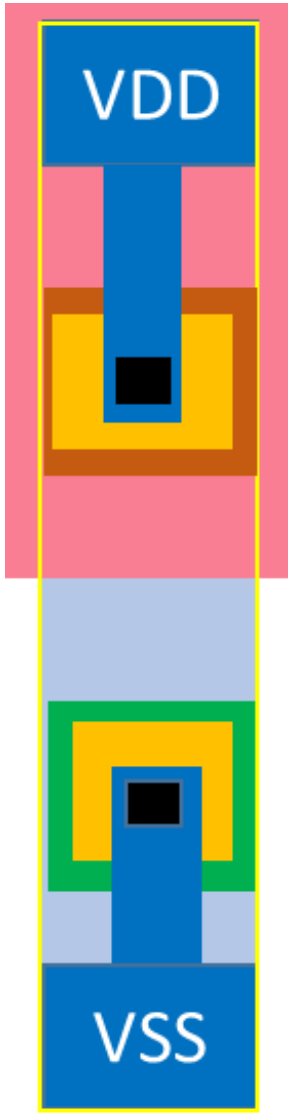
Table of Contents

1 Standard Cells

2 Physical Only Cells

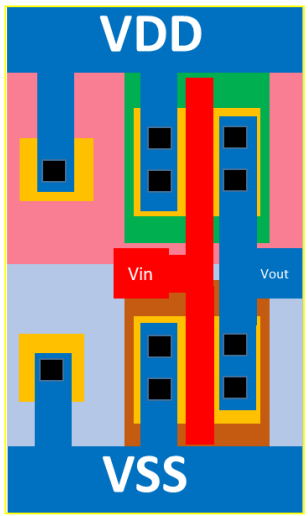
Well Tap Cells

- Well tap cells (or Tap cells) are used to prevent the latch-up issue in the CMOS design.
- Well tap cells have no logical functions, it has only two connections
  - nwell to the power supply (VDD)
  - p-substrate to the ground (VSS)
- Well tap cell has no input and output pins, therefore it is called a physical-only cell.

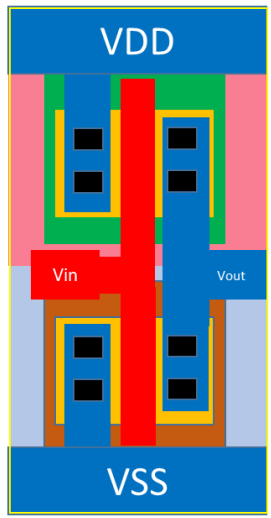


Why Well Tap Cell:

Early days there was no concept of well tap cell, Standard cells were designed in such a way that each standard cell had nwell to VDD and p-substrate to VSS connection within the standard cell. But such a standard cell design had consumed more area and to save the area, later a concept of Tapless cell has evolved. In a tapless cell, there are no well taping inside the standard cell, well taping is provided by a separate standard cell which is called a well tap cell. So well tap cell is a part of a tapless standard cell library



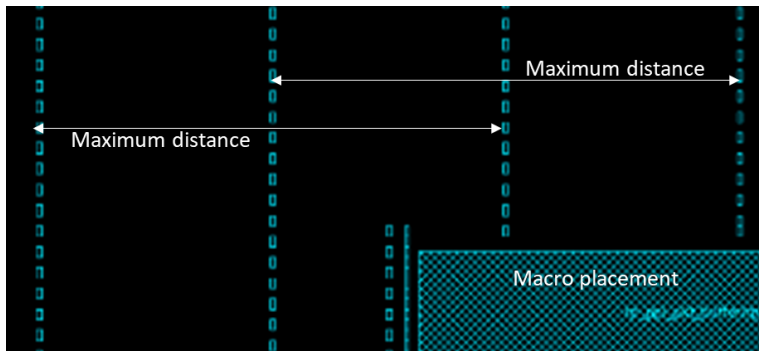
Traditional Standard Cell layout



Tapless Standard Cell layout

Placement of Well Tap Cells:

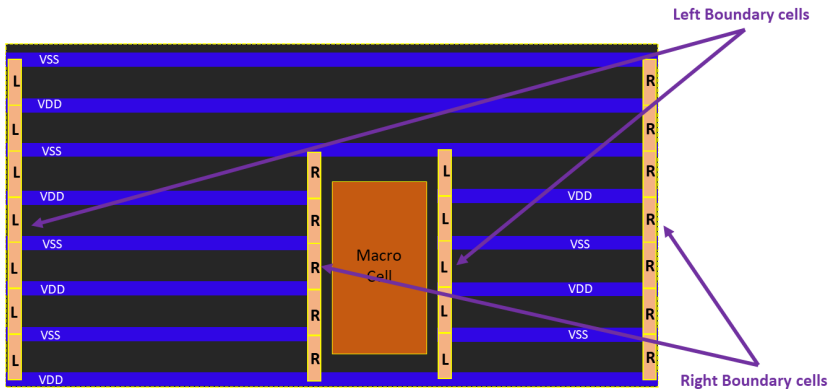
- Well tap cells are placed after the macro placement and power rail creation.
- This stage is called the pre-placement stage.
- Well tap cells are placed in a regular interval in each row of placement.
- The maximum distance between the well tap cells must be as per the DRC rule of that particular technology library.
- If a macro comes in the path of vertical columns, then the placement of vertical column shifted alongside macro as shown in the figure.



End Cap (Boundary) Cells

The end cap cells are placed in the design because of the following reasons:

- Boundary cell is placed at both the ends of each placement row to terminate the row.
- To protect the gate of a standard cell placed near the boundary from damage during manufacturing
- To avoid the base layer DRC (Nwell and Implant layer) at the boundary.
- It has also been placed at the top and bottom row at the block level to make integration with other blocks.



End Cap Cells Notes

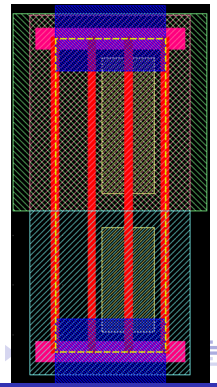
Remember

- The boundary cell is a physical-only cell, has no logical functions and therefore these cells are not a part of the netlist.
- Boundary cells have mainly Nwell layer, implant layers, and dummy poly layer and metal rails.

Remark

Boundary cells are placed just after the macro placement and site row creation. Boundary cell is placed before the placement of standard cells and therefore it is called a pre-placed cell.

- They are also added to isolate any analog IPs and digital part of any chips.



DeCap Cells

Decap cells are basically a charge storing device made of the capacitors and used to support the instant current requirement in the power delivery network

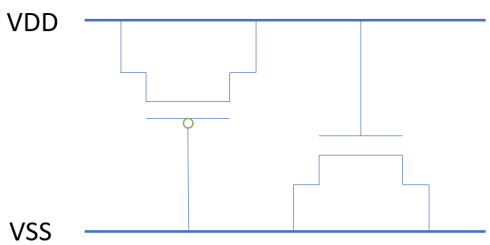
- cells are temporary capacitors added in the design between power and ground rails to counter functional failures due to dynamic IR drop.
- Dynamic IR drop happens at the active edge of the clock at which a high percentage of Sequential and Digital elements switch.
- Due to this simultaneous switching a high current is drawn from the power grid for a small duration.
- If the power source is far away from a flop the chances are that this flop can go into a metastable state due to IR Drop.
- To overcome this decaps are added. At an active edge of clock when the current requirement is high, these decaps discharge and provide boost to the power grid.

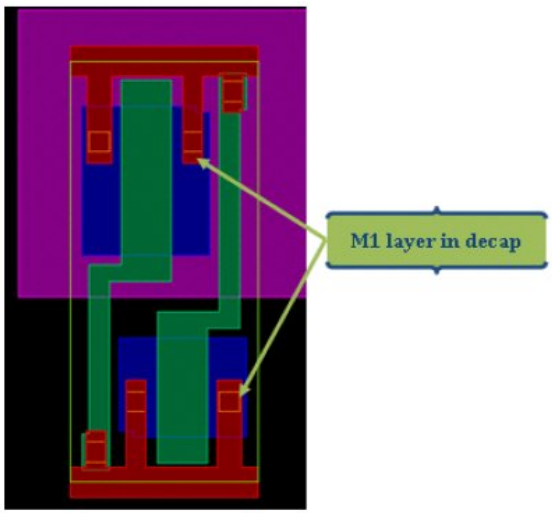
Schematic and layout of Decap cell

Decap cells are typically poly gate transistors where source and drain are connected to the ground rail, and the gate is connected to the power rail.

Remember

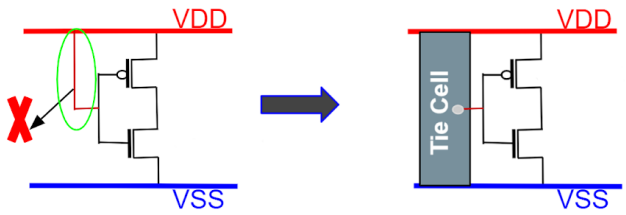
- Decap cells are placed generally after the power planning and before the standard cell placement, that is in the pre-placement stage.
- These cells are placed uniformly throughout the design in this stage. Decap cells can also be placed in the post route stage also if required.





Tie Cells

- The tie cell is a standard cell, designed specially to provide the high or low signal to the input (gate terminal) of any logic gate.
- The high/low signal can not be applied directly to the gate of any transistors because of some limitations of transistors, especially in the lower node.
- In the lower technology node, the gate oxide under the poly gate is a very thin and the most sensitive part of the transistor.
- It has been observed that if the polysilicon gate connects directly to VDD or VSS for a constant high/low input signal, and in case any surge/glitch arises in the supply voltage it results in damage of sensitive gate oxide.
- To avoid theis damages, tie cell is used to connect the input of any logic to the VDD or VSS.



Schematic of tie cells:

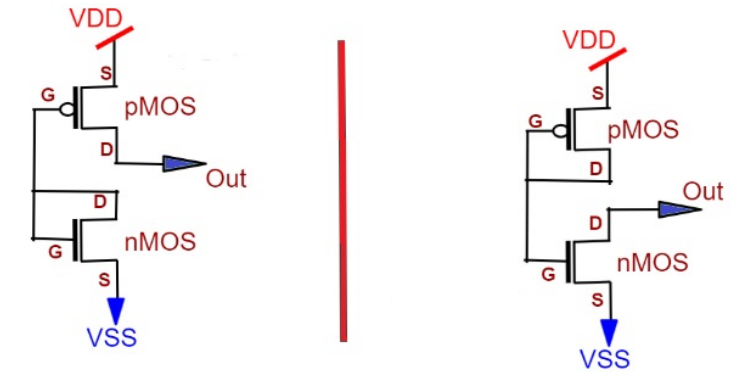
There are two types of tie cells.

- Tie-high cell
- Tie-low cell

As the name suggests, the tie-high cell's output is always high and the tie-low cell's output is always low.

Remember

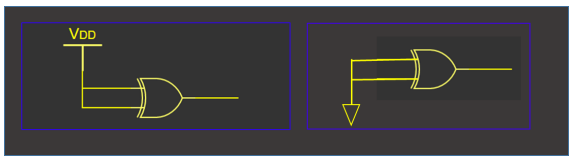
Tie cells are not present in the synthesized netlist and not placed in the initial placement of the standard cells. Tie cells are inserted in the placement stage and more specifically at the final stage of placement.

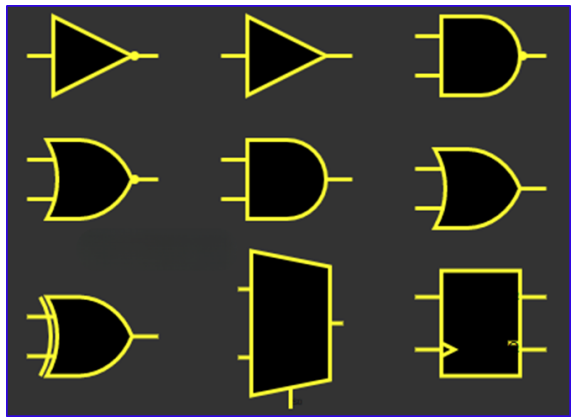


Tie-high Cell Tie-low Cell

Spare cells

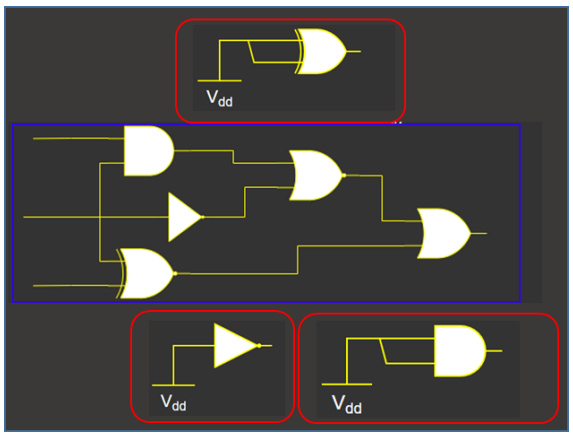
- Spare cells generally consist of a group of standard cells mainly inverter, buffer, nand, nor, and, or, exor, mux, flip flops and maybe some specially designed configurable spare cells.
- spare cells do not perform any logical operation in the design and act as a filler cell only.
- The inputs of spare cells are tied either VDD or VSS through the tie cell and the output is left floating.
- Input can not be left floating as a floating input will be prone to get affected by noise and this could result in unnecessary switching in space cells which leads to extra power dissipation





Use of Spare cells

- Spare cells enable us to modify/improve the functionality of a chip with minimal changes in the mask.
- We can use already placed spare cells from the nearby location and just need to modify the metal interconnect.
- There is no need to make any changes in the base layers. Using metal ECO we can modify the interconnect metal connection and make use of spare cells.
- We only need to change some metal mask, not the base layer masks.



Placement of Spare cells:

Remember

Spare cells are added before the placement of standard cells throughout the design

Remark

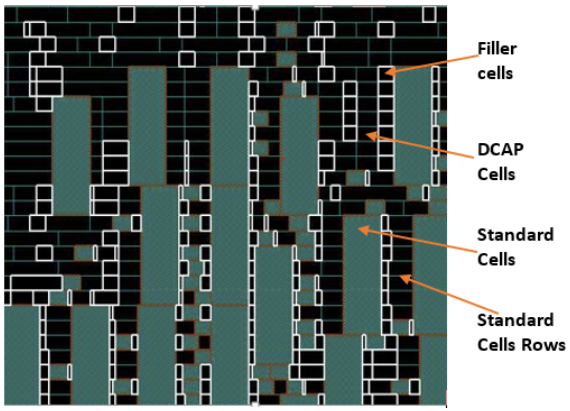
Spare cells can be added either by the netlist or by PnR tool command.

Placing spare cells using ICC

```
place_opt
set physopt_tie_spare_cells true
insert_spare_cells -lib_cell INVX5 DFFCPX2
      -cell_name spare -num_instances 2 -tie -skip_legal
legalize_placement -incremental
spread_spare_cells [get_cells spare*] -bbox 30 30 350 150
psynopt
```

Filler Cells

- Once you have completed placement and routing, there are usually gaps left in the layout where you do not have any standard cells present.
- So, if you say you have 70% utilization, you can expect around 30% of the area unfilled.
- If you do DRC check now(in a tool that can give you base layer DRCs), you can expect to see spacing violations like "NWell minimum spacing not met".
- Filler cells inserted by the P&R tool to fill gaps in the layout after placement and routing is completed. Filler cell insertion must be completed before physical verification can begin.



Filler Cells Continue...

- To ensure that all power nets are connected, you can fill empty space in the standard-cell rows with filler cells.
- Filler cells have no logical connectivity. these cells are provided continuity in the rows for VDD and VSS nets and it also contains substrate nwell connection to improve substrate biasing.
- Filler cell insertion is often used to add decoupling capacitors to improve the stability of the power supply and discontinuity in power

when we placed filler cells in the design

when optimization of clock tree synthesis is completed i.e after timing has been met because let's say if we want to place buffer/inv for optimization purpose we can't place these cells because there is already placed filler cells, and enough area is not there to present buffer/inv, so after timing has been met and routing optimization is done then only placed the filler cells to fill the empty space.

Filler Cells Continue...

بِسْمِ اللَـهِ الرَحمَـن الرَحيمِ

وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلً