Ahmed Abdelazeem

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Summary

Well-versed in physical design implementation of chips and digital processors. Looking for an opportunity to work as a physical design engineer where I can utilize my skills to enhance my knowledge in Circuit Design, SoC and ASIC Back-end flow.

Education

Bachelor of Engineering in in **Electronics and communications** July 2016 - June 2021
Zagazig University **Very Good**

Relevant Coursework: *Electric Circuits, Electronic Devices and Circuits, Logic Design, Signal and Systems, Digital Signal Processing, CMOS Integrated Circuits, Computer Organization and Architecture, VLSI Modeling and Design*

Technical Skills

Languages: C, Python, Matlab

HDL: Verilog, VHDL

Logic Synthesis: DC(Synopsys), Genus(Cadence)

Place & Route: ICC(Synopsys), Innovus(Cadence)

Physical Verification: LVS, DRC, ERC, Density rules

Other Tools: Vivado, VCS, QuestaSim, PrimeTime, Calibre, Cadence Virtuoso, HSpice

Technologies/Frameworks: Linux, GitHub, Git, LaTeX

Experience

FPGA Design Engineer Dec 2021 - Dec 2022
Military Conscription, Benha Electronics Co.

- Designed and implemented FPGA-based solutions for the military services, including signal processing systems for the Air Defense Forces Research and Development department as part of my obligatory military service.

ASIC Physical Design Intern Jul 2022 - Sep 2022
ICpedia

- Responsible for Physical Implementation of an IP: starting from Netlist to GDS, including floorplanning, Placement, Clock design, Optimization, Timing closure, DRC/LVS, and sign-off.

ASIC Physical Design Intern Apr 2021 - Apr 2021
Synopsys

- Responsible for the entire PNR flow for the ORCA TOP chip using DC and IC Compiler using "SAED 32/28nm PDK" with 50K - 60K gates and operates at 60MHz frequency. and also have worked on PT for learning the basics of STA.

ASIC Physical Design Intern Jan 2021 - Feb 2021
Cadence

- 7-Days hands-on workshop: to learn and run complete synthesis and Implementation flow on a design with the given specifications and optimize it for PPA with Cadence Genus Synthesis and Innovus.

ASIC Design Intern Dec 2020 - Dec 2020
Arm Ltd

- 5-Day hands-on workshop: to develop Arm Cortex-M0 based SoCs, from creating high-level functional specifications to design, implementation, and testing on FPGA platforms using standard HDL and software programming languages.

ASIC Physical Design Intern Aug 2020 - Nov 2020
One Lab.

- RTL to GDSII: going through digital design flow starting from Constraint, Synthesis, PnR steps, Timing, Sign off, and Physical verification. Making sure to meet PPA and physical specifications until the design is clean to be fabricated

Projects

High-Speed Microcontroller for Display intensive Application, GP Sep 2020 - July 2021

- I was responsible for the complete physical design of 180nm Digital Top block and also to IP harden the CORTEX-M0 sub chip. Did the entire PnR flow using Cadence Encounter for the same and also the STA using PrimeTime and physical verification for both the hardened IP and Digital Top block.

MSDAP Chip Design **(Verilog, C, FPGA)** Jan 2021 - Mar2021

- Developed Verilog RTL code for high speed, low power MSDAP- ASIC chip using Xilinx ISE consisting of a Controller, ALU, Memories and serial communication unit, and verified the system functionality in C. aslo I synthesized the design in Design Compiler & Performed pre-layout simulation in Modelsim. And also developed Final Physical Design using the IC Compiler, Performed Clock Tree Synthesis, Optimization, Parasitic (RC) extraction, Static Timing Analysis (STA).

Design and Implementation of UART **(Verilog, System-Verilog, FPGA)** Sep 2020 - Nov 2020

- Complete the Digital Design Flow from the RTL2GDS using 45nm Free PDK. synthesized the verilog code using DC Compiler, and aslo did the entire PnR flow using Synopsys IC Compiler.

Design and Implementation of 32 – bit RISC Processor **(Verilog, VHDL, FPGA)** Oct 2019 - May 2020

- Implemented the behavioral model of a 32-bit microprocessor using VHDL on Altera Cyclone IV FPGA
- Complete the Digital Design Flow of the RISC using 45nm, with 10 metal layers, and 500MHZ frequency. Synthesized the VHDL code in DC Compiler
- Developed Final Physical Design using the IC Compiler. Performed Clock Tree Synthesis, Optimization, Parasitic (RC) extraction using PrimeTime., Static Timing Analysis (STA).

COURSES

C Programming. Udemy,2017

Hardware Modeling using Verilog by Prof. Indranil Sengupta. YouTube,2018

Introduction to FPGA Design for Embedded Systems. Coursera,2018

CMOS Analog IC Design by Prof. Hesham Omran. Mahara-Tech ,2019

VLSI CAD Part II: Layout by Rob A. Rutenbar. Coursera,2019

Python and Data Structures. Coursera,2020

Digital VLSI Design (RTL2GDS) by Prof. Adam Teman. YouTube,2020

VLSI Physical Design by Prof. Indranil Sengupta. YouTube,2020

VSD - Static Timing Analysis - I & II. Udemy,2022

VSD - Physical Design Flow. Udemy,2022

UPF Power Aware Design & Verification by Robin Garg. Udemy,2022

EXTRA-CIRRUCULAR

Project Management Jan 2019 - Feb 2020

Enactus ZU

- Conducting several types of research and analysis on the 17 SDGs and connecting them to local problems.
- Prepare clear and concise reports, proposals, and other written materials of a technical nature
- Design, implement, and manage ongoing projects and direct the related resources and activities to successful completion.

PR director Jan 2018 - Sep 2018

Hult Prize Foundation, ZU

- Negotiating and receiving governmental and non-governmental grants up to 40,000 EGP