Ahmed Abdelazeem

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To whom it may concern:

I am a Physical Design Engineer with experience in Synopsys and Cadence tools. I have worked on projects ranging from small to large, and I have a proven track record of success. I am confident that I can be an asset to your team and contribute to the success of your company.

Successfully completed the physical design of multiple block and chip level designs from netlist to GDSII. Performed detailed routing, timing closure, power analysis, clock tree synthesis, place & route for digital standard cell based designs. Involved in full cycle of SoC projects including pre silicon validation (static timing/formal verification), post Si sign-off and tape out support.

As a physical design engineer, I have experience working with various IC layout tools and methodologies. My strengths include being able to work independently as well as in a team environment, being detail-oriented, and having excellent problem solving skills. In addition, I am also proficient in using scripting languages such as Perl/Tcl for automation purposes.

Thank you for taking the time to review my application. I look forward to hopefully meeting with you in the future to further discuss my qualifications for a position as an ASIC Physical Design at [COMPANY NAME] this upcoming summer. If you have any questions, please feel free to email me at a.abdelazeem201@gmail.com or call me at +20-102-876-8232.

Sincerely,

Ahmed Abdelazeem