Ahmed Abdelazeem

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Objective: Digital Design Engineering graduate with 2 years of work experience at various internships seeking opportunities to enhance my knowledge in Digital Design, SoC and ASIC Back-end flow.

Education

Aug 2016 – May 2021 | ***Bachelor of Engineering*** **- Electronics and communications Engineering** GPA: 3.20
Faculty of Engineering,
Zagazig University, Zagazig, Egypt.

Work Experience

Dec 2021 – Dec 2022 | ***Military Conscription*** **- FPGA Design Engineer**
- Developed a FPGA peripheral interfaces (UART, I2C, SPI, storage, high speed serial I/F's).
- Designed and implemented high-performance DSP algorithms on FPGAs for use in radar applications.

Jul 2022 – Sep 2022 | ***Summer Intern @ICpedia*** **- ASIC Physical Design**
- Responsible for Physical Implementation of an IP - starting from Netlist to GDS, including floorplanning, Placement, Clock design, Optimization, Timing closure, DRC/LVS, LEC, ERC, and sign-off.

Apr 2021 – Apr 2021 | ***Summer Intern @Synopsys*** **- ASIC Physical Design**
- Responsible for the entire PNR flow for the ORCA TOP chip using **DC and IC Compiler** using "SAED 32/28nm PDK" with 50K - 60K gates and operates at 60MHz frequency.

Jan 2021 – Feb 2021 | ***Winter Camp @Cadence*** **- ASIC Physical Design**
- Synthesized, implemented and verified a DTMF receiver Chip using **Genus and Innovus** using Artisan 180 nanometer process technology with 6 layers of metal.
- The DTMF design contains almost 6,000 instances, 57 IO pads, and about 6,274 nets.

Dec 2020 – Dec 2020 | ***Winter Camp @Arm Ltd*** **- ASIC Design**
- 5-Day hands-on workshop: to develop Arm Cortex-M0 based SoCs, from creating high-level functional specifications to design, and implementation on FPGA platforms using standard HDL & SW.

Aug 2020 – Nov 2020 | ***Summer Intern @One Lab*** **- ASIC Physical Design**
- RTL to GDSII: going through digital design flow starting from Constraint, Synthesis, PnR steps, Timing, Sign off, and Physical verification.

Technical Projects

Sep 2020 – Jul 2021 | ***Microcontrollers with Graphics Display*** **- Graduation Project**
- PnR execution for Digital Top block and also to IP harden the CORTEX-M0 sub chip. from netlist to GDS which included floorplanning, clock and power distribution timing closure, physical and electrical verification.

Jan 2021 – Mar 2021 | ***MSDAP Chip Design*** **- Freelance Project**
- Developed Verilog RTL code for high speed, low power MSDAP- ASIC chip using Vivado and verified the system functionality in C. aslo synthesized the design in **DC** & developed Final Physical Design using the **IC Compiler**, Performed Parasitic (RC) extraction, Static Timing Analysis (STA).

Sep 2020 – Nov 2020 | ***Design and Implementation of UART*** **- Personal Project**
- Complete the Digital Design Flow from the RTL2GDS using 45nm Free PDK. synthesized the verilog code using DC Compiler, and aslo did the entire PnR flow using Synopsys IC Compiler.

Oct 2019 – Dec 2019 | ***Design and Implementation of 32 – bit RISC Processor*** **- Personal Project**
- Developed the behavioral model of a 32-bit microprocessor using Verilog on Altera Cyclone IV FPGA, aslo synthesized and implemented using DC & IC Compiler.

Technical Skills

Languages: C, Python, Matlab, TCL scripting
Logic Synthesis: DC(synopsys), Genus(Cadence)
Signoff tools: StarRC, PrimeTime, Calibre, Virtuoso
Physical Verification: LVS, DRC, ERC, Density rules
HDL: Verilog, SystemVerilog, VHDL
Place & Route: ICC(Synopsys), Innovus(Cadence)
FE Tools: Vivado, VCS, QuestaSim, HSpice
Technologies: Linux, GitHub, Git, LaTeX