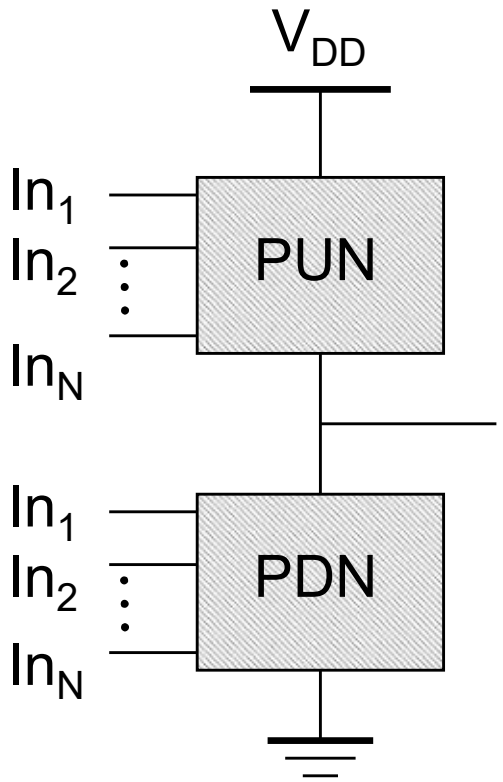
Static Complementary CMOS: Complex Gates

- Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

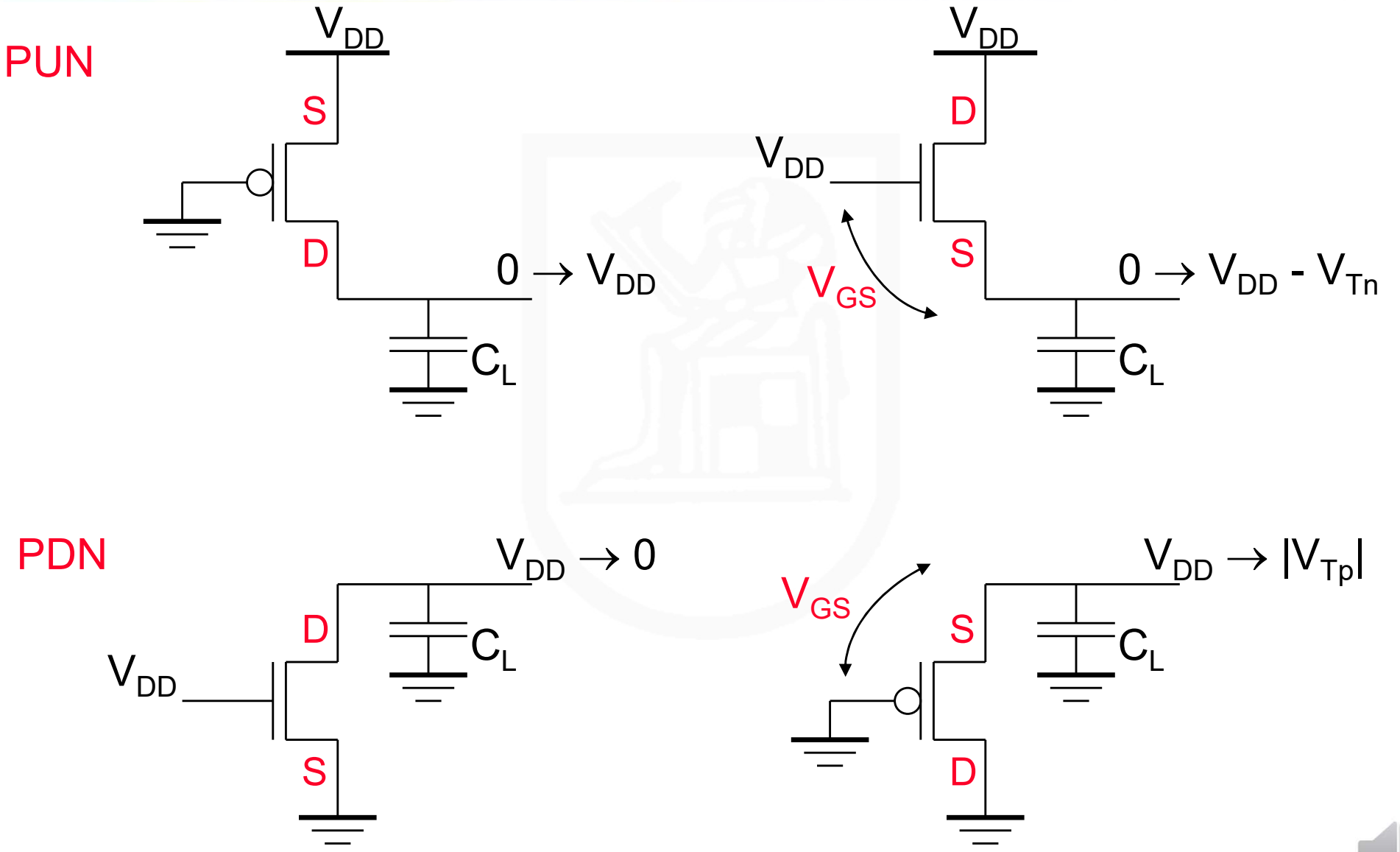
pull-up: make a connection from V_{DD} to F when $F(In_1,In_2,\ldots In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1,In_2,\ldots In_N) = 0$

NMOS transistors only

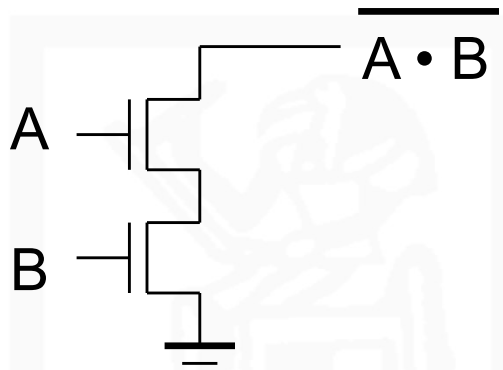
PUN and PDN are dual logic networks

Threshold Drops

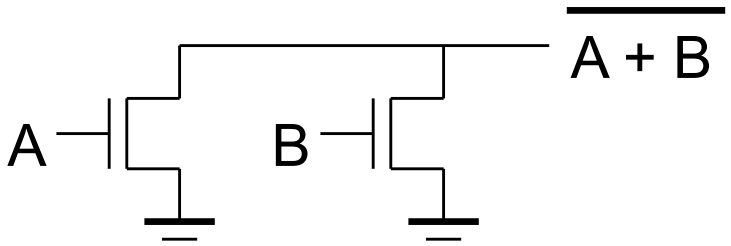


Construction of PDN

- NMOS devices in series implement a NAND function



- NMOS devices in parallel implement a NOR function



Dual PUN and PDN

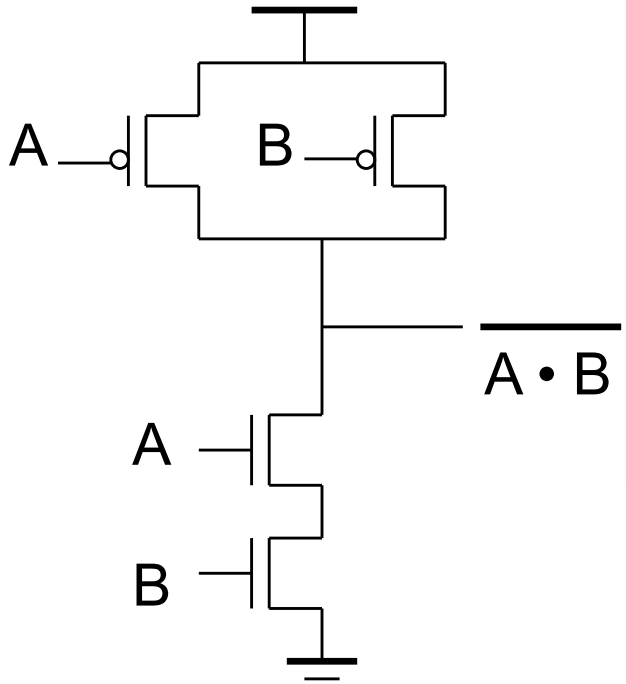
- PUN and PDN are dual networks
  - DeMorgan's theorems

$$\overline{A + B} = \overline{A} \cdot \overline{B} \quad [!(A + B) = !A \cdot !B \text{ or } !(A \mid B) = !A \,\&\, !B]$$

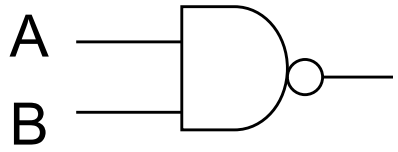
$$\overline{A \cdot B} = \overline{A} + \overline{B} \quad [!(A \cdot B) = !A + !B \text{ or } !(A \,\&\, B) = !A \mid !B]$$

  - a parallel connection of transistors in the PUN corresponds to a series connection of the PDN
- A "complementary gate" is naturally inverting (NAND, NOR, AOI, OAI)
- Number of transistors for an N-input logic gate is 2N

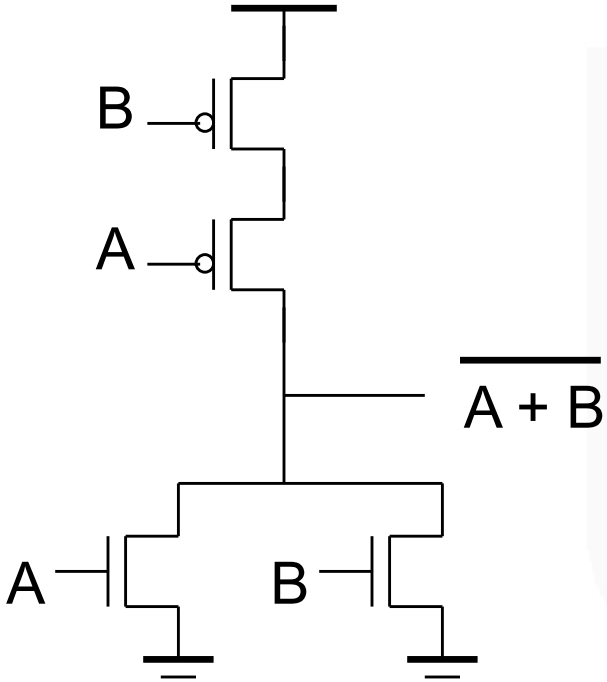
CMOS NAND



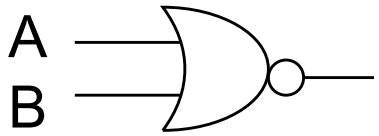
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



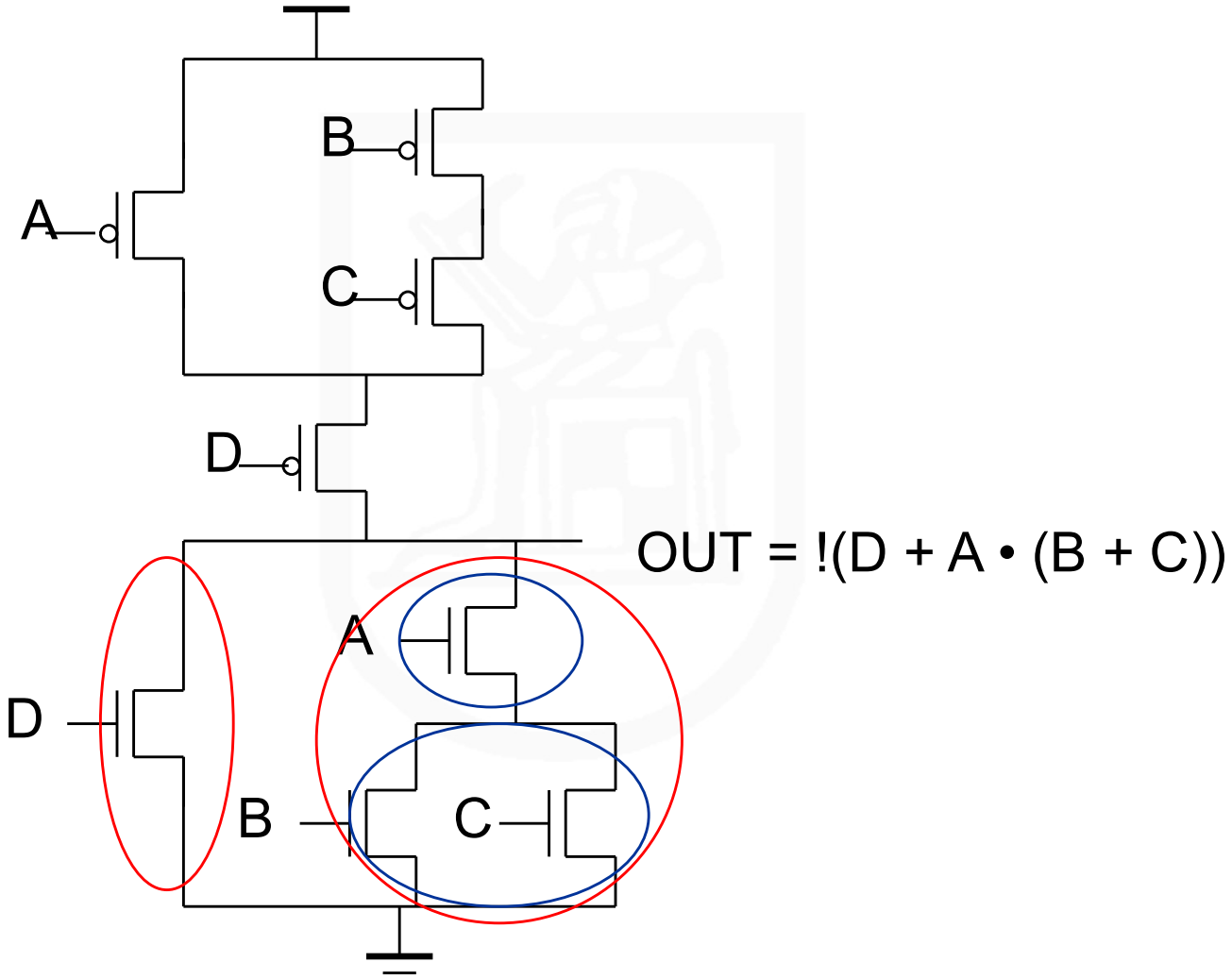
CMOS NOR



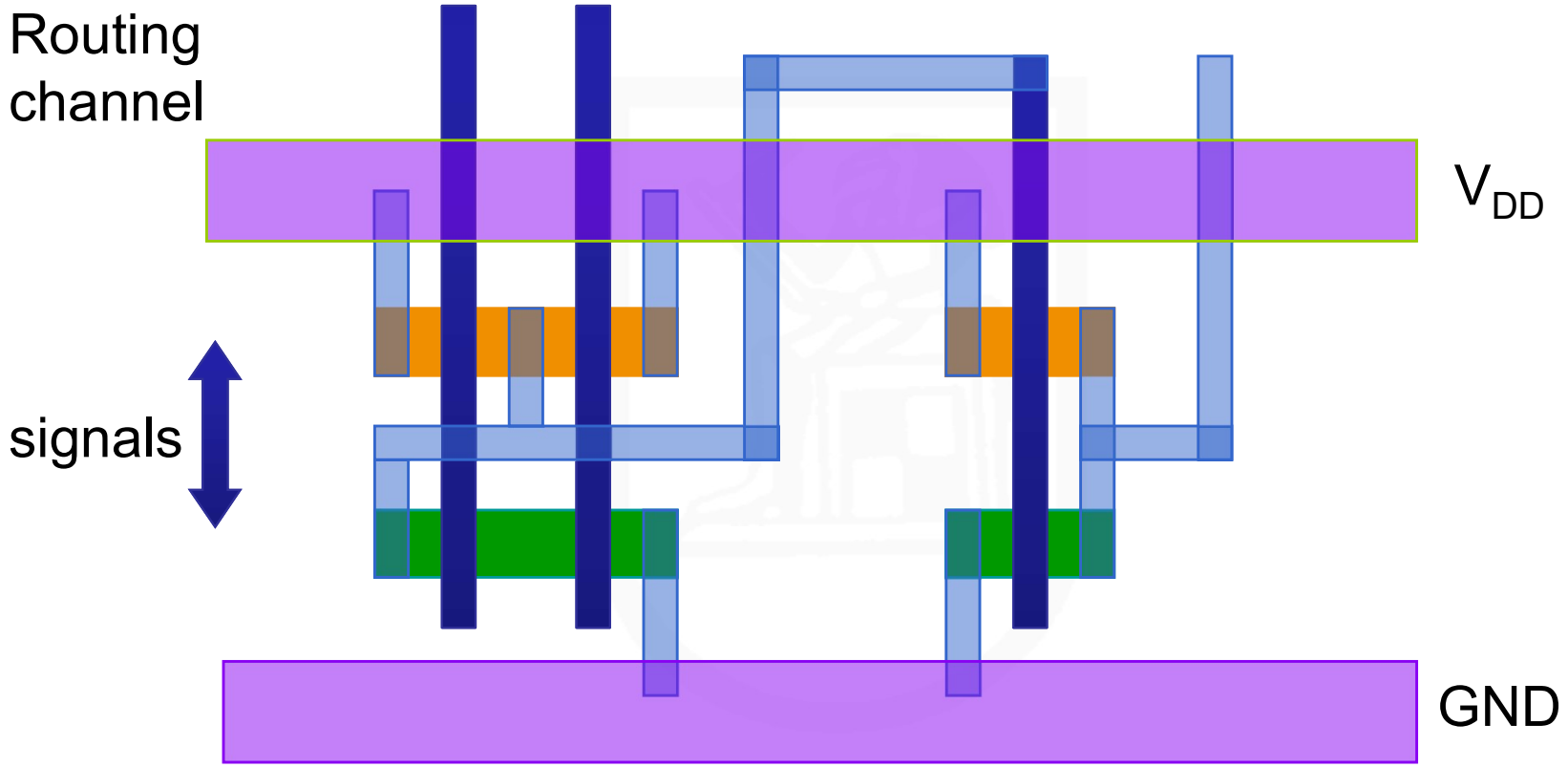
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0



Complex CMOS Gate



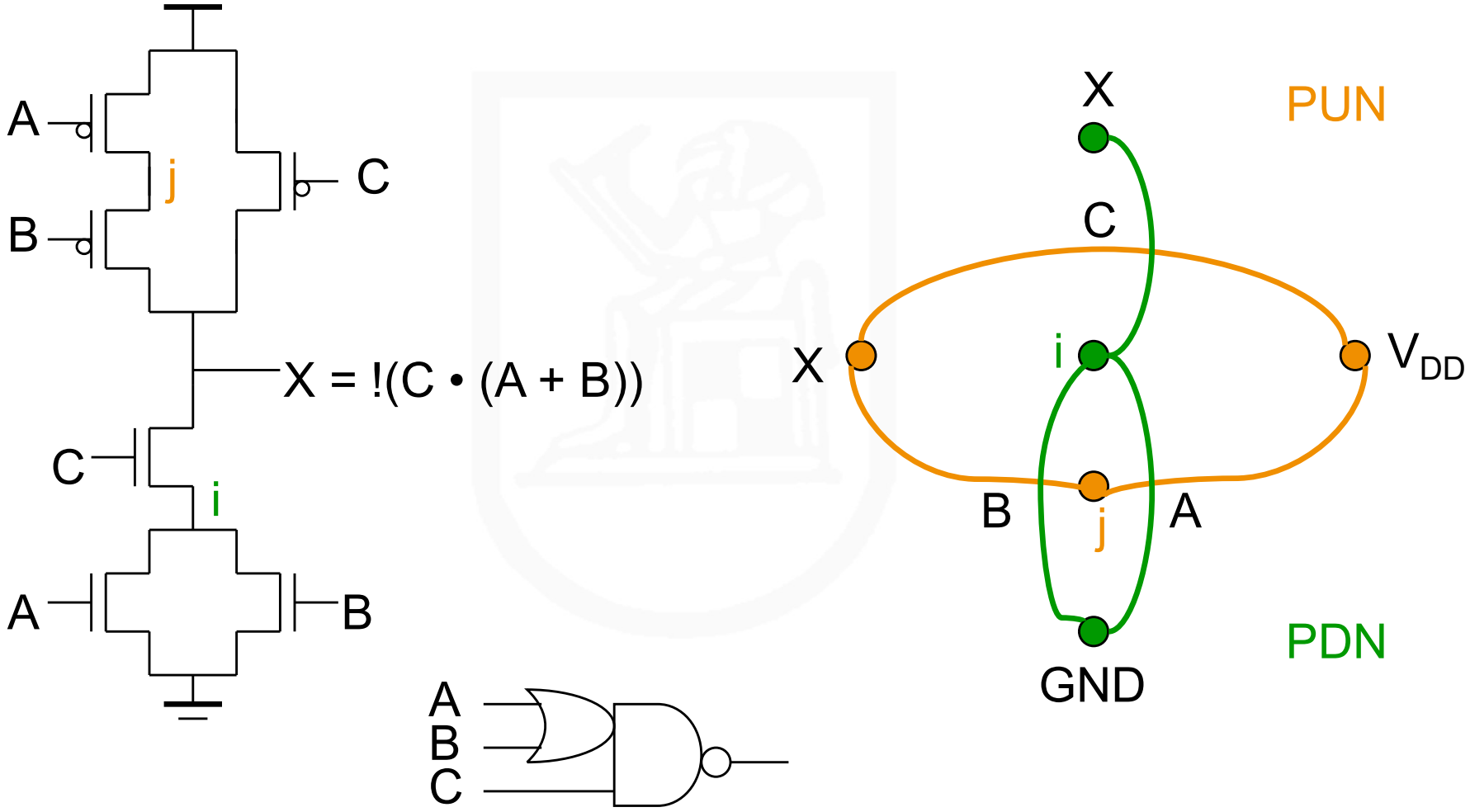
Standard Cell Layout Methodology



What logic function is this?

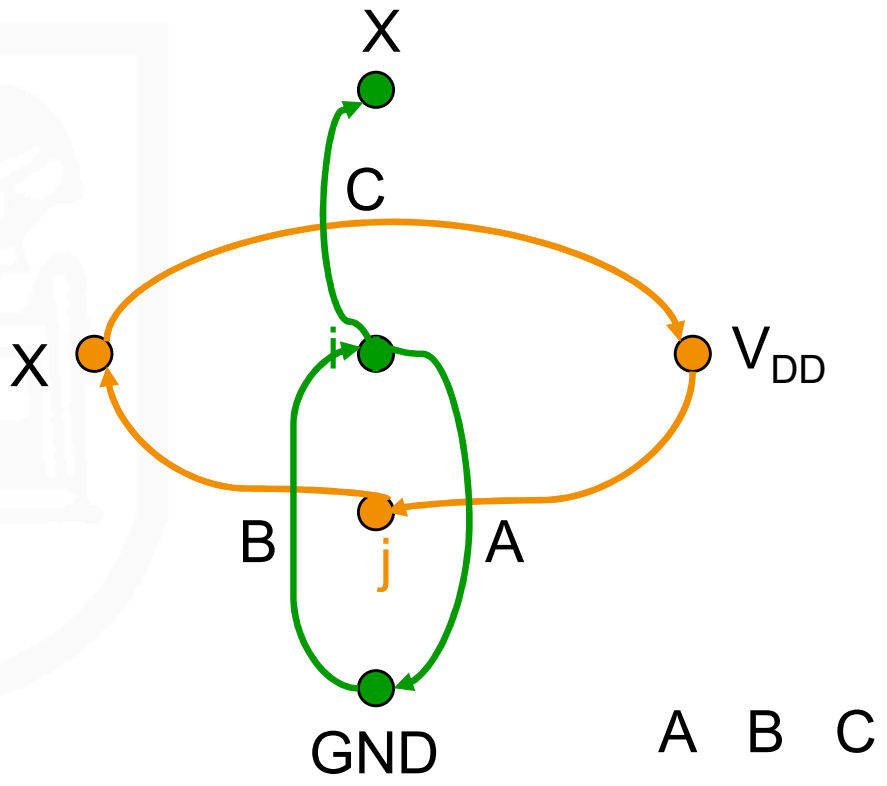
Contacts, vias and wells are not shown!

OAI21 Logic Graph

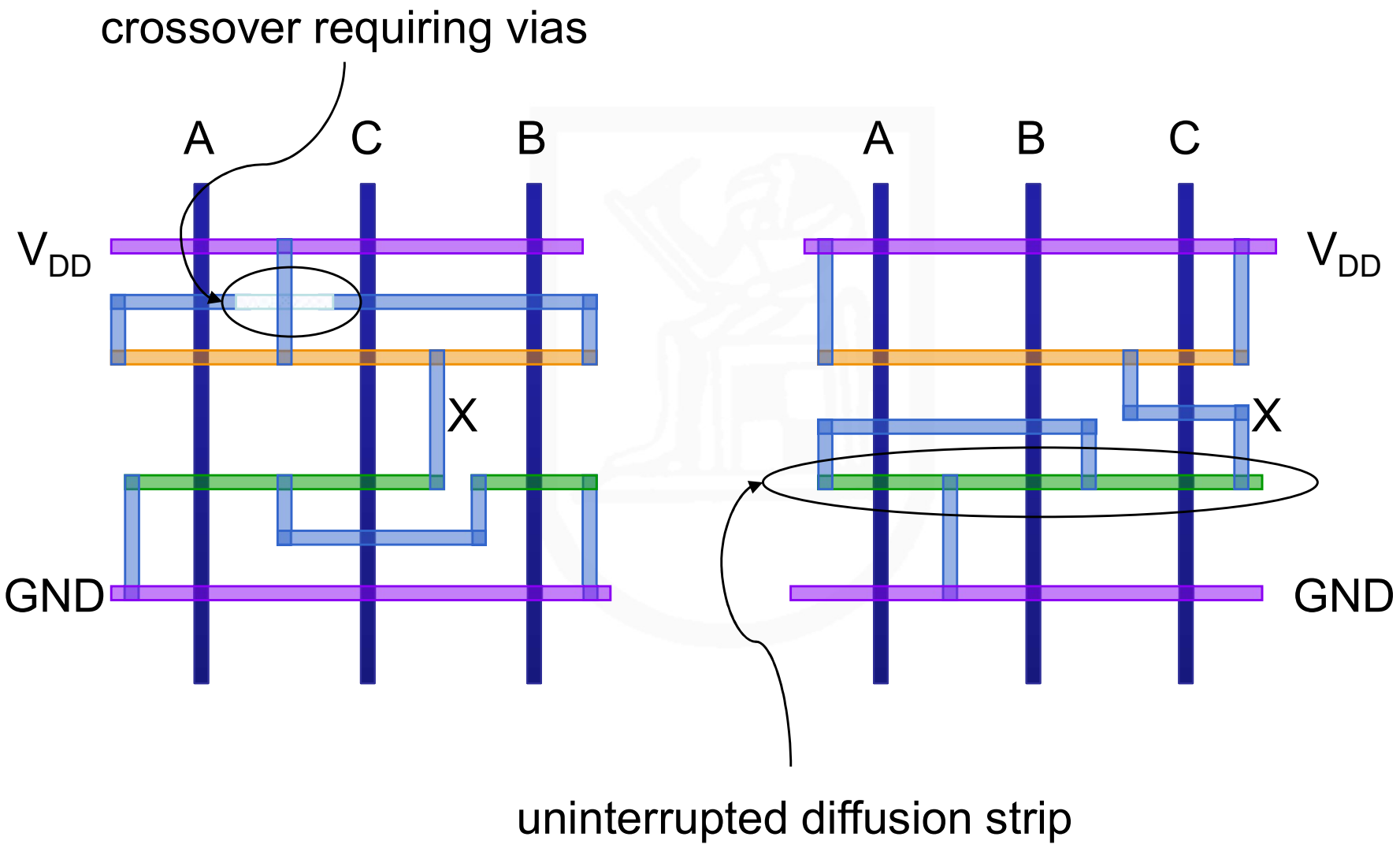


Consistent Euler Path

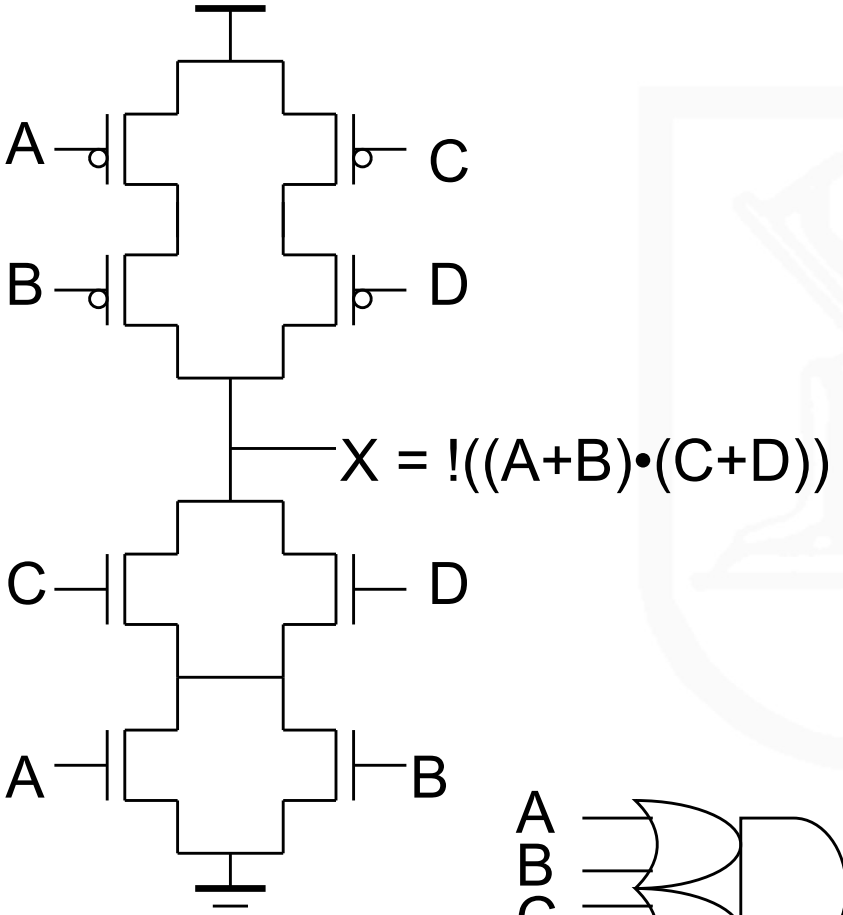
- An uninterrupted diffusion strip is possible only if there exists an Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.
- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

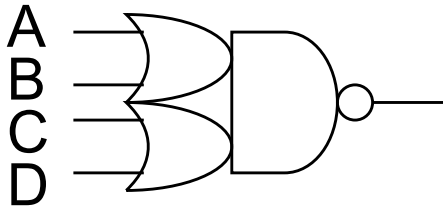


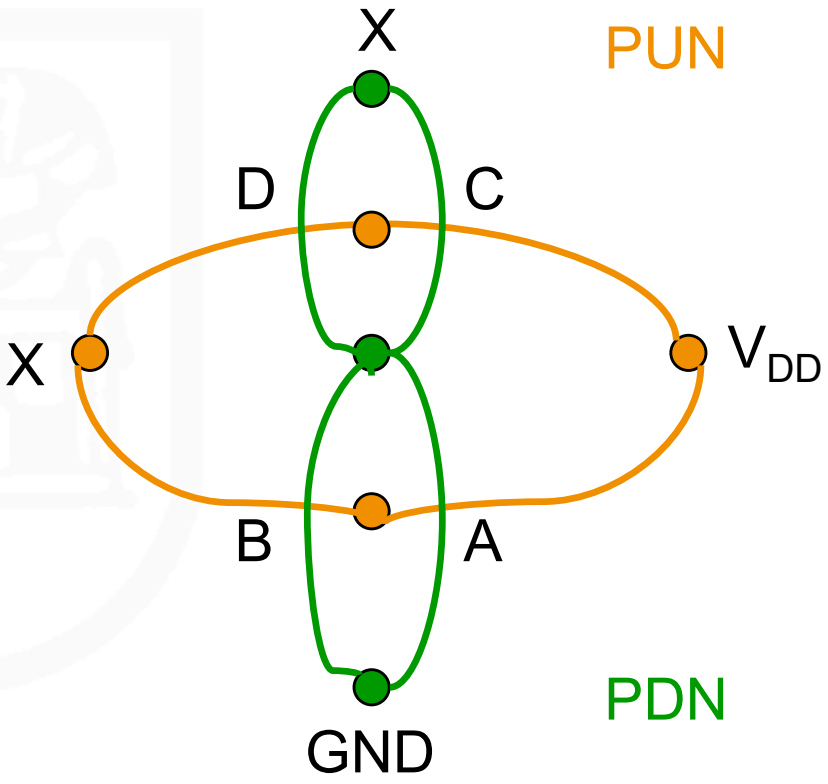
Two Stick Layouts of !(C • (A + B))



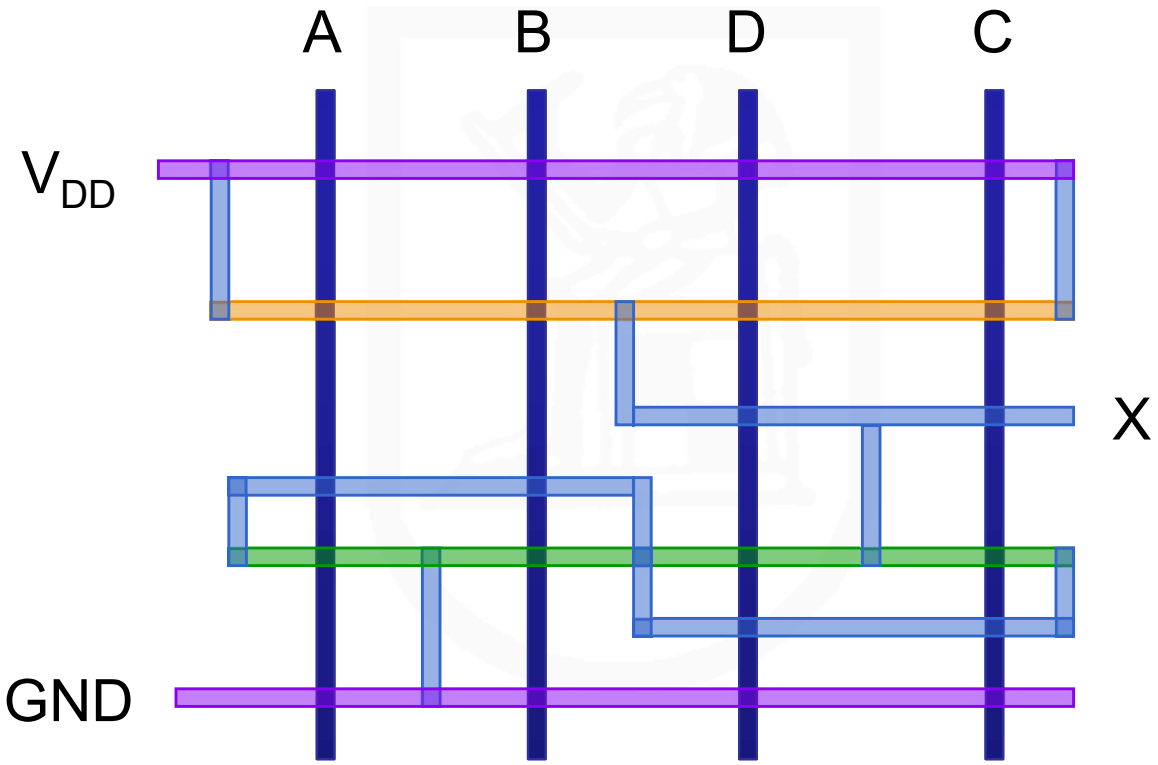
OAI22 Logic Graph



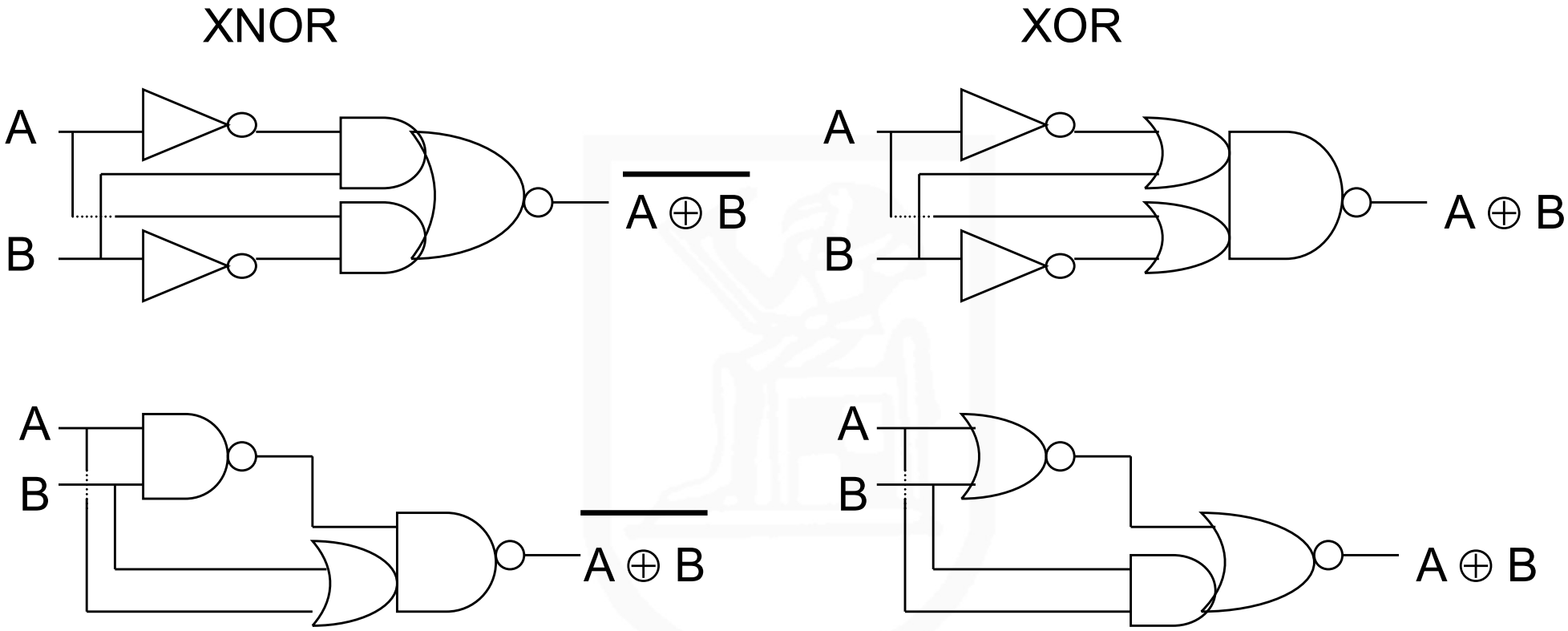




OAI22 Layout



XNOR/XOR Implementation

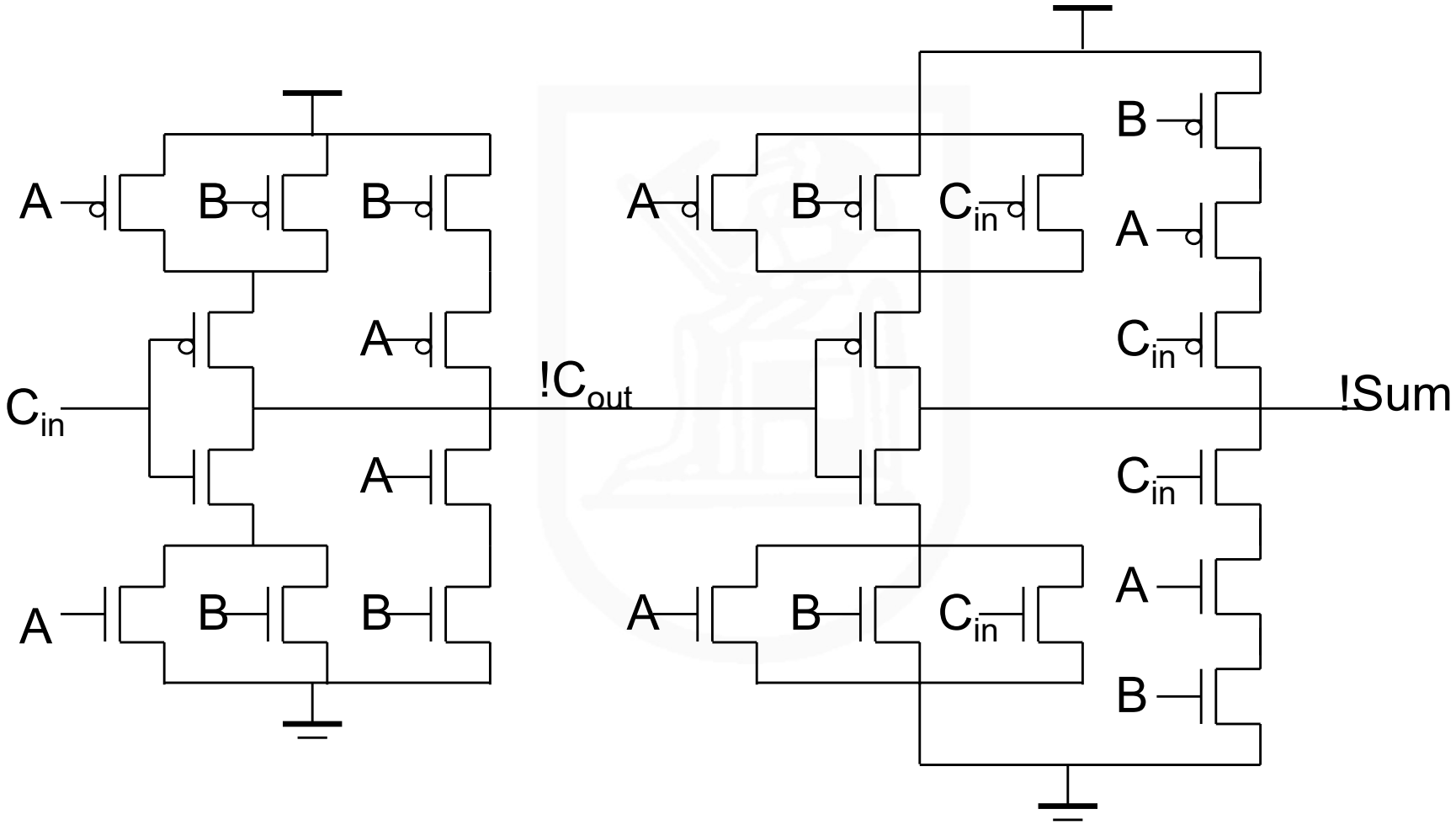


- How many transistors in each?
- Can you create the stick transistor layout for the lower left circuit?

Static CMOS Full Adder Circuit

$!C_{out} = !C_{in} \,\&\, (!A \mid !B) \mid (!A \,\&\, !B)$

$!Sum = C_{out} \,\&\, (!A \mid !B \mid !C_{in}) \mid (!A \,\&\, !B \,\&\, !C_{in})$

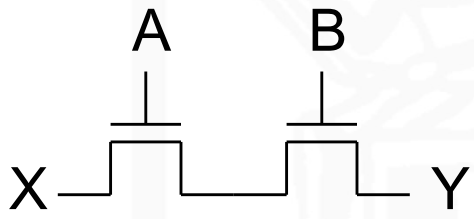


$C_{out} = C_{in} \,\&\, (A \mid B) \mid (A \,\&\, B)$

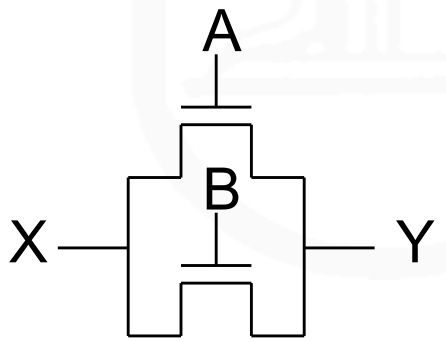
$Sum = !C_{out} \,\&\, (A \mid B \mid C_{in}) \mid (A \,\&\, B \,\&\, C_{in})$

NMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is high



X = Y if A and B

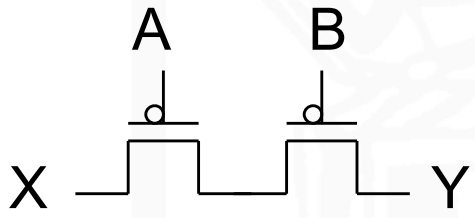


X = Y if A or B

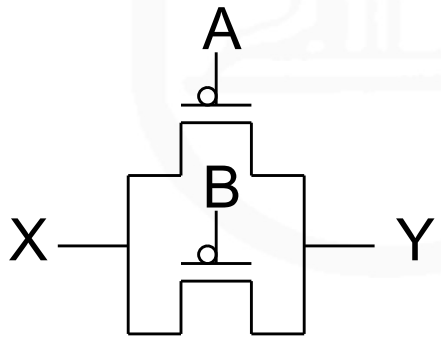
- Remember - NMOS transistors pass a strong 0 but a weak 1

PMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low



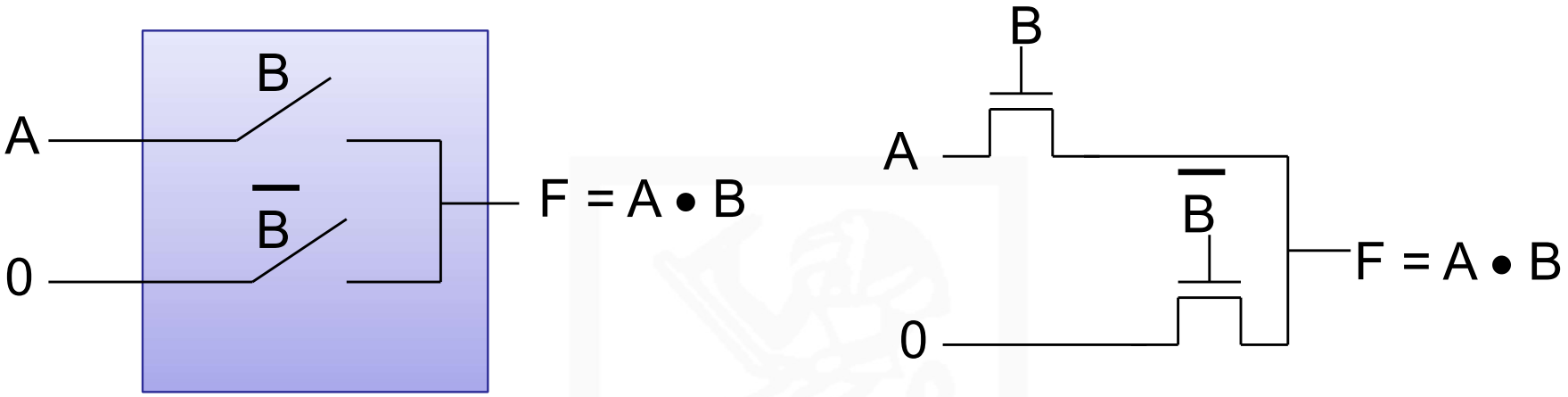
$X = Y$ if $\overline{A}$ and $\overline{B} = \overline{A + B}$



$X = Y$ if $\overline{A}$ or $\overline{B} = \overline{A \bullet B}$

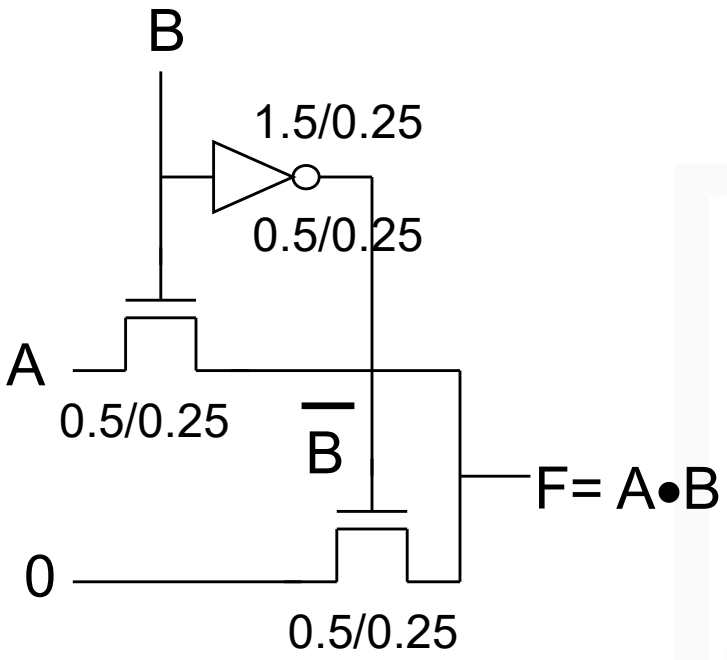
- Remember - PMOS transistors pass a strong 1 but a weak 0

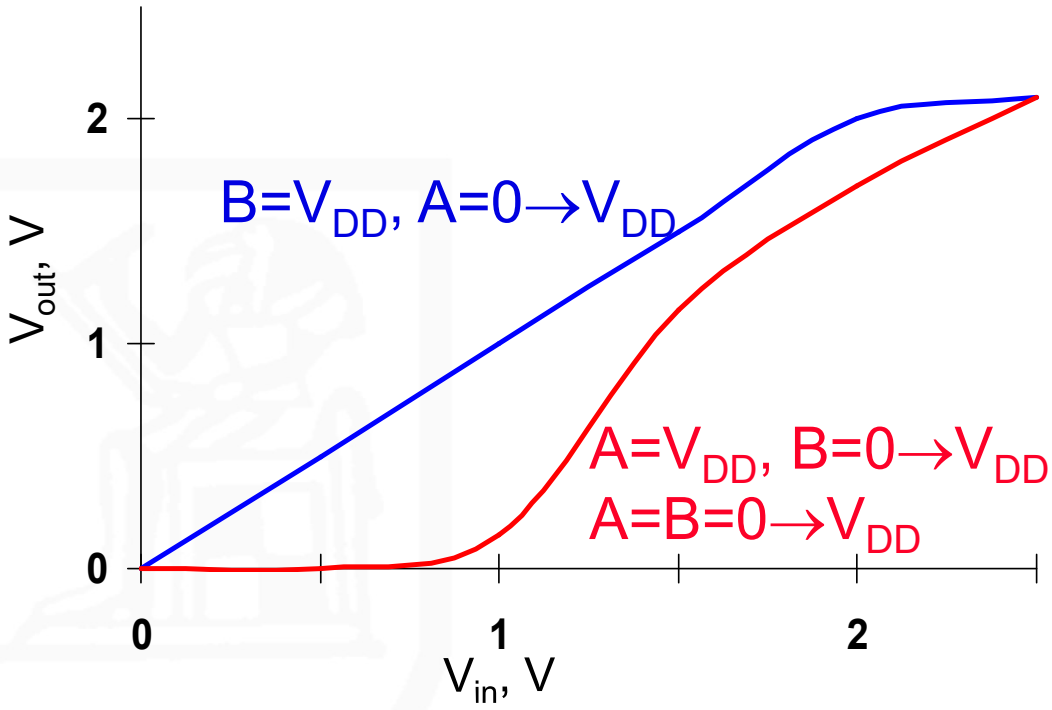
Pass Transistor (PT) Logic



- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)

VTC of PT AND Gate





- Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)

Remember
Voltage-Current Relation: Linear Mode

For long-channel devices (L > 0.25 micron)

- When $V_{DS} \leq V_{GS} - V_T$

$$\mathbf{I_D = k'_n\, W/L\, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]}$$

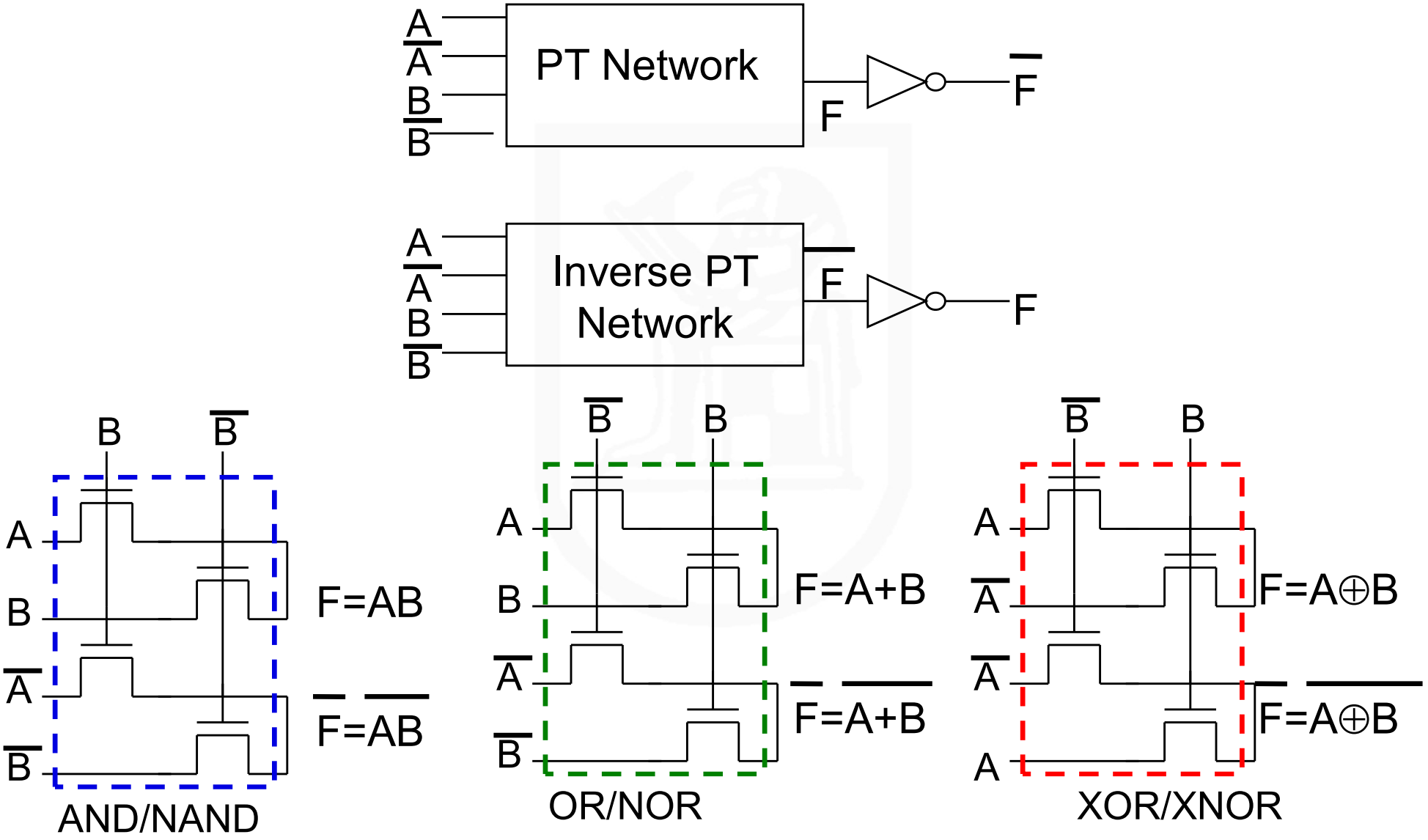
where

$k'_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox}/t_{ox}$ = is the process transconductance parameter (μ_n is the carrier mobility (m^2/Vsec))

$k_n = k'_n\, W/L$ is the gain factor of the device

For small V_{DS}, there is a linear dependence between V_{DS} and I_D, hence the name resistive or linear region

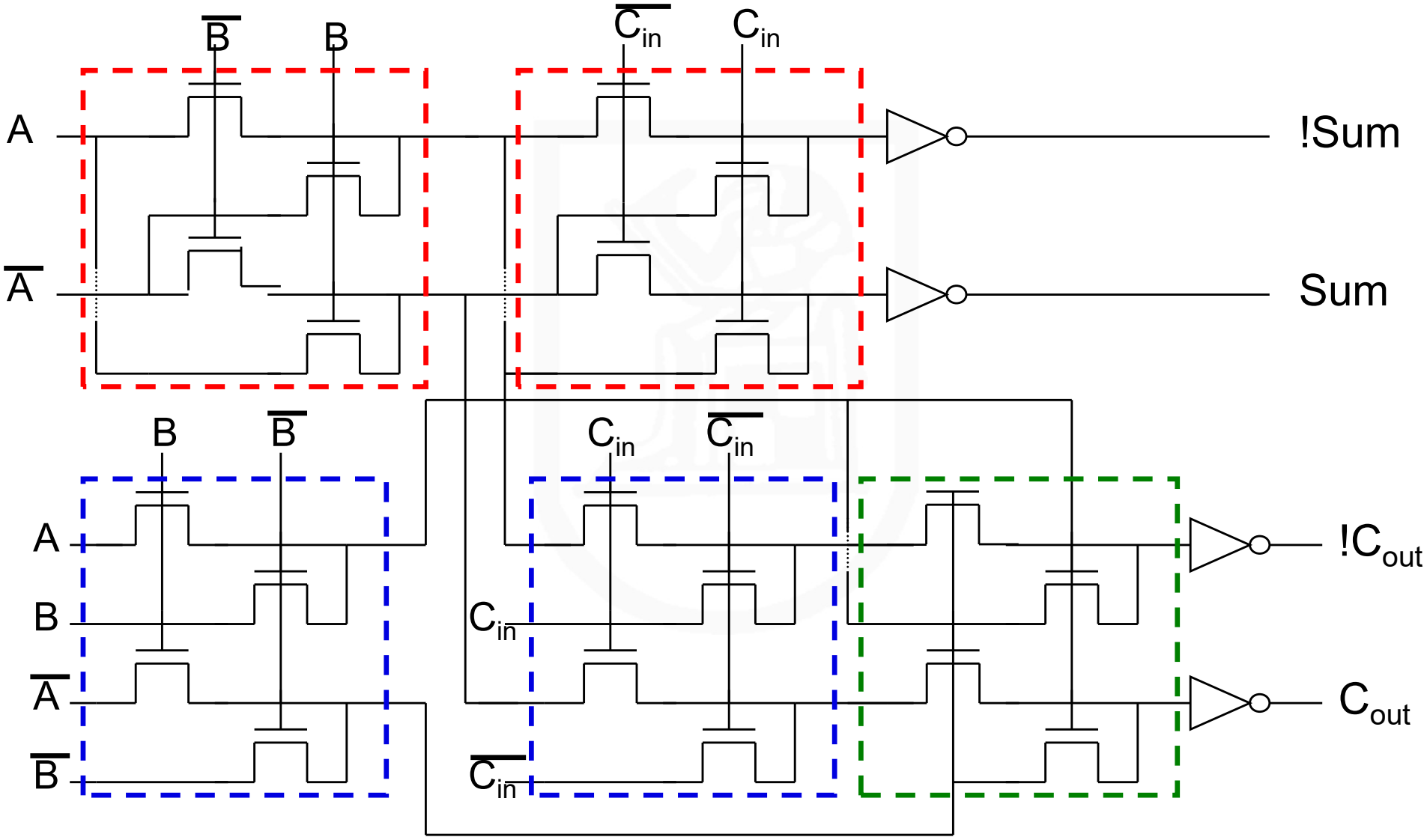
Differential PT Logic (CPL)



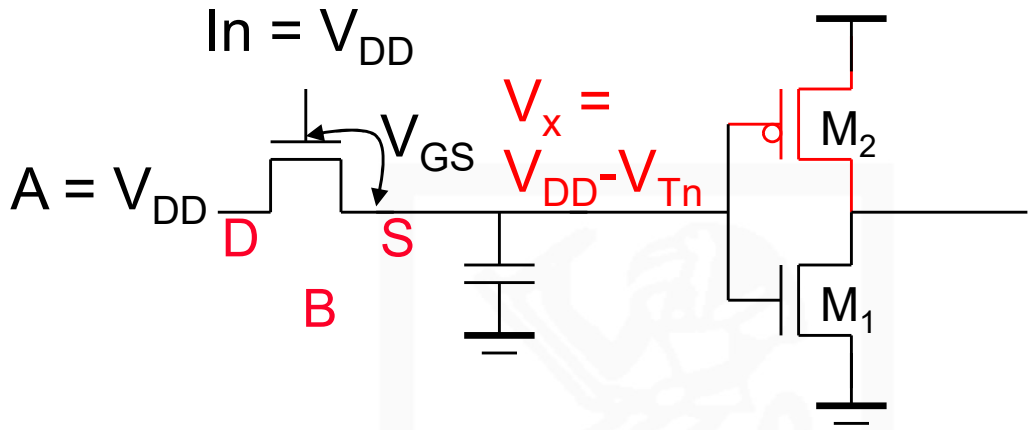
CPL Properties

- Differential so complementary data inputs and outputs are always available (so don't need extra inverters)
- Still static, since the output defining nodes are always tied to V_{DD} or GND through a low resistance path
- Design is modular; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like adders
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
- Still have static power dissipation problems

CPL Full Adder



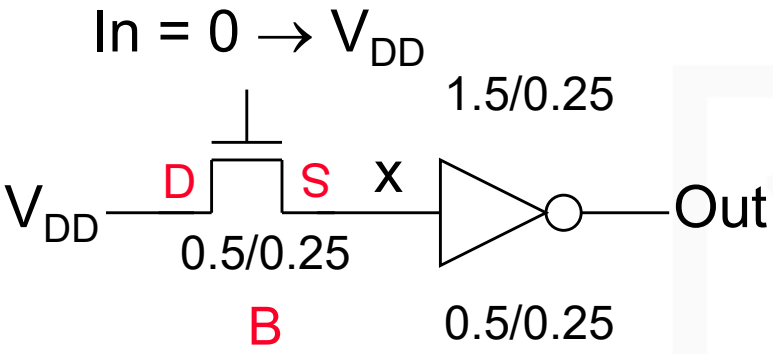
NMOS Only PT Driving an Inverter

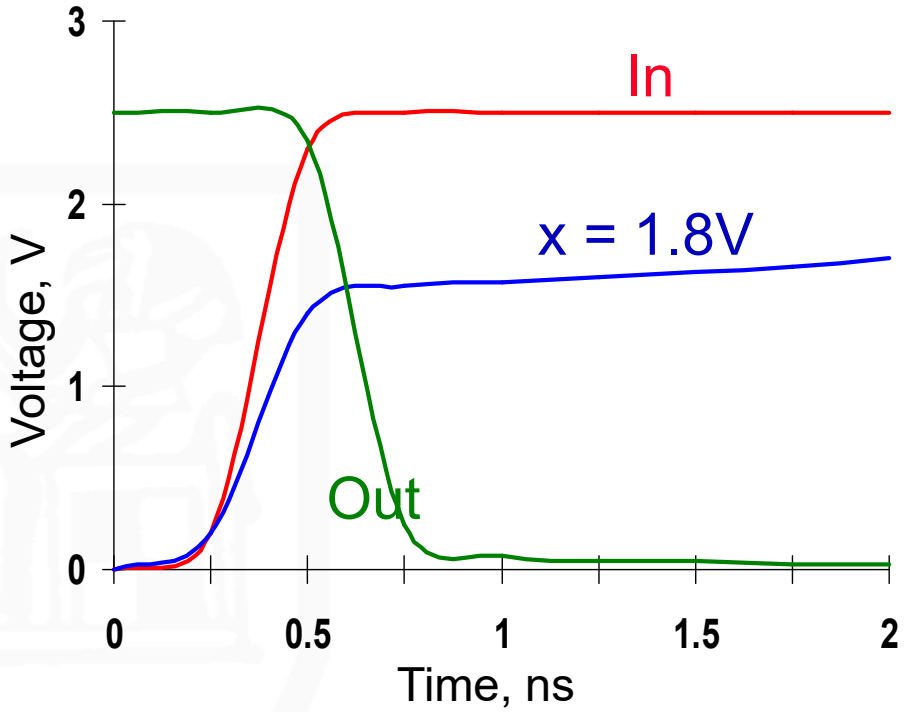


- **V_x does not pull up to V_{DD}, but $V_{DD} – V_{Tn}$**

- Threshold voltage drop causes static power consumption (M_2 may be weakly conducting forming a path from V_{DD} to GND)
- Notice V_{Tn} increases for pass transistor due to body effect (V_{SB})

Voltage Swing of PT Driving an Inverter

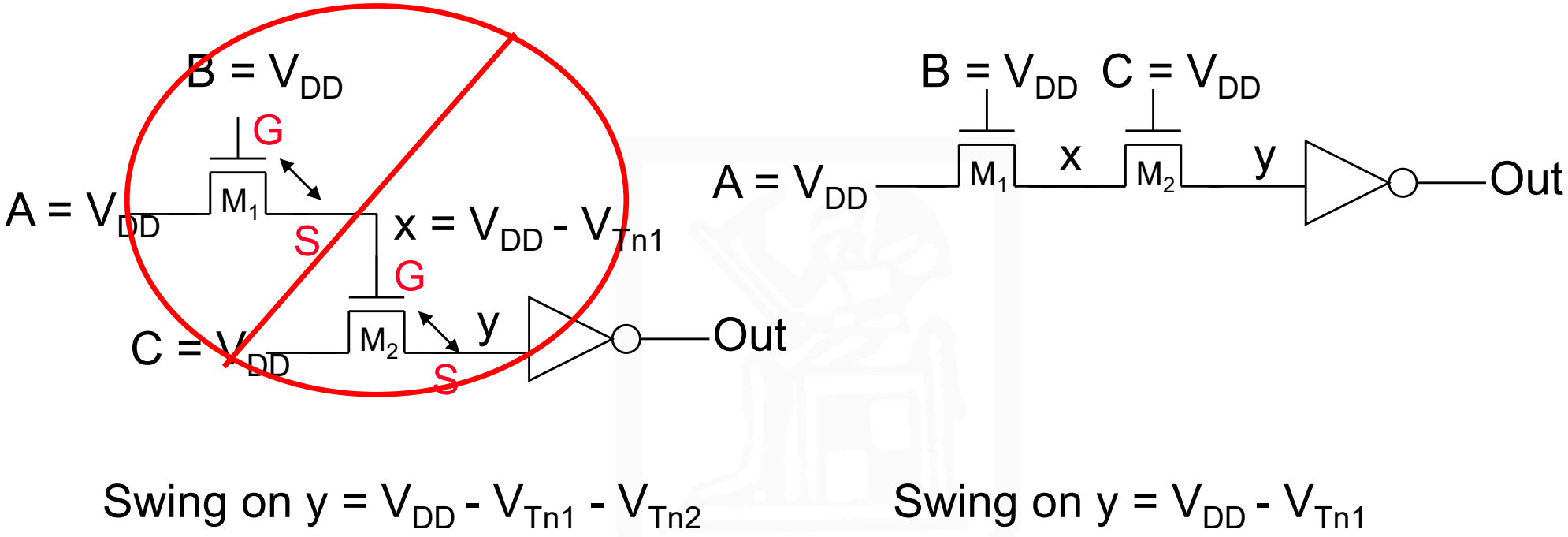




- **Body effect – large V_{SB} at x - when pulling high (B is tied to GND and S charged up close to V_{DD})**
- **So the voltage drop is even worse**

$$V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{(|2\phi_f| + V_x)} - \sqrt{|2\phi_f|}))$$

Cascaded NMOS Only PTs

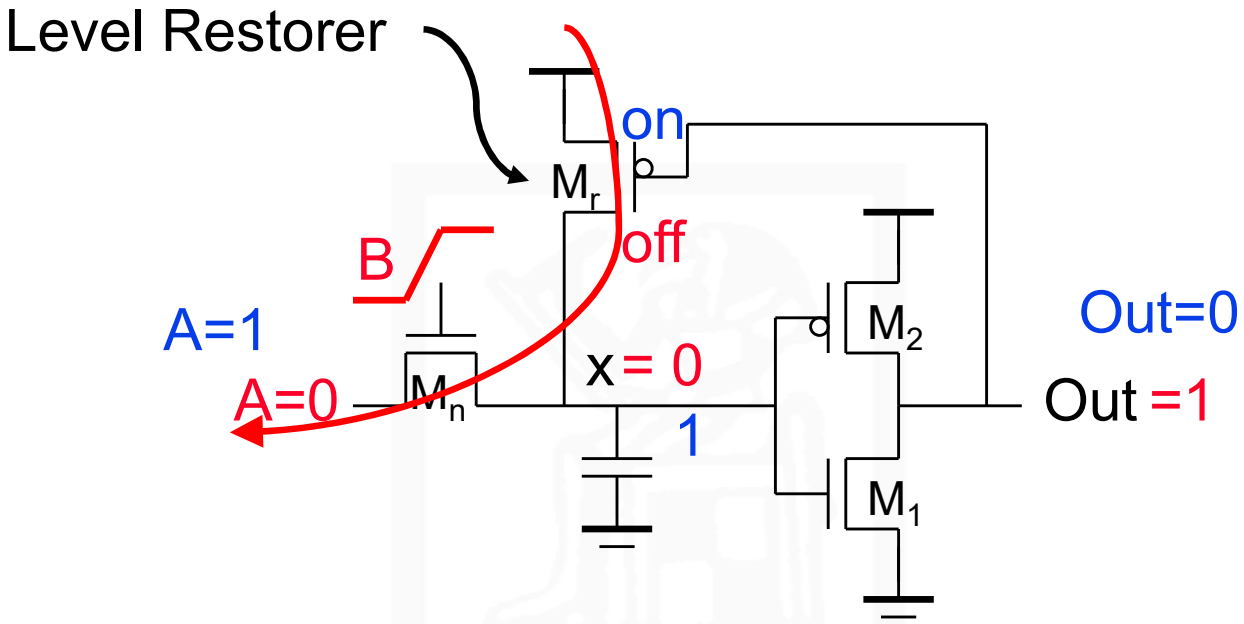


Swing on y = $V_{DD} - V_{Tn1} - V_{Tn2}$

Swing on y = $V_{DD} - V_{Tn1}$

- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins

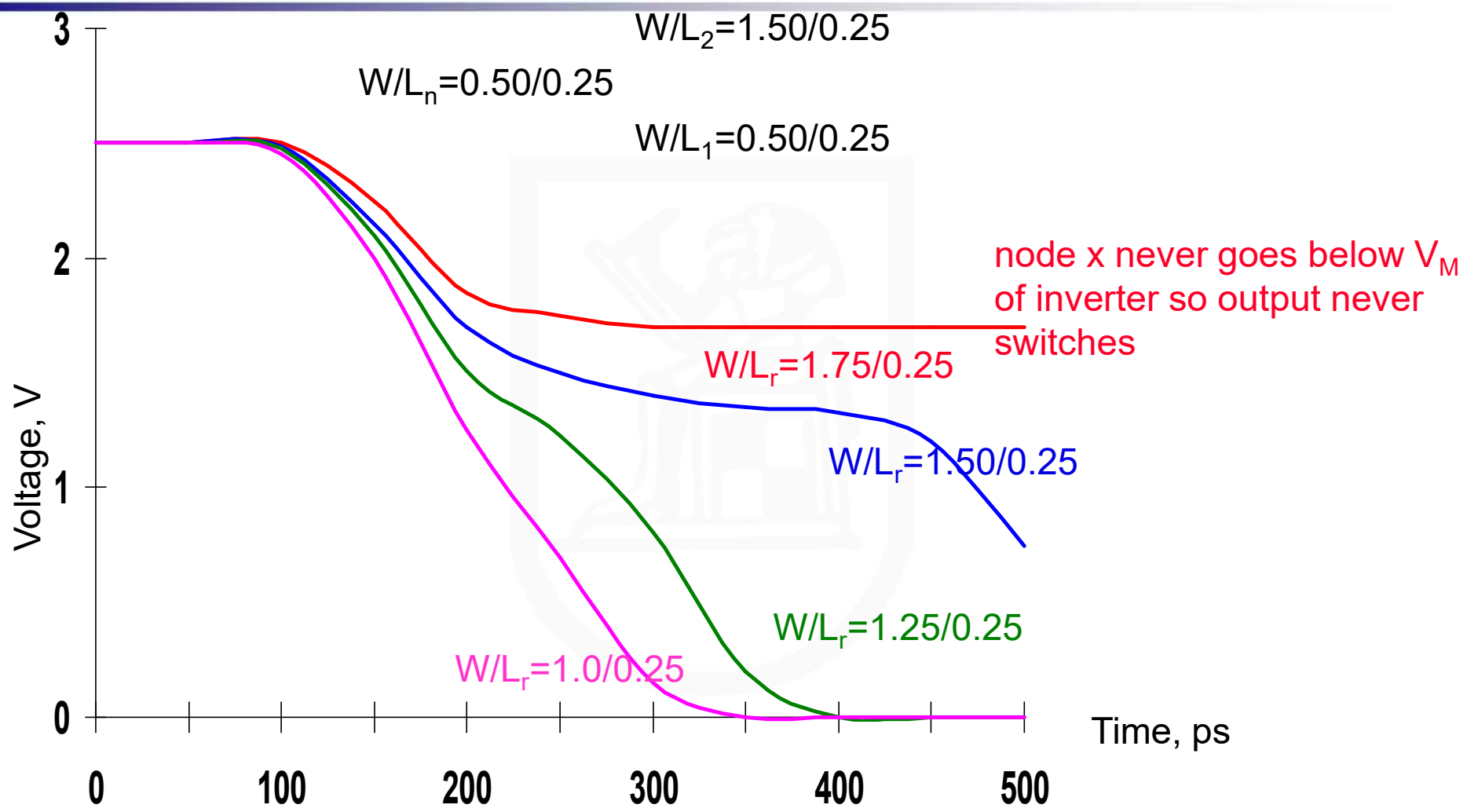
Solution 1: Level Restorer



- Full swing on x (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when A is high

- **For correct operation M_r must be sized correctly (ratioed)**

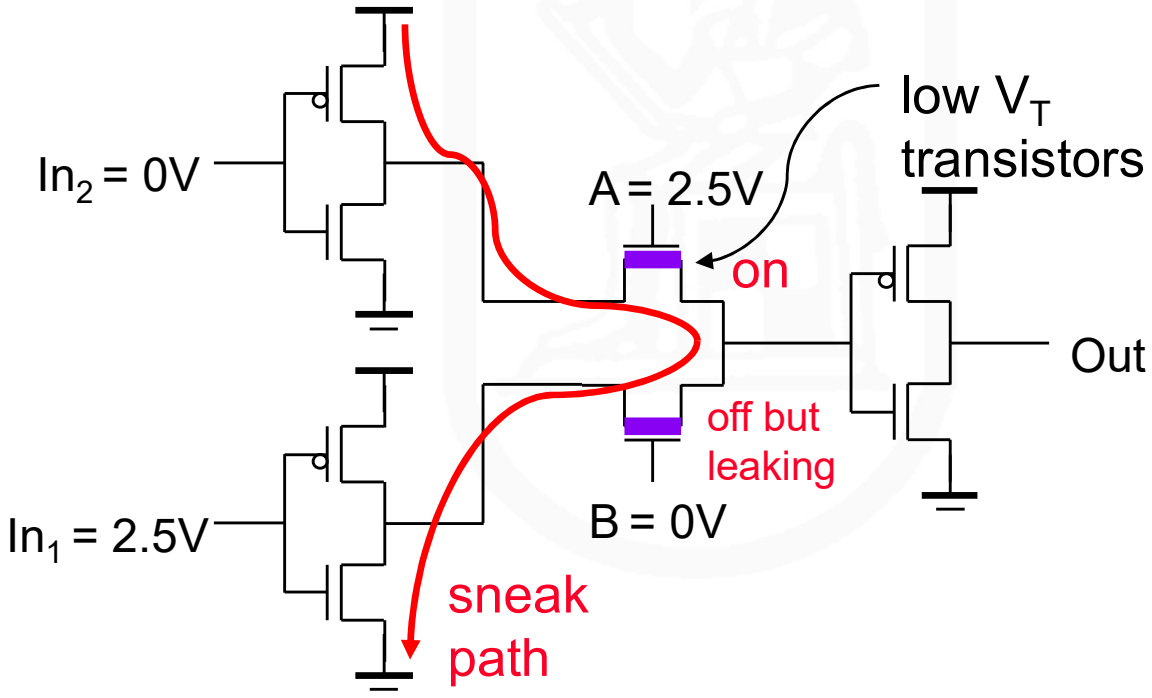
Transient Level Restorer Circuit Response



- Restorer has speed and power impacts: increases the cap at x, slowing down the gate; increases t_r (but decreases t_f)

Solution 2: Multiple V_T Transistors

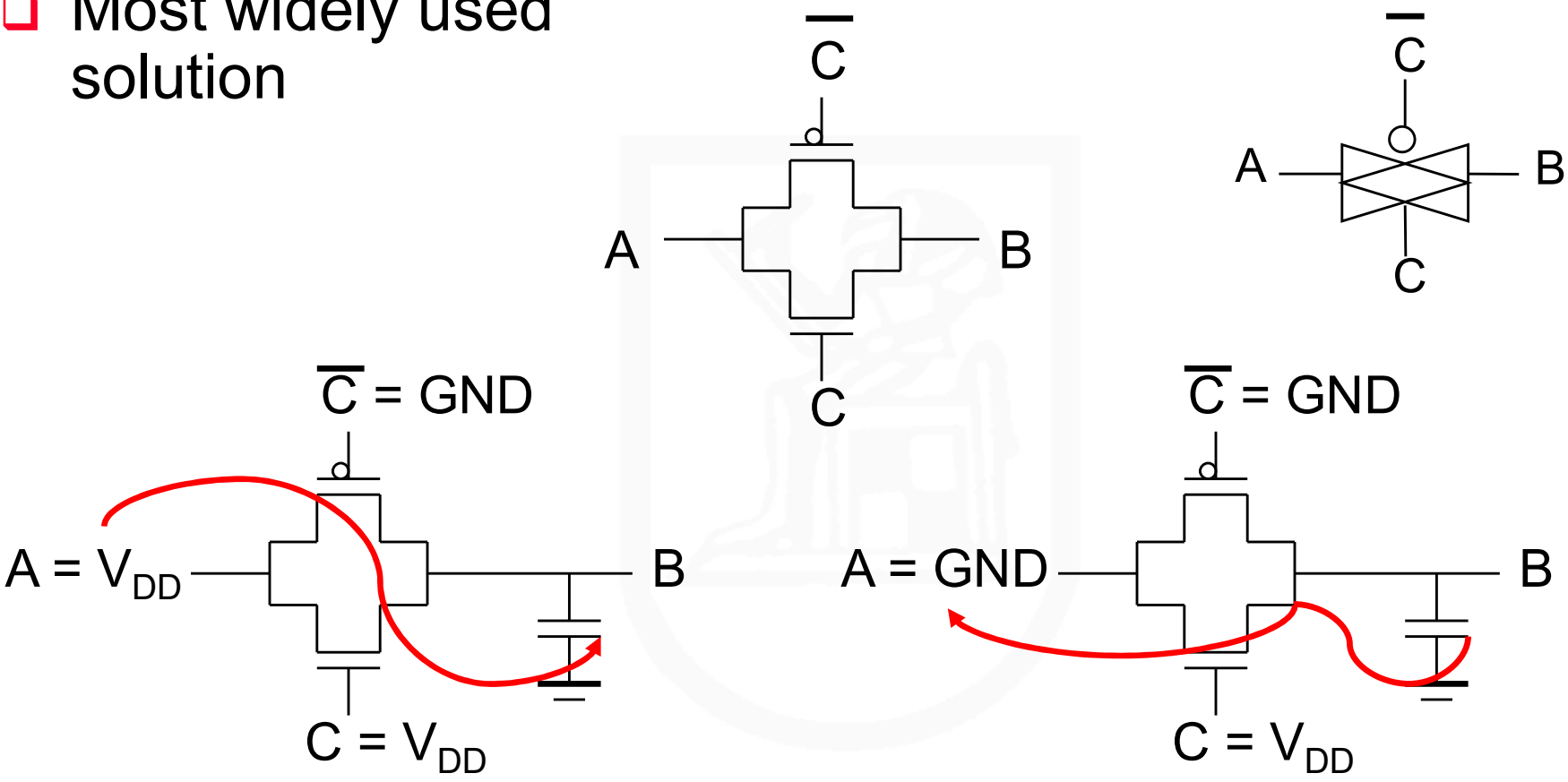
- Technology solution: Use (near) zero V_T devices for the NMOS PTs to eliminate *most* of the threshold drop (body effect still in force preventing full swing to V_{DD})



- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if V_{GS} is below V_T)

Solution 3: Transmission Gates (TGs)

- Most widely used solution



- **Full swing *bidirectional* switch controlled by the gate signal C, A = B if C = 1**