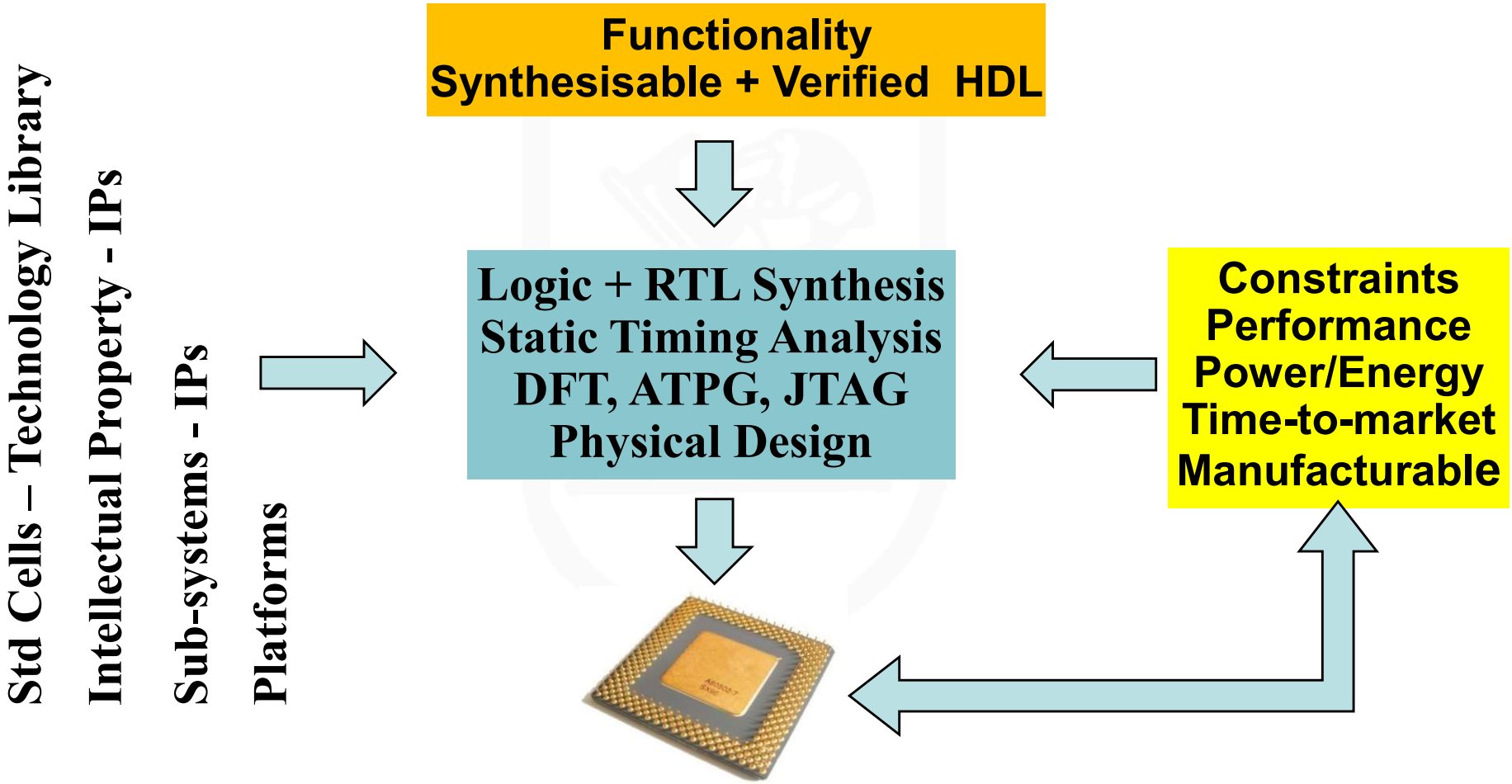
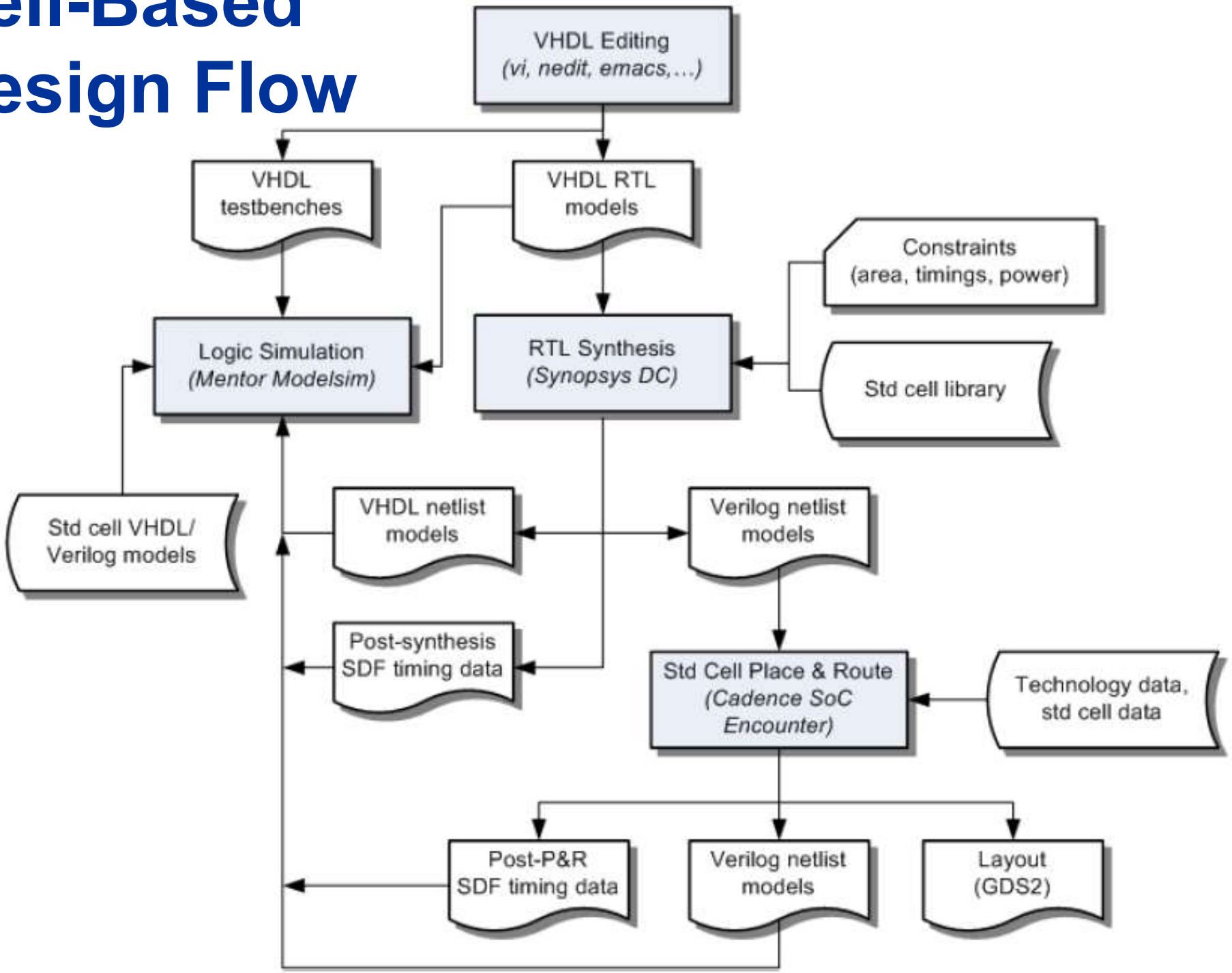
Course Outline

- Semiconductor Industry and Technology Overview
- IC Design Flows
- Timing in Digital Systems
- **Front-end Design Flow**
- Back-end Design Flow
- Interconnection and Signal Integrity
- Low-Power Design
- Design-for-Testability (DFT)

What the ASIC flow is about ?

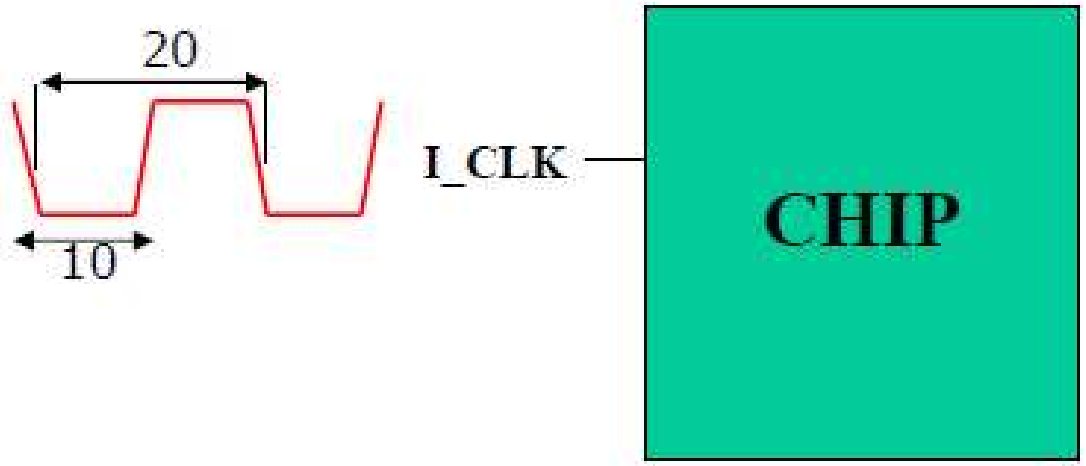


Cell-Based Design Flow



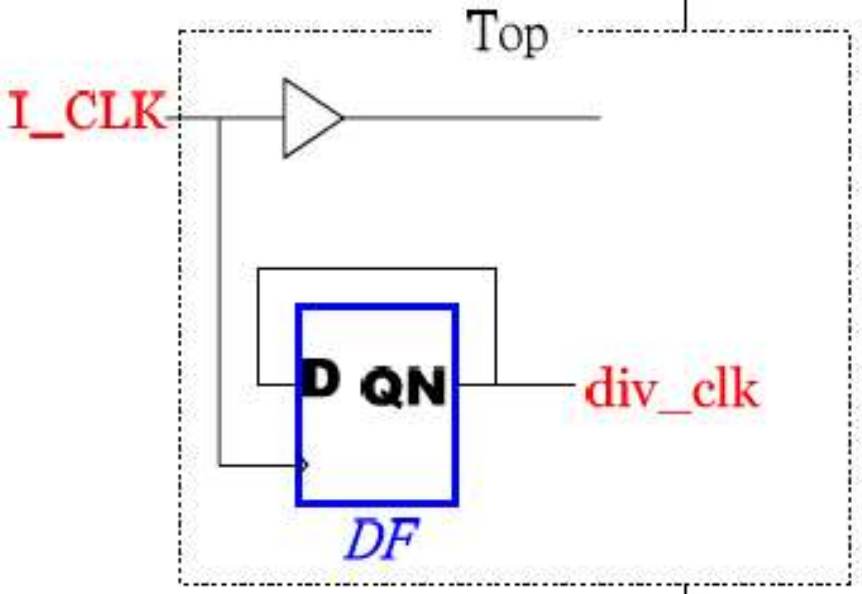
Timing Constraints: Create Clock

```
create_clock  [-name clock_name]
              -period period_value
              [-waveform edge_list]
              [clock_source_list]
```



create_clock –name CLK1 –period 20 –waveform {0 10} [get_ports I_CLK]

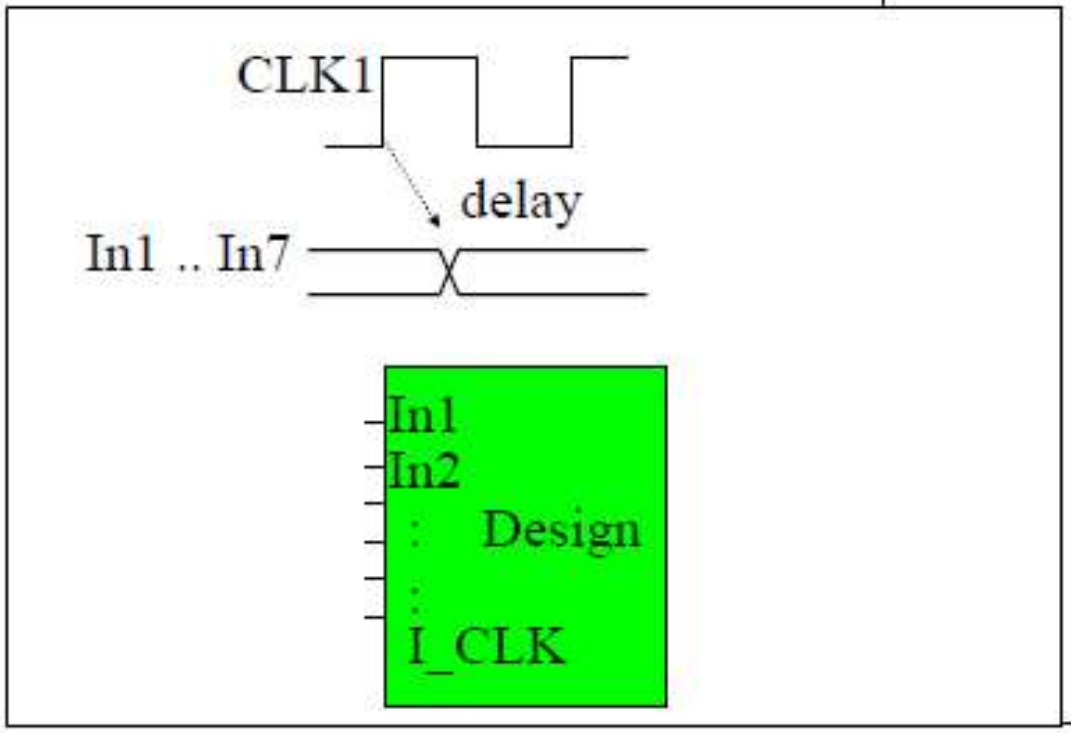
Timing Constraints: Create Generated Clock




```
create_generated_clock  -add  -master_clock
                        [-name clock_name]
                        -source master_clock_root
                        [-multiply_by mult]
                        [-divide_by div]
                        [-duty_cycle dc]
                        [-invert]
                        [-edges edge_list]
                        [-edge_shift edge_shift_list]
                        clock_root_list
```

create_generated_clock –name CLK2 –source [get_ports I_CLK] –divide_by 2 [get_pins DF/QN]

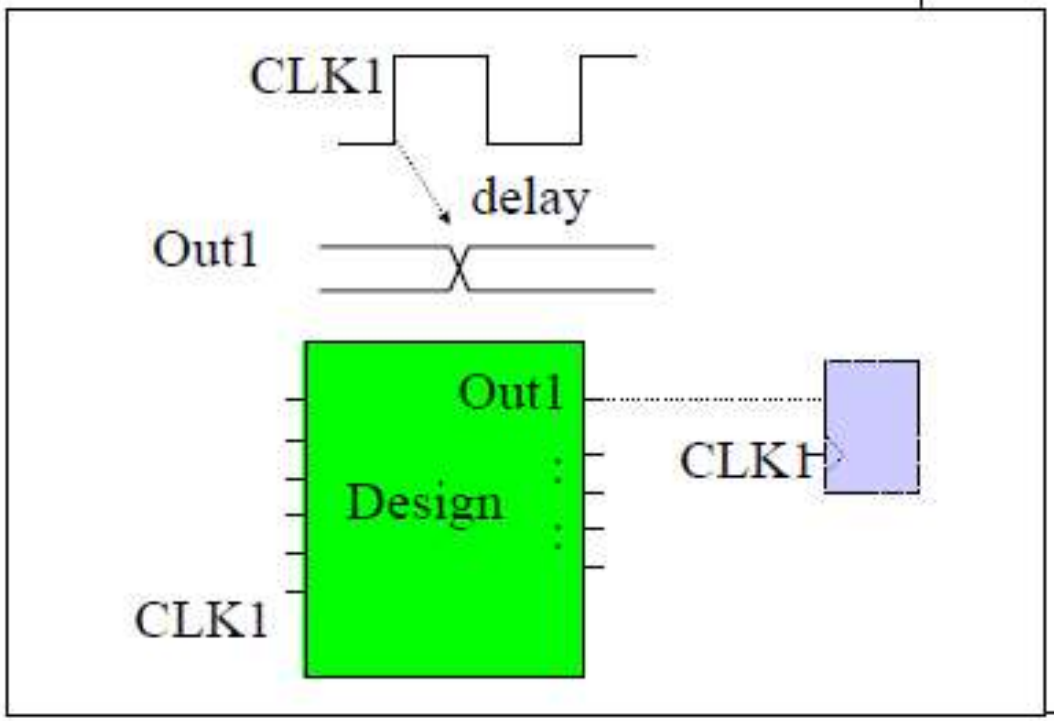
Timing Constraints: Set Input Delay




```
set_input_delay  delay_value
                 [-min]
                 [-max]
                 [-rise]
                 [-fall]
                 [-clock clock_name]
                 [-clock_fall]
                 [-add_delay]
                 [-network_latency_included]
                 [-source_latency_included]
                 port_pin_list
```

set_input_delay 1 –clock [get_clocks {CLK1}] [getports {In1}]

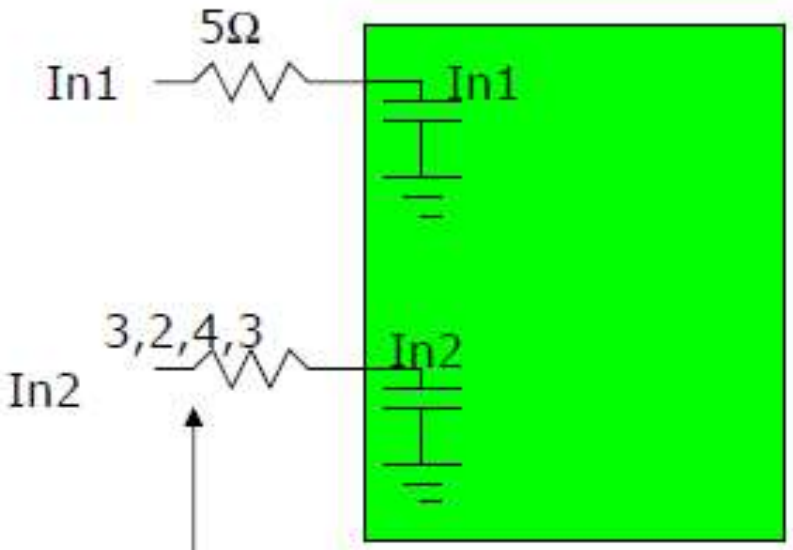
Timing Constraints: Set Output Delay




```
set_output_delay  delay_value
                  [-min]
                  [-max]
                  [-rise]
                  [-fall]
                  [-clock clock_name]
                  [-add_delay]
                  [-network_latency_included]
                  [-source_latency_included]
                  port_pin_list
```

```
set_output_delay 1 -clock [get_clocks {CLK1}] [getports {Out1}]
```

Timing Constraints: Set Drive

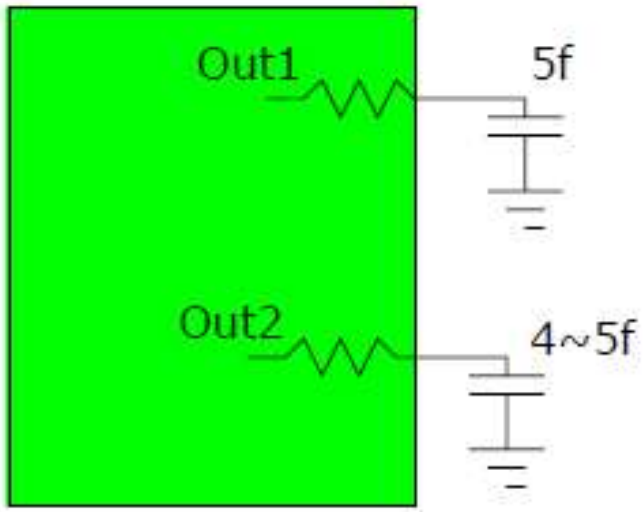


rise_min, rise_max, fall_min, fall_max

```
set_drive  [-min]
           [-max]
           [-rise]
           [-fall]
           drive_strength
           port_list
```

set_drive 1 [get_ports {In1}]

Timing Constraints: Set Load




```
set_load  [-min]
          [-max]
          [-pin_load]
          [-wire_load]
          load_value
          port_list
```

set_load 1 [get_ports {Out1}]

```
#-----------------------------------------------------------------------
#    Define constraints
#-----------------------------------------------------------------------
create_clock -name $CLK_NAME -period $CLK_PERIOD [get_ports $CLK_NAME]

set_input_delay $INPUT_DELAY -clock $CLK_NAME [list [all_inputs]]
set_output_delay $OUTPUT_DELAY -clock $CLK_NAME [list [all_outputs]]

set_max_area 0

# Use only plain DFF cells
set_dont_use [list c35_CORELIB.db:c35_CORELIB/DFE* \
                   c35_CORELIB.db:c35_CORELIB/DFS* \
                   c35_CORELIB.db:c35_CORELIB/TF* \
                   c35_CORELIB.db:c35_CORELIB/JK*]

set_fix_multiple_port_nets -all

#-----------------------------------------------------------------------
#    Set resource allocation and implementation
#-----------------------------------------------------------------------
set_resource_implementation use_fastest
if { $SHARE_RESOURCES } {
   set_resource_allocation area_only
} else {
   set_resource_allocation none
}

#-----------------------------------------------------------------------
#    Save elaborated design and constraints
#-----------------------------------------------------------------------
write -hierarchy -format $DB_MODE -output $DB_ELAB_FILE
```

```
#====================================================================
#    Map design to gates
#====================================================================
if { $COMPILE_SIMPLE } {
   compile
} else {
   compile -map_effort medium -area_effort medium
   ungroup -all -flatten
   compile -incremental -map_effort high
}

#====================================================================
#    Save mapped design
#====================================================================
write -hierarchy -format $DB_MODE -output $DB_MAPPED_FILE

#====================================================================
#    Generate reports
#====================================================================
report_area -nosplit > $RPT_AREA_FILE
report_timing -path full \
              -delay max \
              -nworst 1 \
              -max_paths 1 \
              -significant_digits 2 \
              -nosplit \
              -sort_by group \
              > $RPT_TIMING_FILE
report_resources -nosplit -hierarchy > $RPT_RESOURCES_FILE
report_reference -nosplit > $RPT_REFERENCES_FILE
report_cell -nosplit > $RPT_CELLS_FILE

#====================================================================
#    Generate VHDL netlist
```

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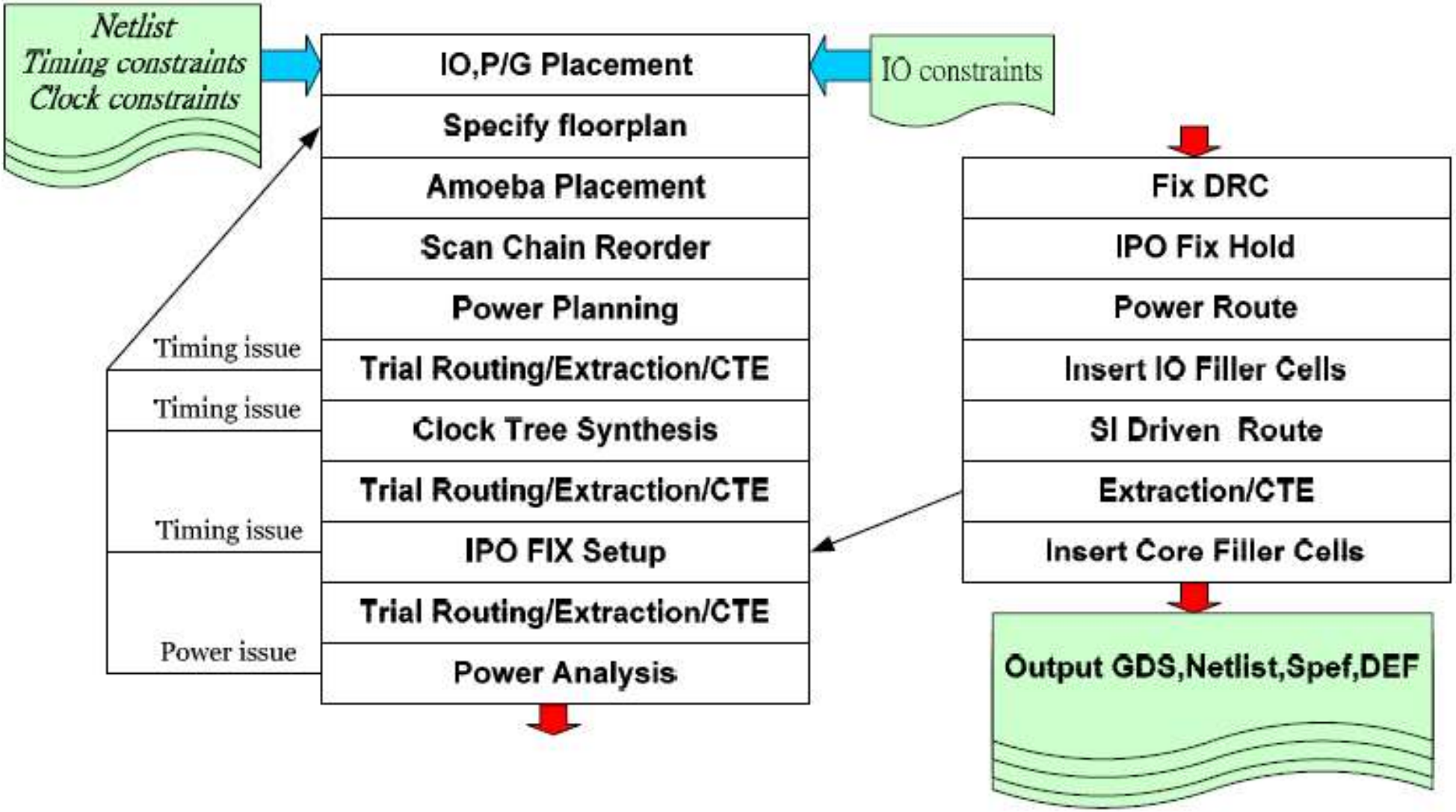
Traditional APR Flow

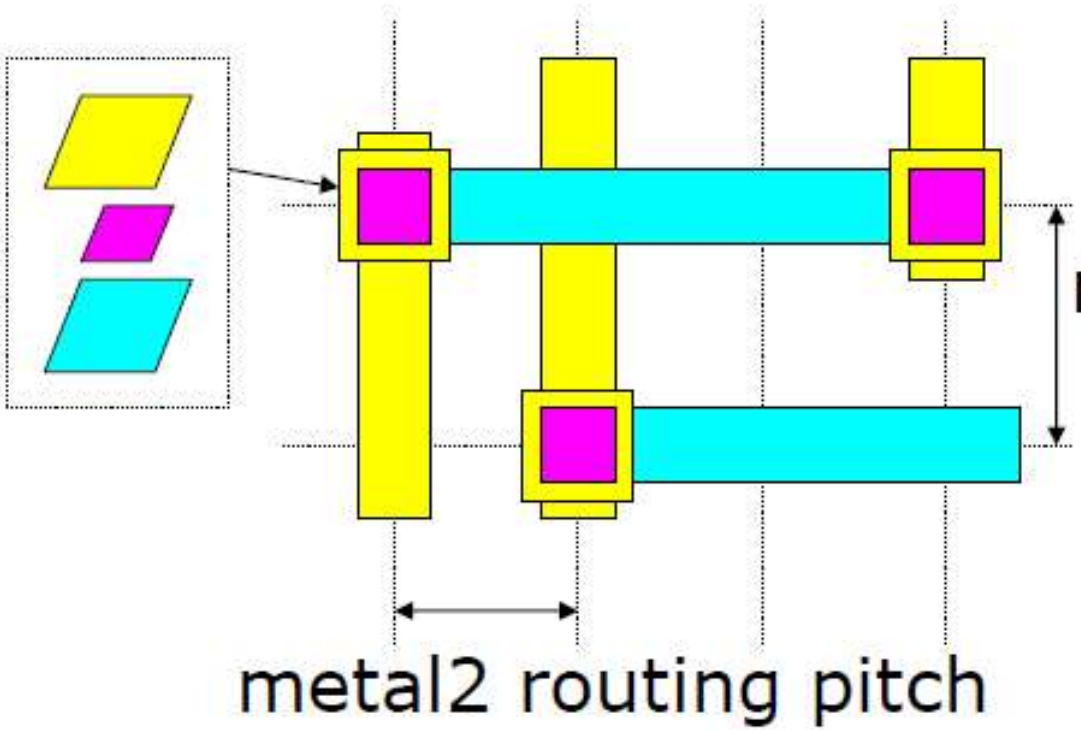
Gate-Level netlist (verilog)
Physical Library (LEF)
Timing Library (LIB)
Timing constraints (sdc)
IO constraint



LEF Data

- **Process technology**
  - Define layers: poly, contact, metal1, via1, metal2, …
  - Design Rules: net width, net spacing, antenna, current density, …
  - Parasitics
- **APR**
  - Unit, site, routing pitch, default direction, via generation, via stacking, …

Routing Pitch

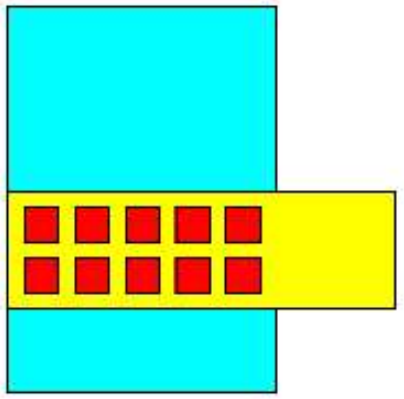


Horizontal routing	Vertical routing
Metal1 Metal3 Metal5	Metal2 Metal4 Metal6

Via Generation

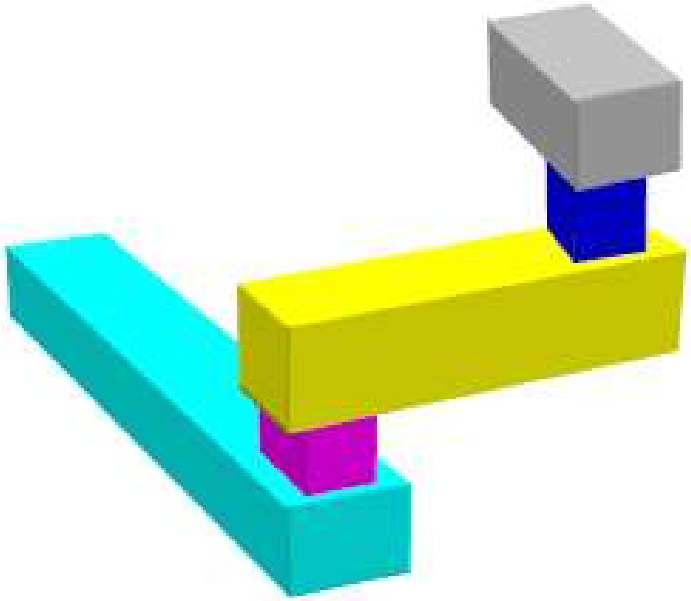
- **To connect wide metal, create a via array to reduce the overall via resistance.**
- **APR LEF data defines formulas for via generation.**

```
Layer Metal1
   Direction HORIZONTAL
   OVERHANG 0.2
Layer Metal2
   Direction VERTICAL
   OVERHANG 0.2
Layer Via1
   RECT –0.14 –0.14 0.14 0.14
   SPACING 0.56 BY 0.56
```

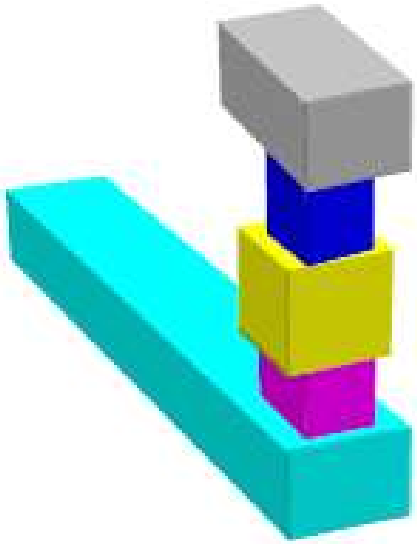


Via Stacking

- **Higher density routing.**
- **Easier access to upper metal.**
- **Must use minimum area rules.**



Without via stack



With via stack

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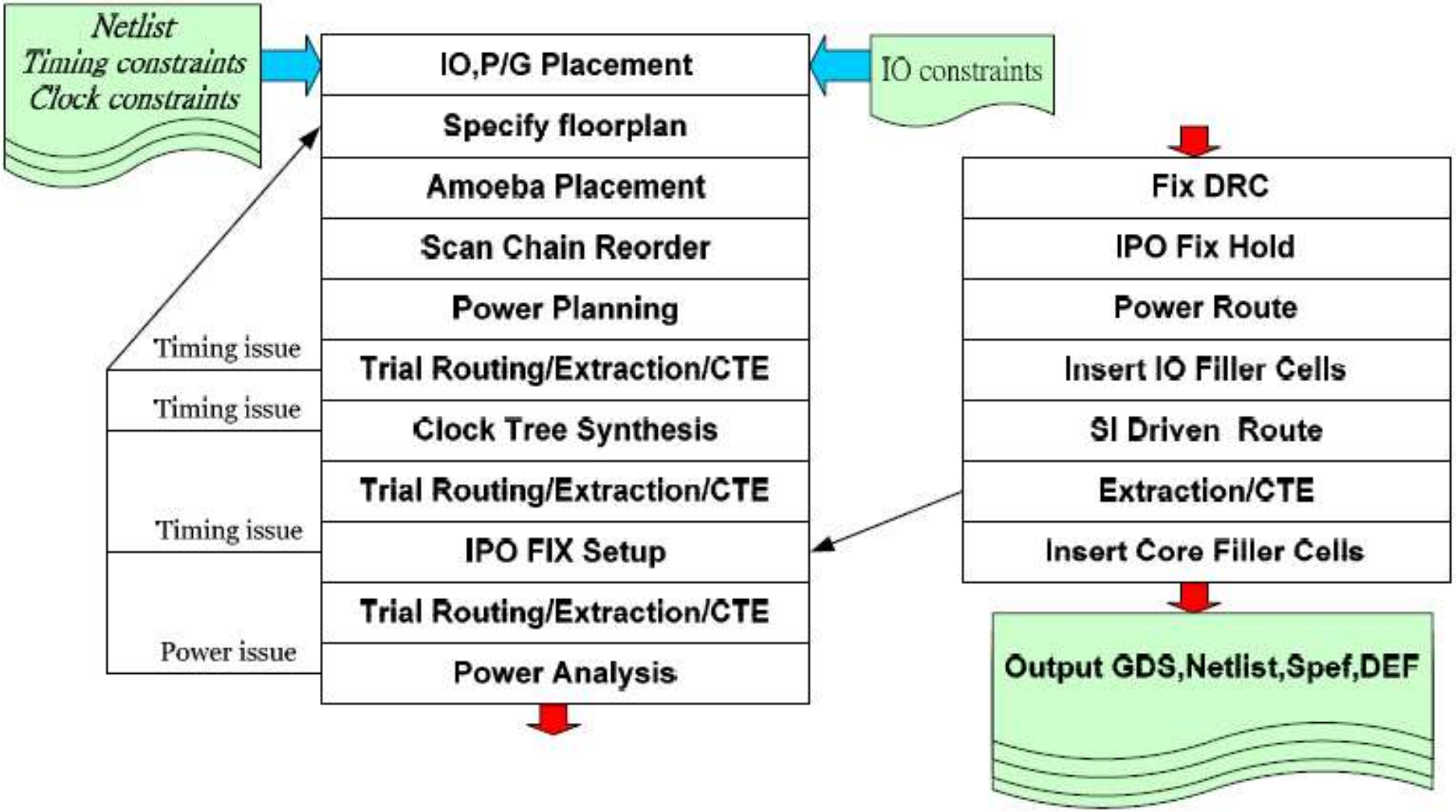
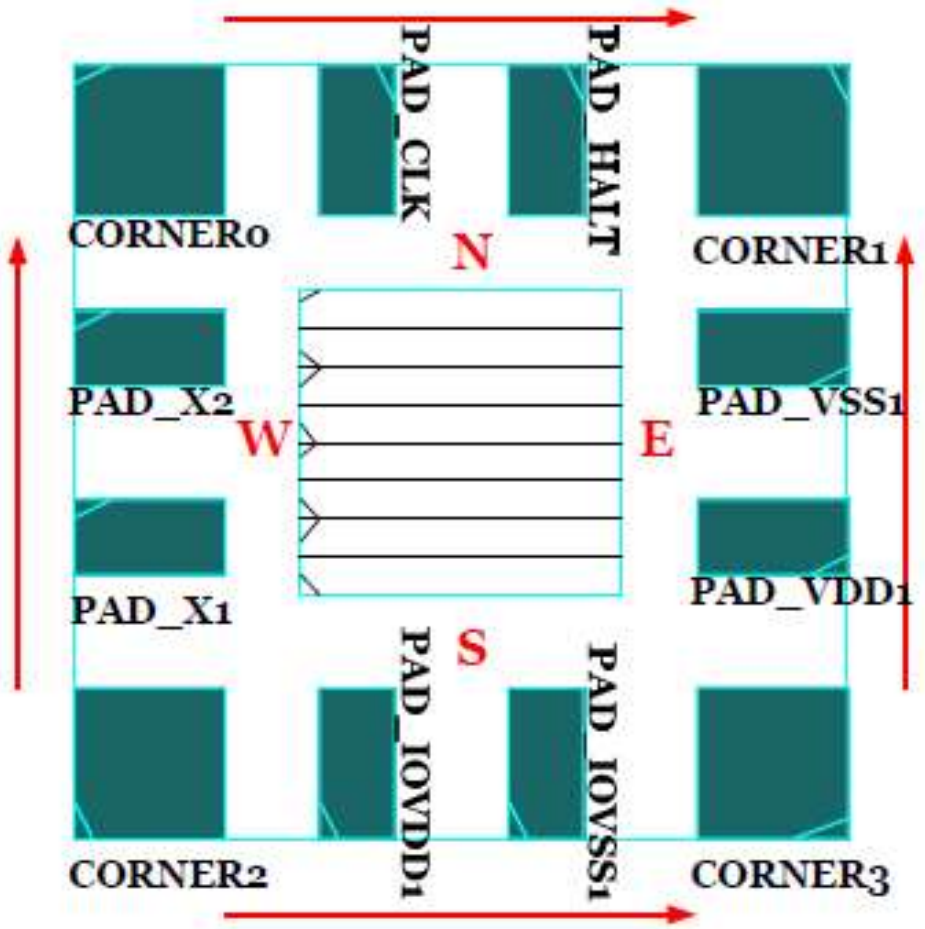
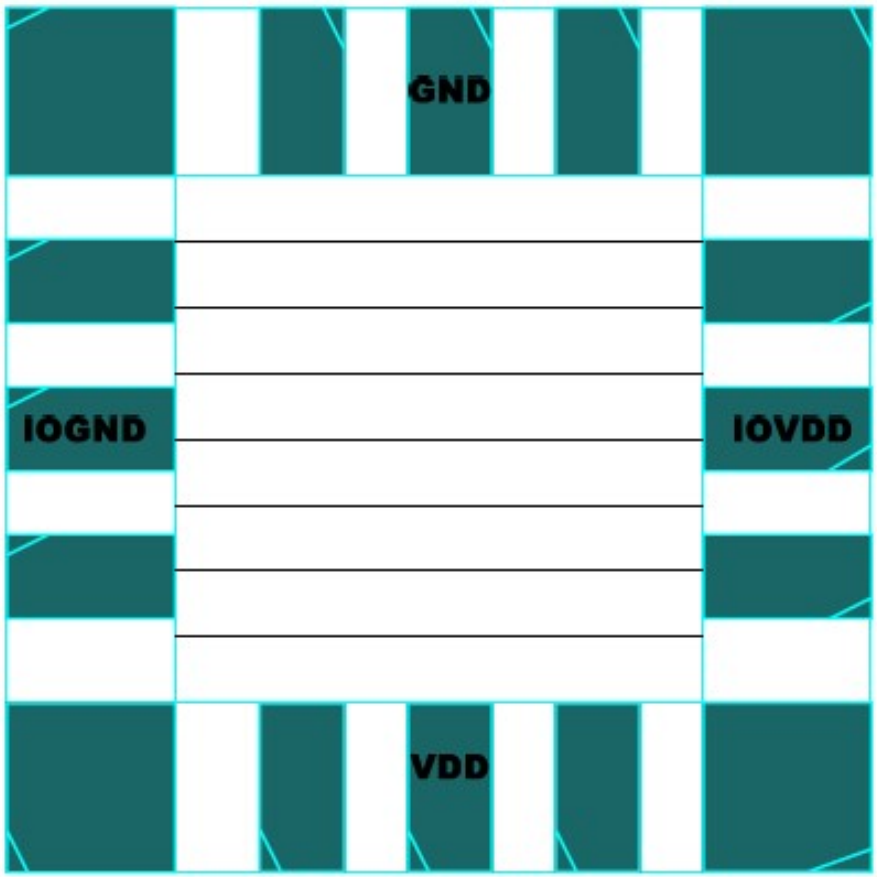


IO Assignment

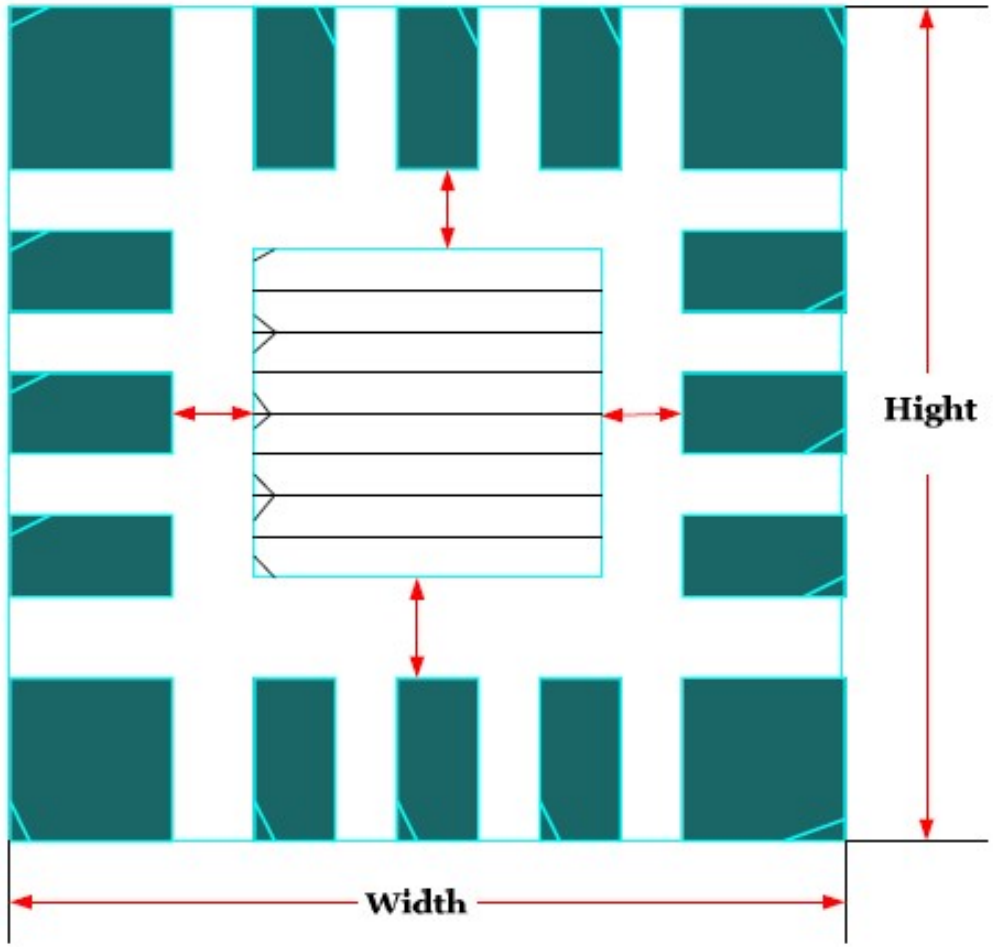
```
Version: 1
Pad: CORNER0 NW
Pad: PAD_CLK      N
Pad: PAD_HALT     N

Pad: CORNER1      NE
Pad: PAD_X1       W
Pad: PAD_X2       W

Pad: CORNER2      SW
Pad: PAD_IOVDD1   S
Pad: PAD_IOVSS1   S

Pad: CORNER3      SE
Pad: PAD_VDD1     E
Pad: PAD_VSS1     E
```



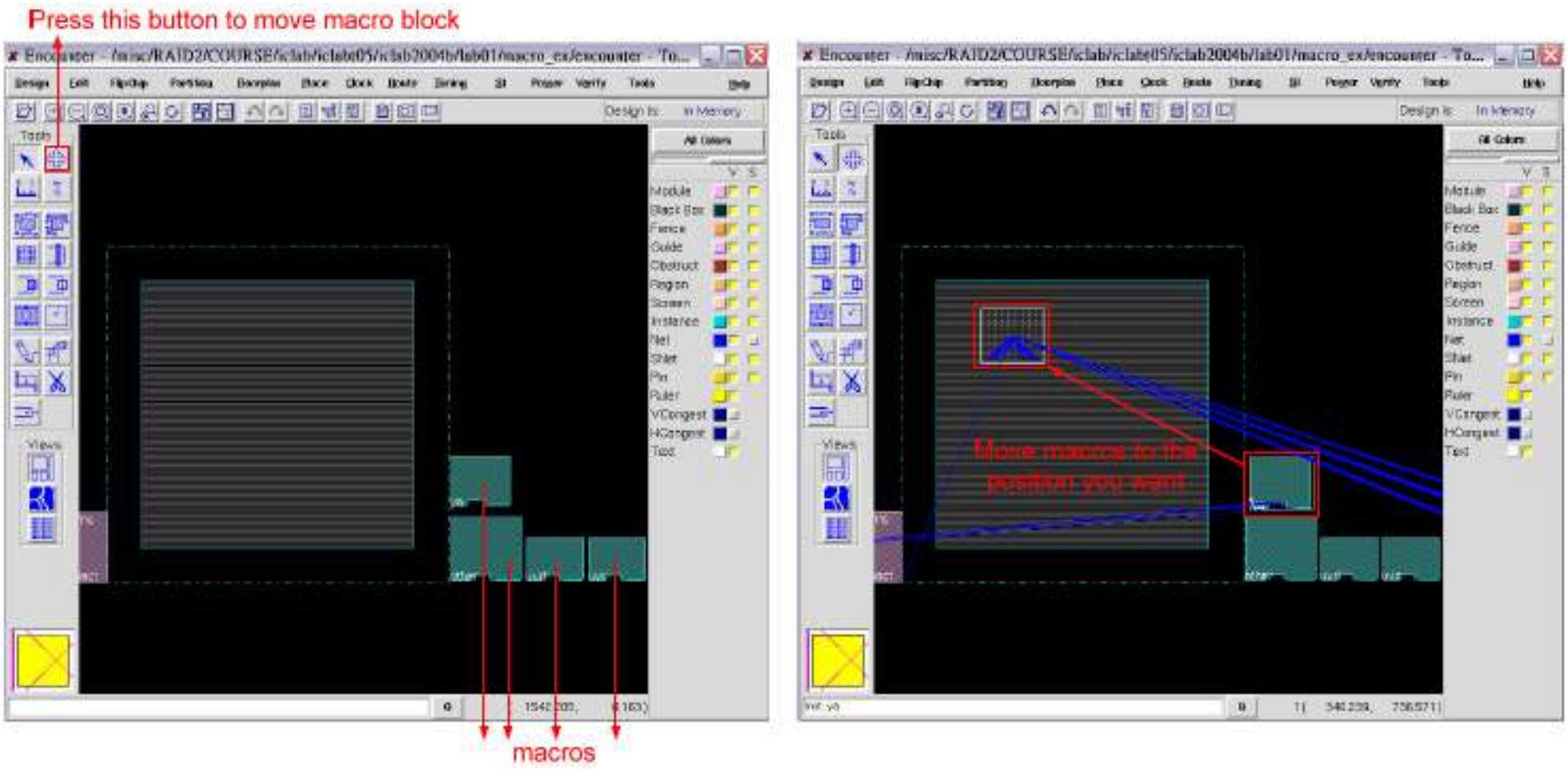
PG Assignment



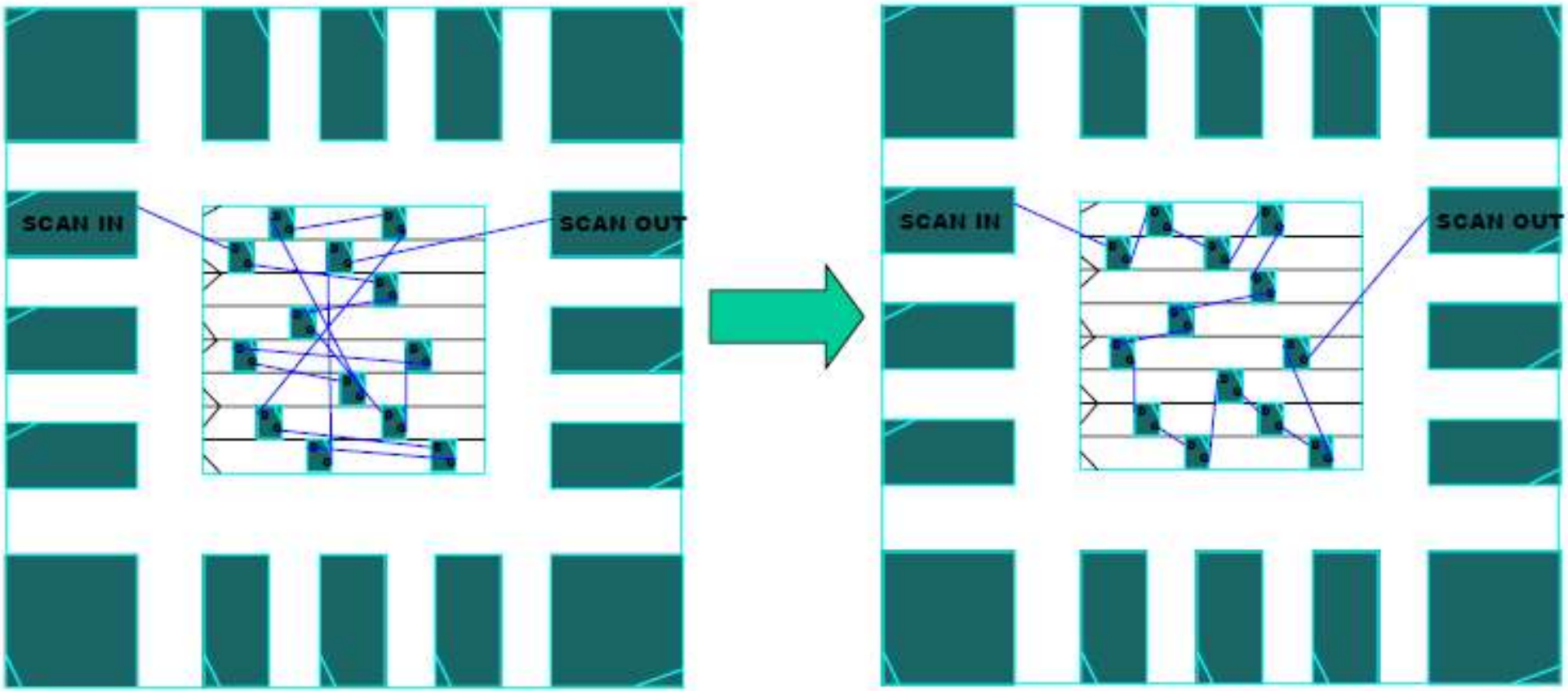
Specify Floorplan



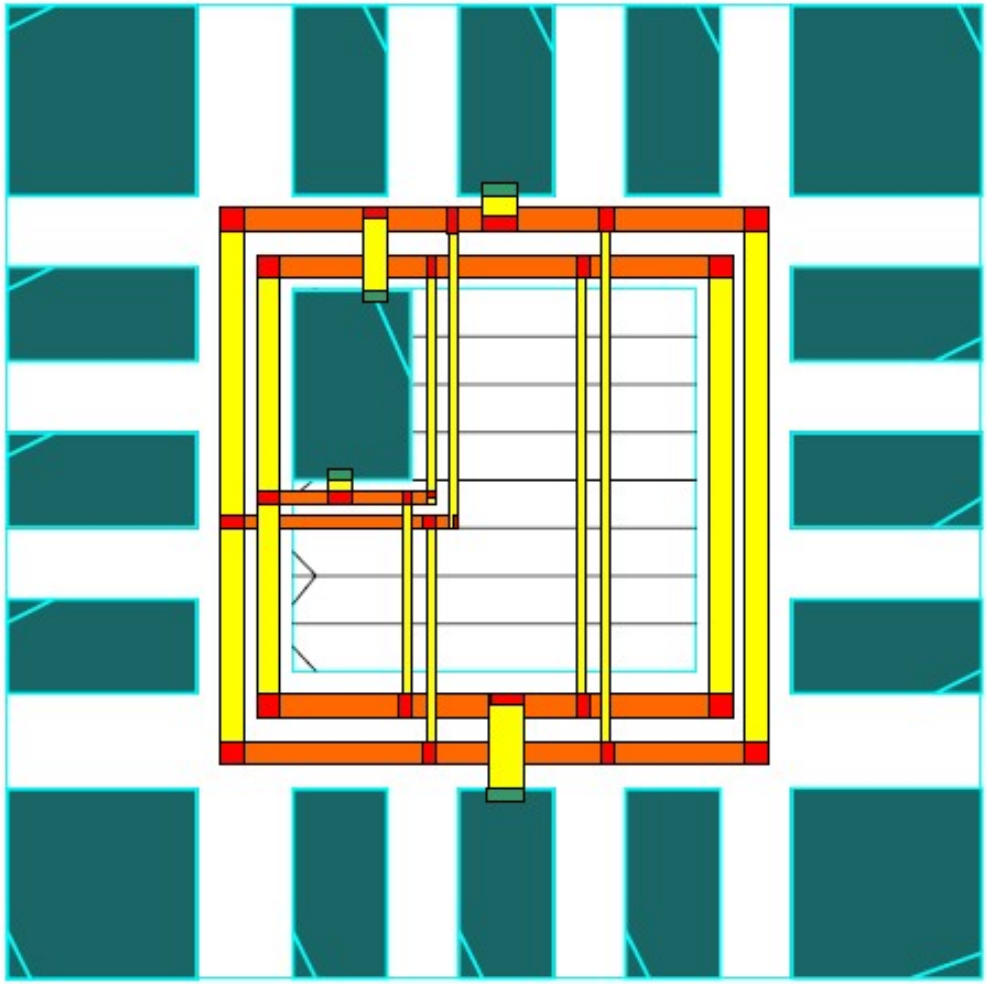
Placement



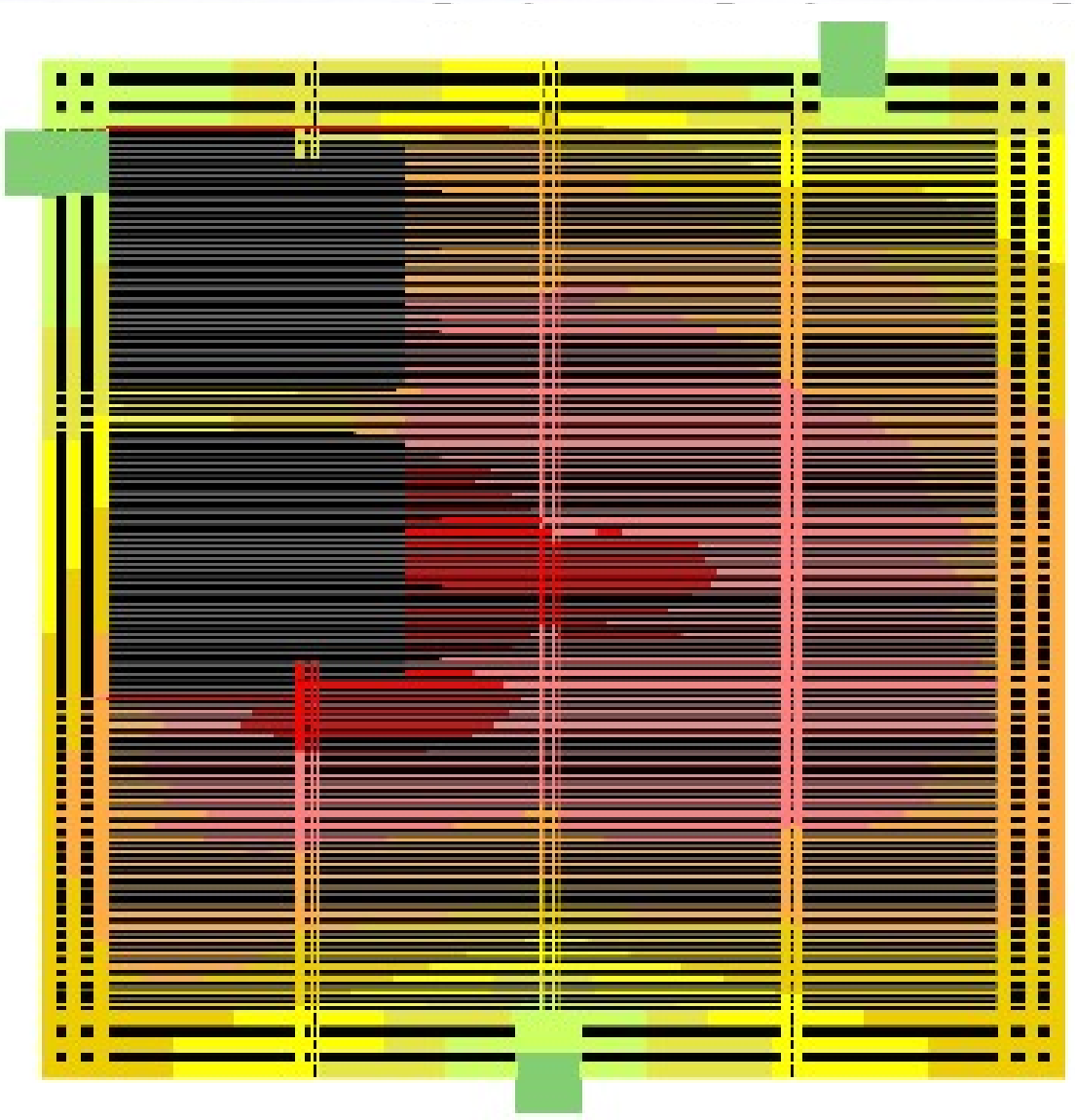
Scan Chain Reordering



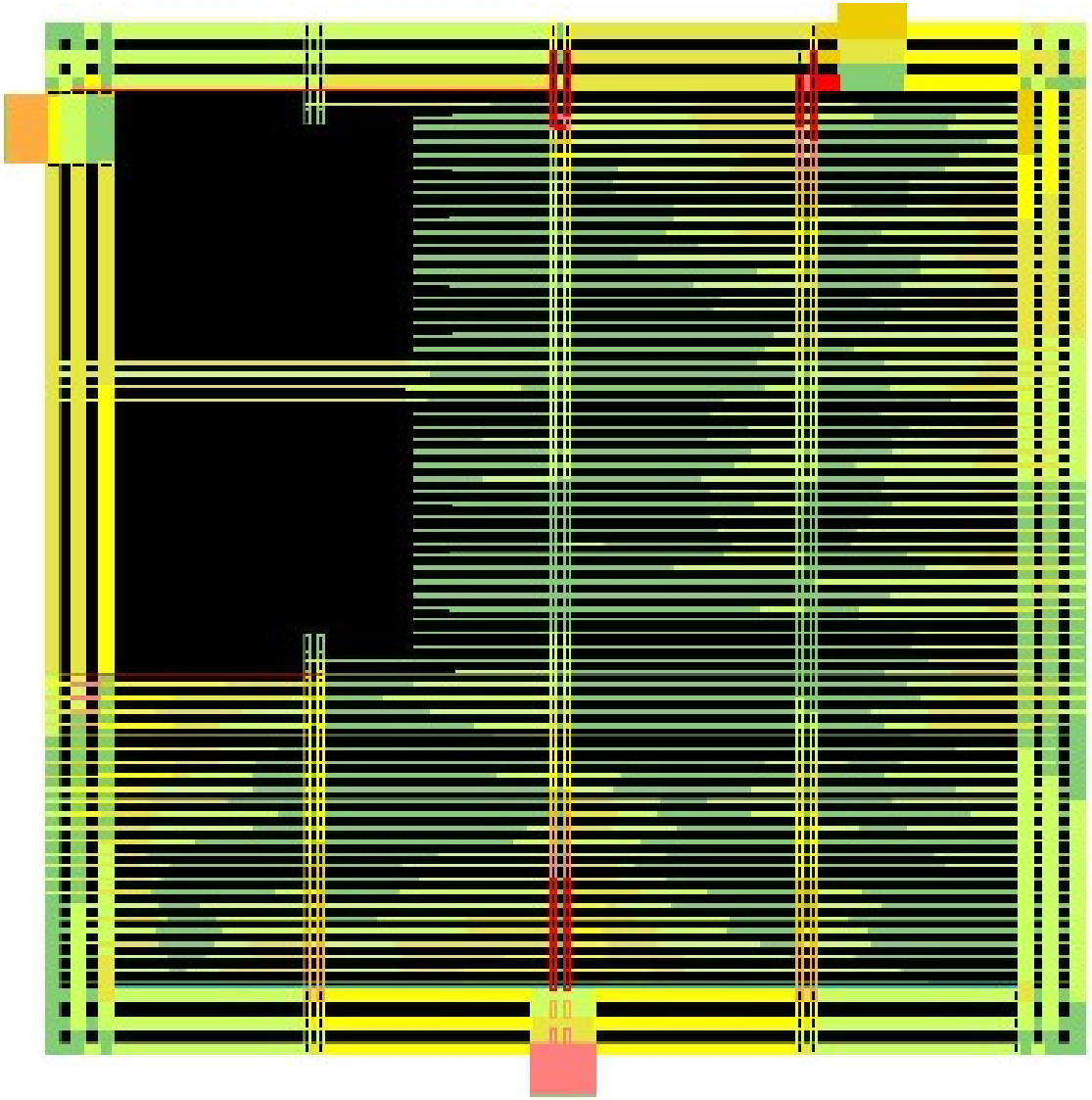
Power Planning



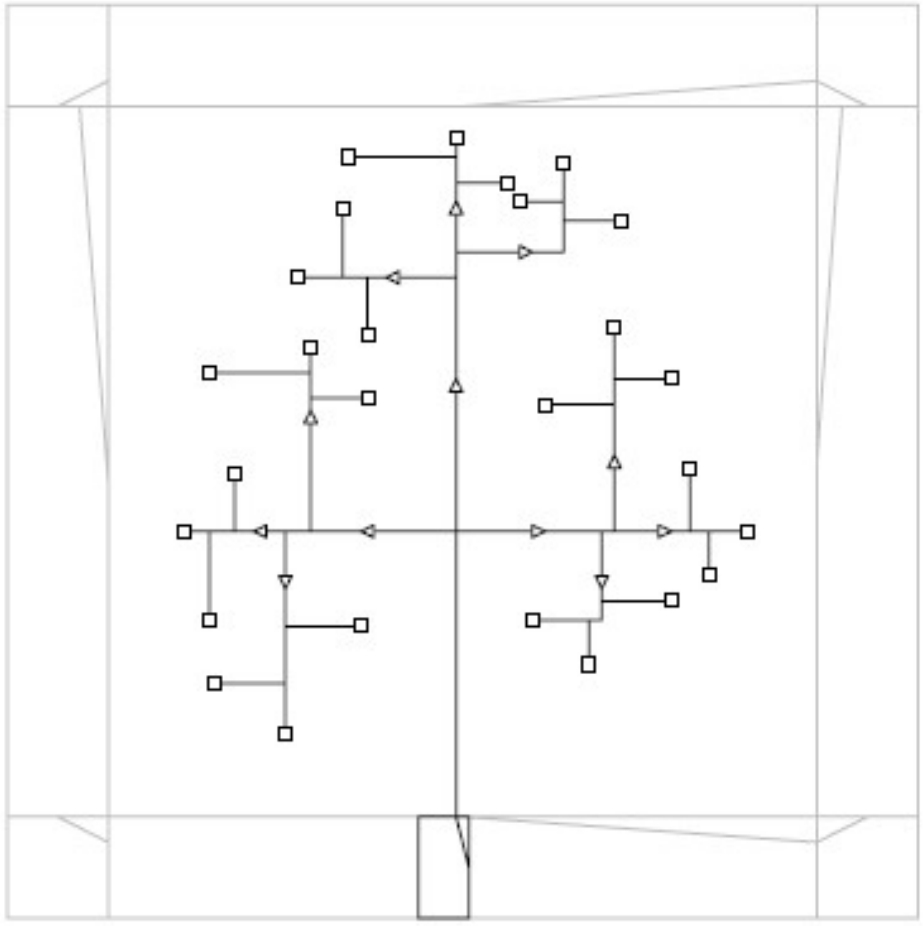
IR Drop – Power Analysis



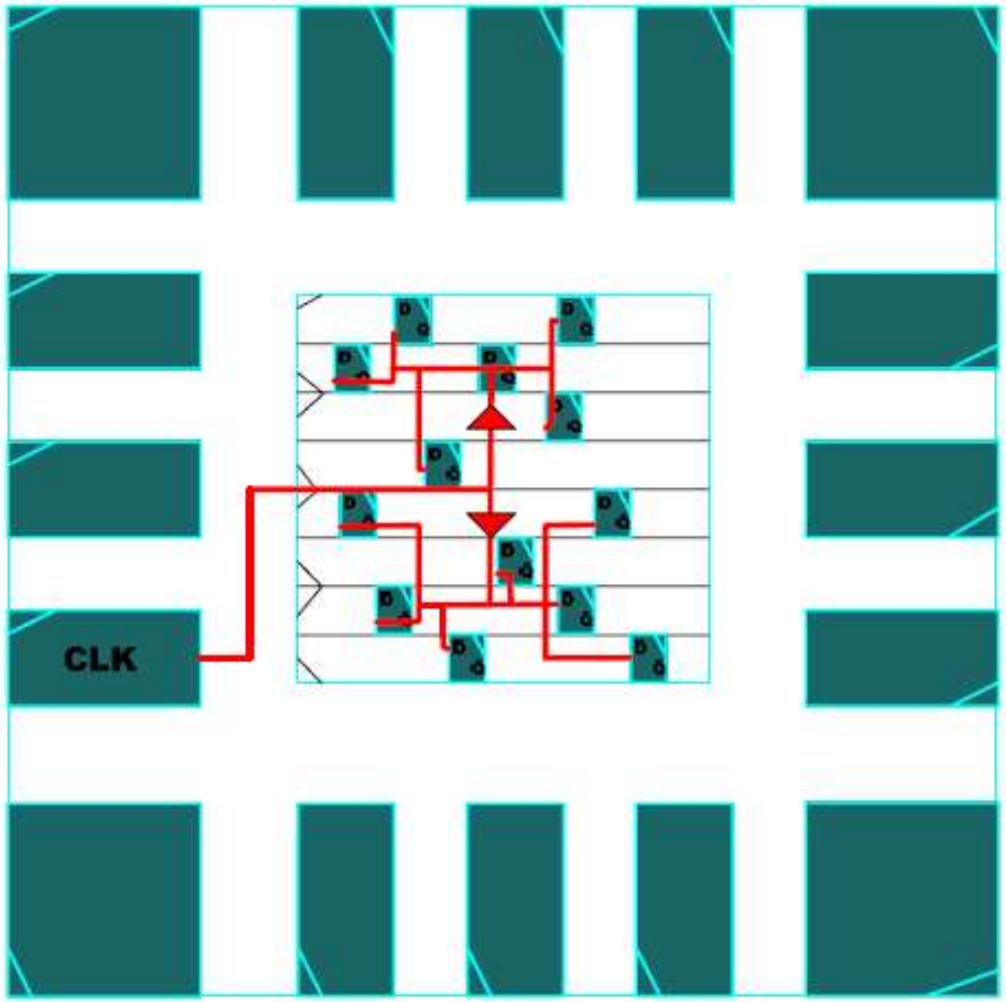
Electron Migration – Power Analysis



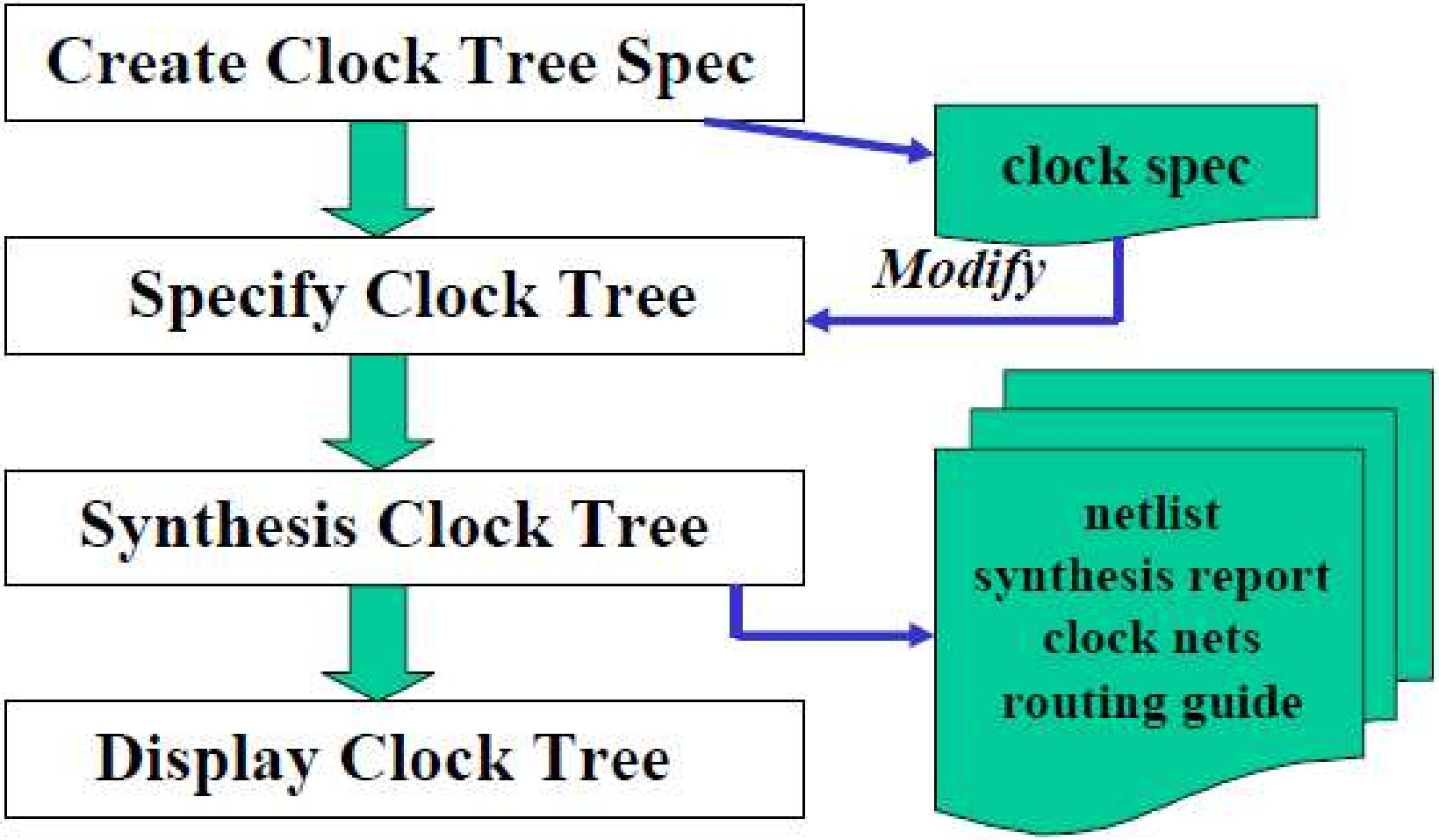
Clock Tree Topology



Clock Tree Synthesis



Clock Tree Synthesis



Clock Tree Synthesis Constraints

AutoCTSRootPin *clockRootPinName*

MaxDelay *number{ns|ps}*

MinDelay *number{ns|ps}*

SinkMaxTran *number{ns|ps}*

- maximum input transition time for sinks(clock pins)

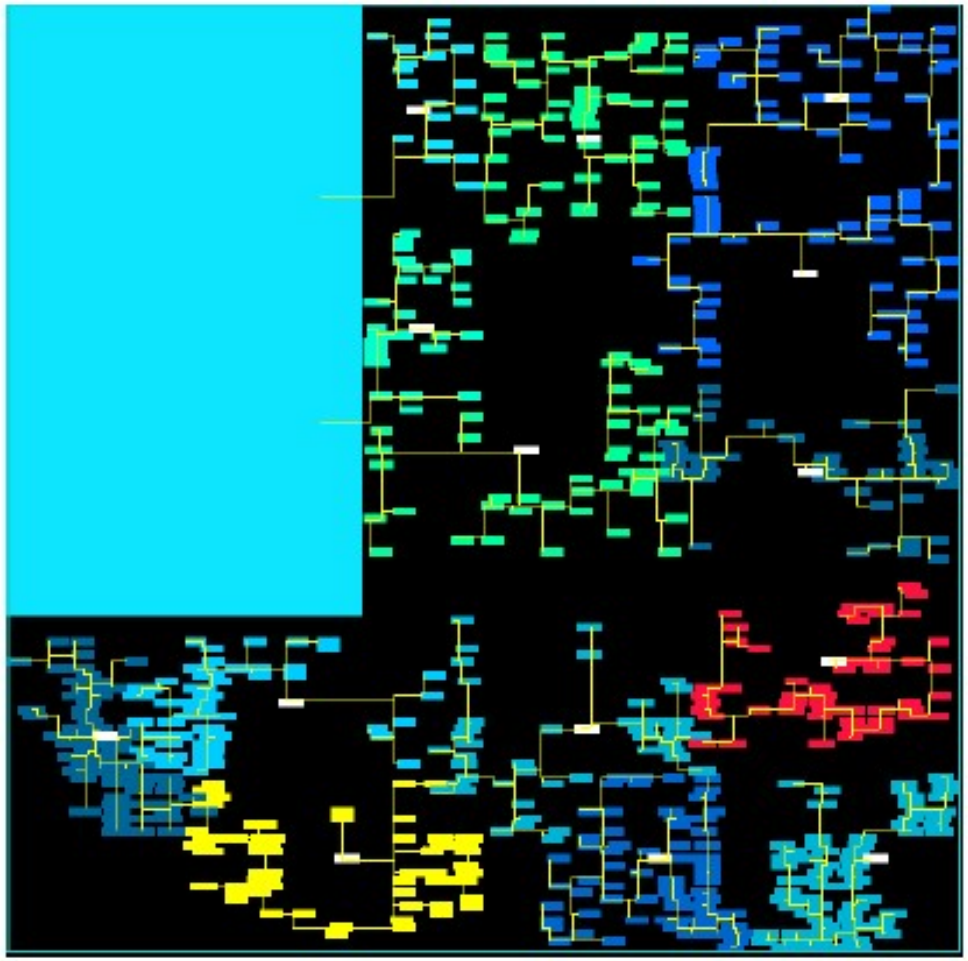
BufMaxTran *number{ns|ps}*

- maximum input transition time for buffers

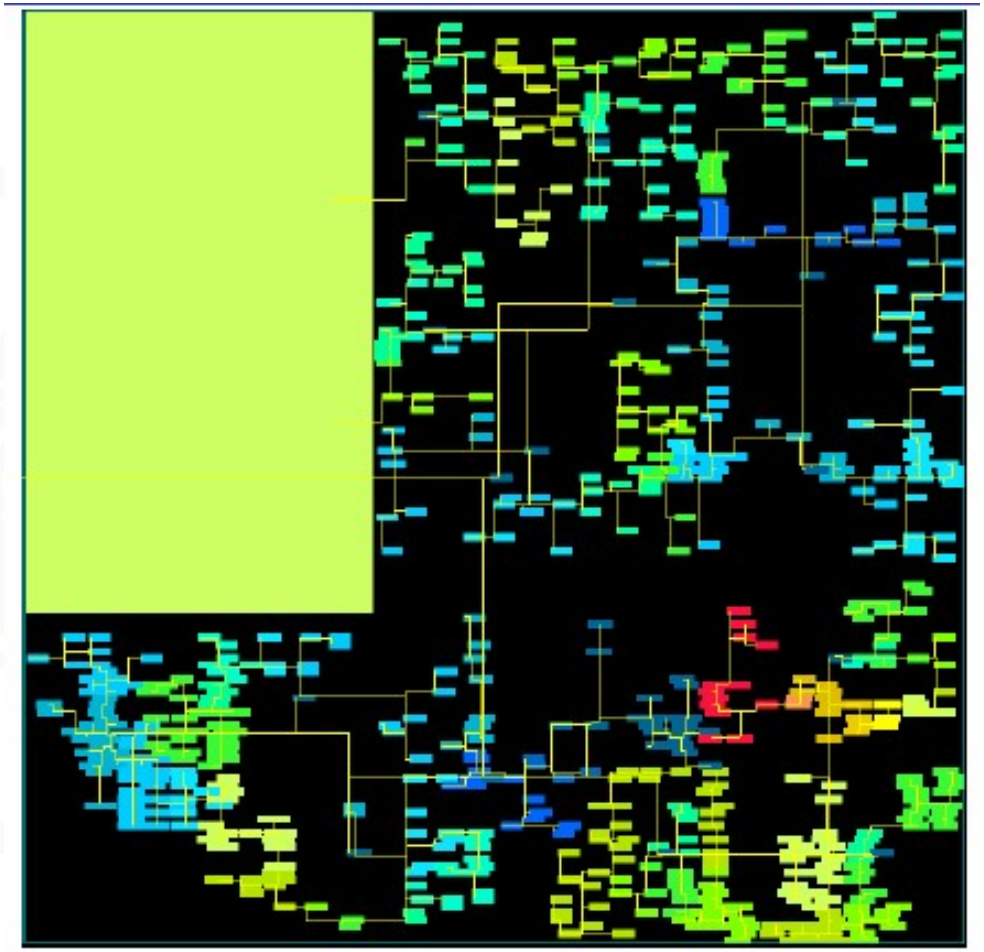
MaxSkew *number{ns|ps}*

- **There are a lot more details to it…**

Display Clock Tree

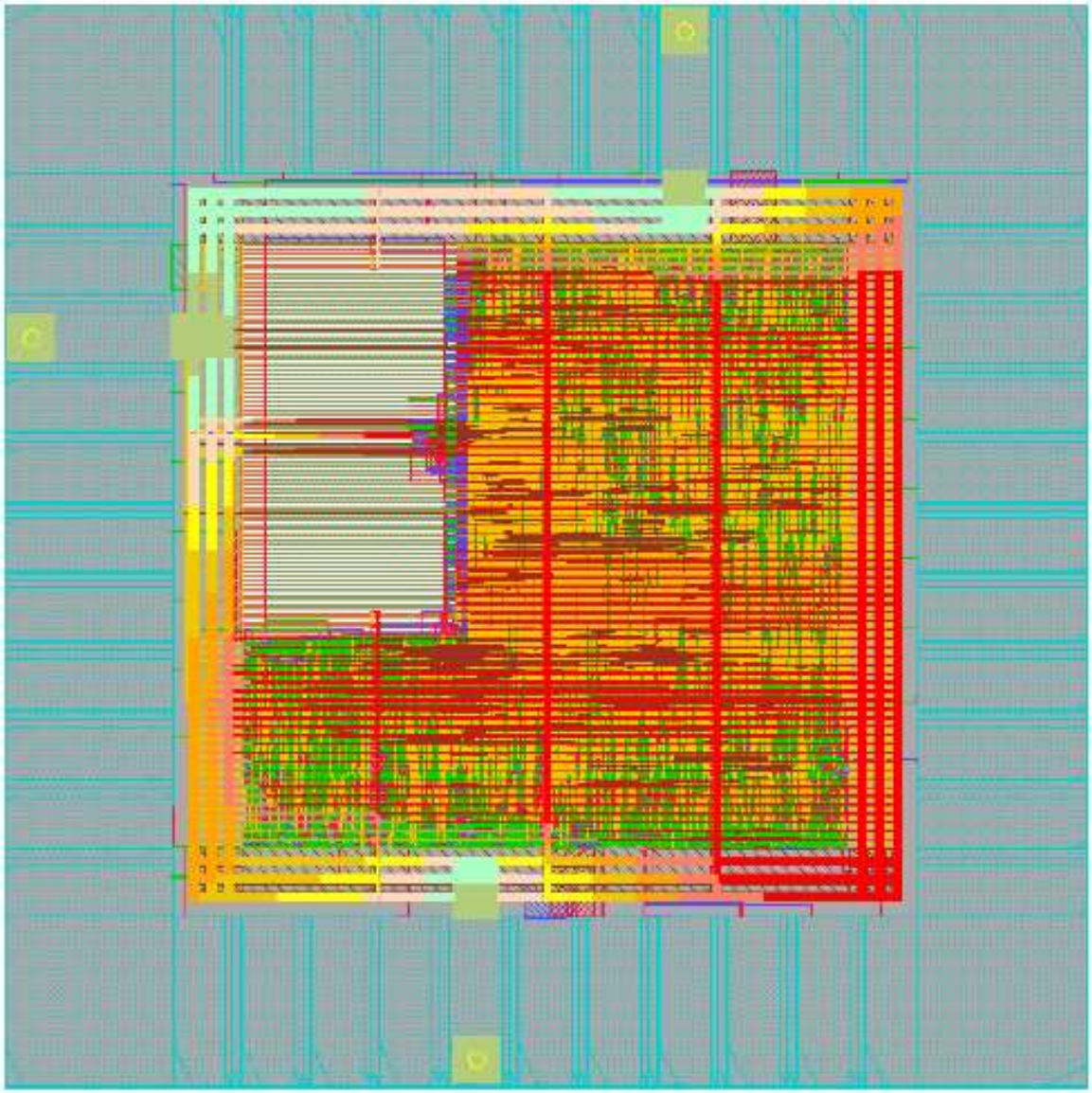


By Level

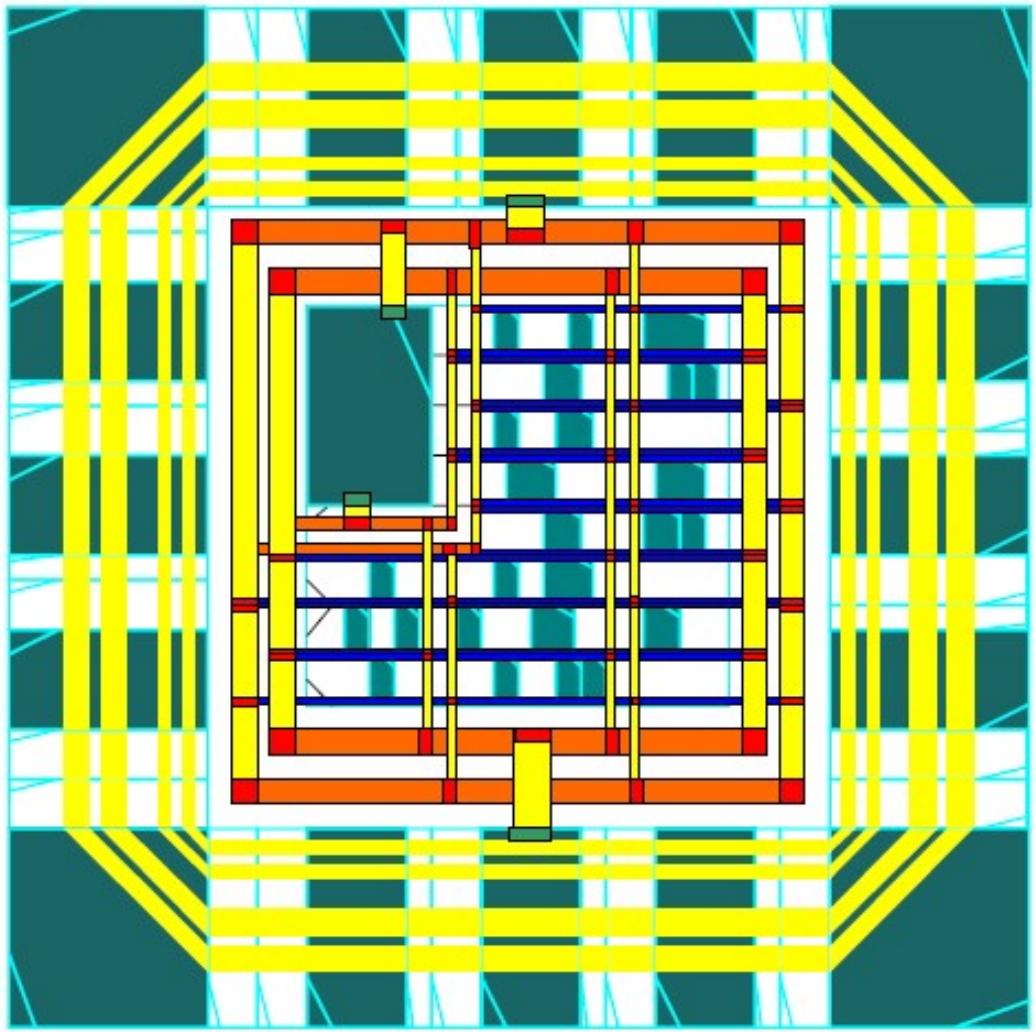


By Phase

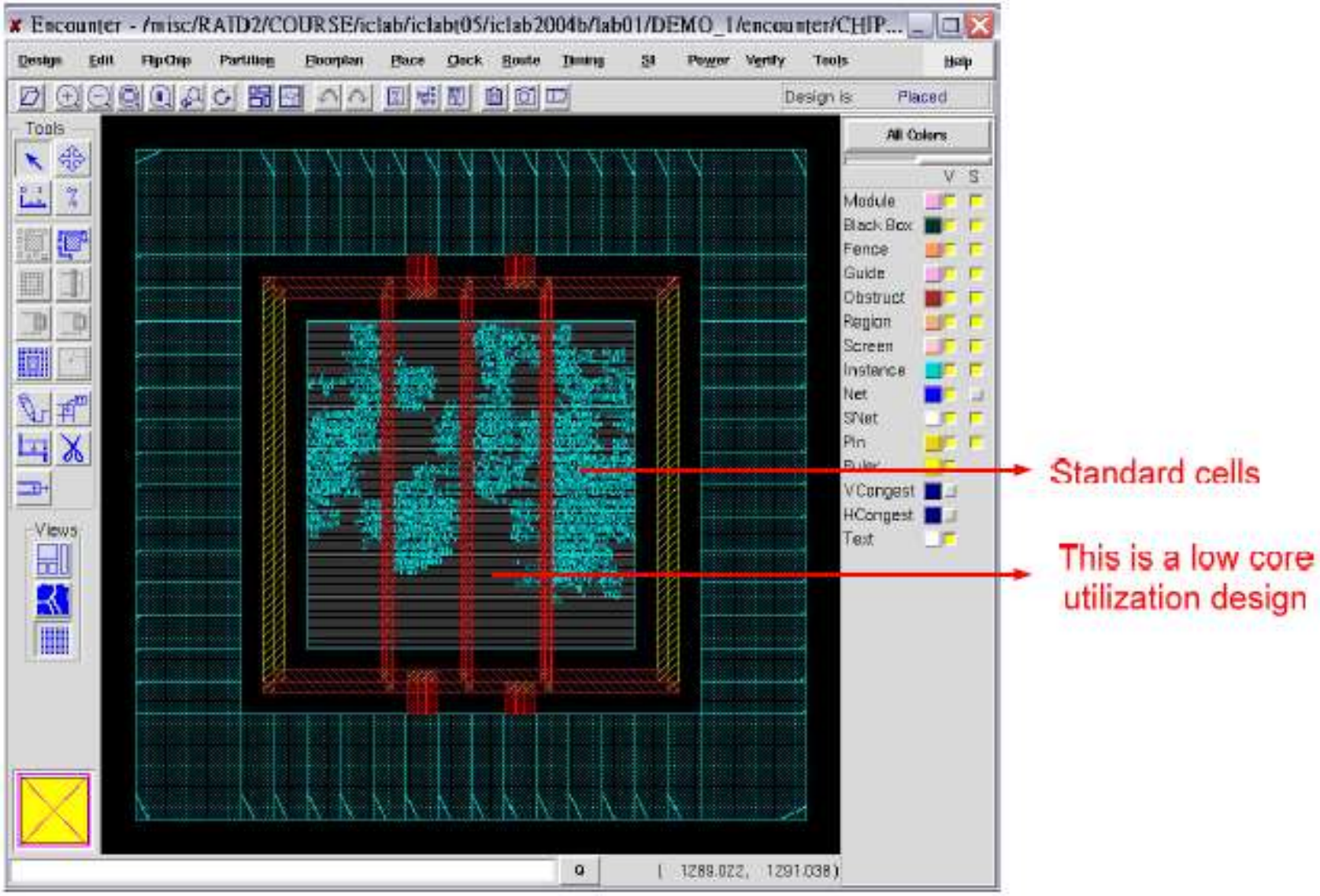
Confirm Power Analysis



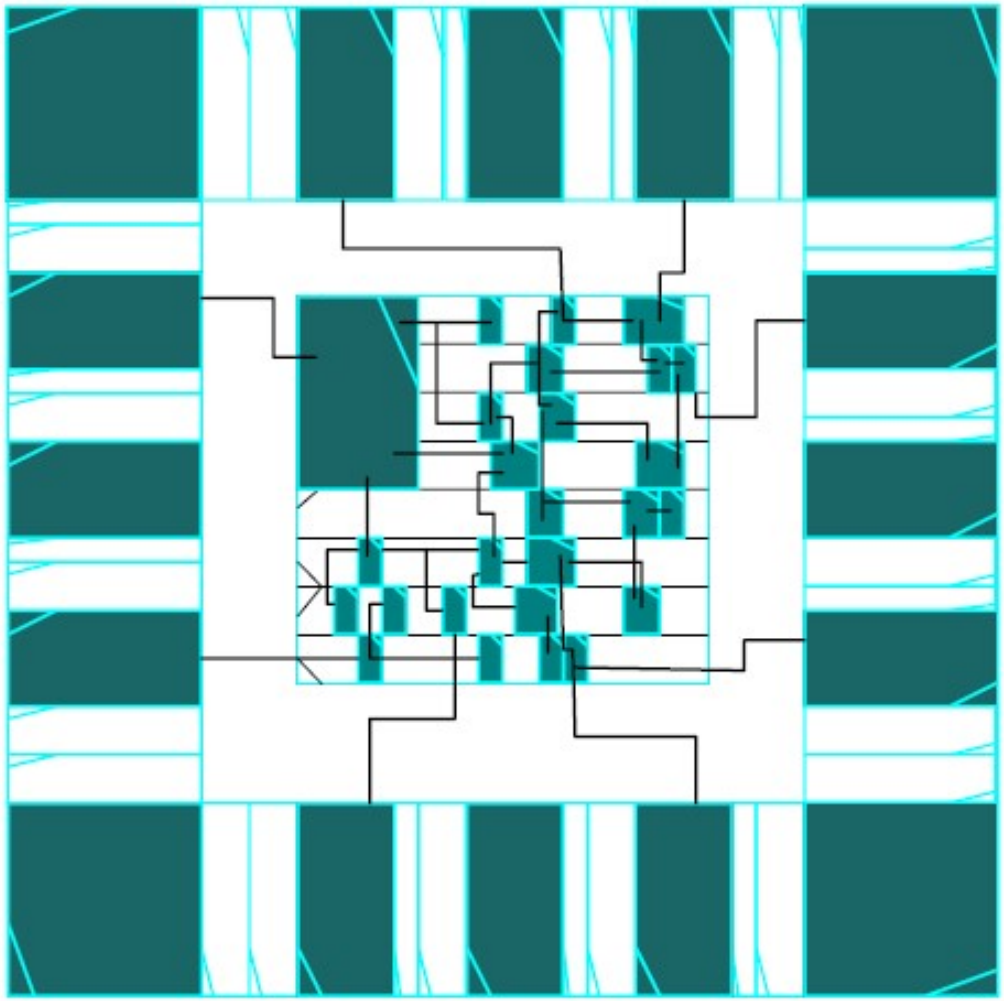
Power Route



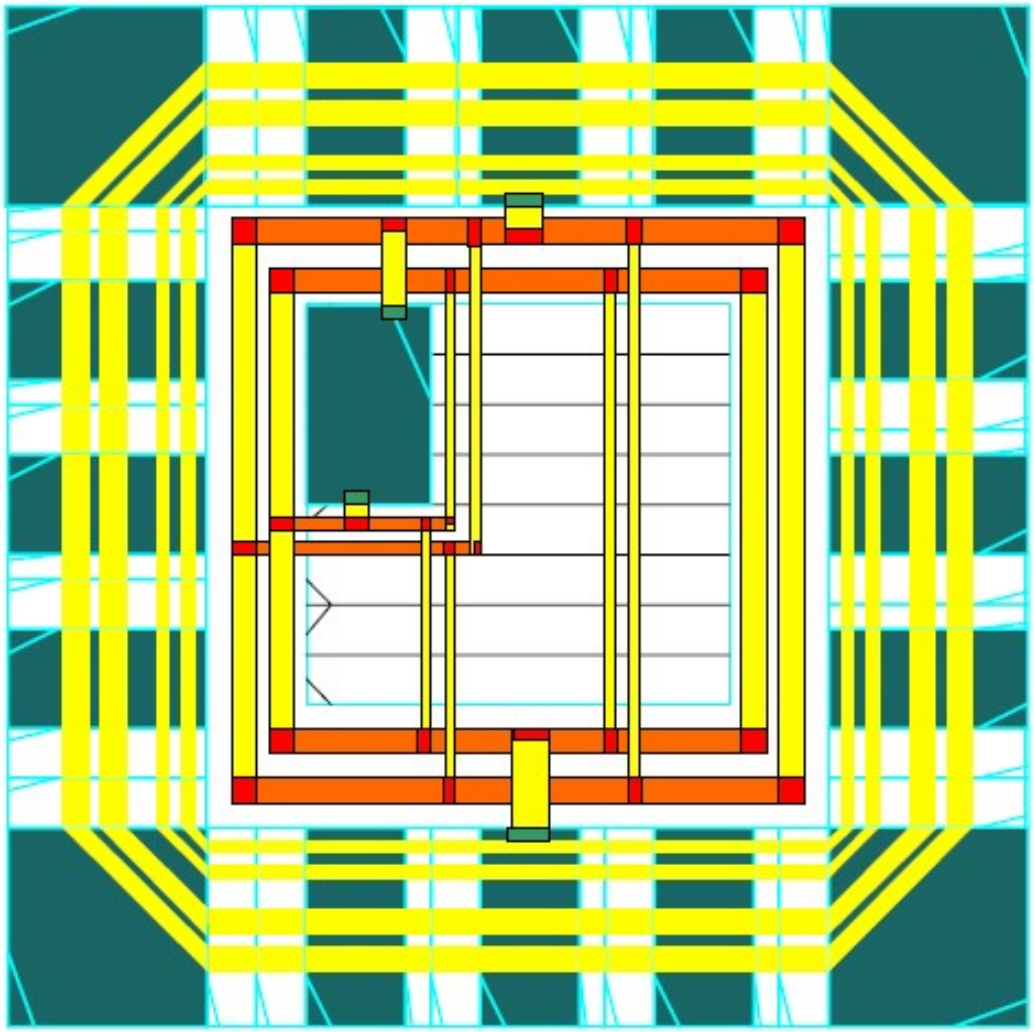
Power Route


Encounter - /misc/RAID2/COURSE/iclab/iclab05/iclab2004b/lab01/DEMO_1/encounter/CHIP...
Design
Edit
FlipChip
Partition
Floorplan
Place
Clock
Route
Timing
SI
Power
Verify
Tools
Help
Design is
Placed
Tools
Views
All Colors
V
S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
VCongest
HCongest
Text
Standard cells
This is a low core utilization design

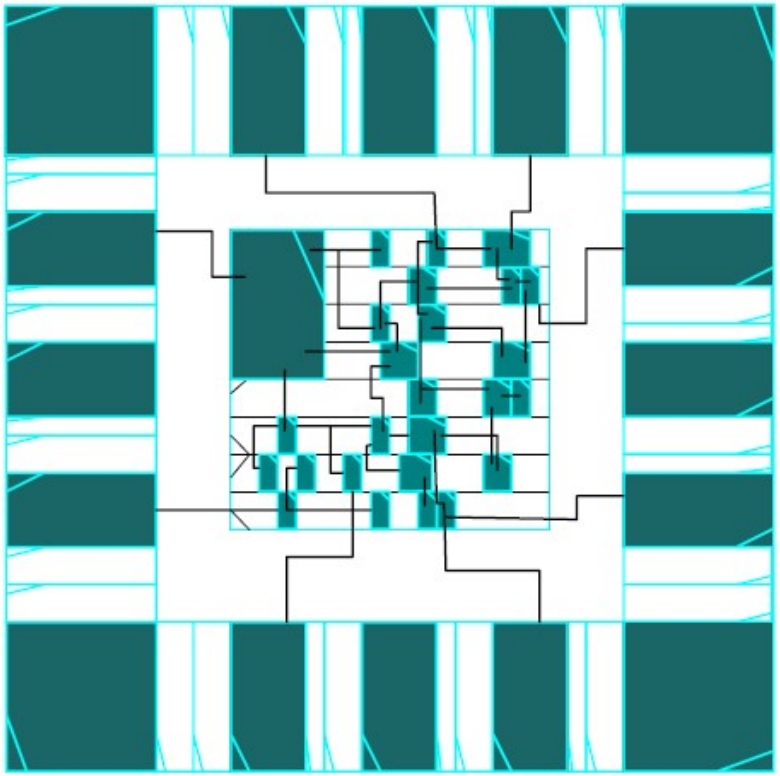
Cell Placement & Routing

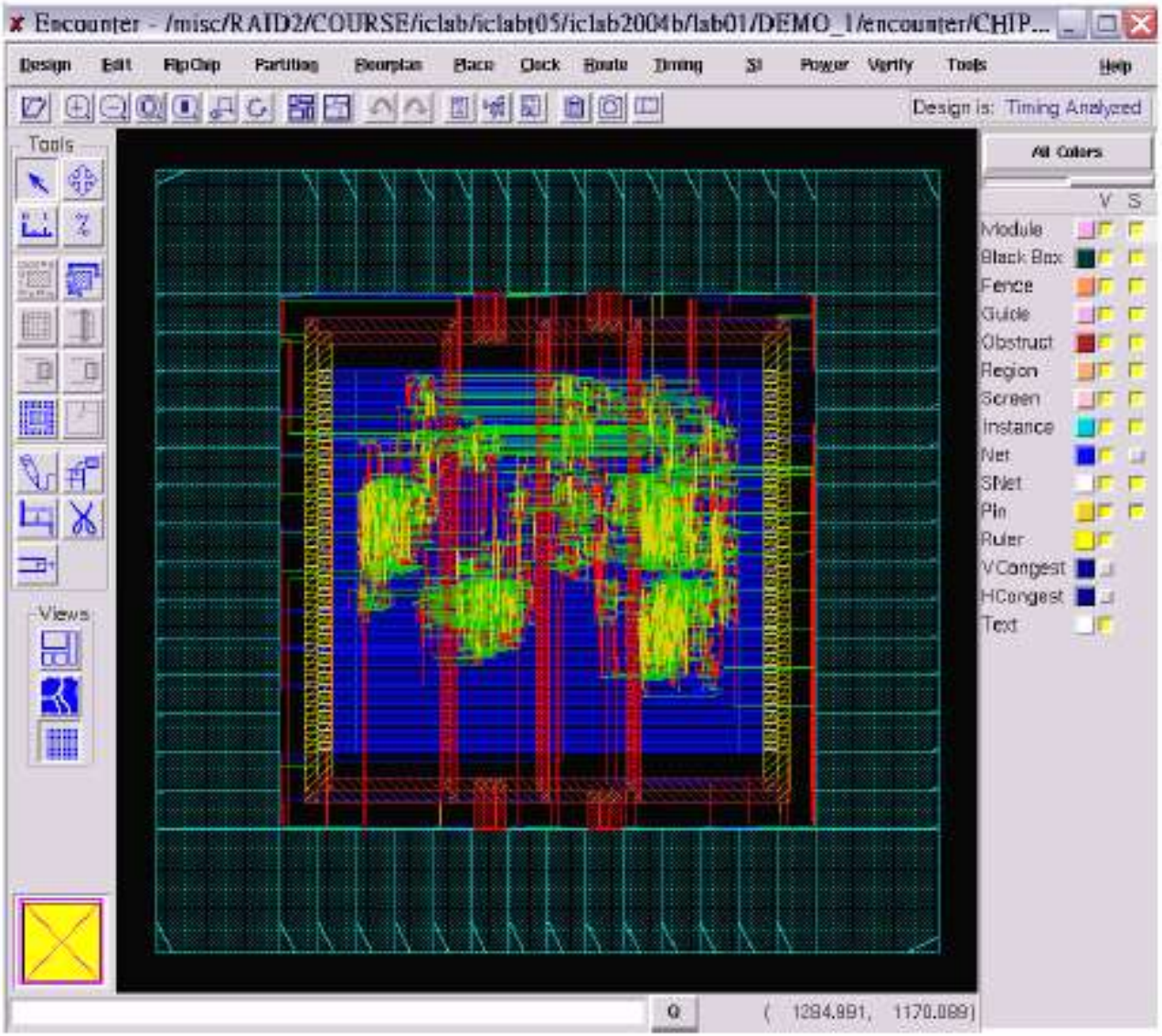


Add Fillers



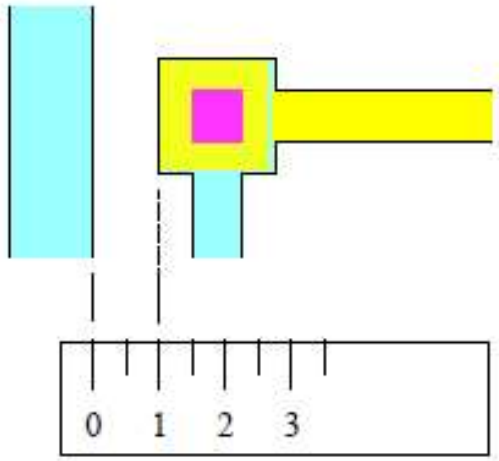
Routing



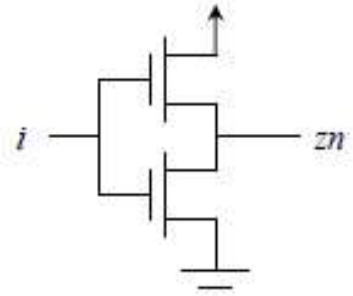

Encounter - /misc/RAID2/COURSE/iclab/iclab105/iclab2004b/lab01/DEMO_1/encounter/CHIP...
Design
Edit
FlipChip
Partition
Floorplan
Place
Clock
Route
Timing
SI
Power
Verify
Tools
Help
Design is: Timing Analyzed
Tools
Views
All Colors
V
S
Module
Black Box
Fence
Guide
Obstruct
Region
Screen
Instance
Net
SNet
Pin
Ruler
VCongest
HCongest
Text
(1294.991, 1170.089)

Post-Layout Physical Verification

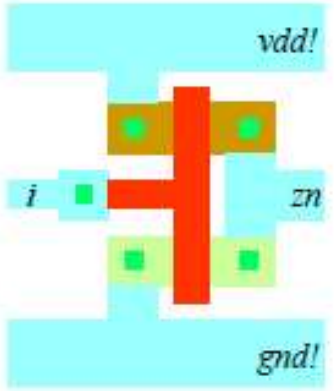
DRC



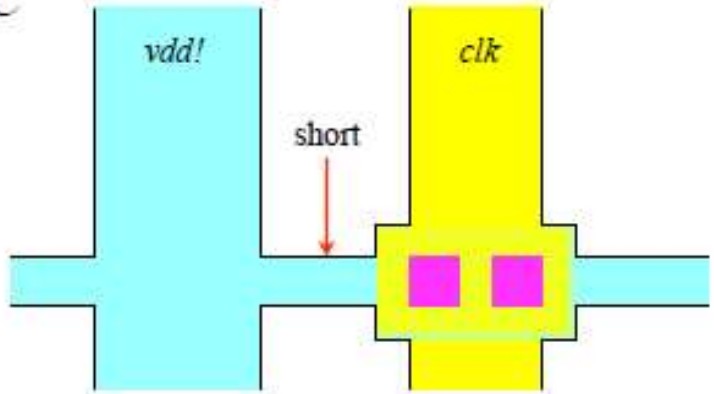
LVS



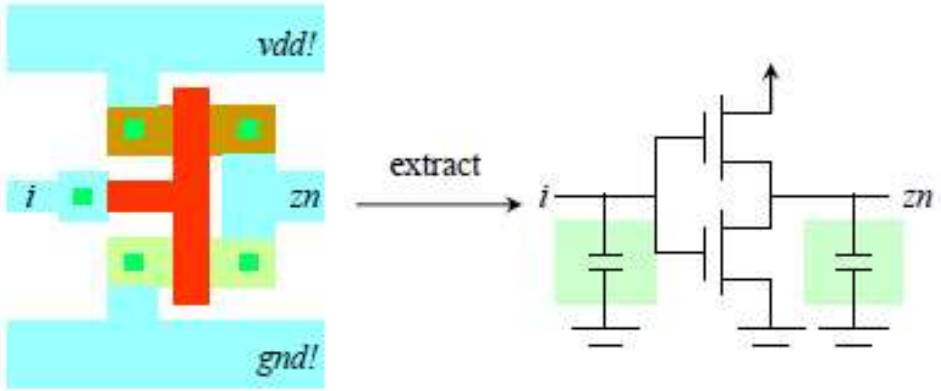
compare with



ERC



LPE/PRE



Post-Layout Physical Verification