Computer Engineering Department
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CMP3020 VLSI Design **Problem Set #1**

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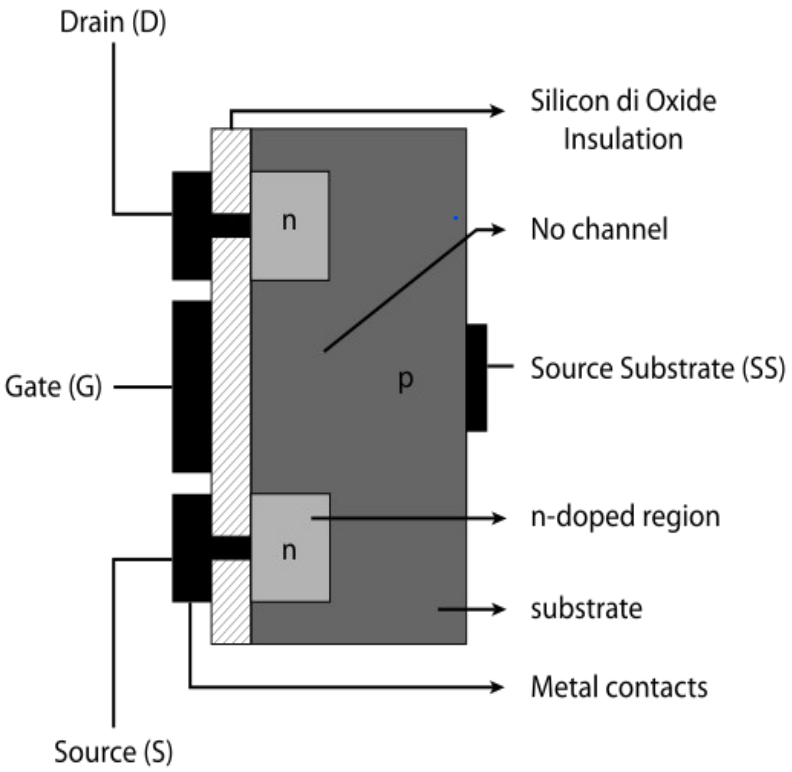
1) What is the difference between IDM, Fabless and Merchant Foundry? Can you give example for each?
2) What are self-Aligned Gates? Why to use it?
3) What is the Critical dimension?
4) True or False:
   a) The critical dimension depends on the wavelength of the incident light used in fabrication while it doesn't depend on the type and size of the optical lens used
   b) Having a low output impedance is a desirable property of the CMOS inverter (and gates)
   c) A ***positive resist*** is a type of photoresist in which the portion of the photoresist that is exposed to light becomes soluble to the photoresist developer. The portion of the photoresist that is unexposed remains insoluble to the photoresist developer.
5) What are the steps to fabricate a Transistor (photolithography)?

   This is a good resource http://www.renesas.com/company_info/fab

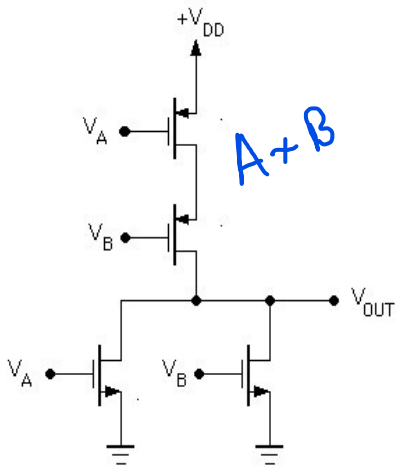
   OPS PAS PP
6) Why do we use a photomask?
7) …… is the interface between the circuit designer and process engineer. (Complete)
8) What is the difference between Micro Design rules and Scalable Design Rules? Which is better?
9) What is the difference between intra and inter layer design rules? Support your answer with examples
10) Design rules are used to ensure that design works even when small fab errors (within some tolerance) occur, can you give example of those errors.
11) What is the difference between a vias and contacts ?
12) Draw 2-input NAND stick diagram.
13) [Revision] Sketch a CMOS 2-input XOR gate

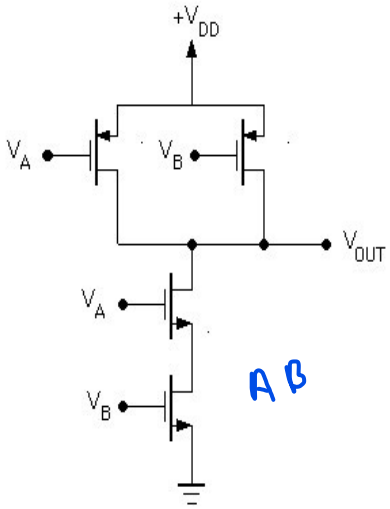
14) [Revision] An NMOS transistor is shown below

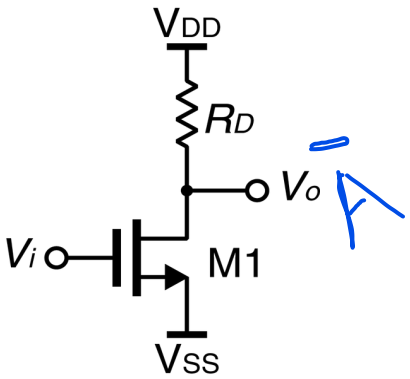
State the modes of operation for different values of Vgs



15) [Revision] Write the truth table for the following gates

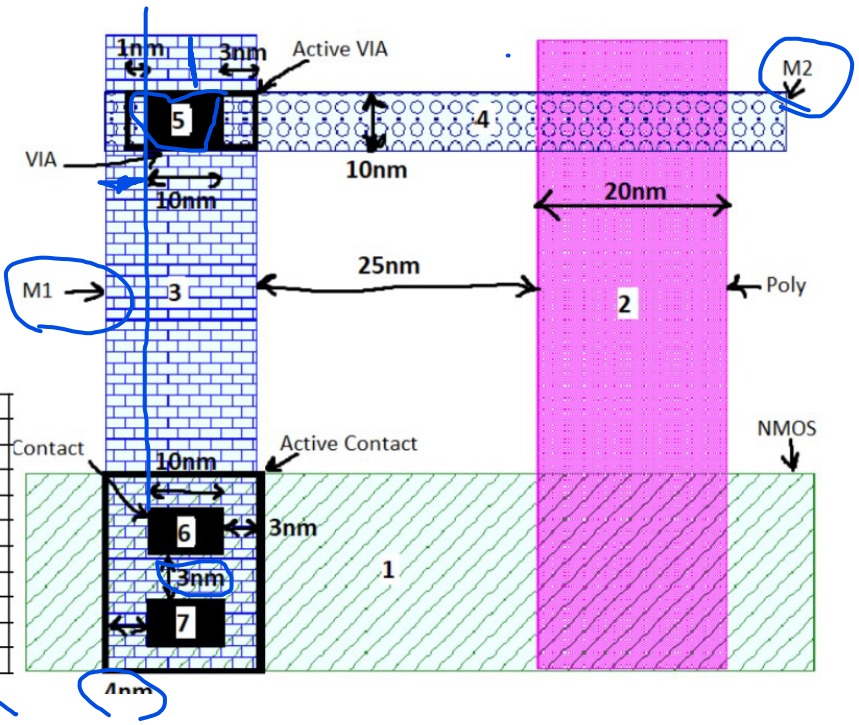






16)

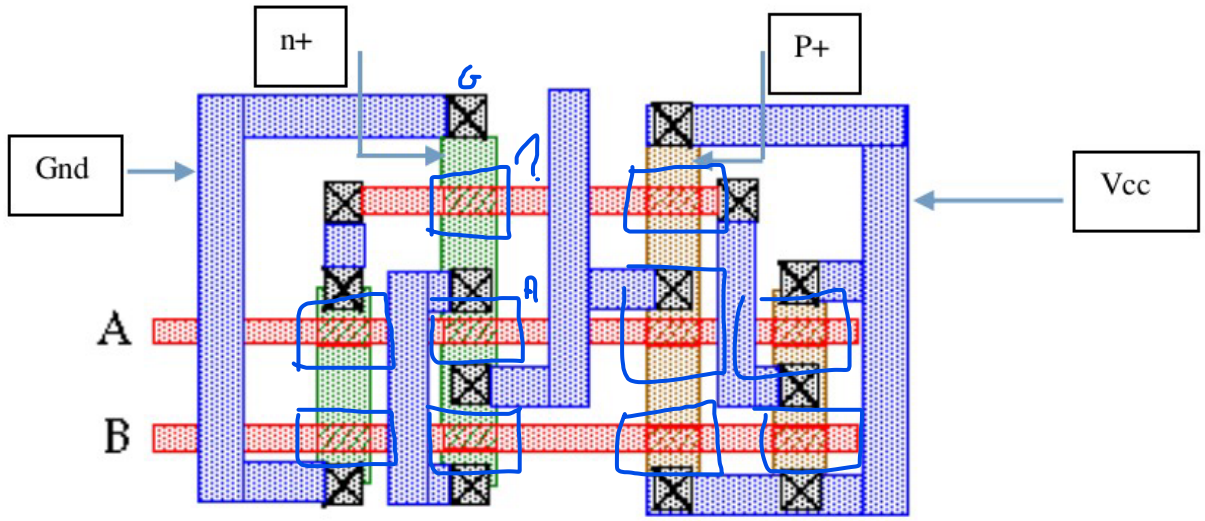
identify which design rules will pass and which will fail the DRC check



DRC Rule	Dimension
M1 Width	15
M1 Spacing	30
M2 Width	15
M2 Spacing	40
M1-M2 Spacing	30
M1-M2 Via Area	80
M1 Edge to Via Width	5
M2 Edge to Via Width	1
M1-M2 Via Spacing	5
Contact Spacing	5

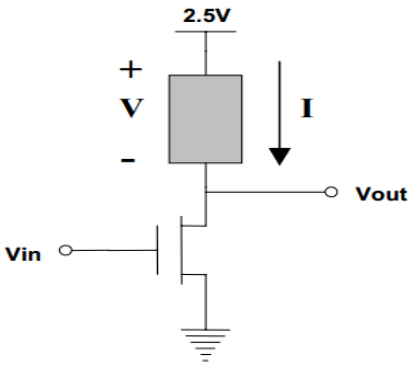
17) For the given layout ,

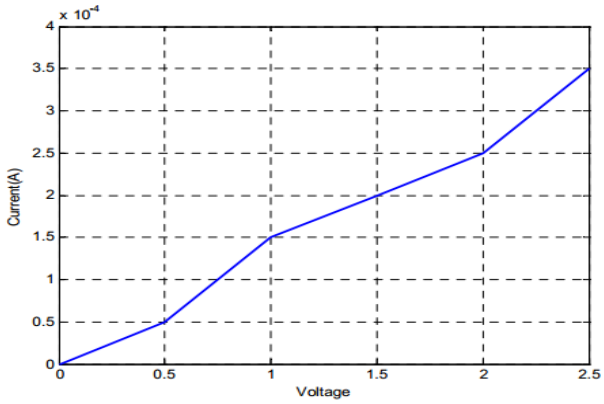
a. Write the logical expression
b. Draw the equivalent transistor diagram
c. Can you optimize it (take care: you **don't** have A' and B' as an input)



17) Generating a Voltage Transfer Characteristic

The circuit below features an NMOS transistor that is coupled with a non-linear load device represented by the shaded box. Accompanying the figure is the I-V characteristic for this non-linear load device.





Of course, we also have the family of I-V curves for our NMOS transistor given below (see next page):

A) Draw the VTC for this circuit. Determine (or estimate, if necessary, from your VTC) the following parameters: VOH, VOL

B) This circuit can be used as an alternative to a traditional CMOS inverter (where the non-linear device is a load to NMOS transistor). From the conceps discussed thus far in lecture and from the results of your VTC, what are the disadvantages of this design?

this circuit cause a leakage of current even when the transistor is off which consume very high static power.

I-V curve: max output and min output Volt disadvantage?