IC Design Flows

- The MOS Transistor
- Analog and Circuit Design
- **Digital Logic Families**
- Productivity Gap
- Digital Design Flows

CMOS Circuit Styles

- **Static complementary CMOS** - except during switching, output connected to either V_{DD} or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - V_{OH} and V_{OL} are at V_{DD} and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between V_{DD} and GND (**no** static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)
- **Dynamic CMOS** - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates, cycle has pre-charge and evaluation phases
  - increased sensitivity to noise

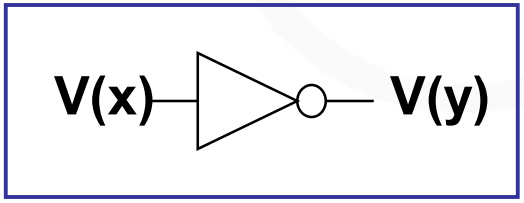
Static Inverter Behavior

- Steady-state parameters of a gate – *static behavior* – tell how robust a circuit is with respect to both variations in the manufacturing process and to noise disturbances.
- Digital circuits perform operations on Boolean variables

$$x \in \{0,1\}$$

- A logical variable is associated with a *nominal voltage level* for each logic state

$$1 \Leftrightarrow V_{OH} \text{ and } 0 \Leftrightarrow V_{OL}$$



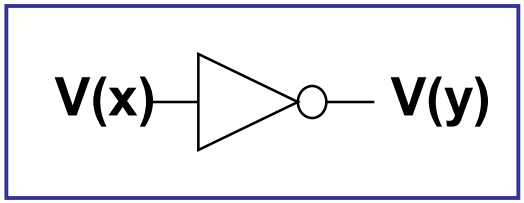
$$V_{OH} = !\,(V_{OL})$$

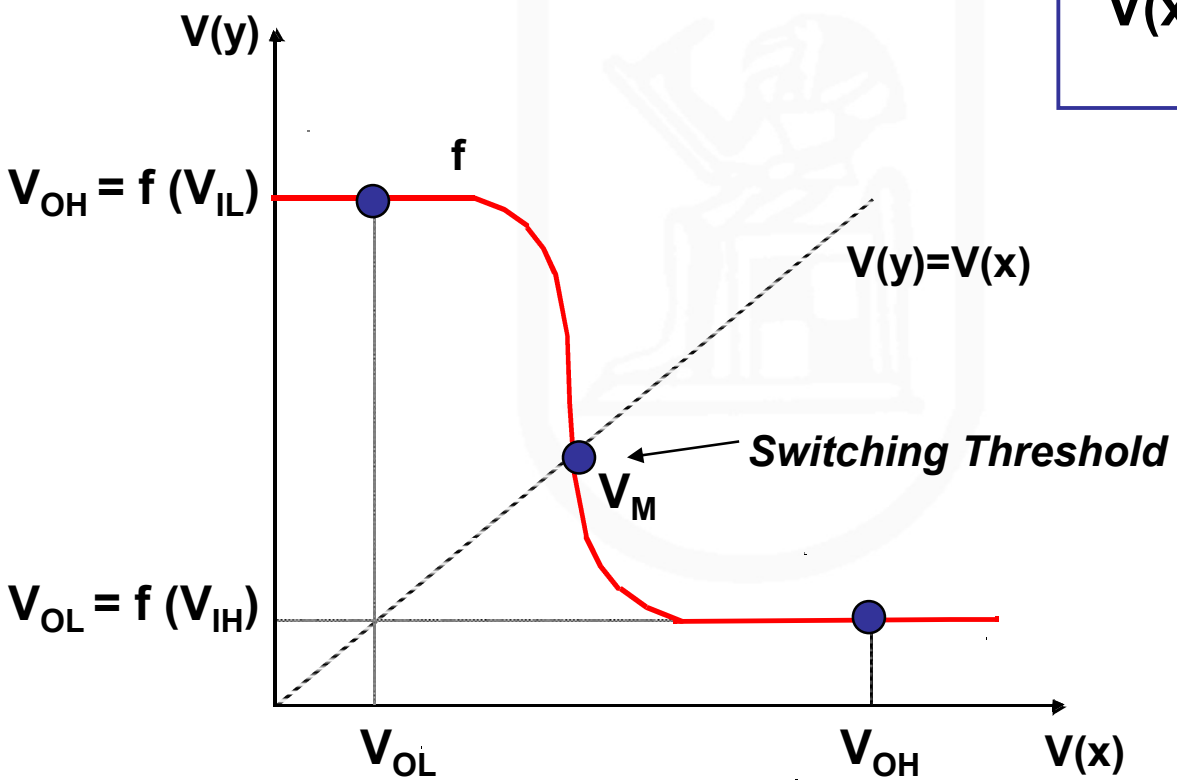
$$V_{OL} = !\,(V_{OH})$$

- Difference between V_{OH} and V_{OL} is the logic or *signal swing* V_{sw}

DC Operation
Voltage Transfer Characteristics (VTC)

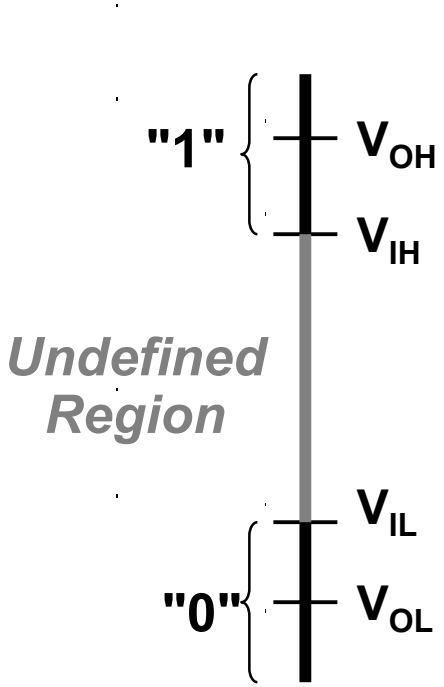
- Plot of output voltage as a function of the input voltage

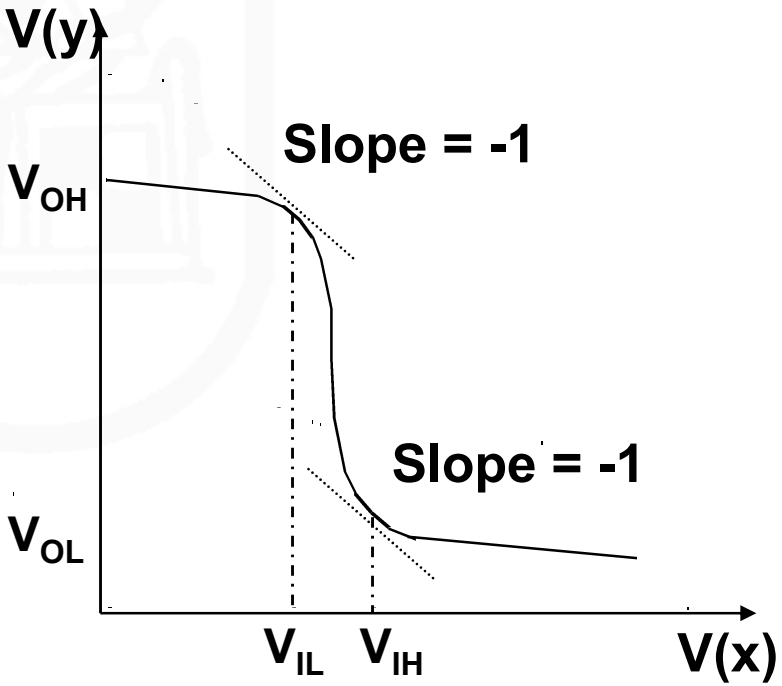




Mapping Logic Levels to the Voltage Domain

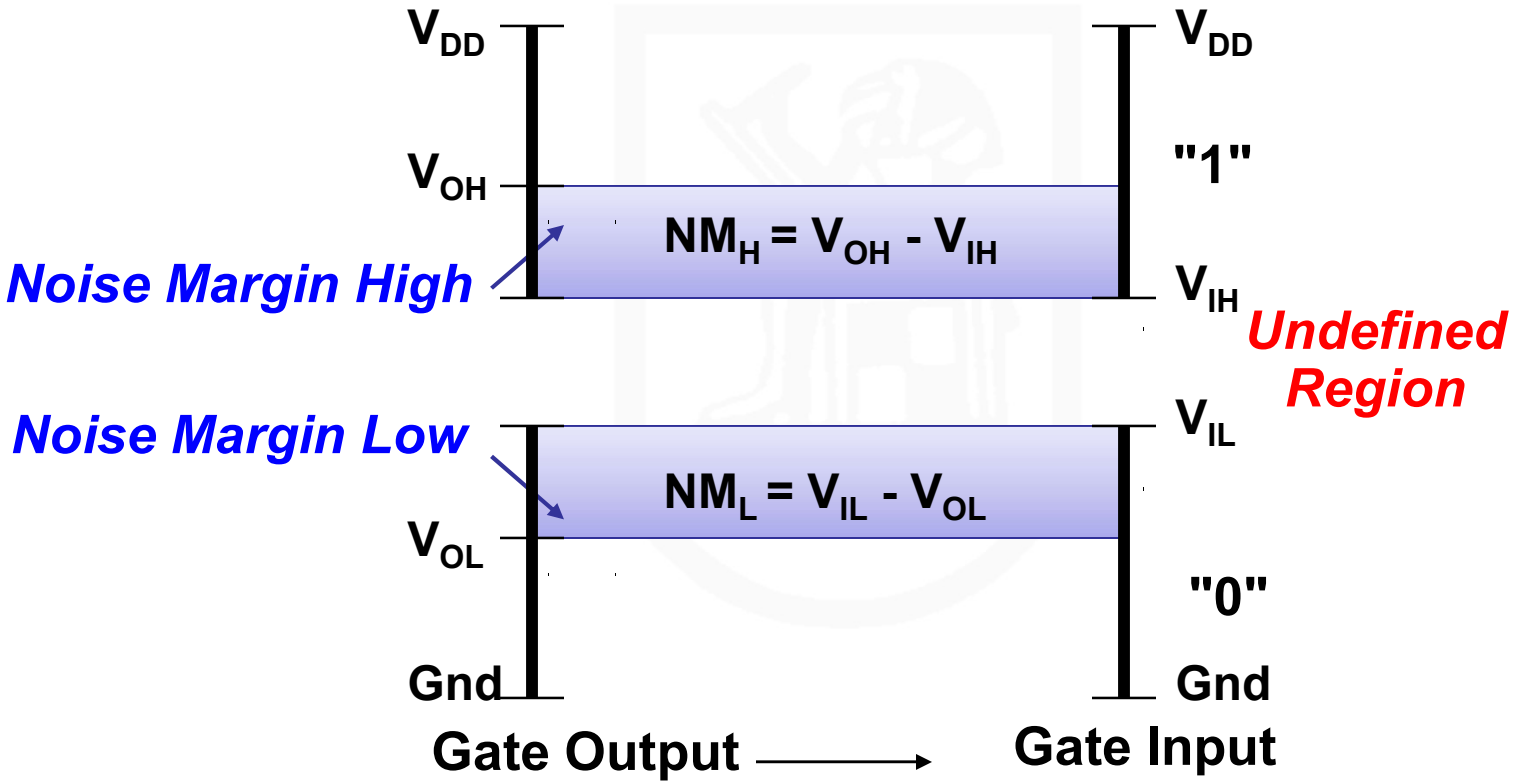
- The regions of acceptable high and low voltages are delimited by V_{IH} and V_{IL} that represent the points on the VTC curve where the gain = -1





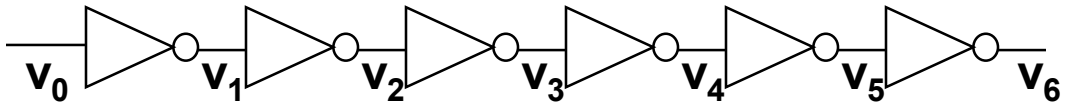
Noise Margins

- For robust circuits, want the “0” and “1” intervals to be a s large as possible

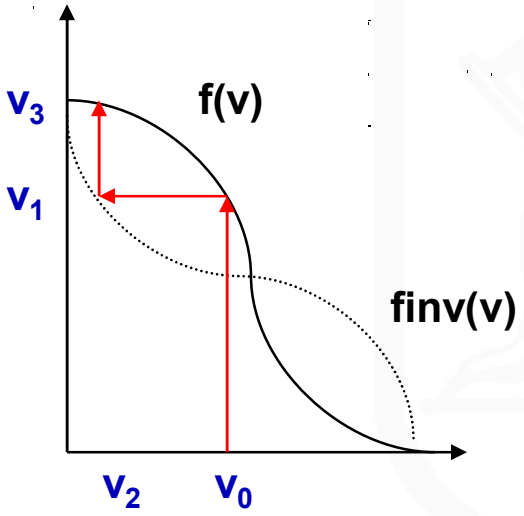


- Large noise margins are desirable, but not sufficient

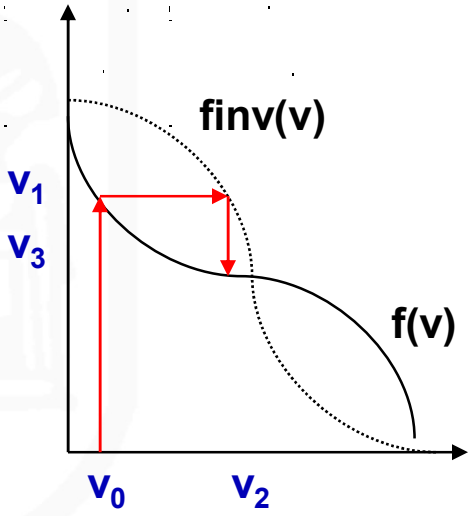
The Regenerative Property



$v_1 = f(v_0) \Rightarrow v_1 = finv(v_2)$



Regenerative Gate

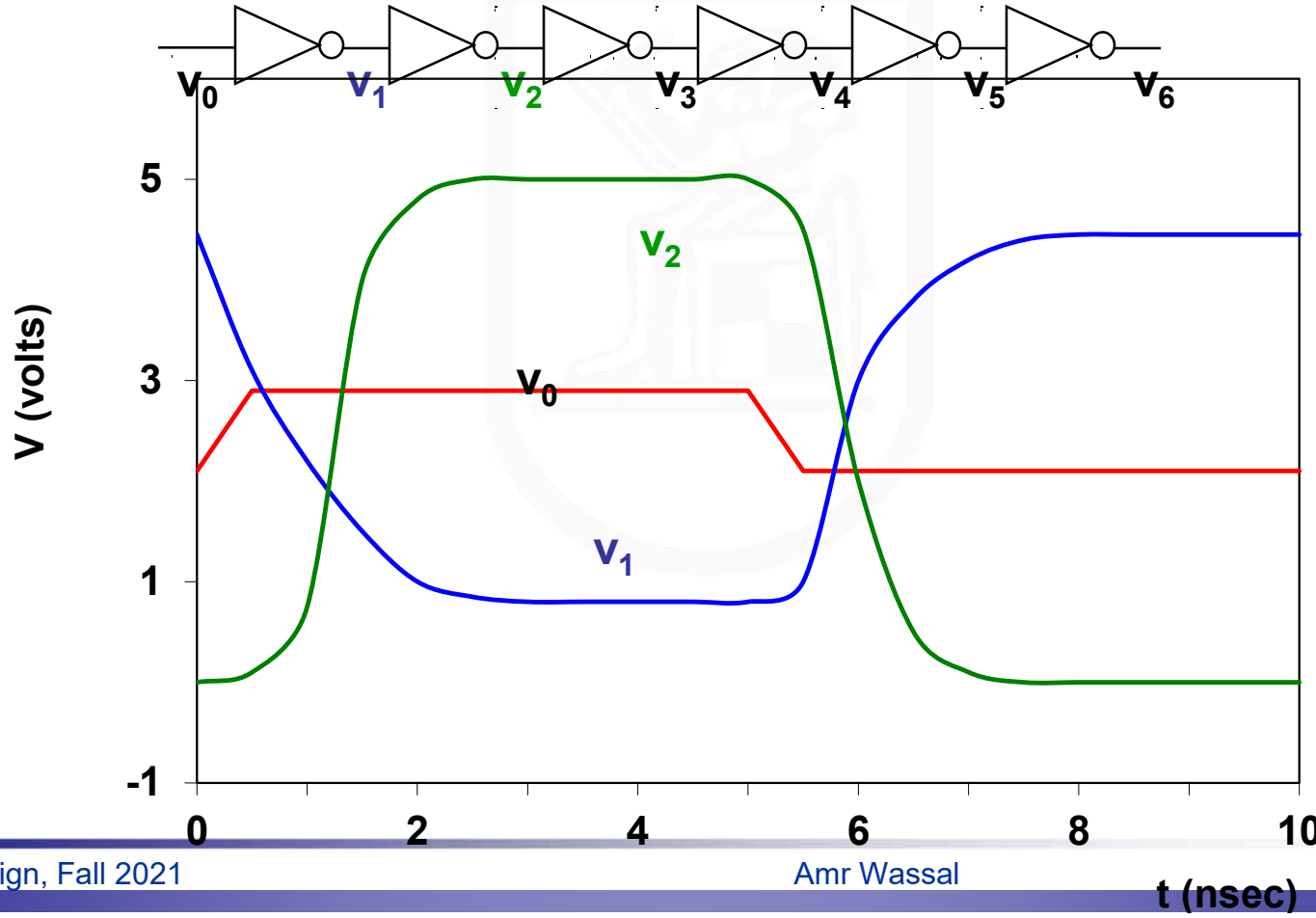


Nonregenerative Gate

- The VTC must have a transient region with a gain greater than 1 (in absolute value) bordered by two valid zones where the gain is smaller than 1. Such a gate has two stable operating points.

The Regenerative Property

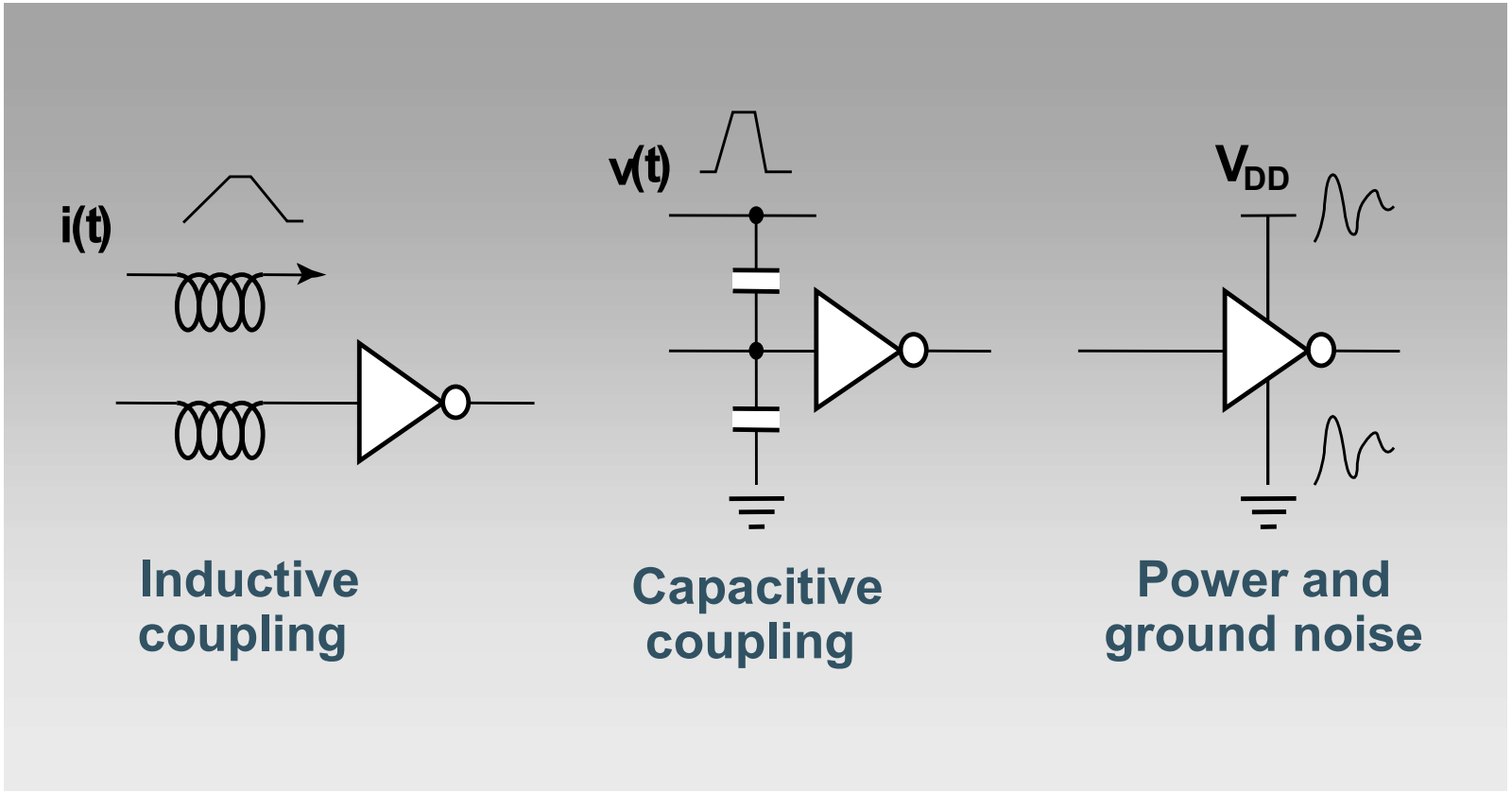
- A gate with regenerative property ensures that a disturbed signal converges back to a nominal voltage level



Noise Immunity

- Noise margin expresses the ability of a circuit to overpower a noise source
  - noise sources: supply noise, cross talk, interference, offset
- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- *Noise immunity* expresses the ability of the system to process and transmit information correctly in the presence of noise
- For good noise immunity, the signal swing (i.e., the difference between V_{OH} and V_{OL}) and the noise margin have to be large enough to overpower the impact of fixed sources of noise

Noise in Digital Integrated Circuits



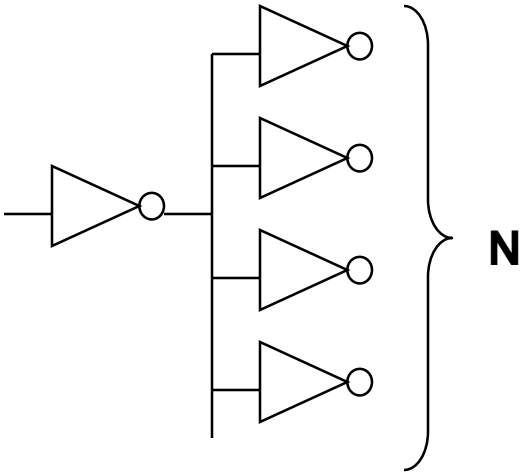
Directivity

- **A gate must be *unidirectional*: changes in an output level should not appear at any unchanging input of the same circuit**
  - In real circuits, *full* directivity is an illusion (e.g., due to capacitive coupling between inputs and outputs)

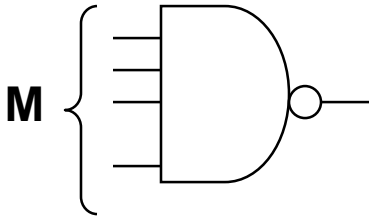
- **Key metrics: *output impedance* of the driver and *input impedance* of the receiver**
  - ideally, the output impedance of the driver should be zero and
  - input impedance of the receiver should be infinity

Fan-In and Fan-Out

- Fan-out – number of load gates connected to the output of the driving gate
  - gates with large fan-out are slower

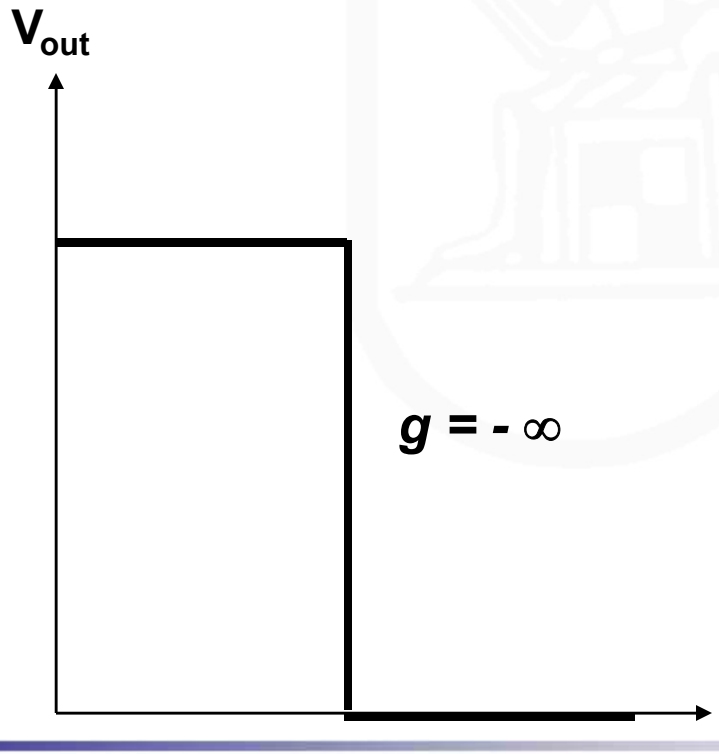


- Fan-in – the number of inputs to the gate
  - gates with large fan-in are bigger and slower



The Ideal Inverter

- **The ideal gate should have**
  - infinite gain in the transition region
  - a gate threshold located in the middle of the logic swing
  - high and low noise margins equal to half the swing
  - input and output impedances of infinity and zero, resp.



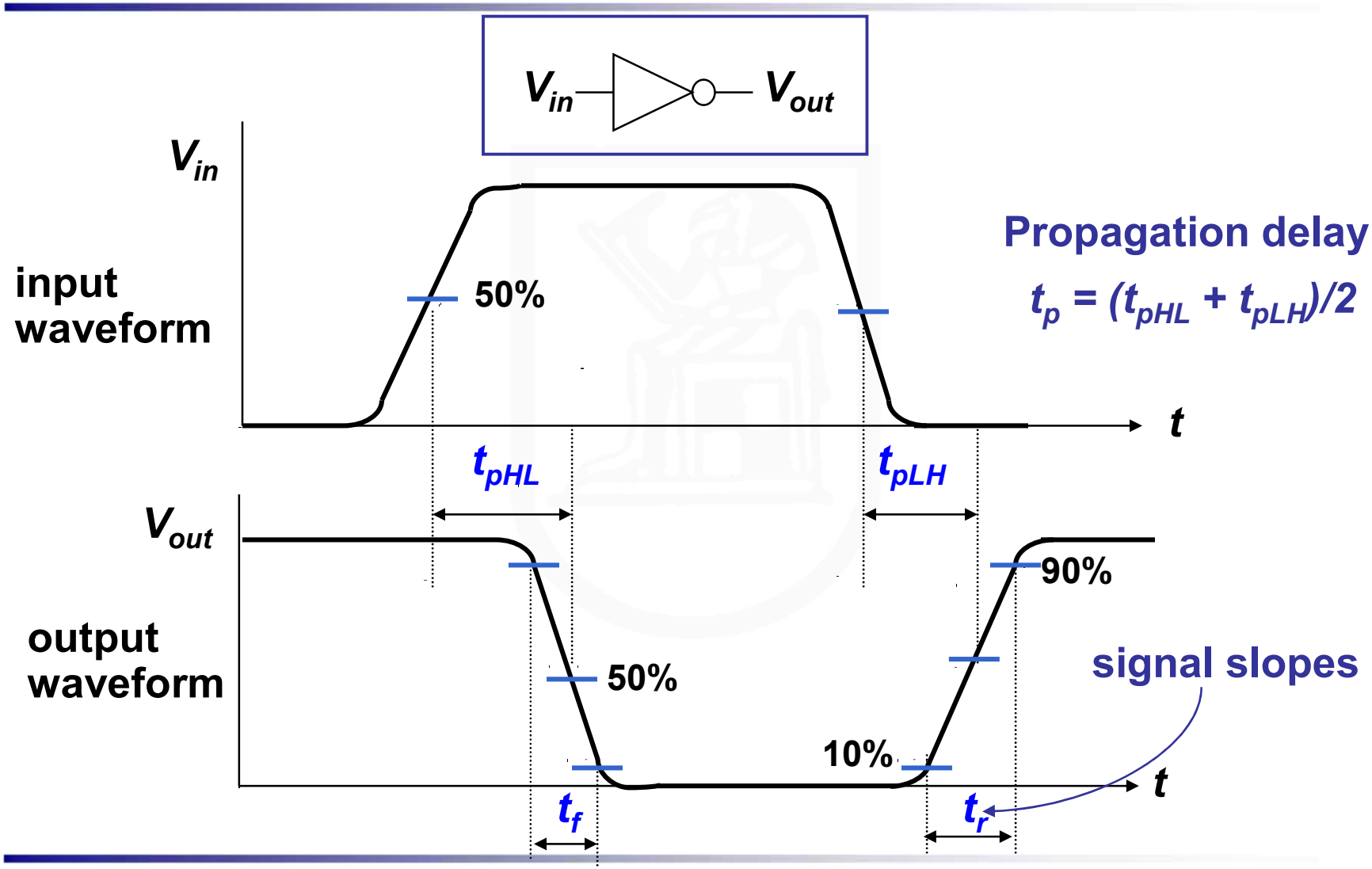
$R_i = \infty$

$R_o = 0$

Fanout = ∞

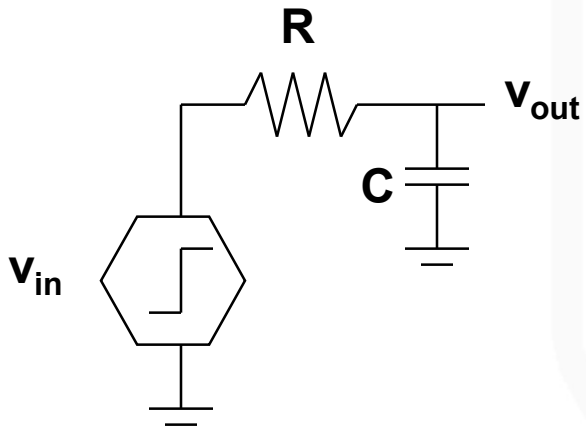
$NM_H = NM_L = VDD/2$

Delay Definitions



Modeling Propagation Delay

- **Model circuit as first-order RC network**



$$v_{out}(t) = (1 - e^{-t/\tau})V$$

where $\tau = RC$

Time to reach 50% point is
$t = \ln(2)\,\tau = 0.69\,\tau$

Time to reach 90% point is
$t = \ln(9)\,\tau = 2.2\,\tau$

- Matches the delay of an inverter gate

Power and Energy Dissipation

- Power consumption: how much energy is consumed per operation and how much heat the circuit dissipates
  - supply line sizing (determined by peak power)

$$P_{peak} = V_{dd} i_{peak}$$

  - battery lifetime (determined by average power dissipation)

$$p(t) = v(t)i(t) = V_{dd} i(t)$$

$$P_{avg} = 1/T \int p(t)\, dt = V_{dd}/T \int i_{dd}(t)\, dt$$

  - packaging and cooling requirements
- Two important components: static and dynamic

$$f_{0\to1} = P_{0\to1} * f_{clock}$$

$$P \text{ (watts)} = C_L V_{dd}^2 f_{0\to1} + t_{sc} V_{dd} I_{peak} f_{0\to1} + V_{dd} I_{leakage}$$

Power and Energy Dissipation

- Propagation delay and the power consumption of a gate are related
- Propagation delay is (mostly) determined by the speed at which a given amount of energy can be stored on the gate capacitors
  - the faster the energy transfer (higher power dissipation) the faster the gate
- For a given technology and gate topology, the product of the power consumption and the propagation delay is a constant
  - **Power-delay product (PDP) – energy consumed by the gate per switching event = $P_{av} \times t_p$**
- An ideal gate is one that is fast and consumes little energy, so the ultimate quality metric is
  - **Energy-delay product (EDP) = $E \times t_p$ = power $\times$ delay ^{2}**