Cairo University
Faculty of Engineering
Computer Engineering Department

VLSI
Sheet 2

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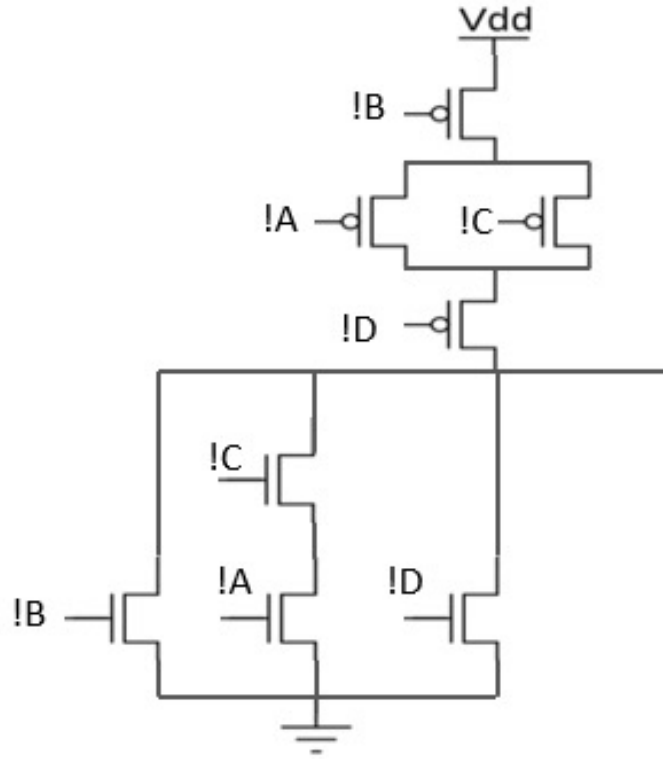
Problem 1:

- $Z = (AB+BC) \cdot D$
- First step get Z’
- Z’= (AB+BC)’+D’
- Z’=(AB)’(BC)’+D’
- Z’=(A’+B’)(B’+C’)+ D’
- Here how many transistors: **each input 1 transistor** then all ***2** since we have both N and P networks.
- →5*2=10 transistors
- Can further optimize:
- Z’=A’B’+A’C’+B’B’+B’C’+D’
- Z’=A’B’+A’C’+B’+B’C’+D’
- Z’=B’(A’+1+C’)+A’C’+D’
- Z’=B’+A’C’+D’
- →4*2=8 transistors
- Assume input and inverted input as given (e.g.: A and A’ are both given)

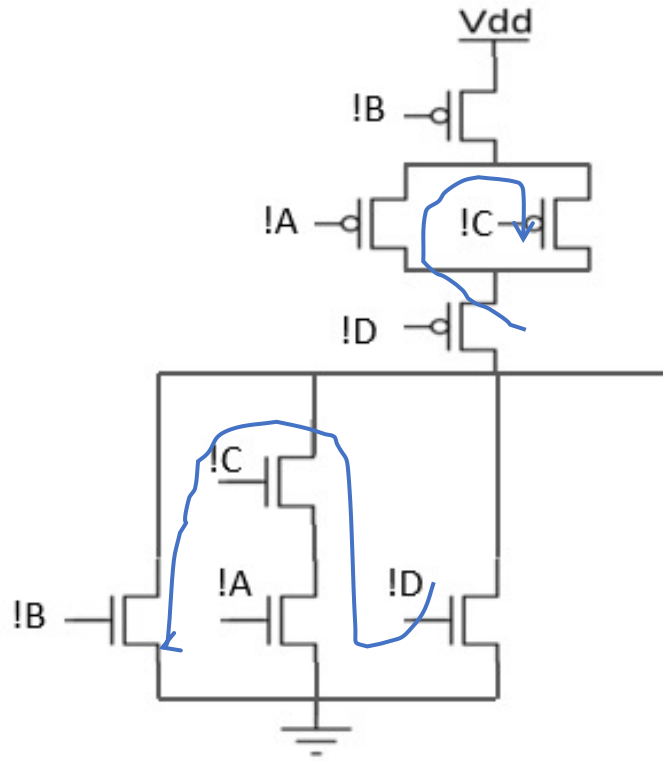
Draw Transistors and Get Euler path (if any)

Z’=B’+A’C’+D’

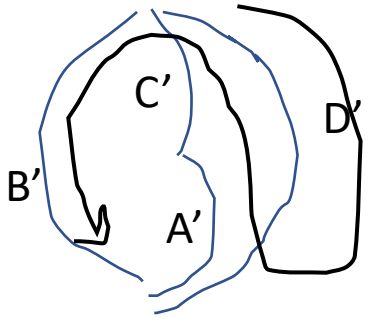


- An uninterrupted diffusion strip is possible only if there exists an Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.
- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

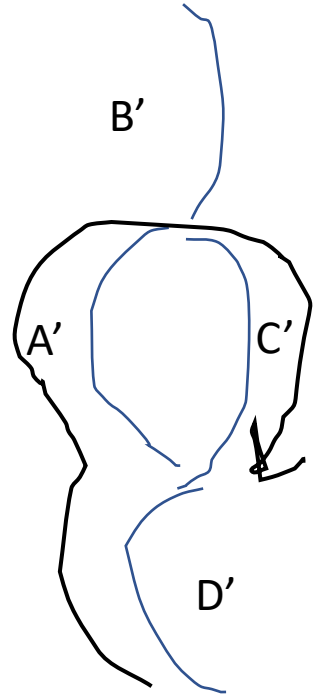
Euler Path Graphs



Arcs are transistors
Nodes are vertices



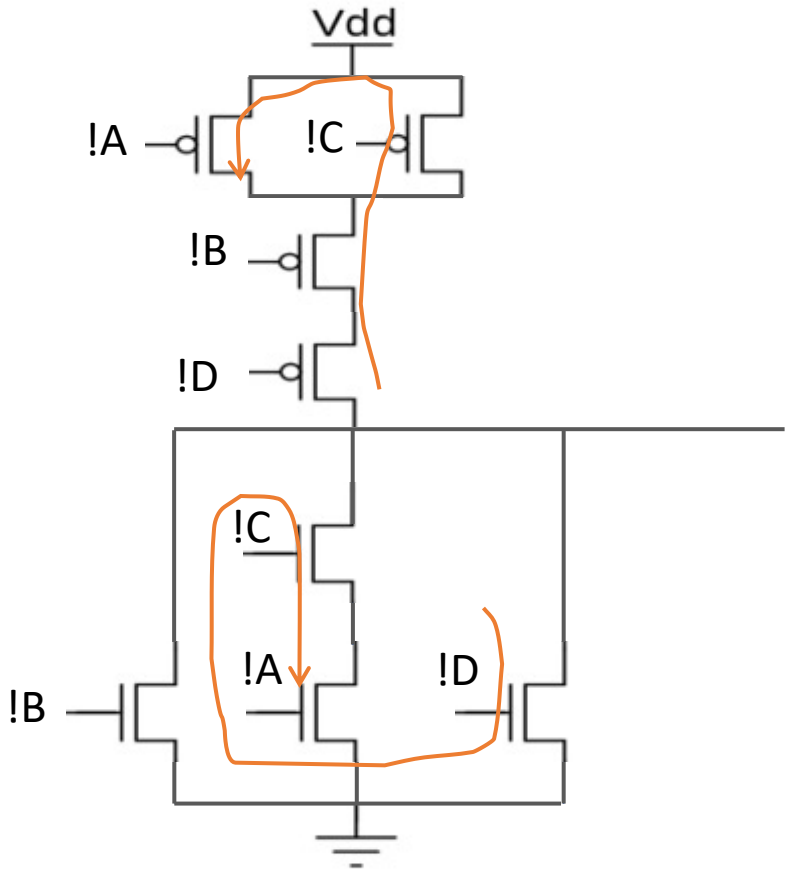
N-graph



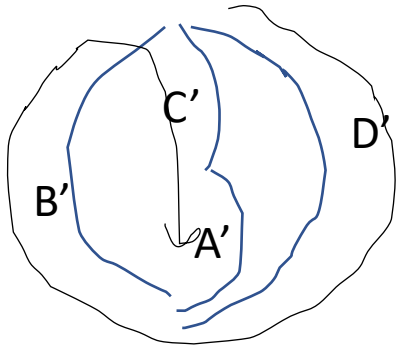
P-graph

D’A’C’B’ in N but in P no

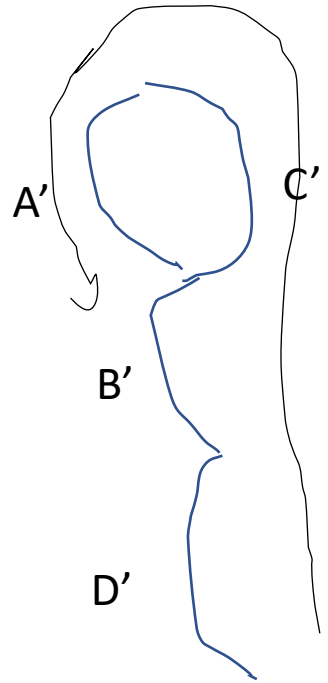
Euler Path Graphs



Arcs are transistors
Nodes are vertices



N-graph

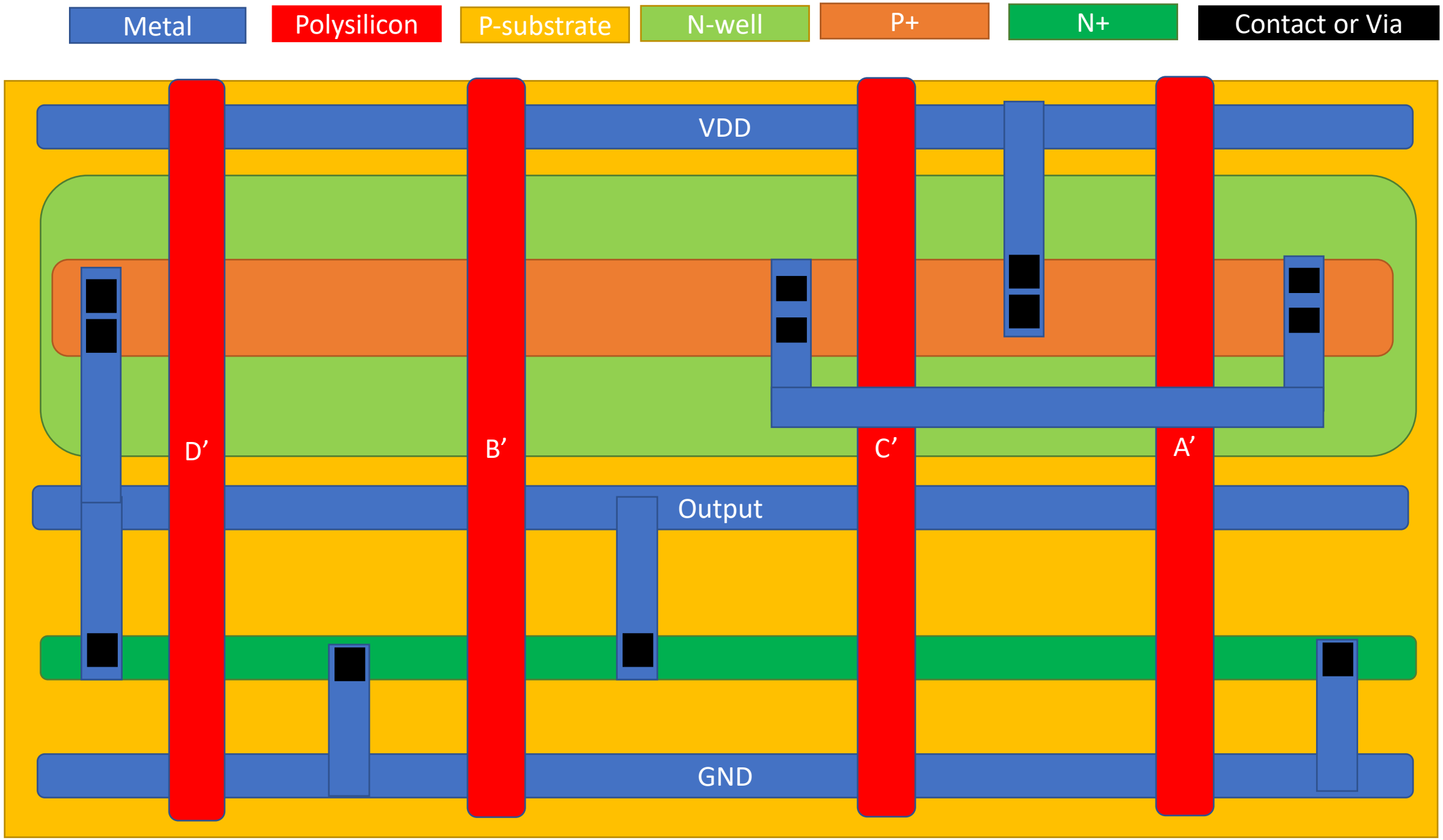


P-graph

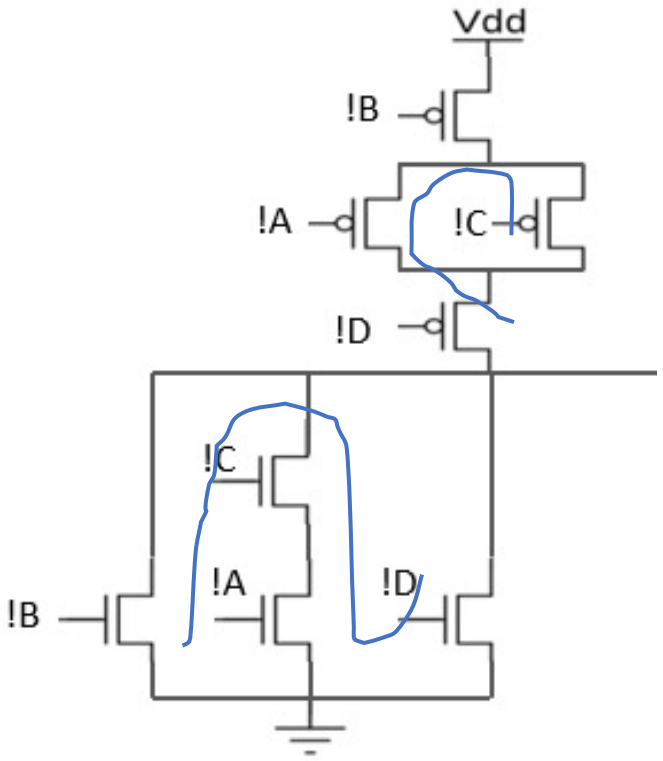
Common Euler path D'B'C'A' in N and also in P

Layout Drawing Steps

- 1-Insert the substrate (mostly P or N)
- 2-Insert the well
  - of P-MOS: N-well if substrate is P
  - of N-MOS: P-well if substrate is N
- 3-Insert diffusions (N+ or P+)
  - P diffusion is wider than N diffusion to compensate the lower speed of holes than electrons.
- 4-Insert VDD, GND and Output
- 5-Insert the poly's (in same order as in Euler's path)
- 6-Use metal to connect the sources and drains of the gates.
  - Add appropriate contacts
  - Easiest method is to follow the order in Euler path while connecting


Metal
Polysilicon
P-substrate
N-well
P+
N+
Contact or Via
VDD
D’
B’
C’
A’
Output
GND

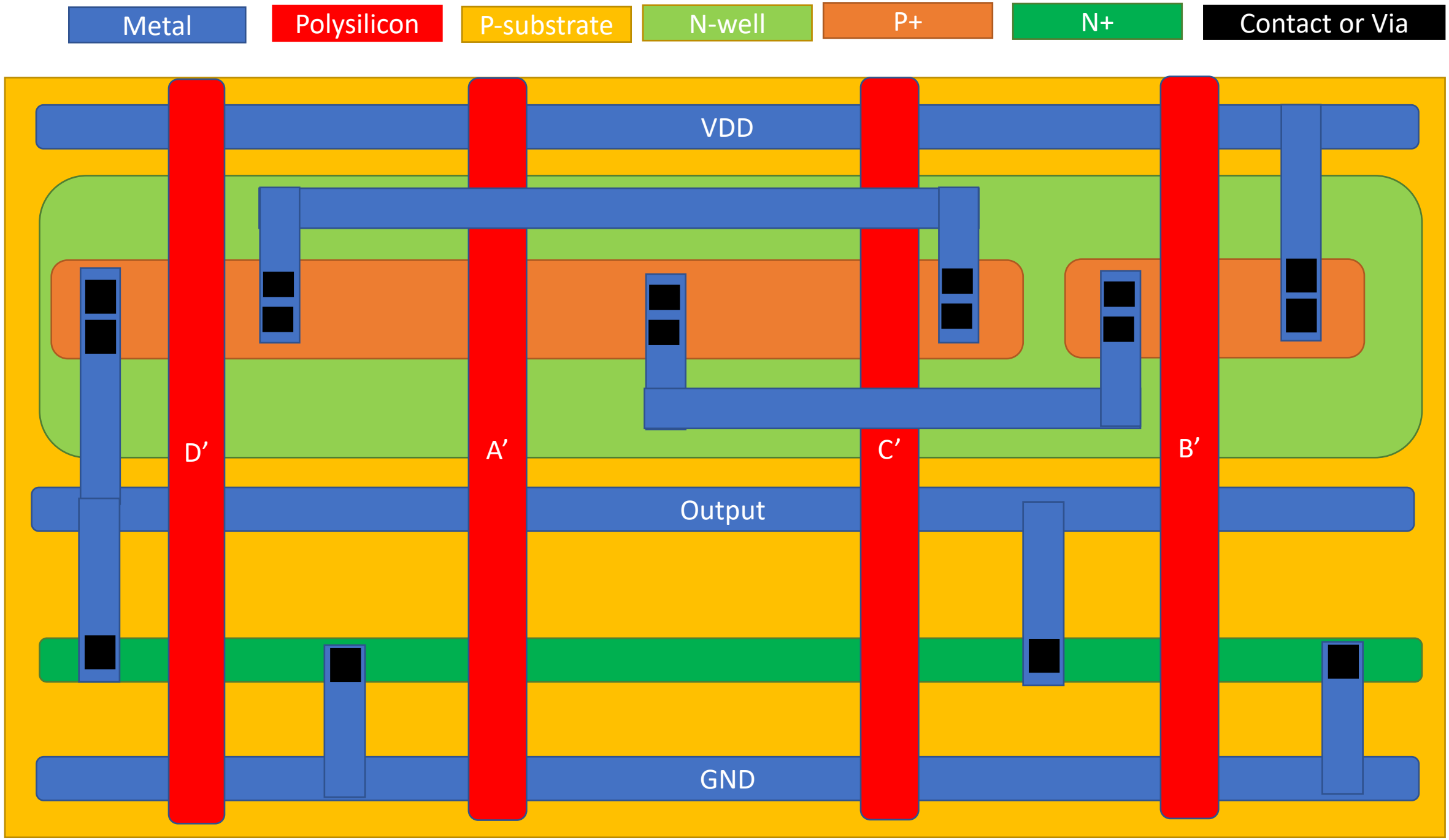
Get Euler path



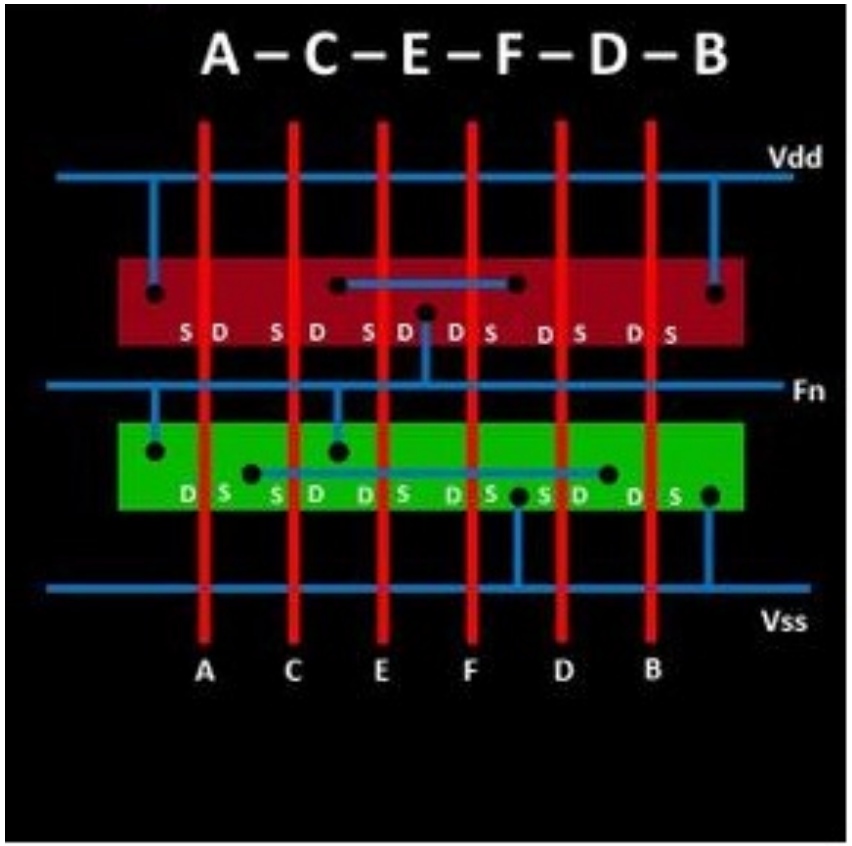
What if the euler path in the pull-up is not similar to euler in the pull down ?

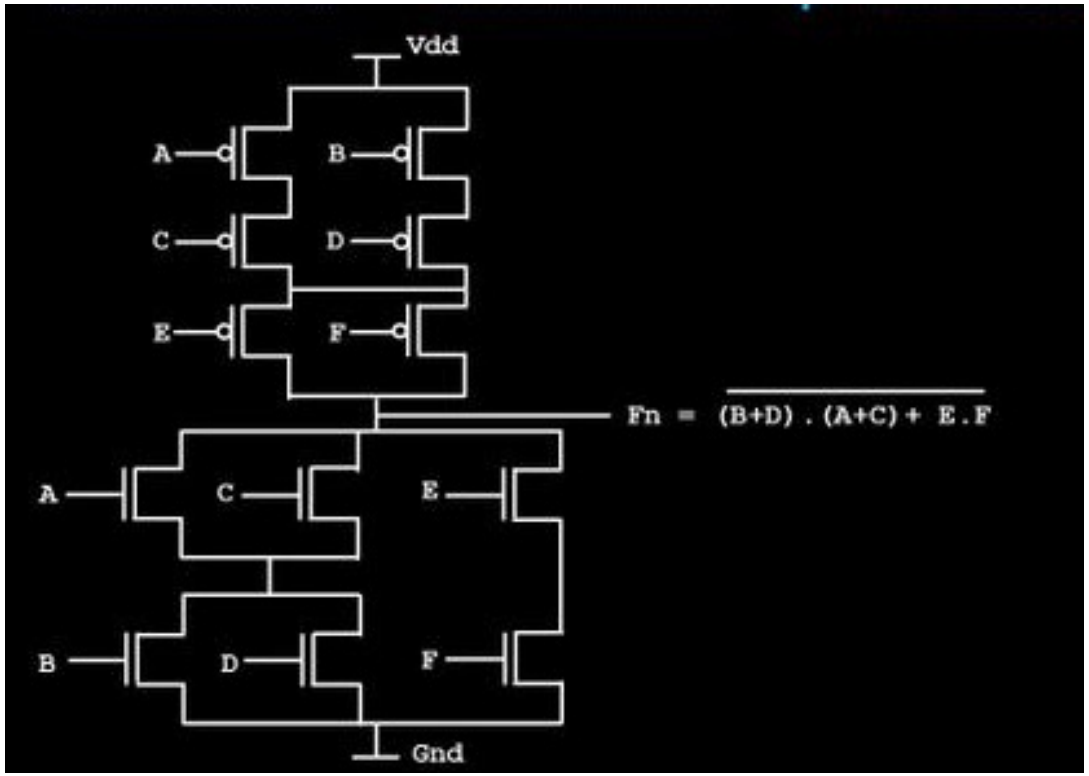
D'A'C'B' in N but in P no

Solution: follow euler path in the pull-down and cut the diffusion in pull-up

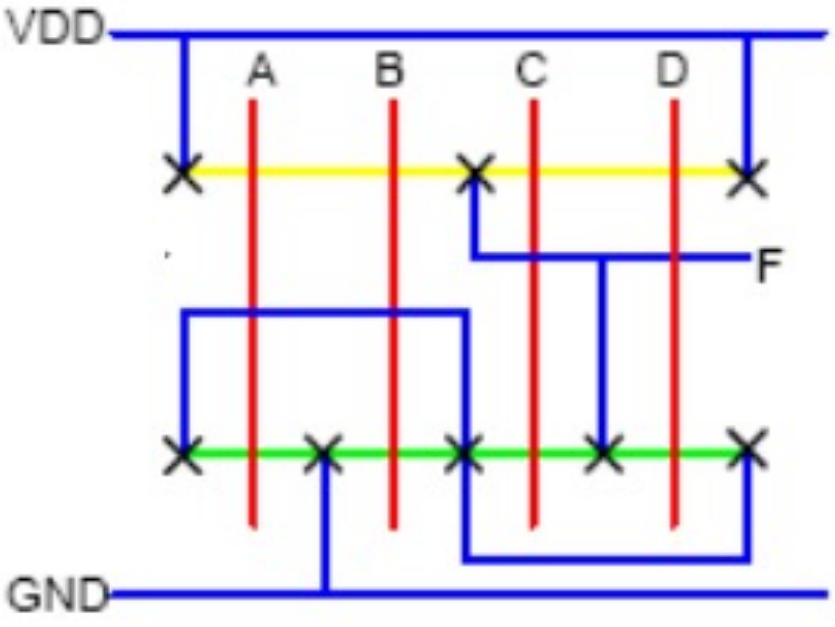

Metal
Polysilicon
P-substrate
N-well
P+
N+
Contact or Via
VDD
D’
A’
C’
B’
Output
GND

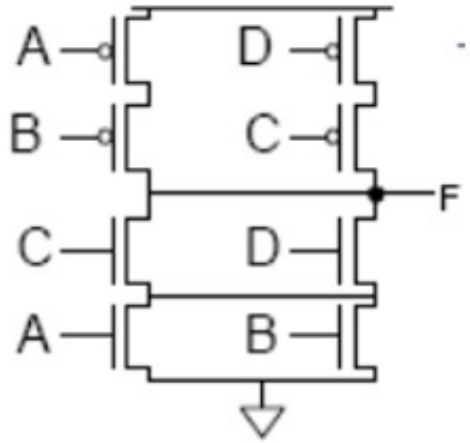
Problem 2:





Problem 3:





$$F = \overline{(A+B)(C+D)}$$

THANK YOU