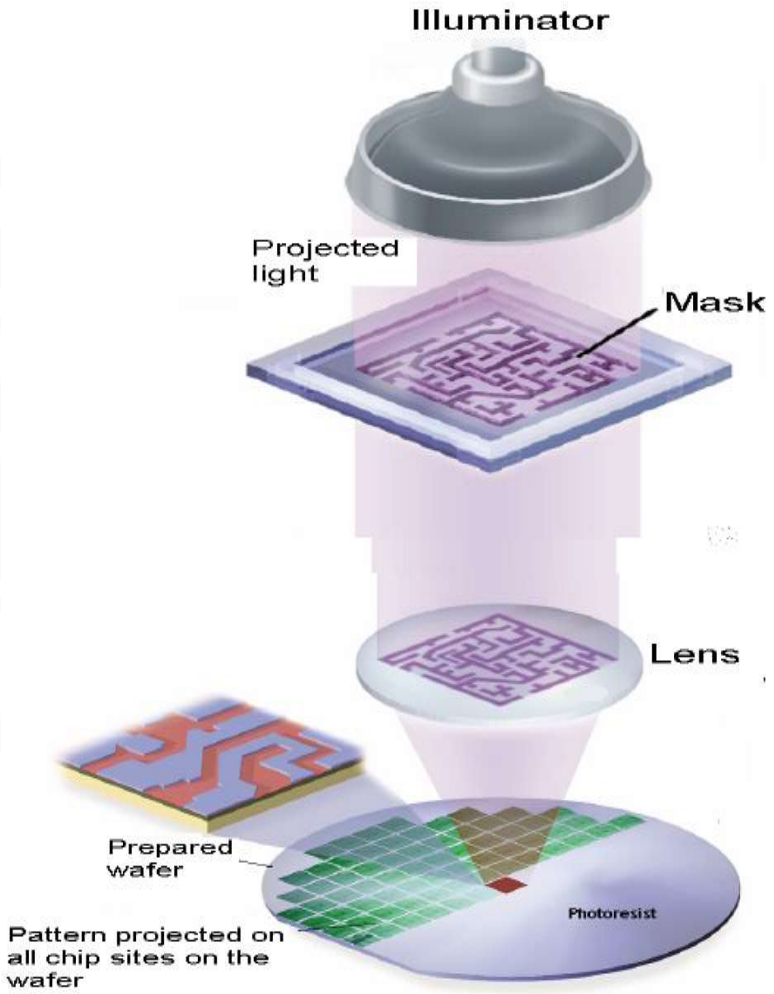
Technology Generations (or Nodes)

- **We refer to the smallest feature size or Critical Dimension (CD).**
- **10um 5um 2um 1um 0.8um 0.5um 0.35um 0.25um 0.18um 0.13um 90nm 65nm 45nm 32nm 22nm**
- **Possible through the magic of device scaling**
- **Desirable due to manufacturing economics (wafer and batch processing)**
- **Usually limited by lithography, implies new patterning technology, equipment for each node. $$$$$$**

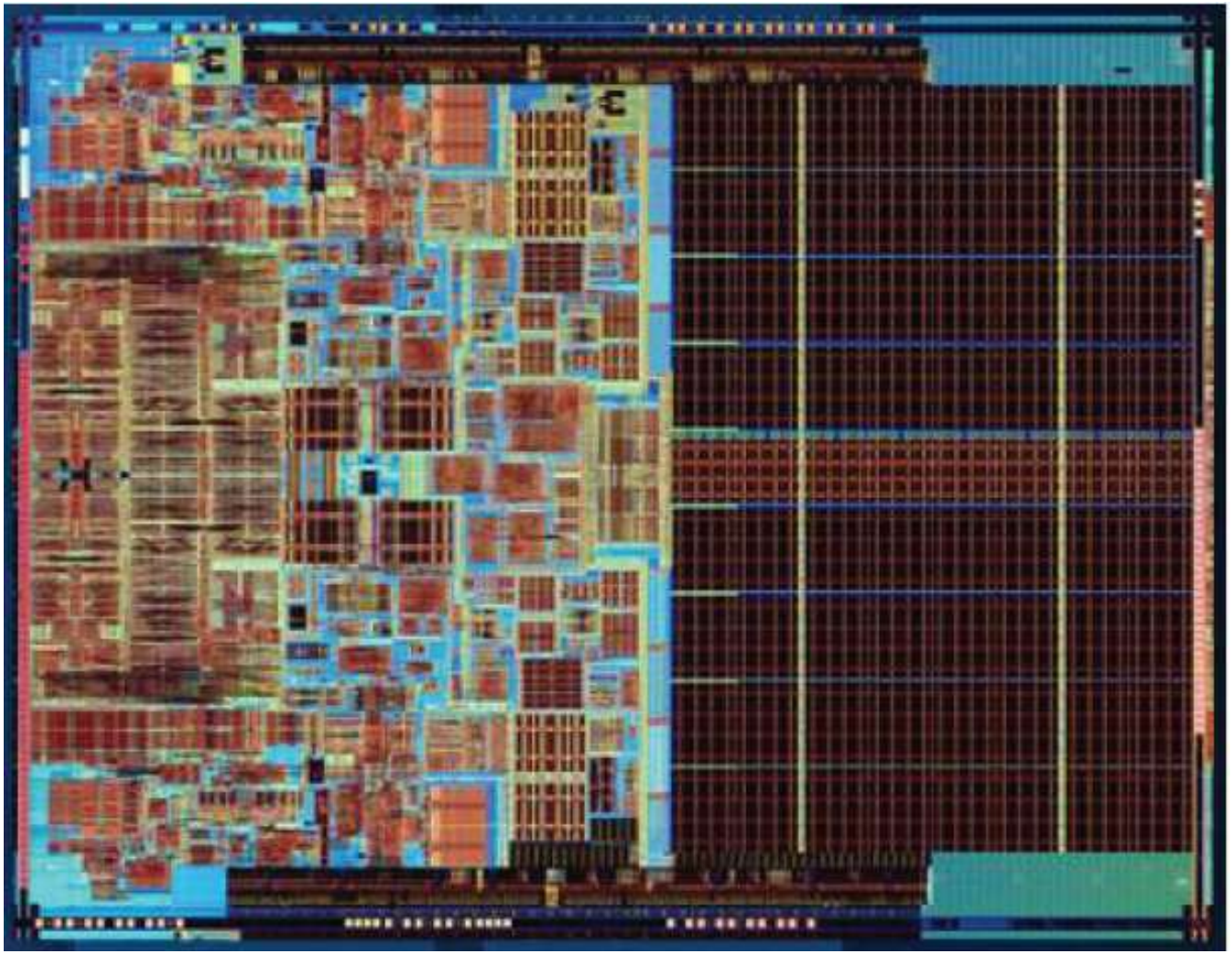
Critical Dimension

$$CD = P_{min} / 2$$
$$= k1 \cdot \lambda / NA$$

- CD is the critical dimension
- Pmin/2 is the minimum half pitch
- k1 is a process factor
- λ is the wavelength of the exposure light
- NA is the numerical aperture of the projection optics.

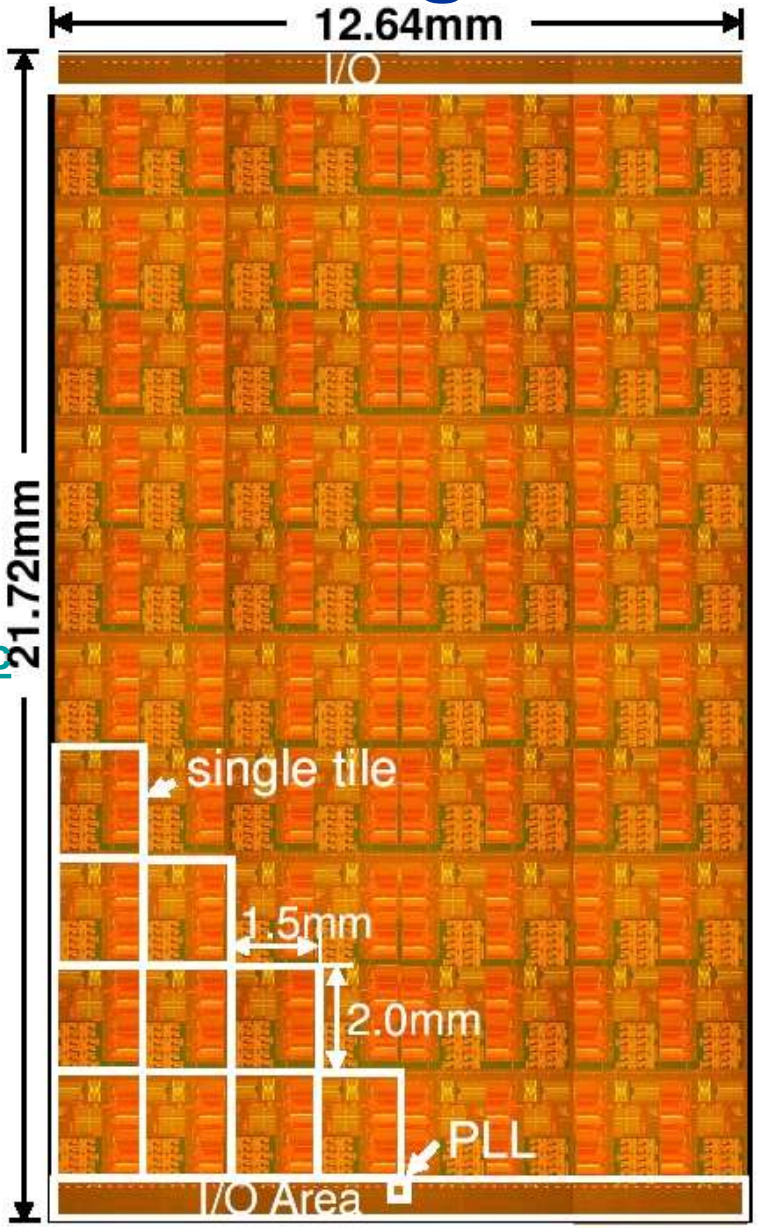


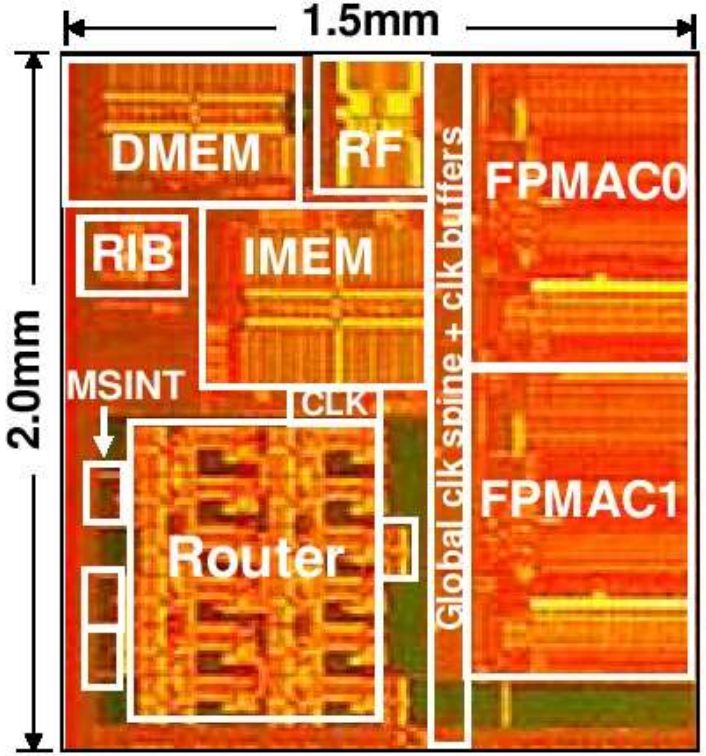
Basic Structure of Computers: Technology Trends (cont.)



Advances in Integration - 2007

- Intel Teraflop Chip 2007
- An 80-core ManyCore processor.
- http://techresearch.intel.com/articles/Tera-Scale/1449.htm

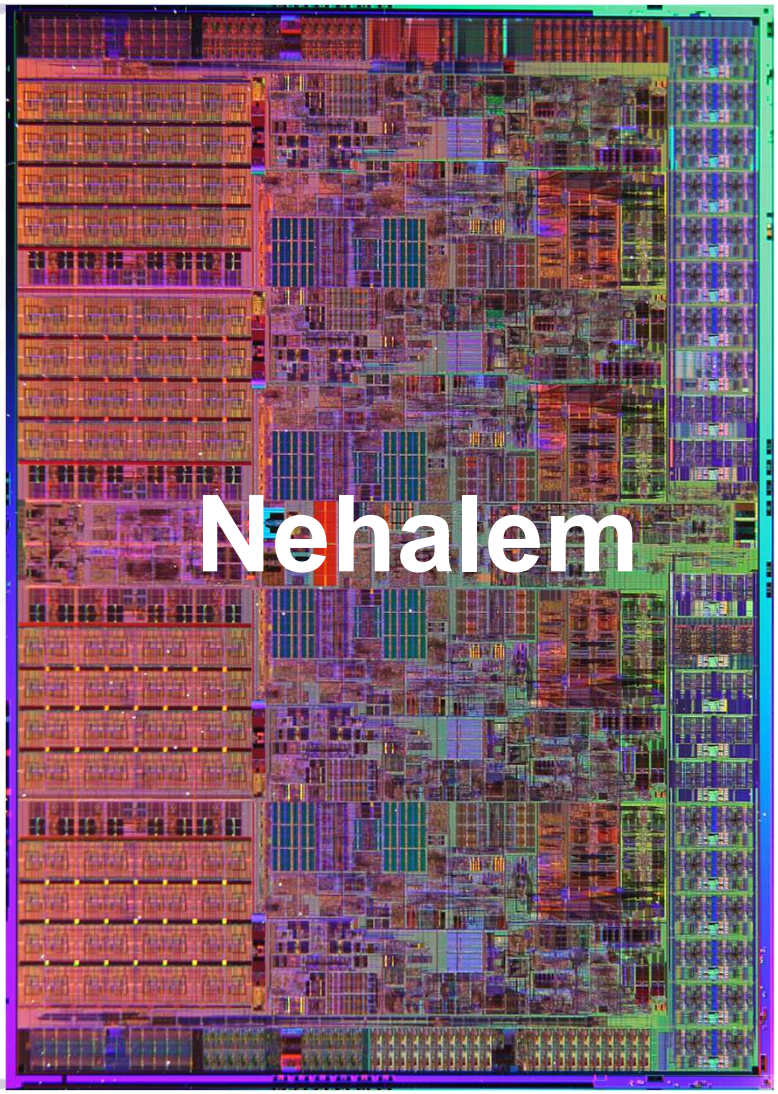




Technology	65nm CMOS Process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 Million
Die Area	275mm^2
Tile area	3mm^2
Package	1248 pin LGA, 14 layers, 343 signal pins

Technology is constantly on the move!

- **Num. of transistors is not limiting factor**
  - Currently ~ 1 billion transistors/chip
  - Problems:
    - Too much Power, Heat, Latency
    - Not enough Parallelism
- **3-dimensional chip technology?**
  - Sandwiches of silicon
  - "Through-Vias" for communication
- **On-chip optical connections?**
  - Power savings for large packets
- **The Intel® Core™ i7 microprocessor ("Nehalem")**
  - 4 cores/chip
  - 45 nm, Hafnium hi-k dielectric
  - 731M Transistors
  - Shared L3 Cache - 8MB
  - L2 Cache - 1MB (256K x 4)

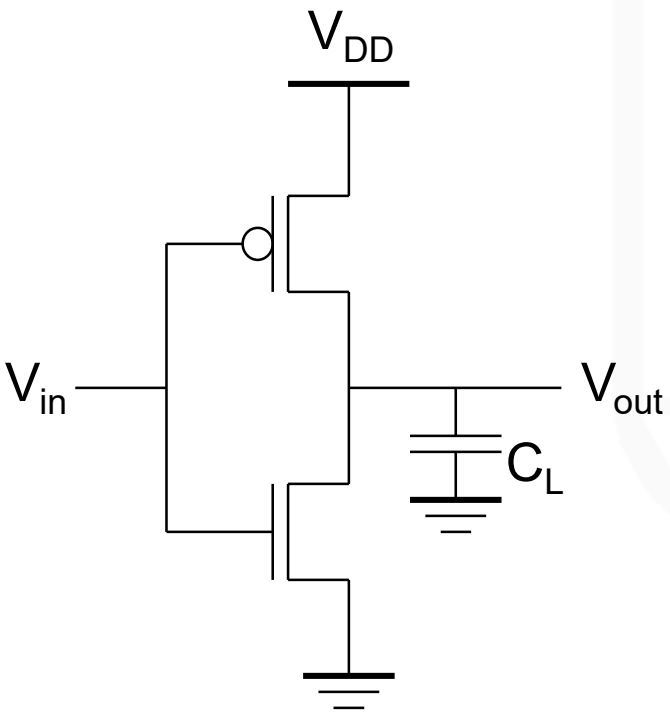


Moore's Law over 10 years $2^{10/1.5} \approx 100$

	Design Element Granularity		Methodology	Architecture
2010	10^8 X	Sub-system	Platform Based Design System Level Synthesis	Networks on a Chip CGRA
2000	10^6 X	IPs	IP Based Design High Level Synthesis.	System on a Chip
1990	10^4 X	Arithmetic Register	RTL / Logic Synthesis	Algorithm on a Chip
1980	10^2 X	Std. Cells	Physical Synthesis	Controller on a Chip
1970	X	Polygons	Manual Design	SSI / MSI

The granularity of reusable objects increases by 100 X every decade
-- Moore's EDA Law

Review: CMOS Inverter

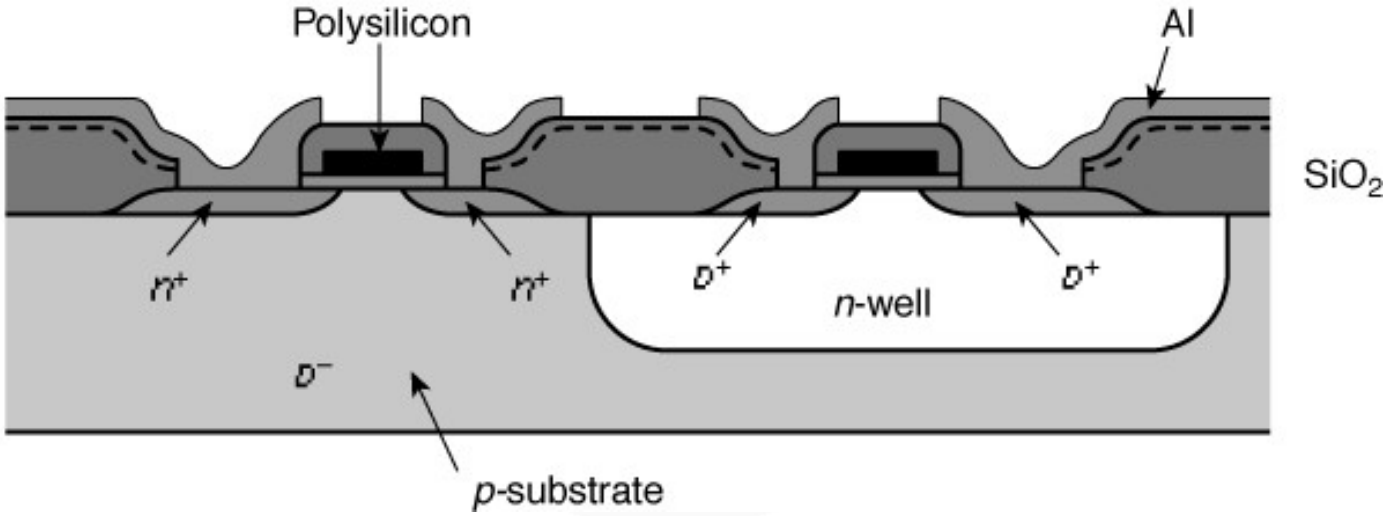


- Full rail-to-rail swing ⇒ high noise margins
- Low output impedance
- High input impedance
- No direct path steady-state between power and ground ⇒ no static power dissipation
- Propagation delay a function of load capacitance and on resistance of transistors

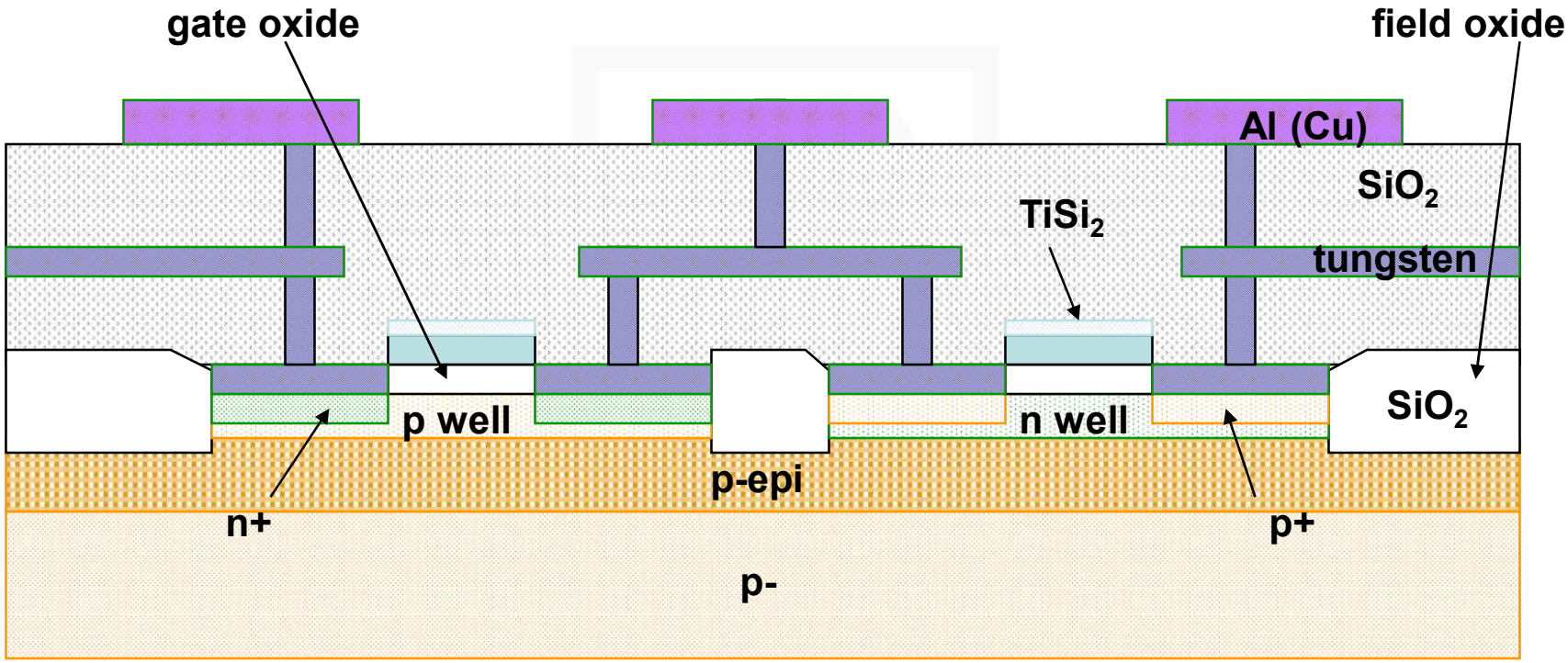
CMOS Properties

- **Full rail-to-rail swing ⇒ high noise margins**
  - Logic levels not dependent upon the relative device sizes ⇒ transistors can be minimum size ⇒ ratioless
- **Always a path to V_{dd} or GND in steady state ⇒ low output impedance (output resistance in kΩ range) ⇒ large fan-out (albeit with degraded performance)**
- **Extremely high input resistance (gate of MOS transistor is near perfect insulator) ⇒ nearly zero steady-state input current**
- **No direct path steady-state between power and ground ⇒ no static power dissipation**
- **Propagation delay function of load capacitance and resistance of transistors.**

Inverter in CMOS Process

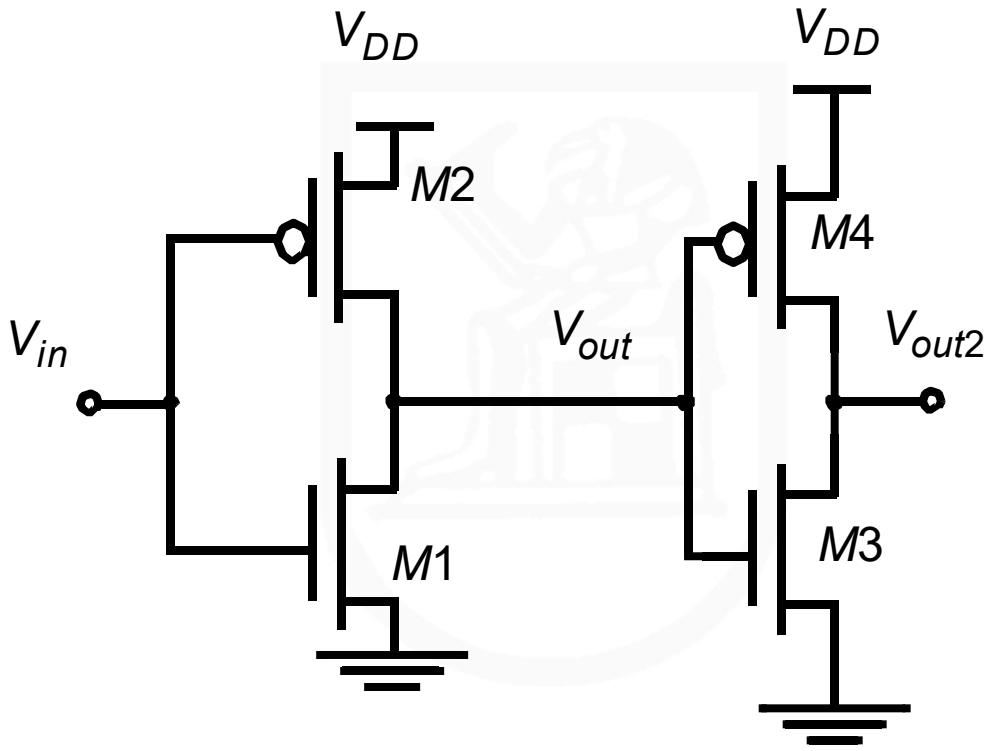


A Modern CMOS Process

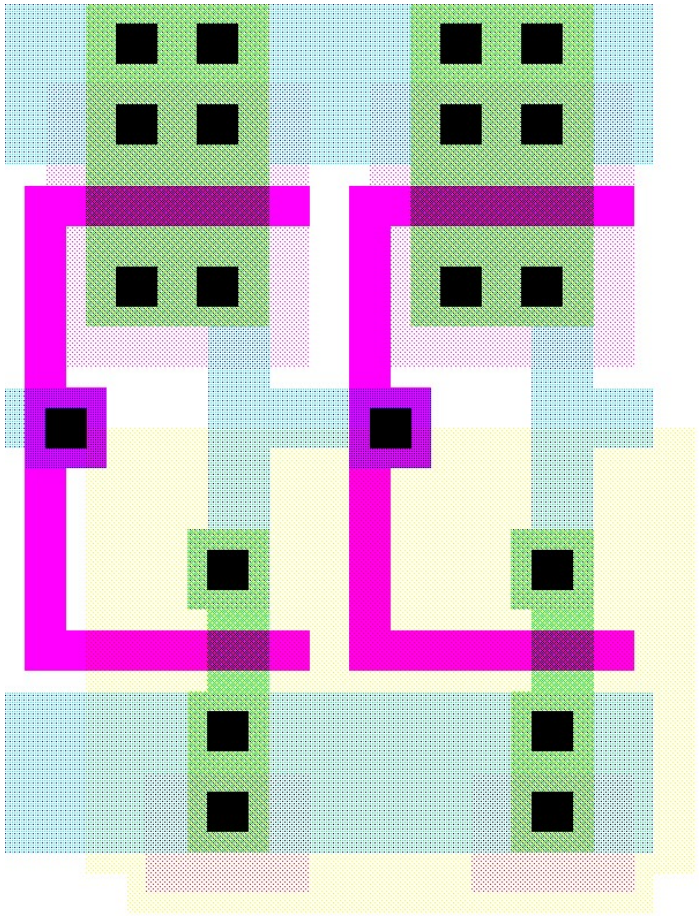


Dual-Well Trench-Isolated CMOS

Review: CMOS Buffer

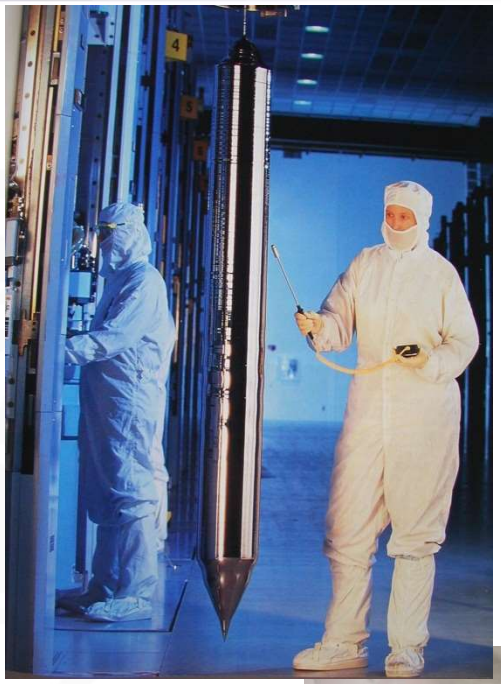


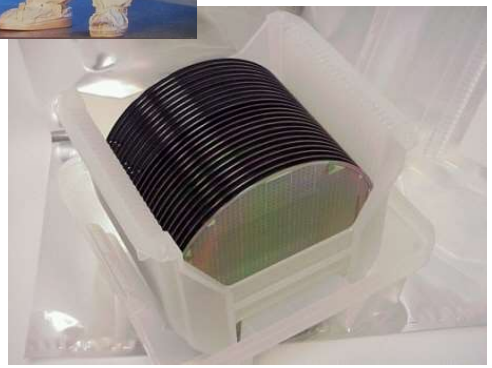
Its Layout View



Growing the Silicon Ingot

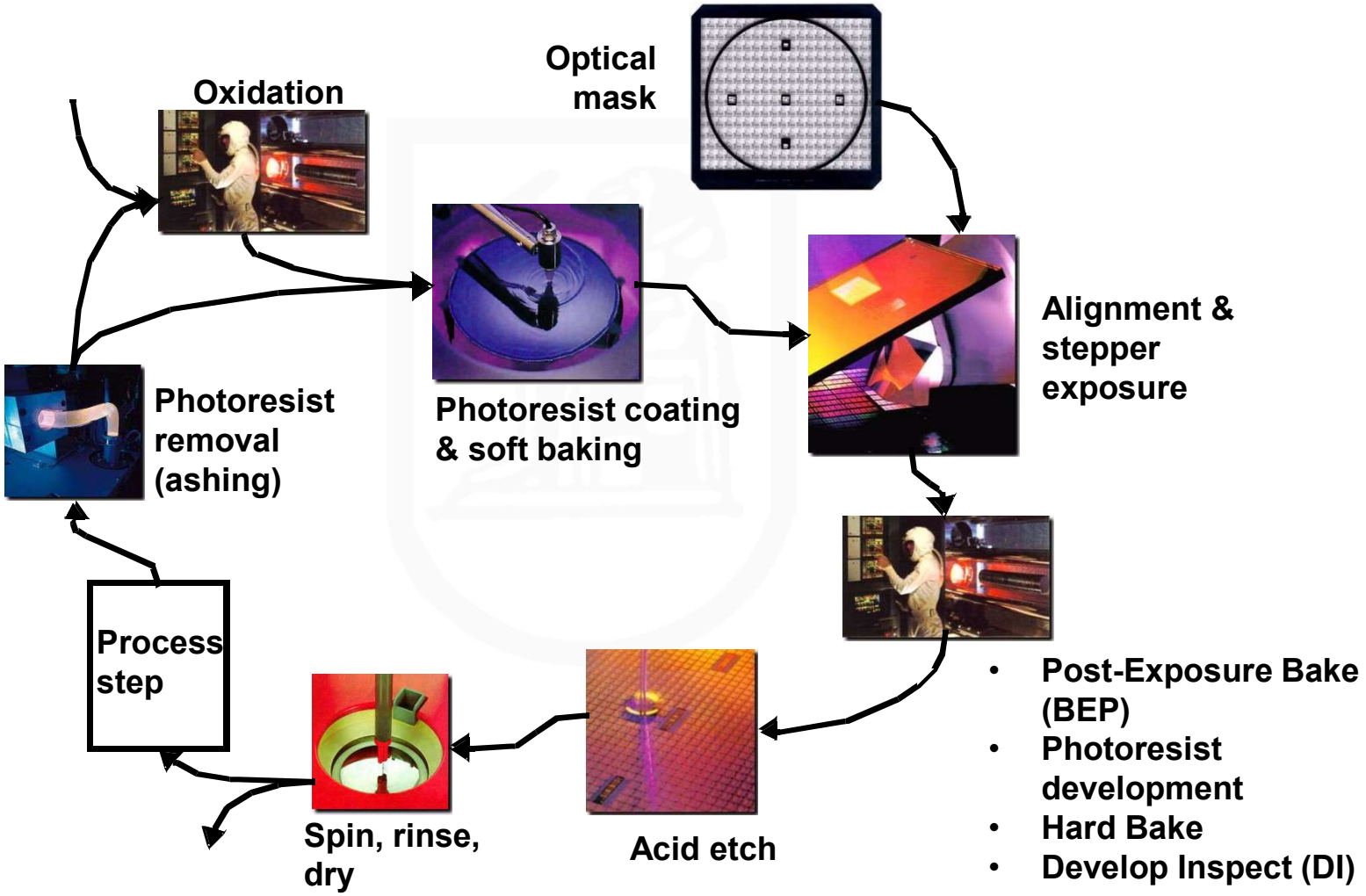
- Start with clean sand, melt into liquid
- Grown as a high purity crystal: “boule”
- Sliced into wafers which are polished
- Notch or flat indicates crystal orientation
- 200 mm $30-$100/wafer
- 300 mm $50-$300/wafer





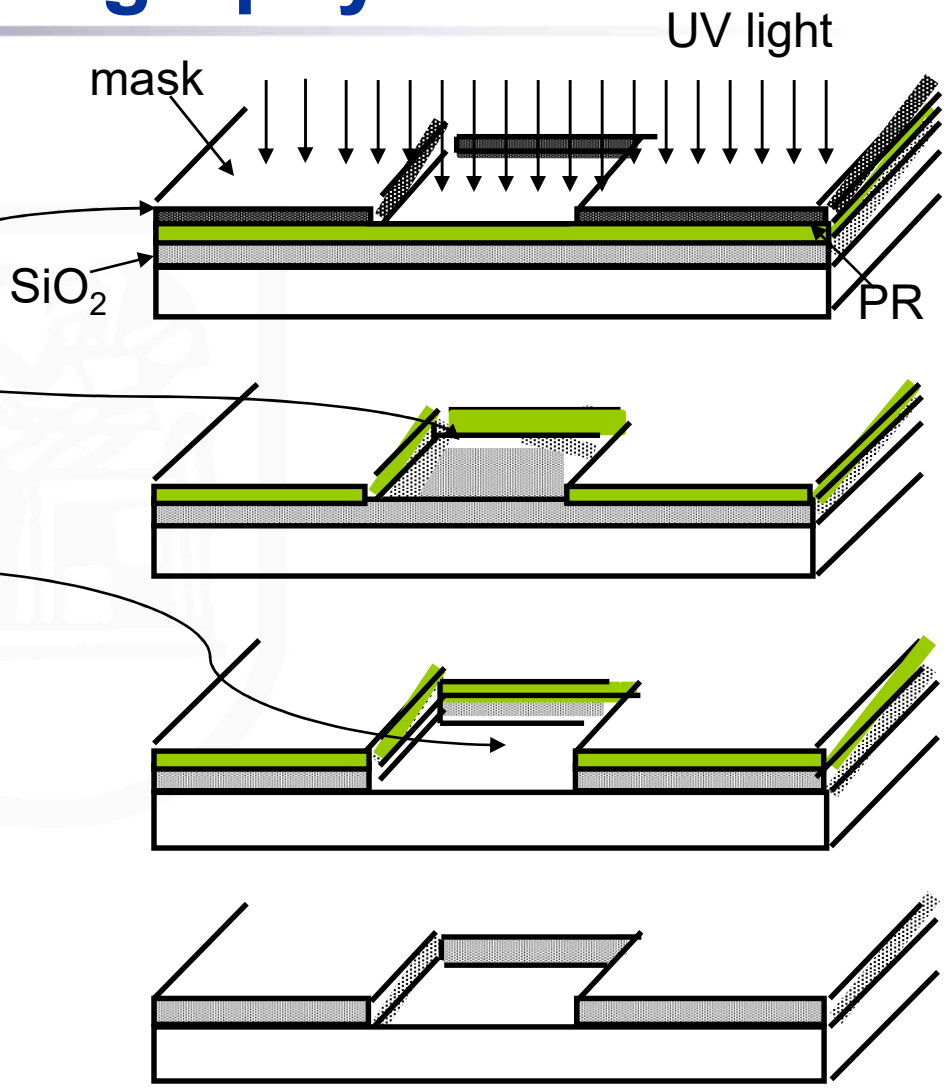
From *Smithsonian*, 2000

Photolithographic Process

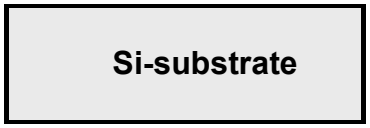


Patterning - Photolithography

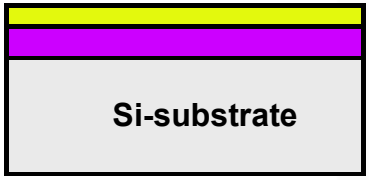
1. **Oxidation**
2. **Photoresist (PR) coating**
3. **Stepper exposure**
4. **Photoresist development and bake**
5. **Acid etching**
   - Unexposed (negative PR)
   - Exposed (positive PR)
6. **Spin, rinse, and dry**
7. **Processing step**
   - Ion implantation
   - Plasma etching
   - Metal deposition
8. **Photoresist removal (ashing)**



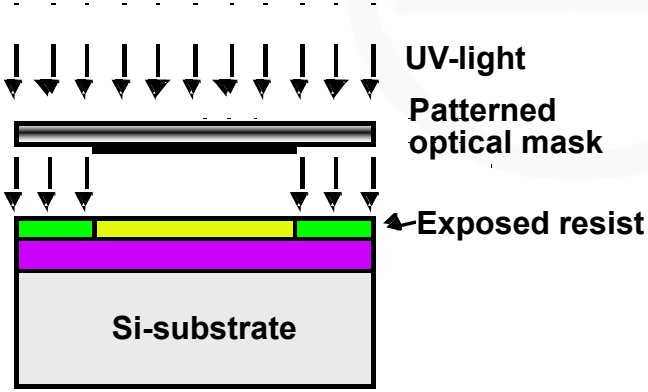
Example of Patterning of SiO2



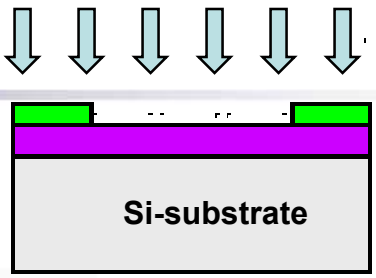
Silicon base material



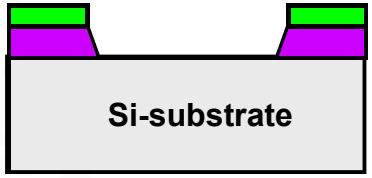
1&2. After oxidation and deposition of negative photoresist



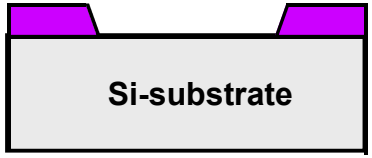
3. Stepper exposure



4. After development and etching of resist, chemical or plasma etch of SiO_2



5. After etching



8. Final result after removal of resist

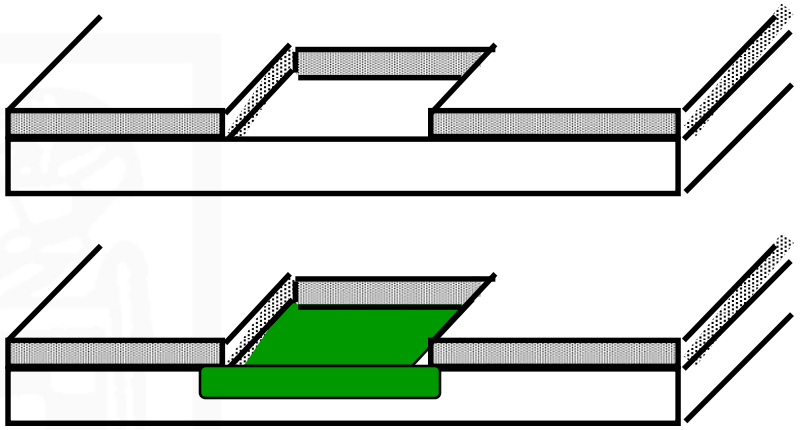
Diffusion and Ion Implantation

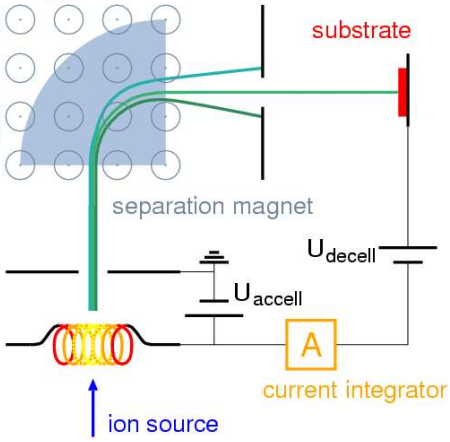
1. **Area to be doped is exposed (photolithography)**

2. **Diffusion**

   or

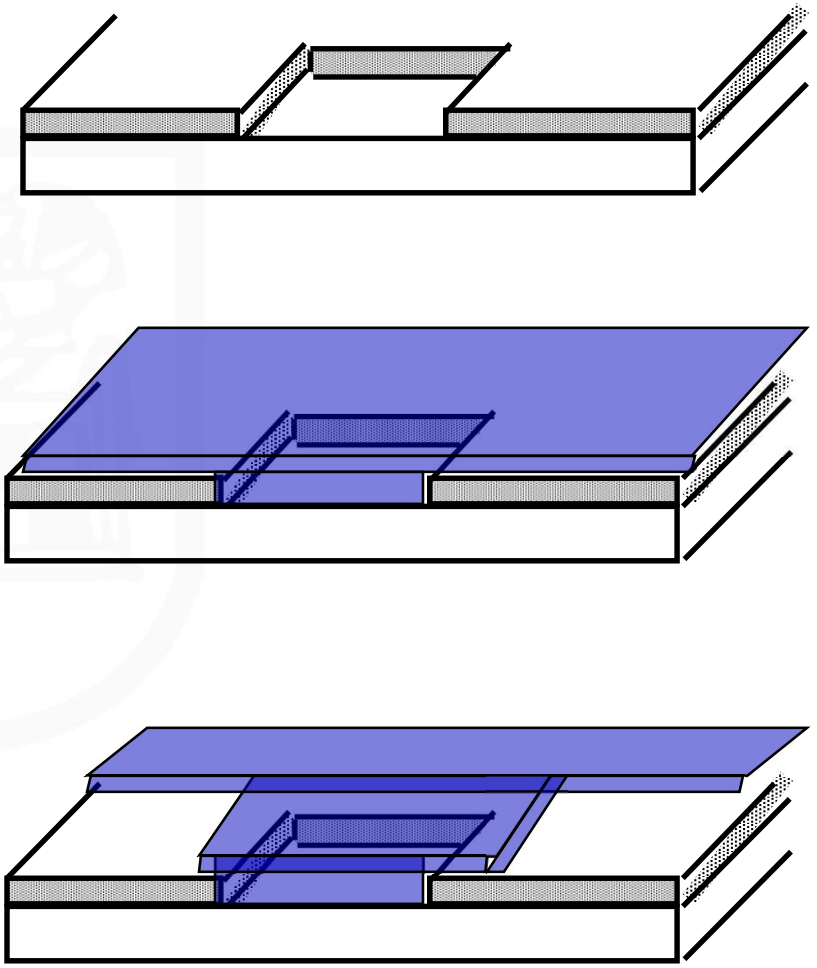
   Ion implantation





Deposition and Etching

1. **Pattern masking (photolithography)**
2. **Deposit material over entire wafer**
   - CVD (Si_3N_4)
   - chemical deposition (polysilicon)
   - sputtering (Al)
3. **Etch away unwanted material**
   - wet etching
   - dry (plasma) etching



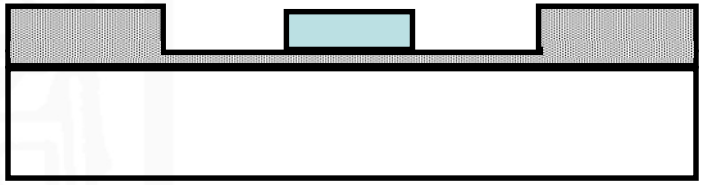
Planarization: Wafer Polishing

From *Smithsonian*, 2000

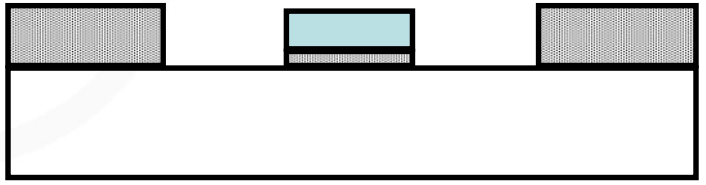
Self-Aligned Gates

1. Create thin oxide in the "active" regions, thick elsewhere

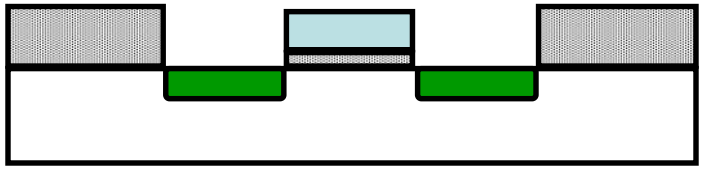
2. Deposit polysilicon



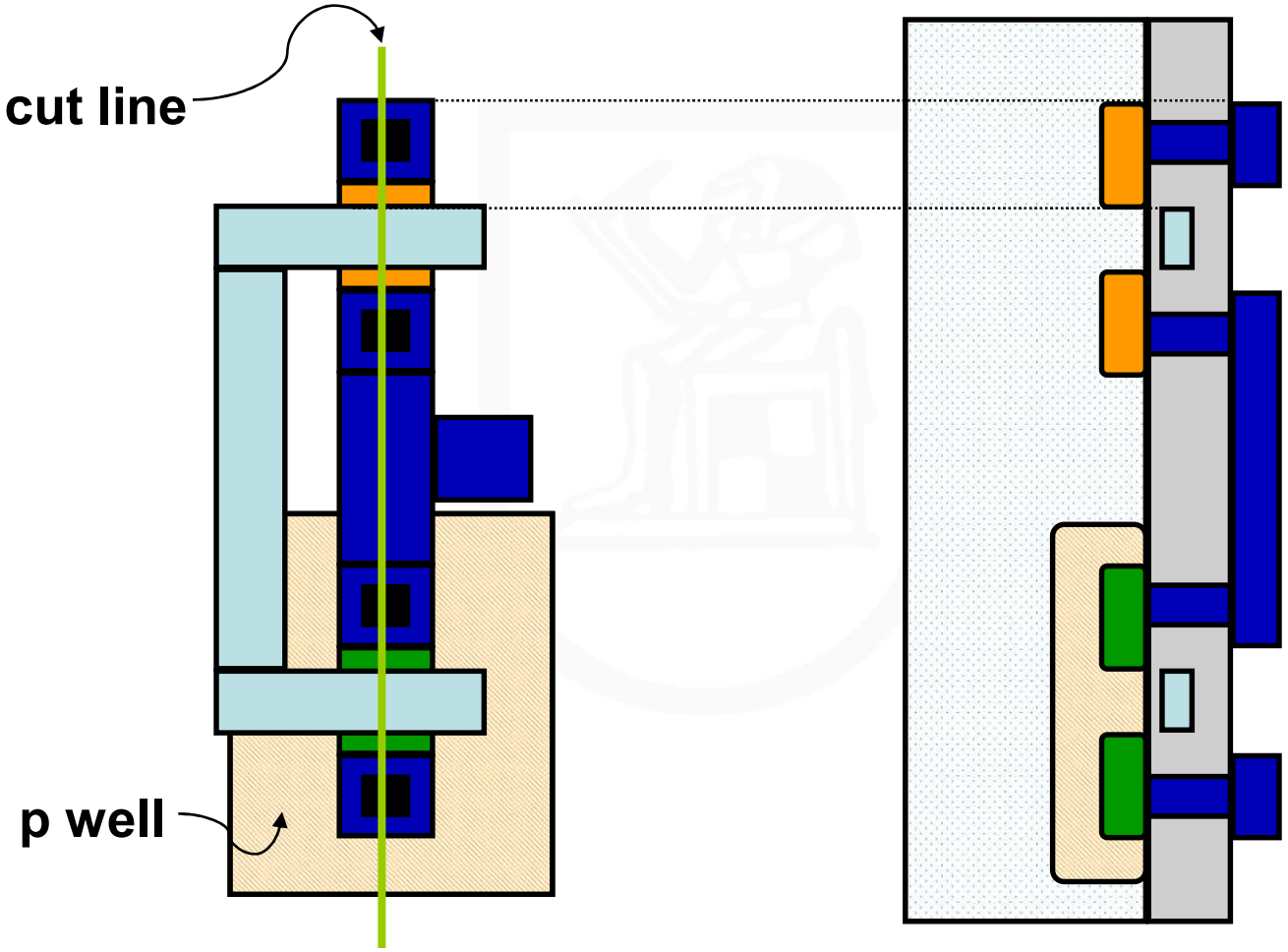
3. Etch thin oxide from active region (poly acts as a mask for the diffusion)



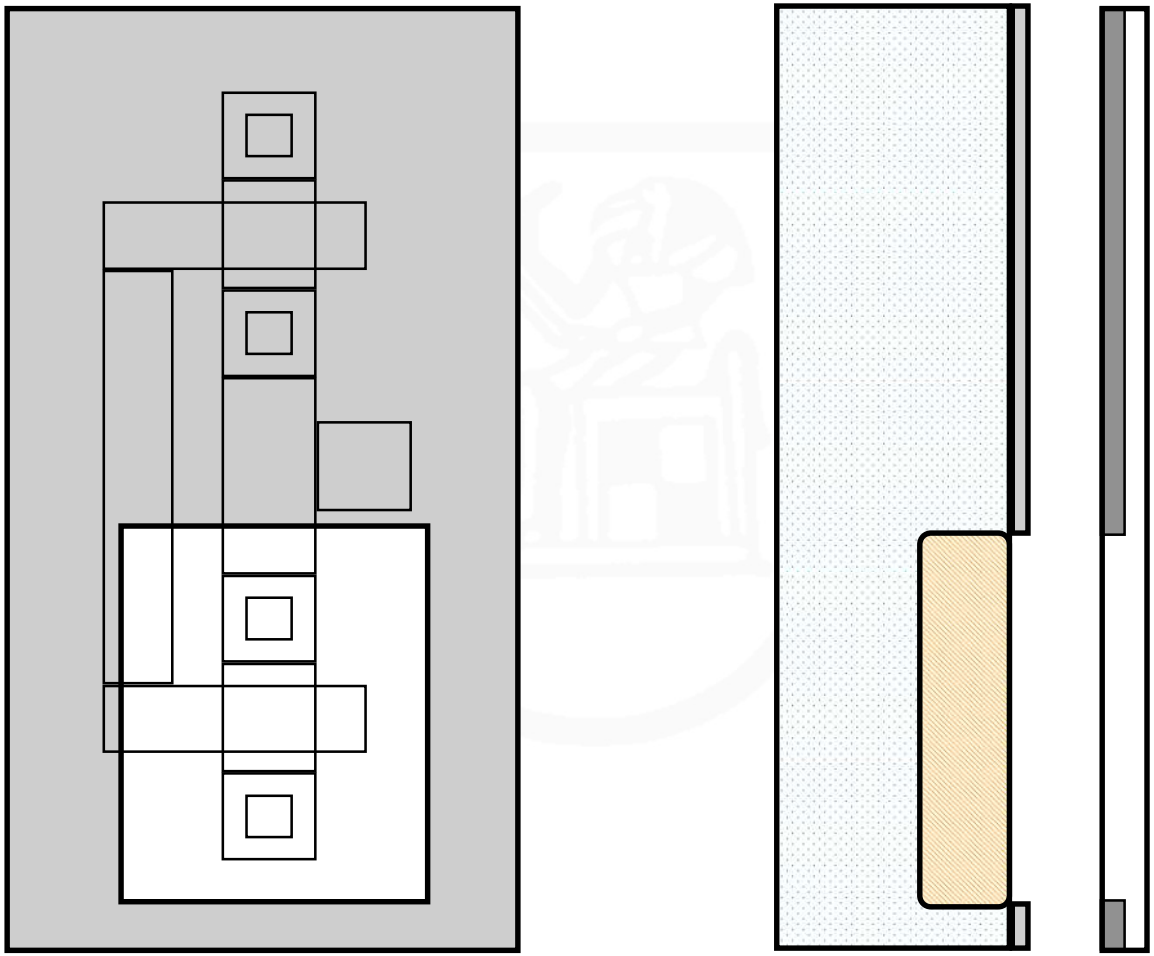
4. Implant dopant



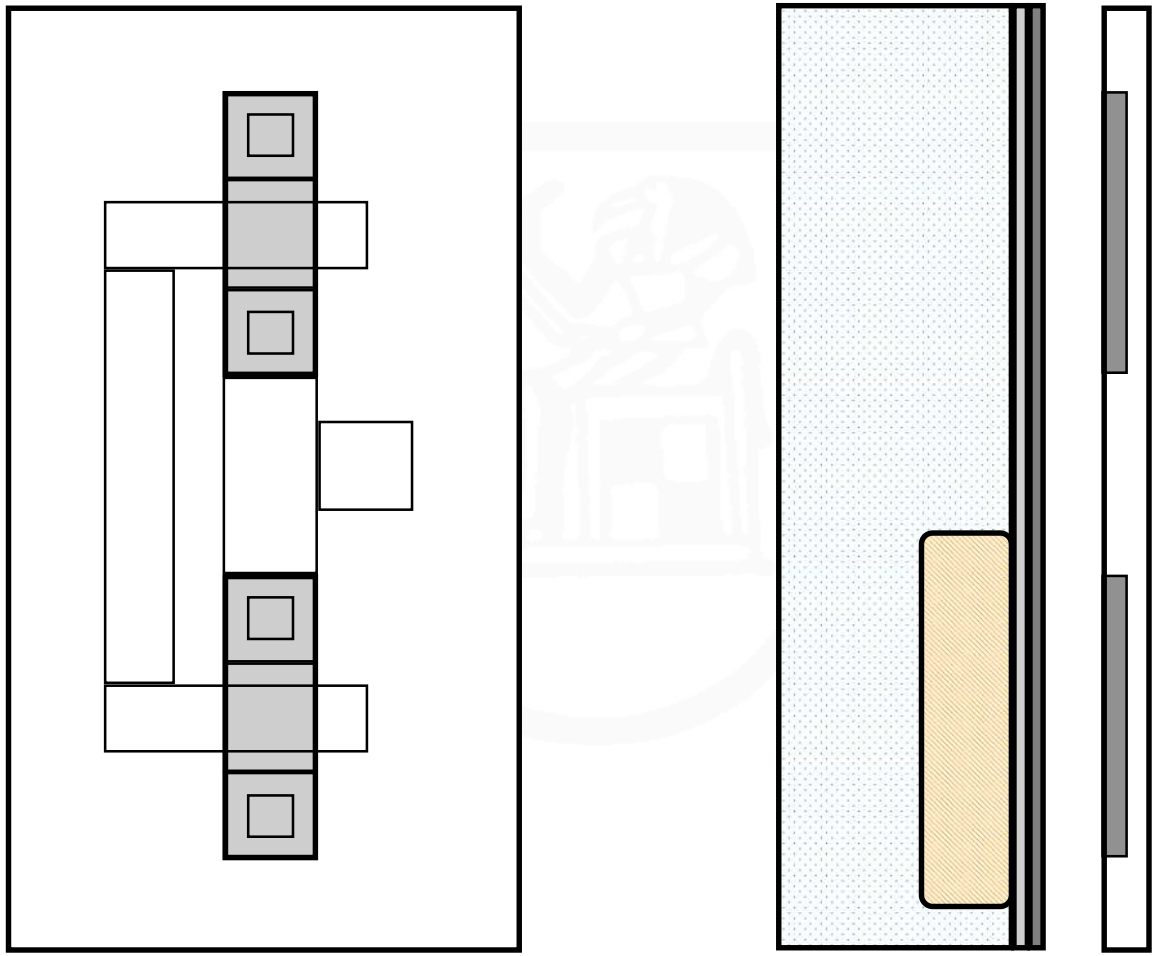
Simplified CMOS Inverter Process



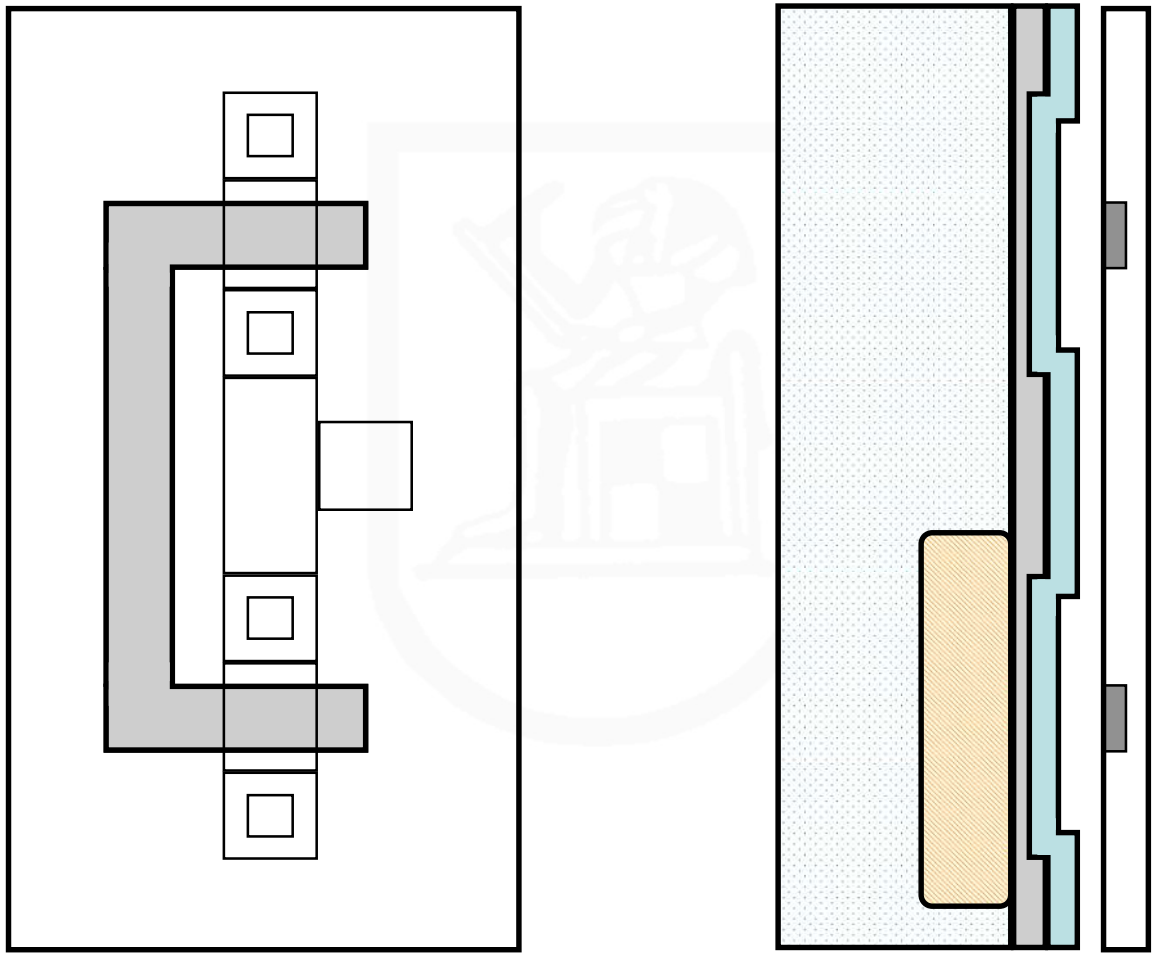
P-Well Mask



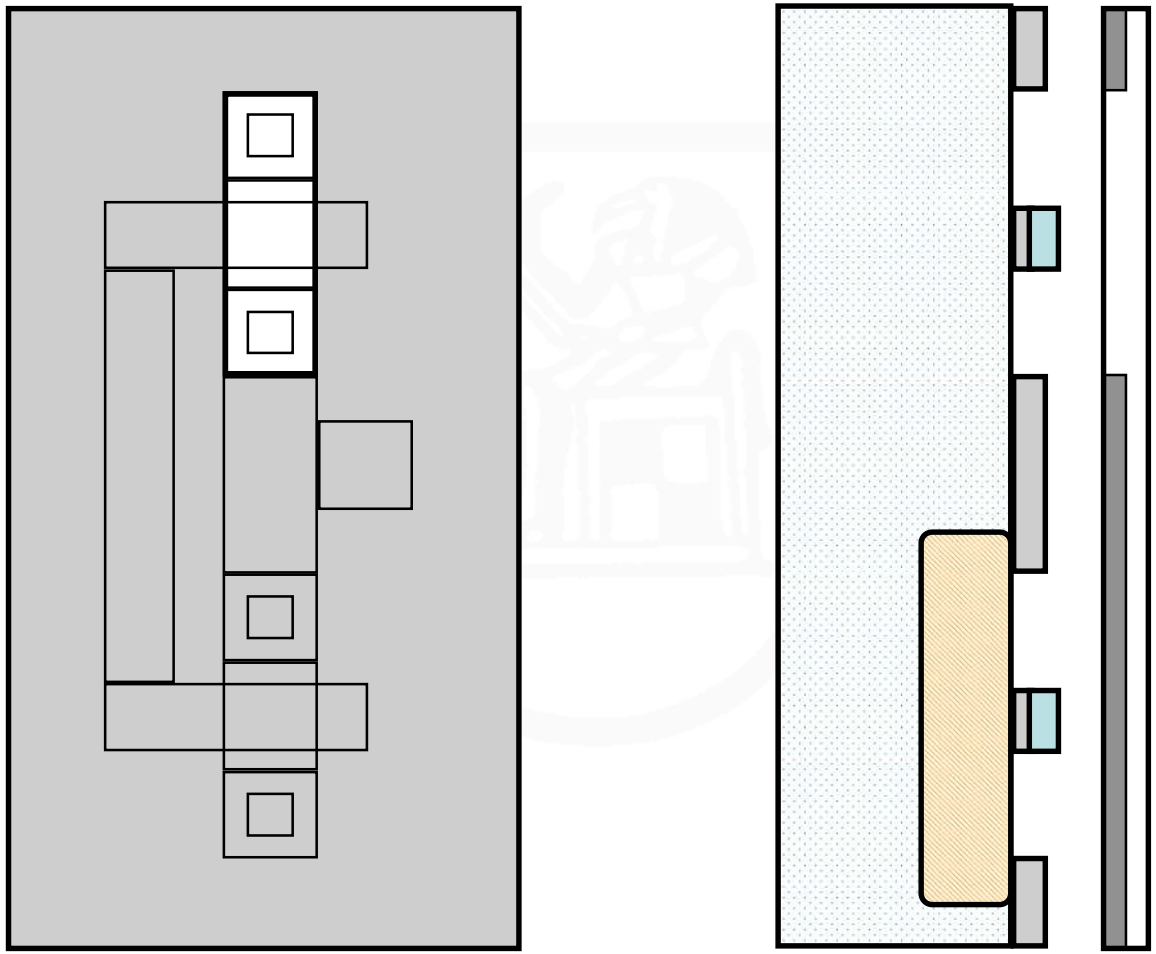
Active Mask



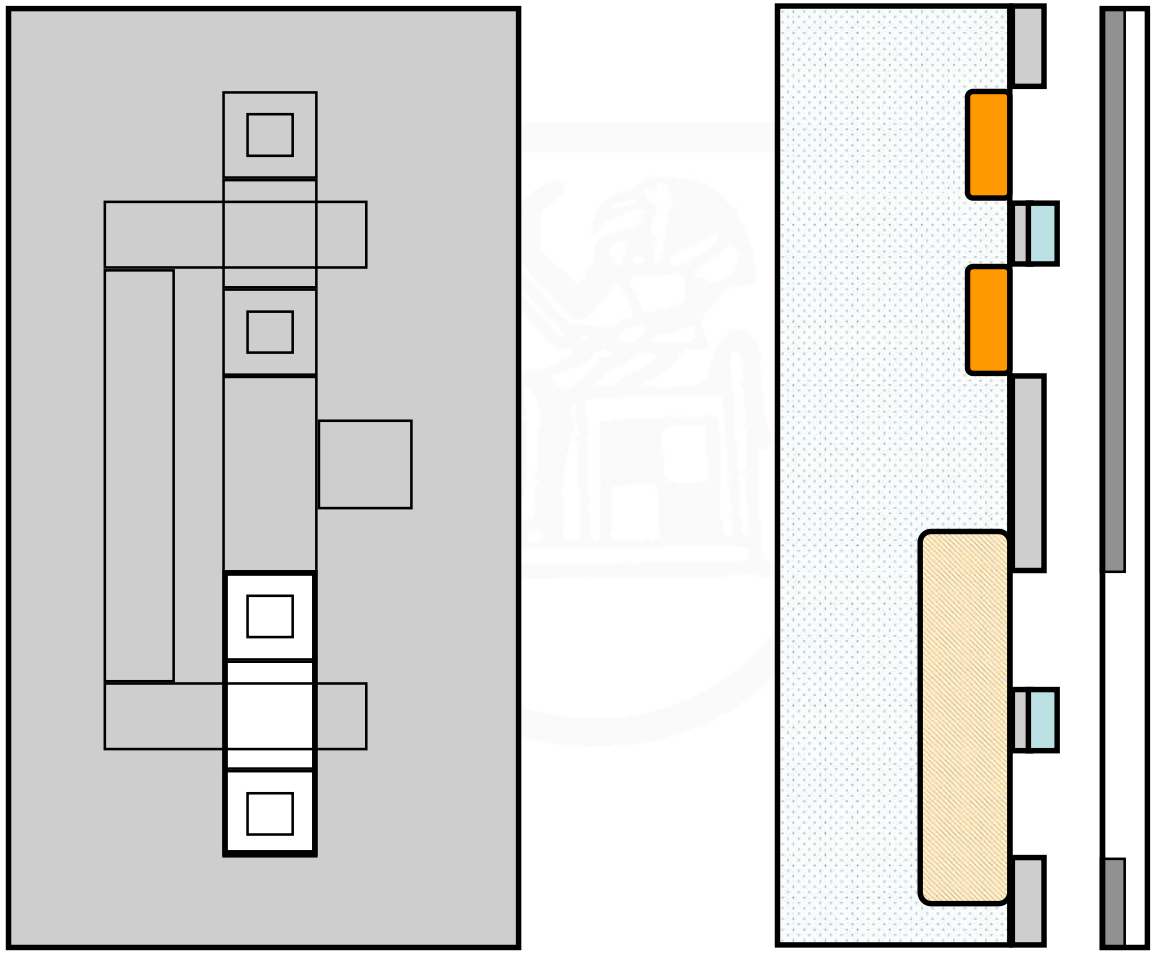
Poly Mask



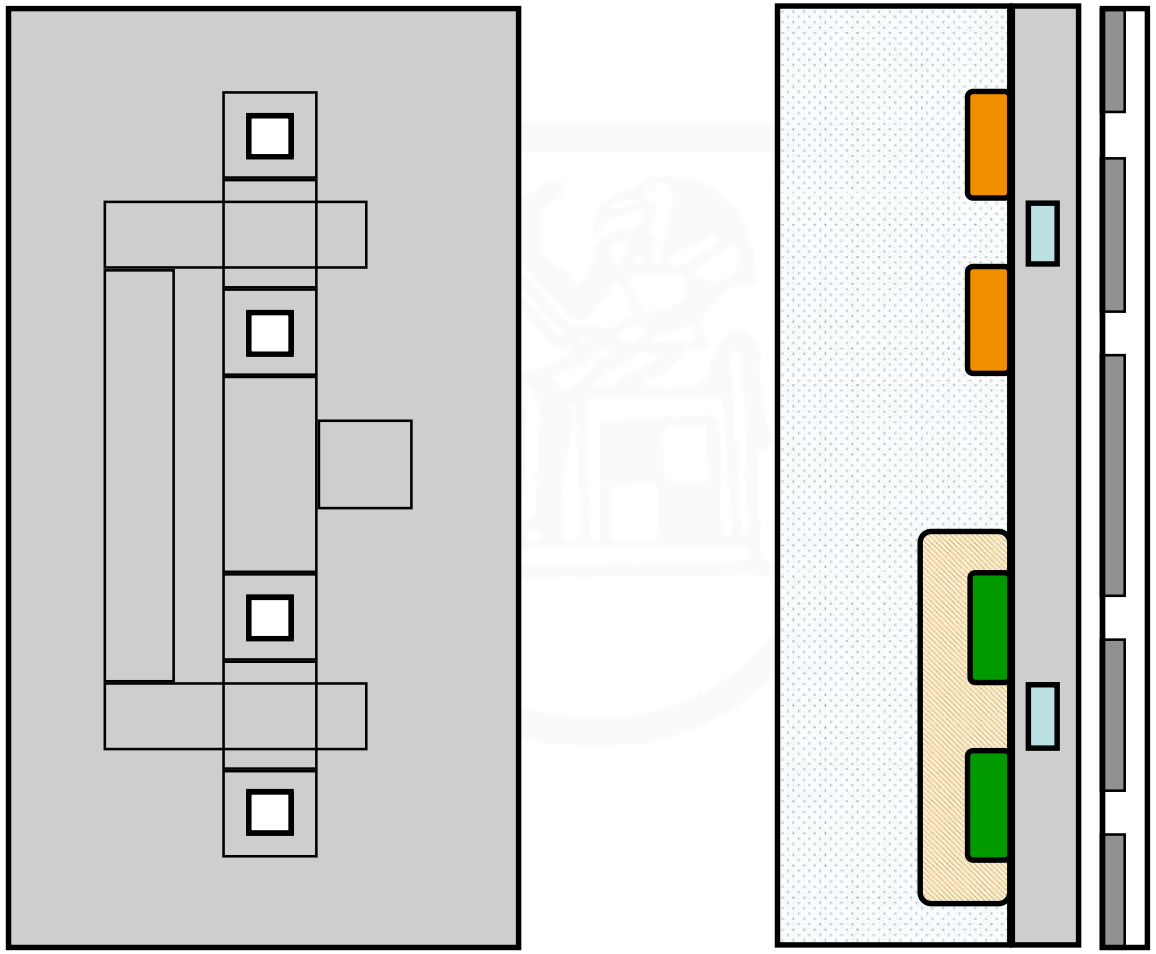
P+ Select Mask



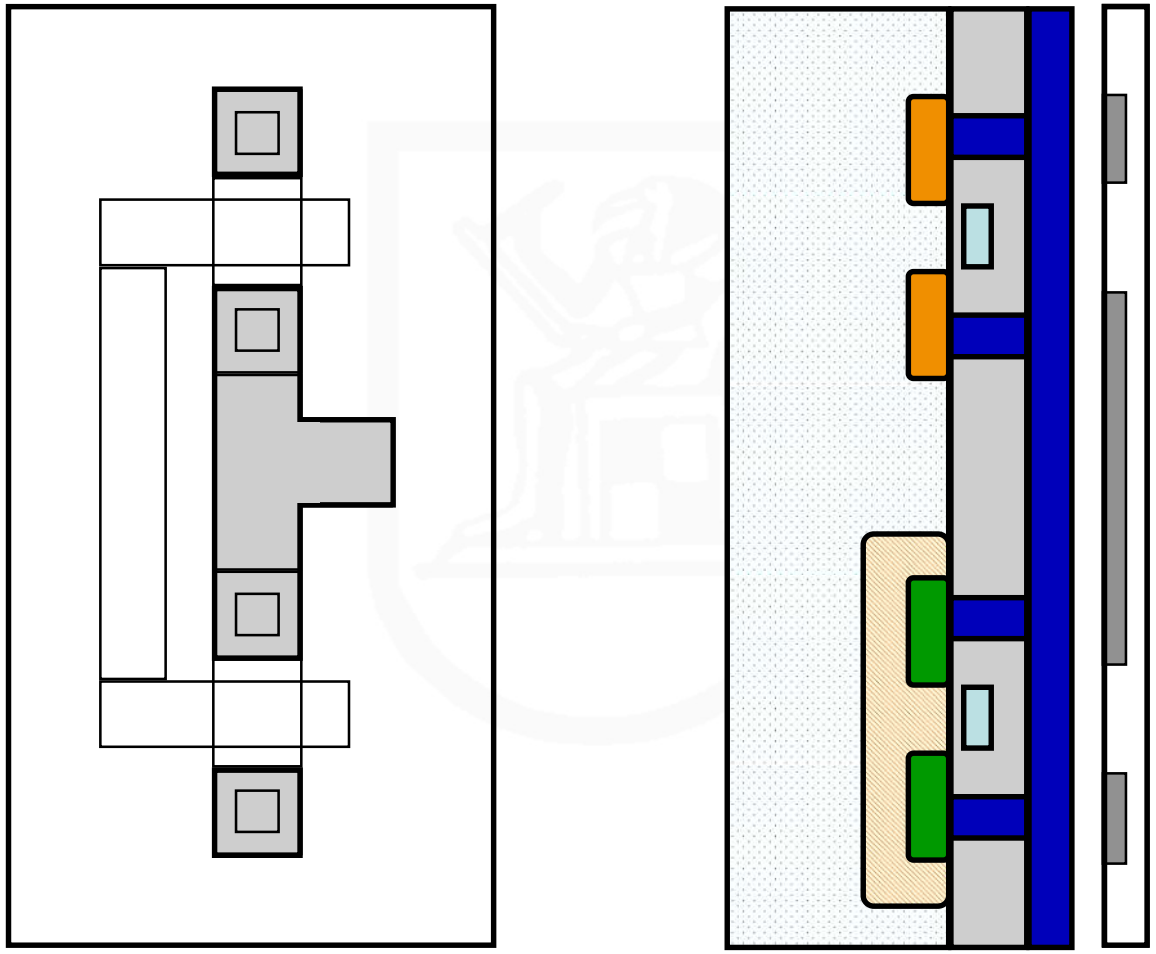
N+ Select Mask



Contact Mask



Metal Mask

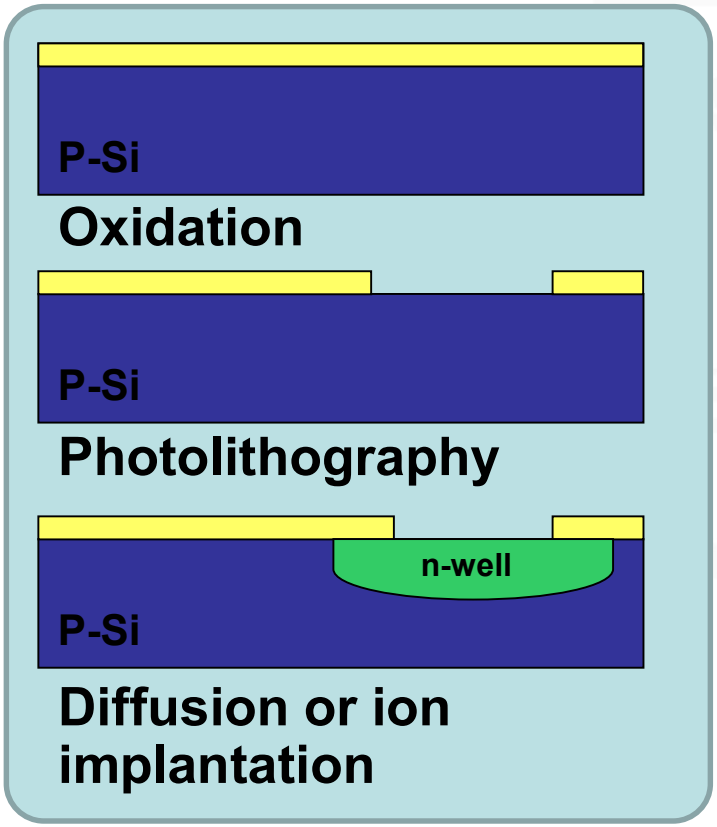


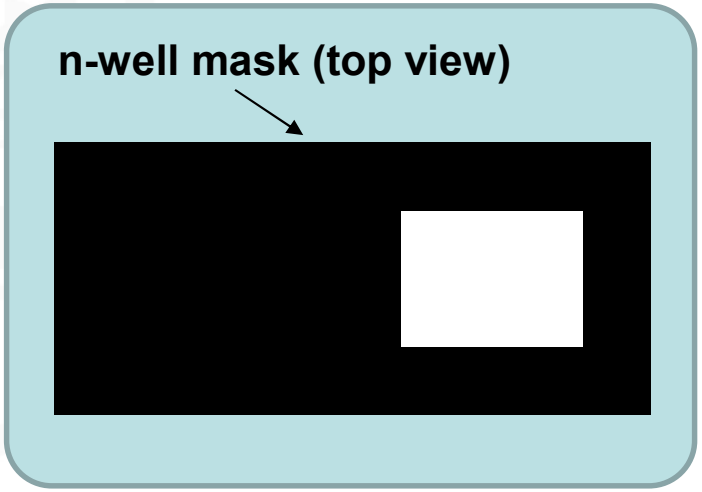
Building a Tool

- **Videos 6**

Mask Example (1)

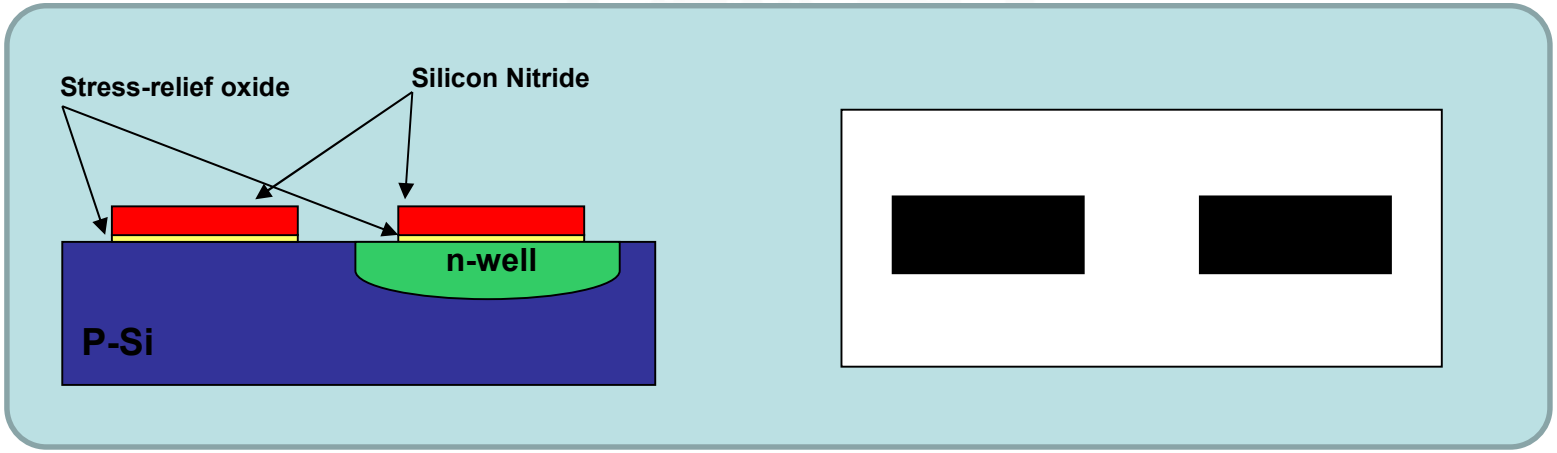
N-well Process mask





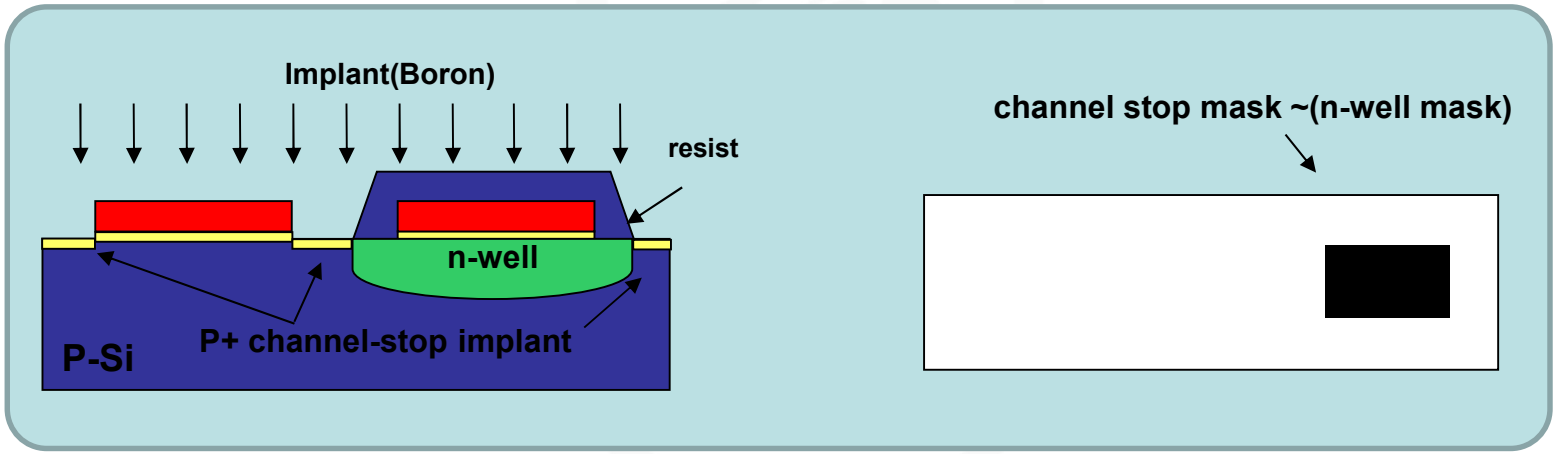
CMOS Fabrication Sequence (2)

- **Active area definition**
  - active area is a planar section of the surface
  - defines transistors regions
  - defines the n+ and p+ regions
  - defines the gate region



CMOS Fabrication Sequence (3)

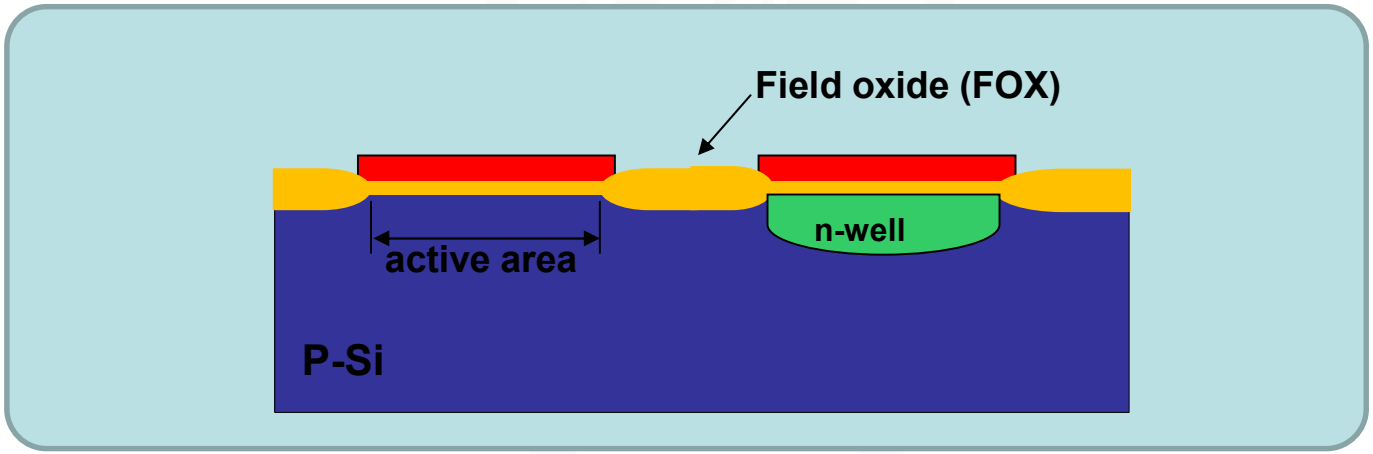
Channel-stop implant



Ion implantation

CMOS Fabrication Sequence (4)

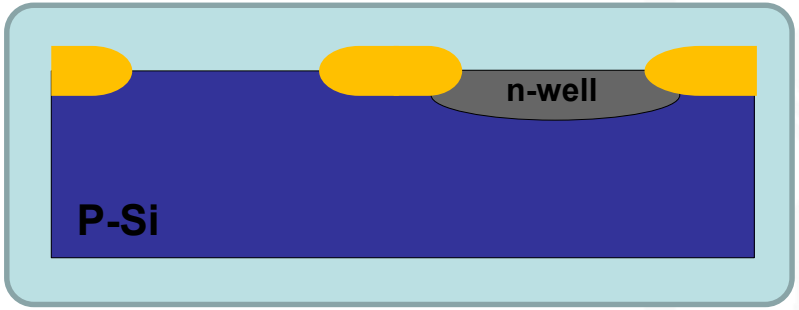
LOCOS (Local oxidation of silicon)



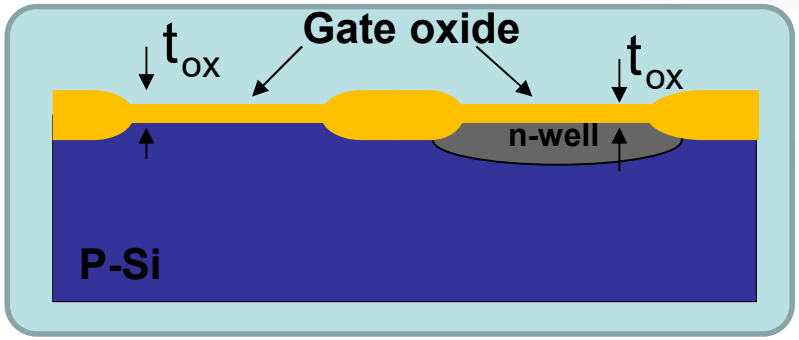
Field oxide formation

CMOS Fabrication Sequence (5)

Thin Gate Oxide Growth



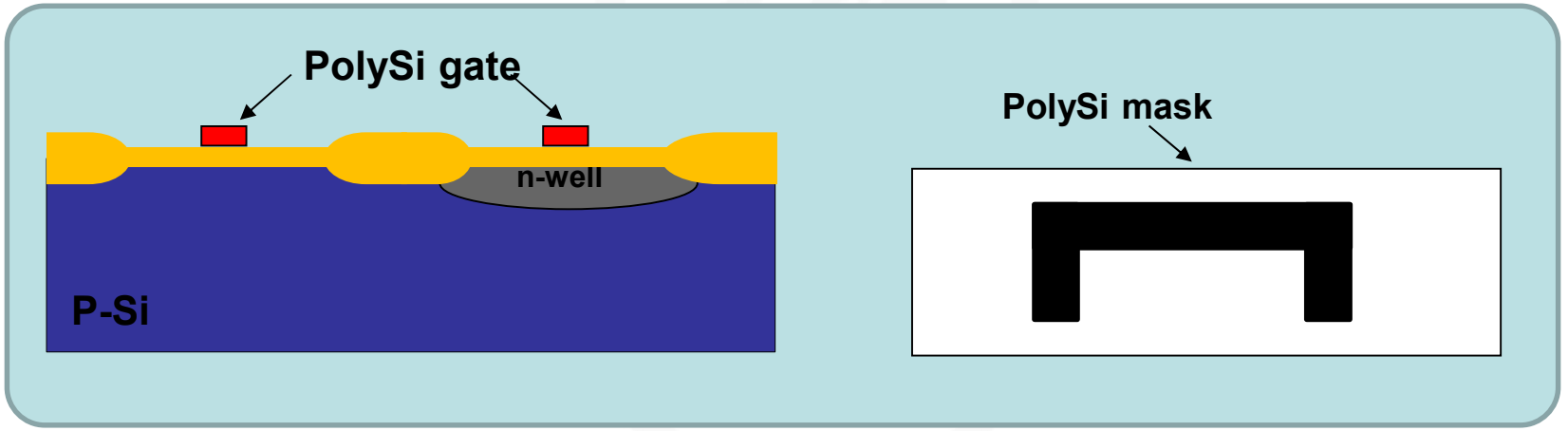
- The nitride and stress-relief oxide is removed.
- The threshold voltage is adjusted by ion implantation.



- Gate oxide growth, t_{ox} =50…2nm
- Thermal oxidation

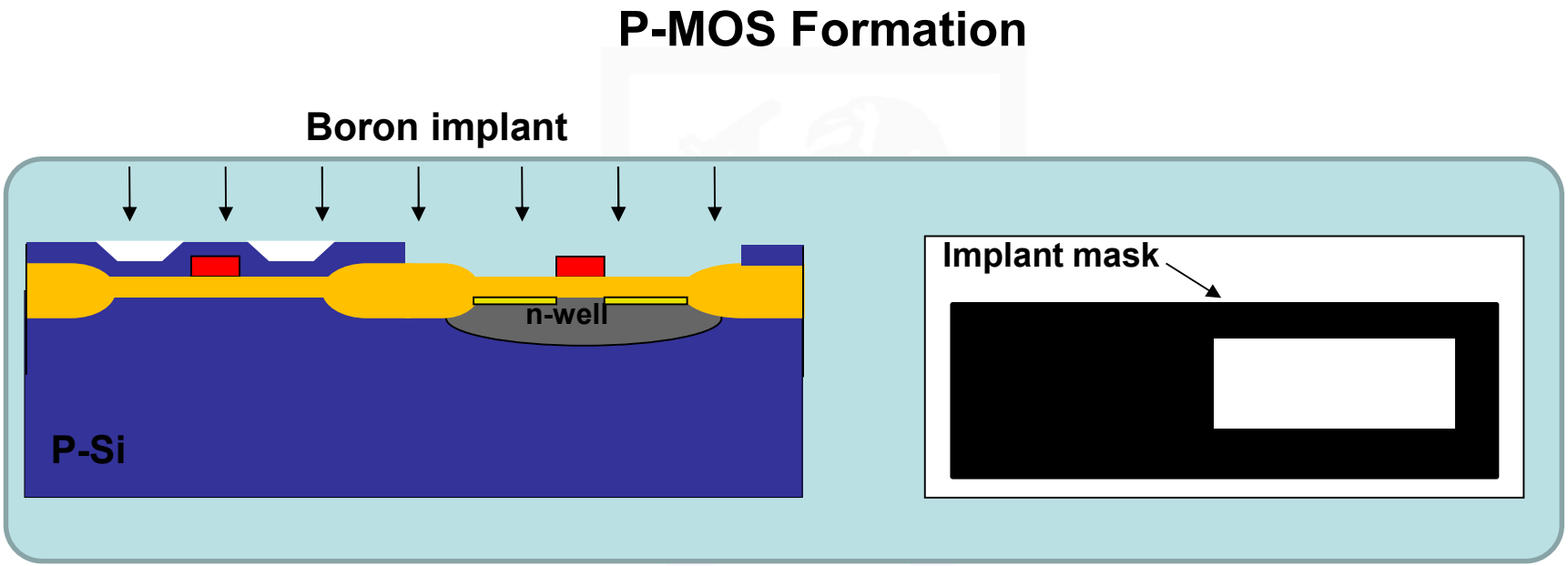
CMOS Fabrication Sequence (6)

Polysilicon deposition and photolithography



All the gates are formed and doped (n+) by CVD technique in the single step.

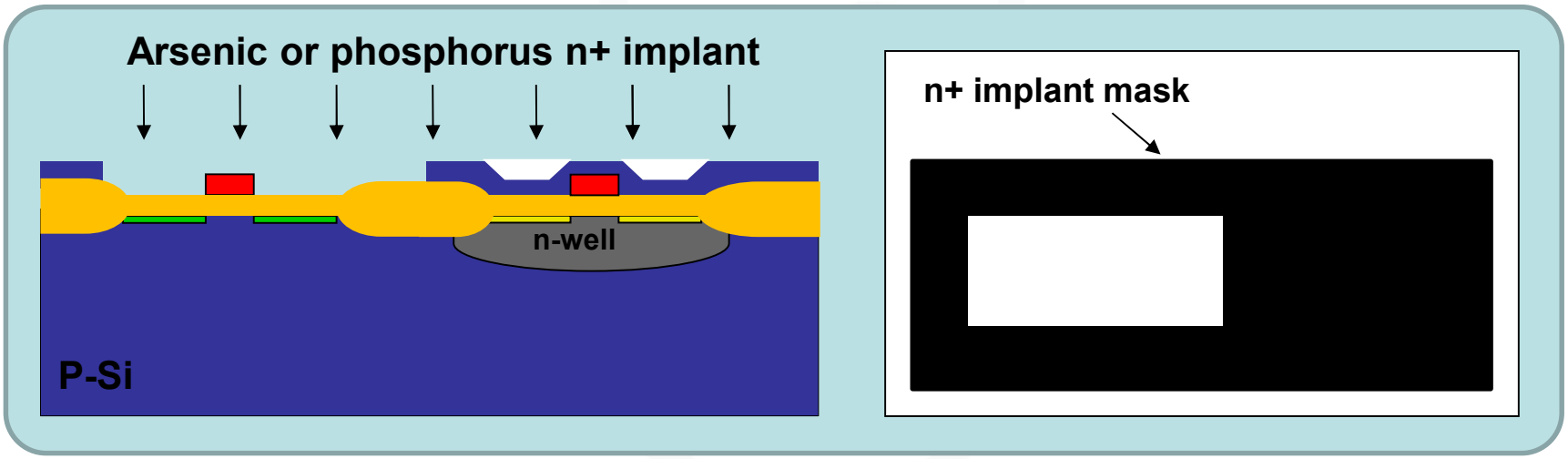
CMOS Fabrication Sequence (7)



Photolithography and boron ion implantation – Self aligned process

CMOS Fabrication Sequence (8)

N-MOS Formation

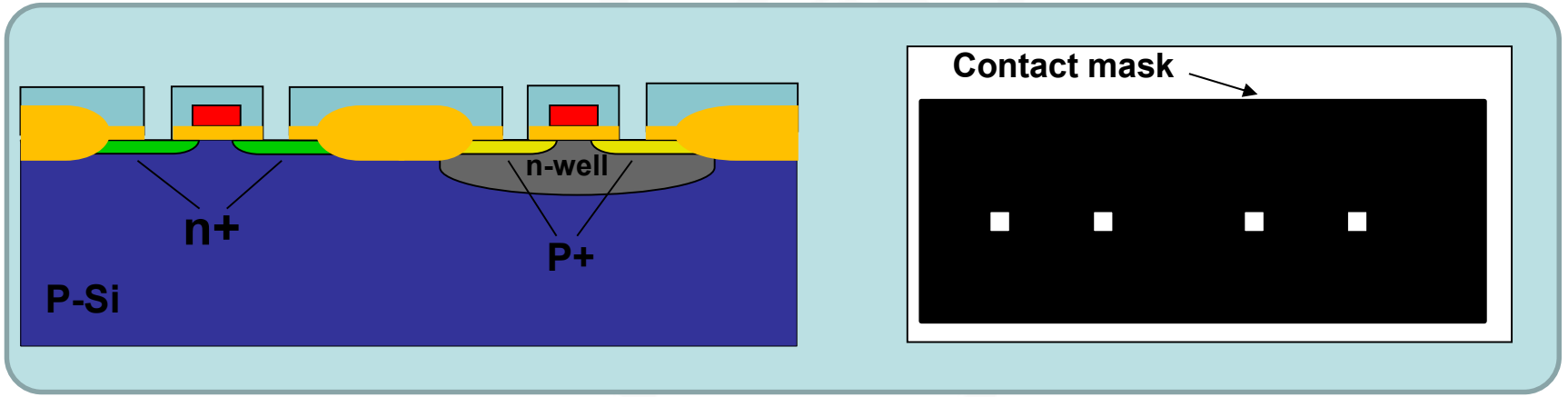


Photolithography and ion implantation – Self aligned process (n+ doped gate)

Thermal annealing cycle is performed.

CMOS Fabrication Sequence (9)

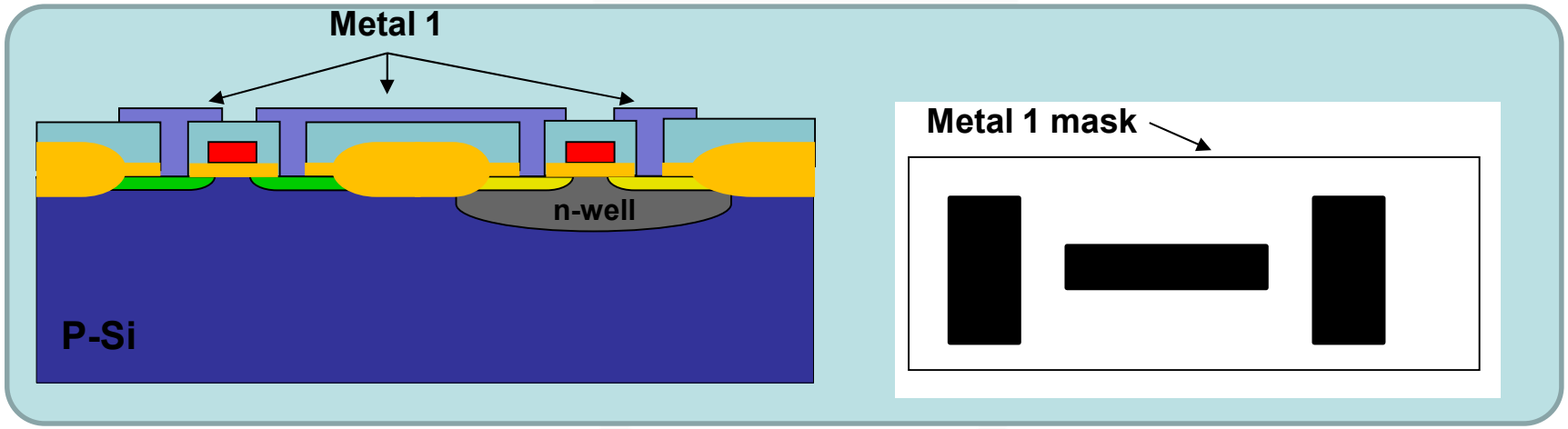
Contact cut formation



- **Oxide deposition by low temperature CVD process.**
- **Photolithography and SiO_2 etching.**

CMOS Fabrication Sequence (10)

Contact formation



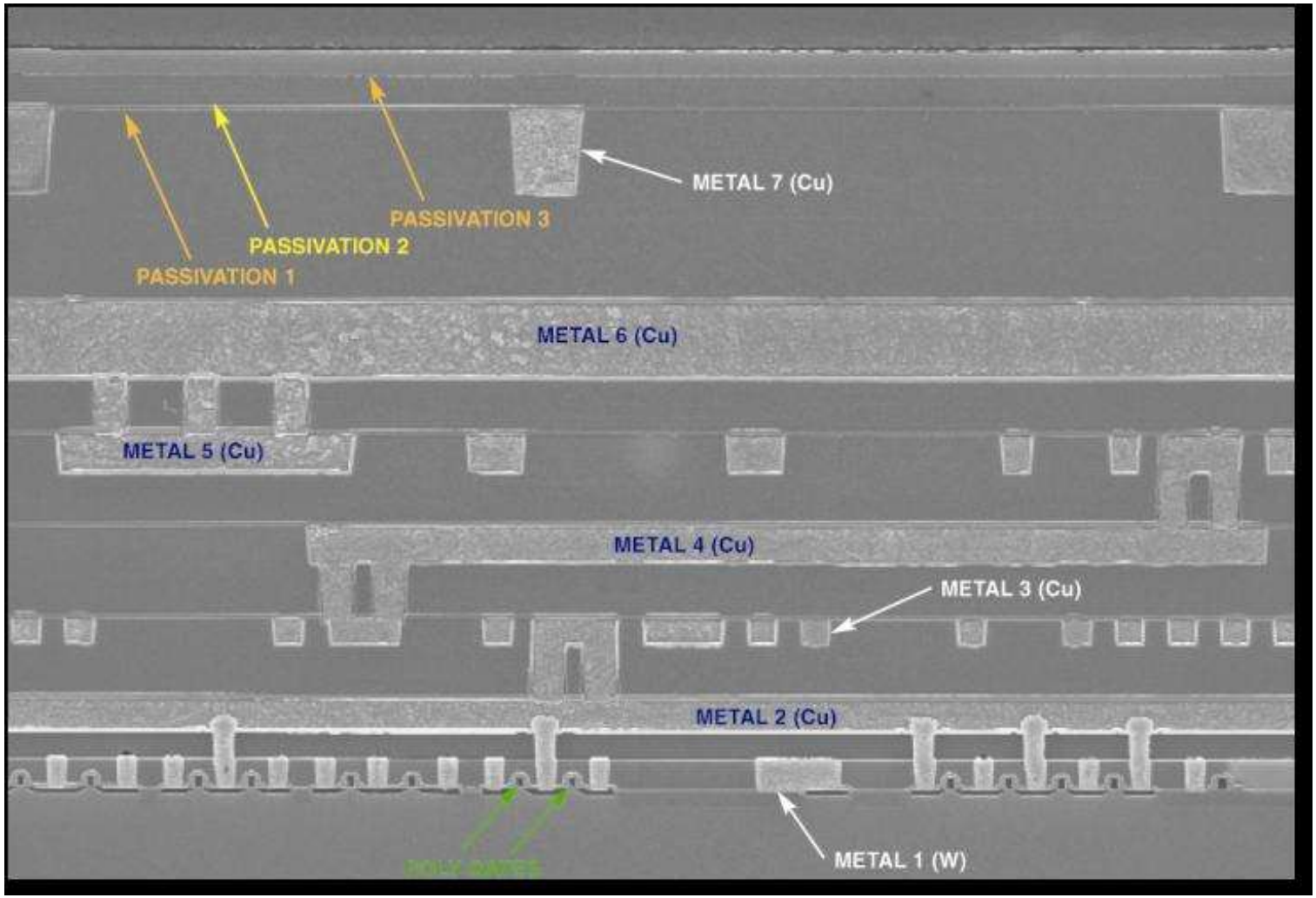
- Metal (Al or Cu) deposition and photolithography.
- Contacts and interconnects are formed.
- In just the same way the other metal layers are formed.
- After surface glass passivation and pad opening, the chips pass to the next step according to general IC fabrication flow.

Other CMOS Processes

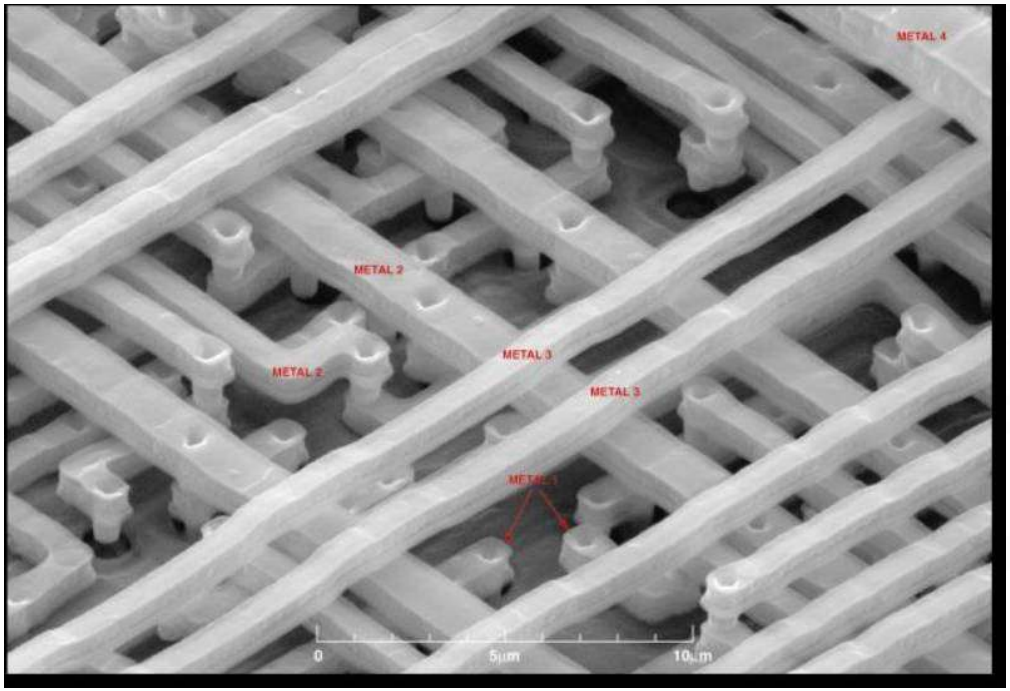
- **Other CMOS Processes**
  - P-well
  - Twin-well
  - Silicon on insulator (SOI-SIMOX)
  - Shallow trench isolation (STI)

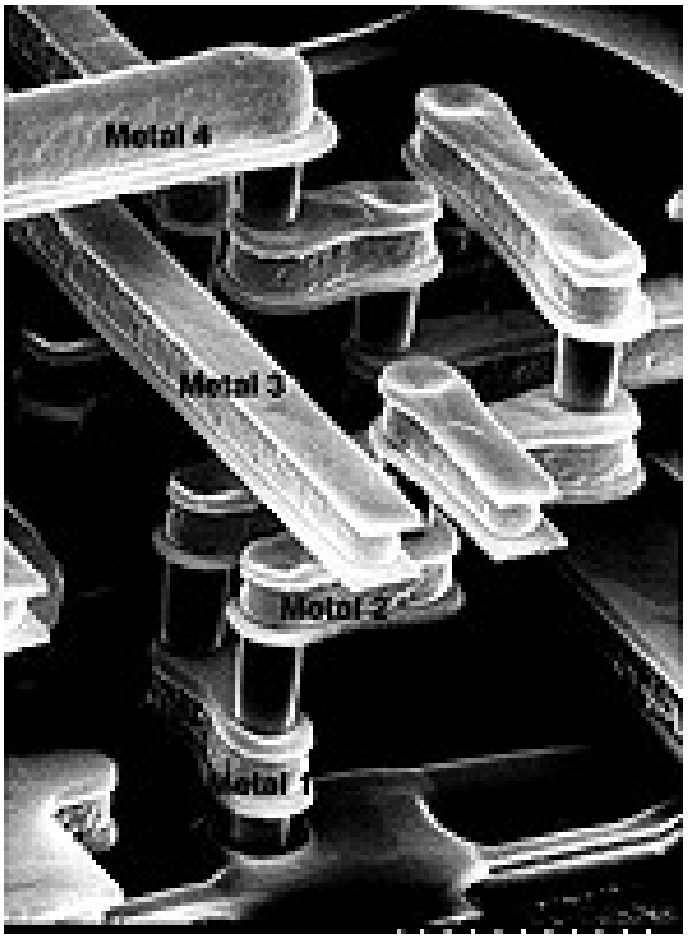
- **Process enhancements**
  - Increase of metal levels
  - Copper for interconnects and vias
  - Very thin oxide layers(1,0…2nm), stacked contacts and vias
  - Chemical and Mechanical Polishing (CMP)

Copper Metallization

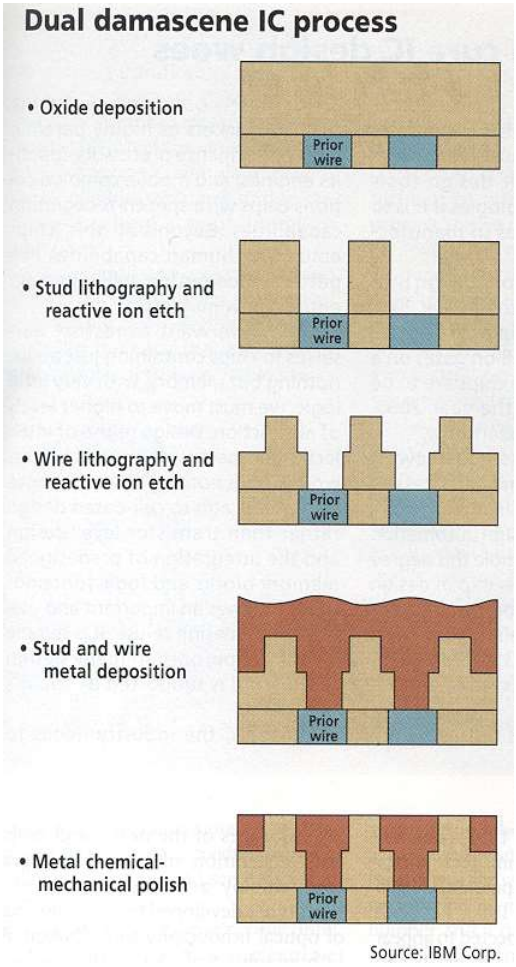


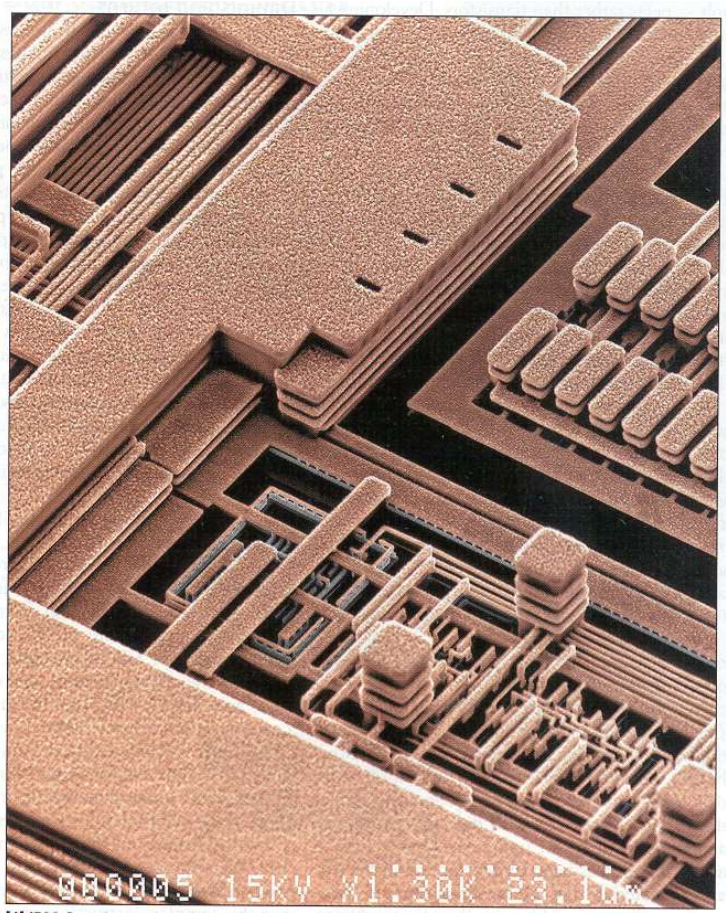
Advanced Metallization





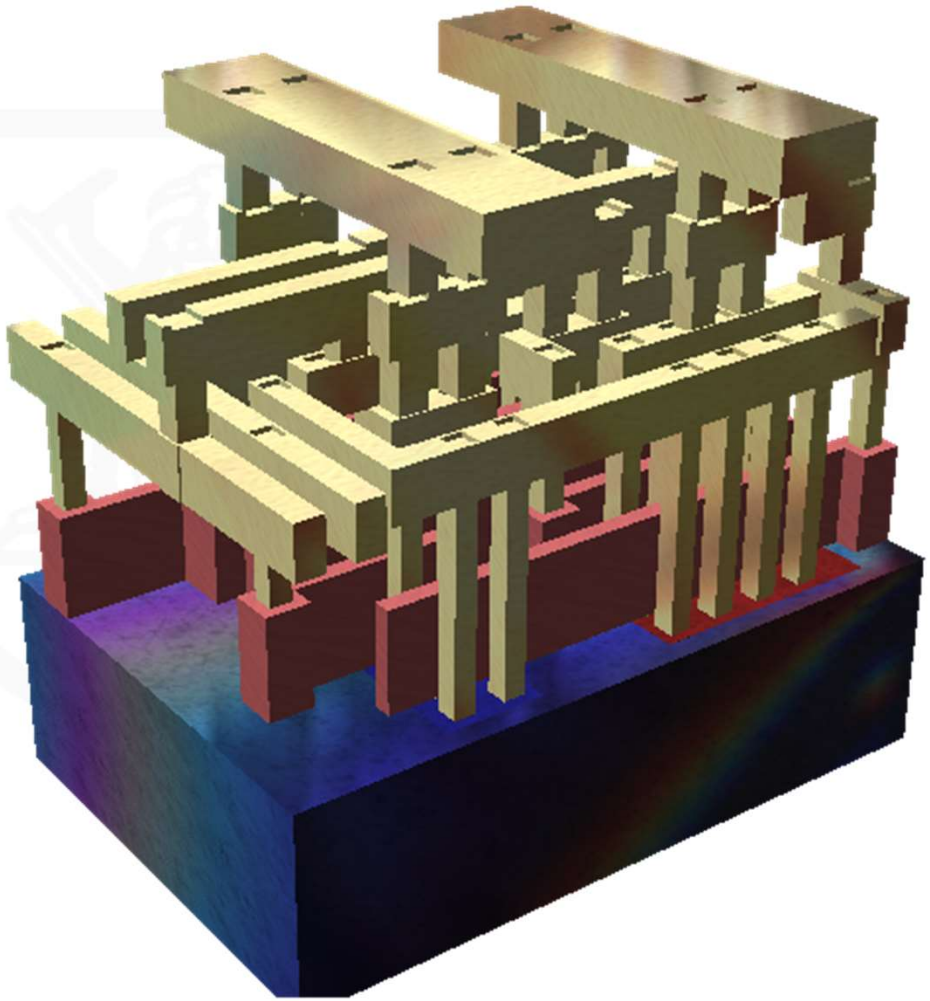
Advanced Metallization (cont.)





Advanced Metallization (cont.)

- **3D view of a modern standard cell**



Let’s see that again

- **Video 6**