Computer Engineering Department
Faculty of Engineering
Cairo University

CMP 305 – VLSI Design | Final Exam – Closed Book – 2 Hours | Spring 2014

ANSWER ALL QUESTIONS

Problem #1

State your opinion regarding the following issues. Note that your opinion does not have to be the same as that discussed in the lectures and can still earn you the full mark for this question if supported by simple, clear, and logical arguments.

a) State the different roles (at least 6 – there are more) a company can play in the supply chain of the semiconductors industry. Give one example of an International company for each role.

1. 2.

3. 4.

5. 6.

b) In your opinion, which role in the semiconductors industry can be readily adopted by starting-up Egyptian companies (i.e., first 5 years or so of a company's life)?

c) Again, in your opinion, how can they evolve and grow beyond that role (i.e., longer term, beyond 5 years)?

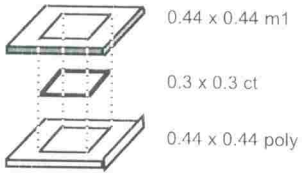
Problem #2

a) **Using wafer cross-sectional diagrams, explain how the photo-lithographic process is used to construct a self-aligned gate of a MOS transistor in a modern CMOS technology. Why is it called self-aligned?**

b) **Design rules are the interface between the circuit designer and the process engineer.**

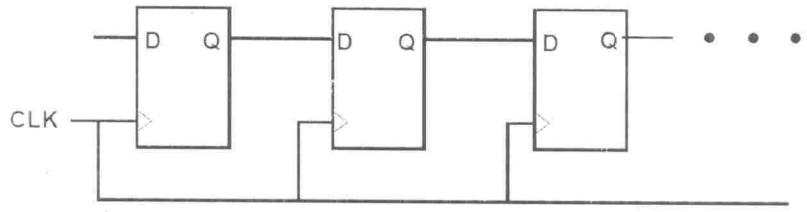
   i. **What is the difference between inter-layer design rules and intra-layer ones? Provide two examples of each.**

ii. For the diagram shown below illustrating a contact between metal 1 and polysilicon layers, list 2 inter-layer and 2 intra-layer design rules that apply and explain how they can be related to the given dimensions.



Problem #3

The flops used in the shift register below have a setup time of 100ps, a maximum clock-Q delay of 150ps, and a minimum clock-Q delay of 100ps. The clock source has a cycle-to-cycle jitter of 25ps.



(a) How fast can this circuit be clocked?

Clock frequency = MHz

(b) What is the limit on the hold time of the flops at this frequency?

Hold time < ps

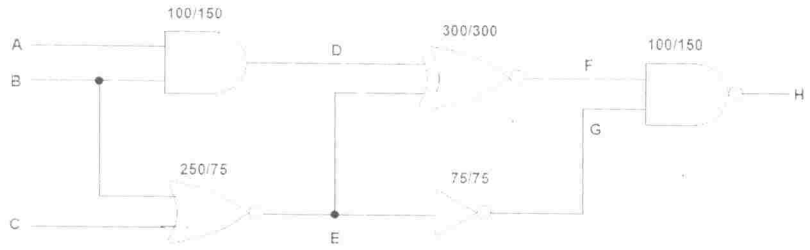
(c) What is the limit on the hold time of the flops at a frequency of 1 GHz?

Hold time < ps

(d) What is the limit on the hold time of the flops if the circuit is clocked at a frequency of 100 MHz?

Hold time < ps

(e) For the circuit below, write down all the paths from input B to the output and the worst-case and best-case delays for each path. The rise and fall times (in picoseconds) for each gate are shown above the gate symbol as rise-time/fall-time.

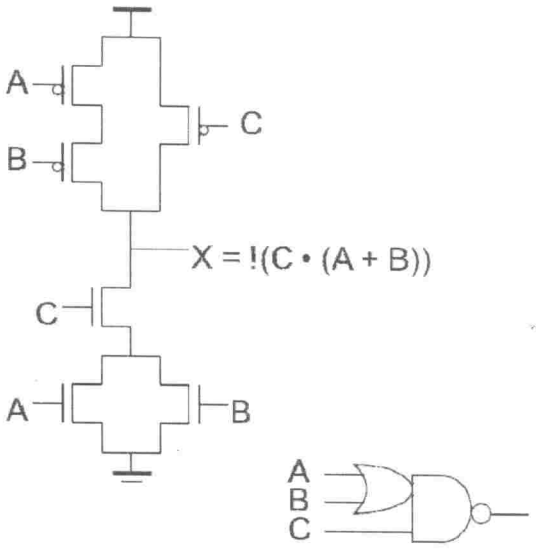


For example, the paths from input A to the output, and the delays are:

Path	Worst-case delay	Best-case delay
ADFH	600ps	500ps

Problem #4

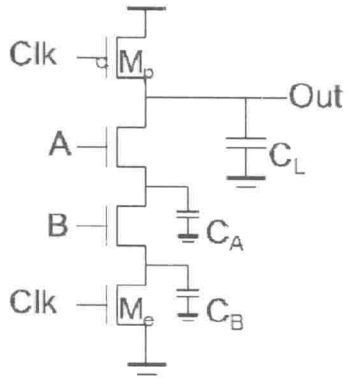
a) The function implemented in the circuit below is an OAI21. Draw a logic graph with identifying Euler Path(es) for the circuit and use it to draw a consistent stick diagram representation of an optimized layout for the circuit to have uninterrupted diffusion and minimize crossover metal requiring vias?



Logic Graph with Euler Path identified on it:

Stick diagram representation of an optimized layout for the circuit:

b) **The circuit show below is a dynamic implementation of a 2-input NAND gate. The circuit also shows the parasitic capacitance of the internal nodes along with the load capacitance. Explain briefly how charge sharing or redistribution can occur and draw a new circuit showing a solution for the charge sharing problem.**



How charge sharing occurs:

Proposed circuit to solve the charge sharing problem:

Problem #5

a) **Draw a flow chart detailing the cell-based design flow for digital ASICs. Make sure the inputs and outputs of each stage are clearly annotated on your chart. Include both front and back-ends of the design flow.**

b) List the most important design metrics usually used to optimize a design.

c) Write a short script for Design Compiler to synthesize the "detailed_RTL" architecture of the entity "toplevel" defined in the file toplevel.vhd and check its timing in the worst case corner. Make sure your script includes at least 4 constraints. (Correct syntax is a good indicator but is not essential)