Cairo University
Faculty of Engineering
Computer Dept.

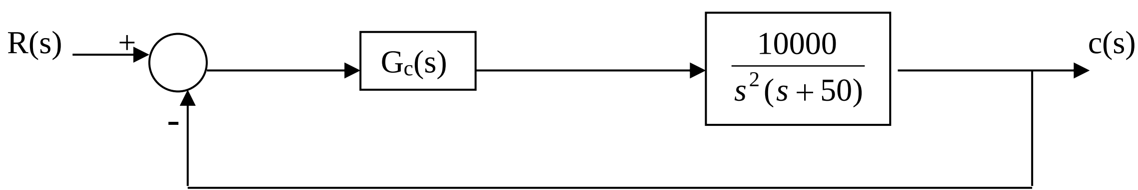
ELC 3252
CONTROL ENGINEERING
3rd Year - 2022

Sheet 5
Control Design and Compensation

[1] The block diagram of a type 2 system with a cascade controller $G_c(s)$ is shown in figure. The objective is to design a controller $G_c(s)$ so that:

- Maximum overshoot < 10%
- Settling time <1

Design the controller that satisfies the performance specifications given above.



[2] Consider a unity feedback controller system whose feedforward transfer function is:

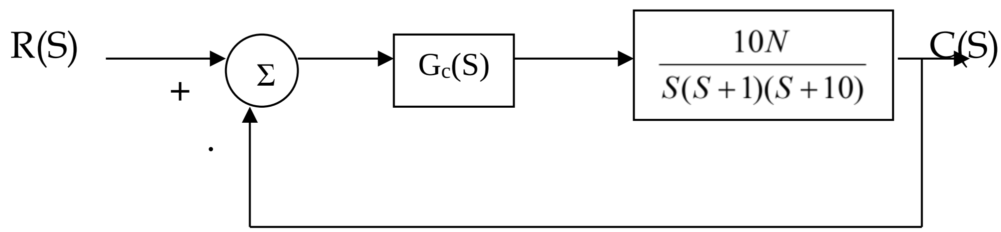
$$G(s) = \frac{2}{s(s+2)(s+8)}$$

a. Find the static error coefficients and the error as a function of time for unit ramp input.
b. Design a compensator so that the closed loop dominant poles are located at $s = -1 \pm j2\sqrt{3}$

[3] The following figure shows the block diagram of the liquid level control system. The liquid level is represented by c(t), and N denotes the number of inlets. It is desired that N=20.
Design a controller $G_c(S)$ such that:

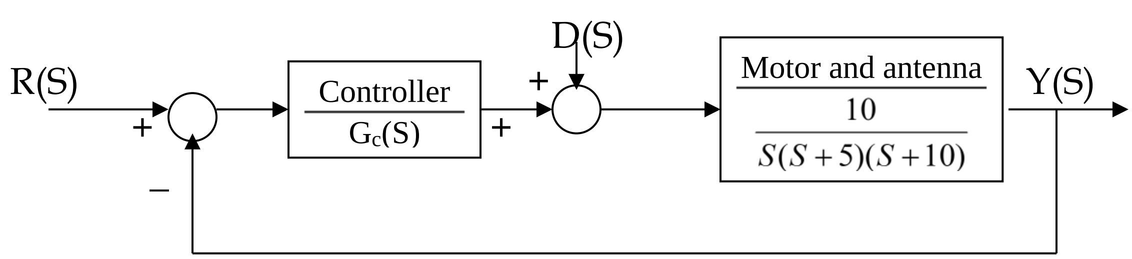
- The overshoot is zero.
- The tank is filled to the reference level within 2.5 sec.

What is the effect of the controller on the steady state response? And why?



[4] A large antenna is used to receive satellite signals and must accurately track the satellite as it moves across the sky. The control system uses an armature controlled motor and a controller to be selected as shown in figure. The system specifications require an overshoot to a step input less than or equal 10% with a settling time less than or equal 2 seconds.

- Design a controller $G_c(S)$ to achieve the required specifications and plot the resulting response.
- Determine the effect of the disturbance [D(S)=Q/S] on the steady state output.



[5]A control system with a type 0 process and PID controller is shown in figure . Design the parameters of the PID controller so that the following specifications are satisfied:

a. Settling time ≤ 0.2
b. Max. Overshoot ≤ 5 percent.
c. Steady state error due to unit step disturbance =zero.