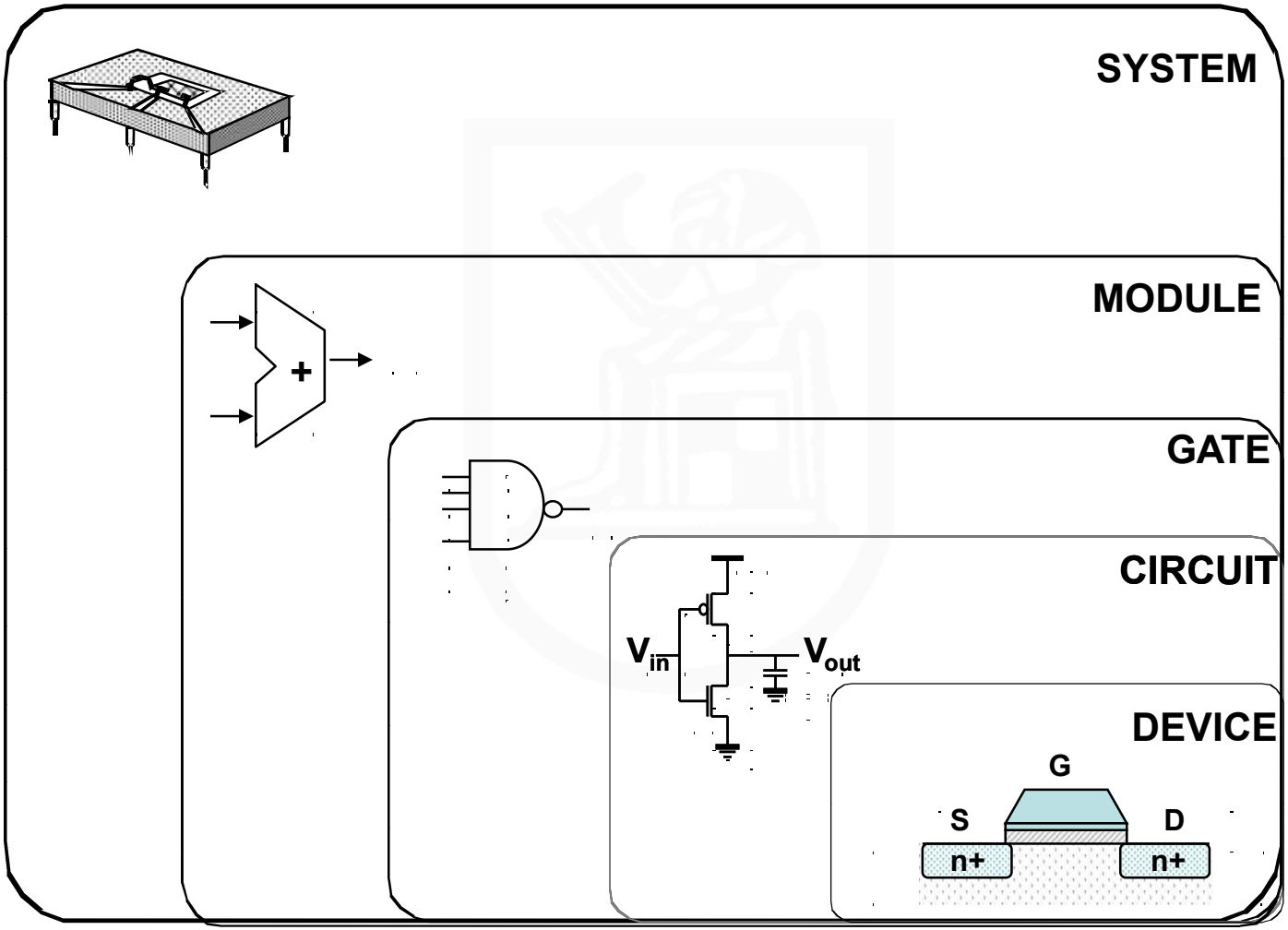
Course Outline

- Semiconductor Industry and Technology Overview
- **IC Design Flows**
- Timing in Digital Systems
- Front-end Design Flow
- Back-end Design Flow
- Interconnection and Signal Integrity
- Low-Power Design
- Design-for-Testability (DFT)

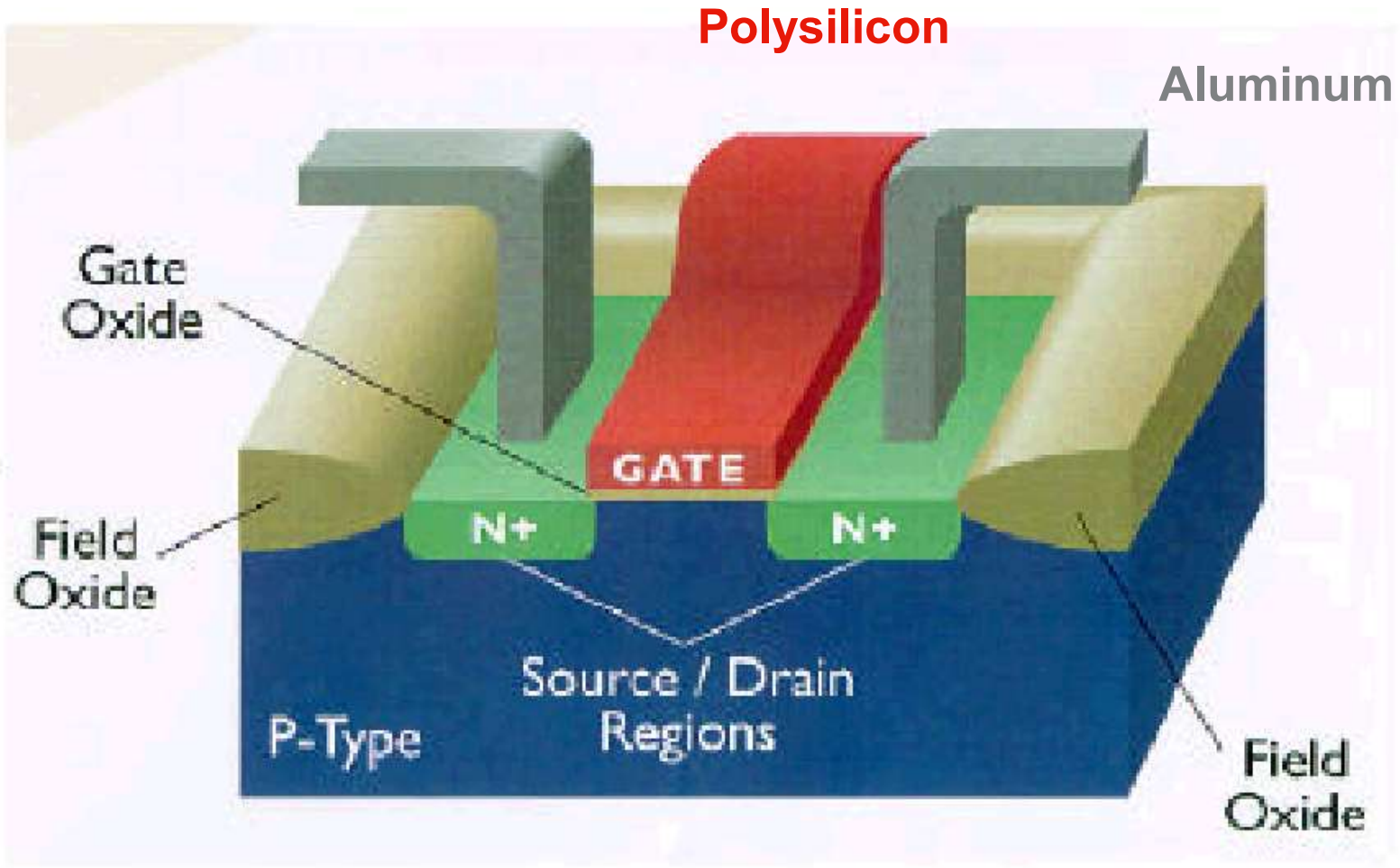
IC Design Flows

- **The MOS Transistor**
- Analog and Circuit Design
- Digital Logic Families
- Productivity Gap
- Digital Design Flows

Design Abstraction Levels

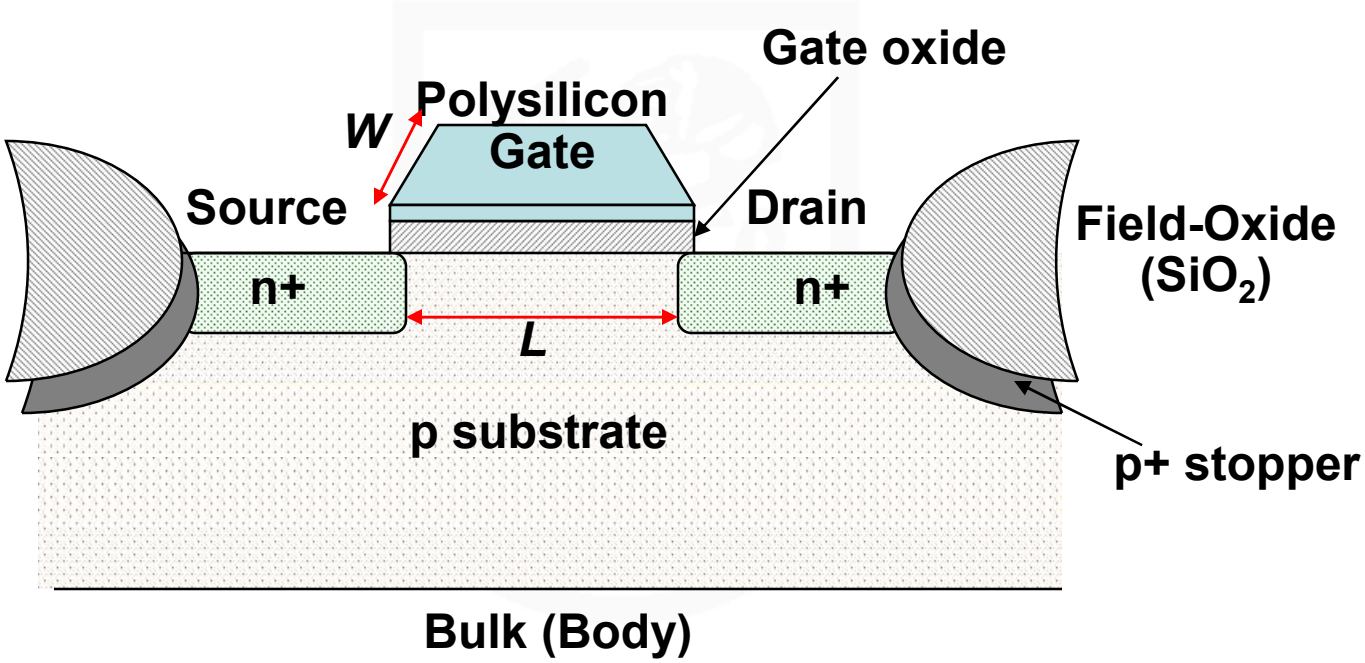


The MOS Transistor



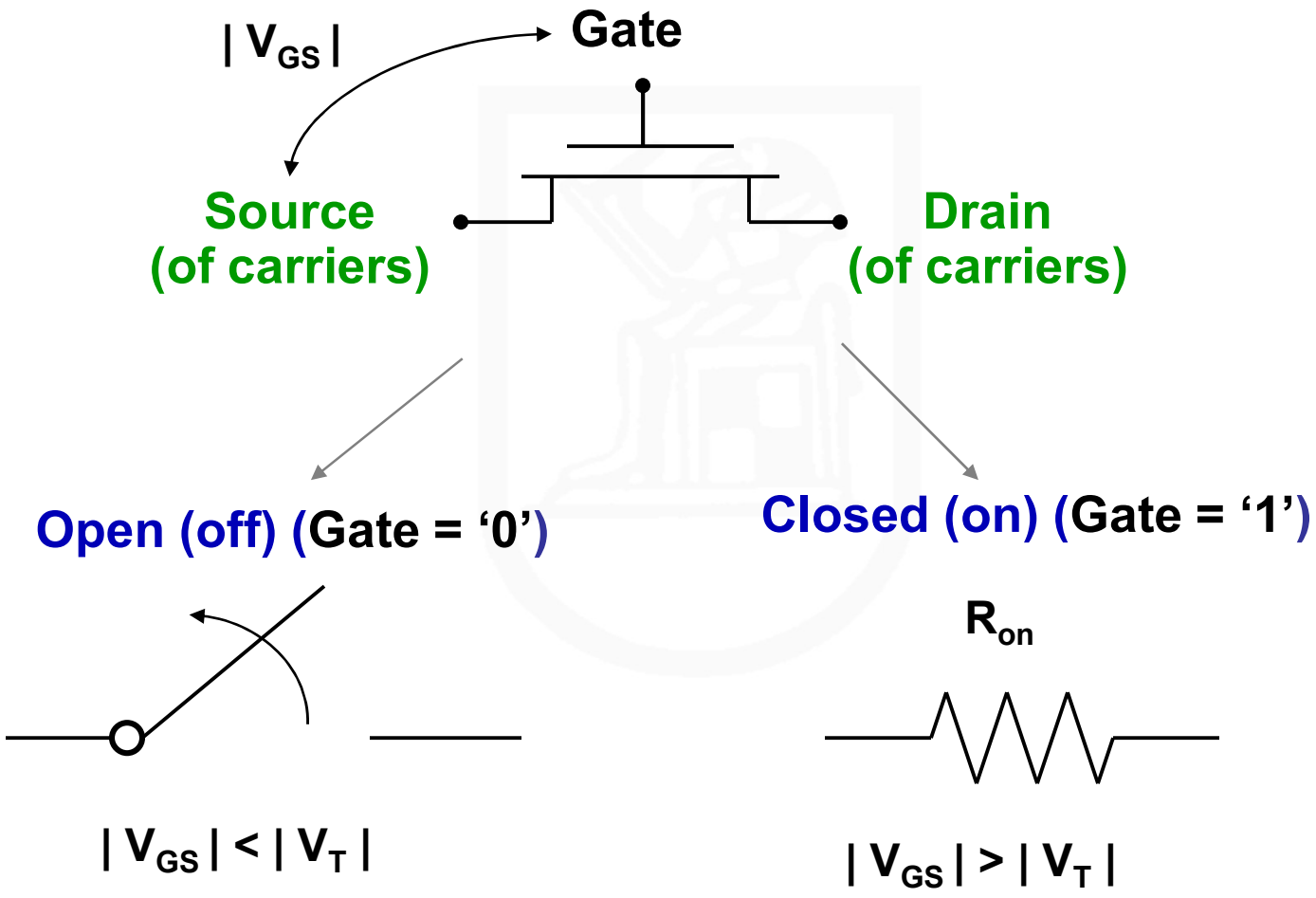
The NMOS Transistor Cross Section

n areas have been doped with donor ions (arsenic) of concentration N_D - electrons are the majority carriers

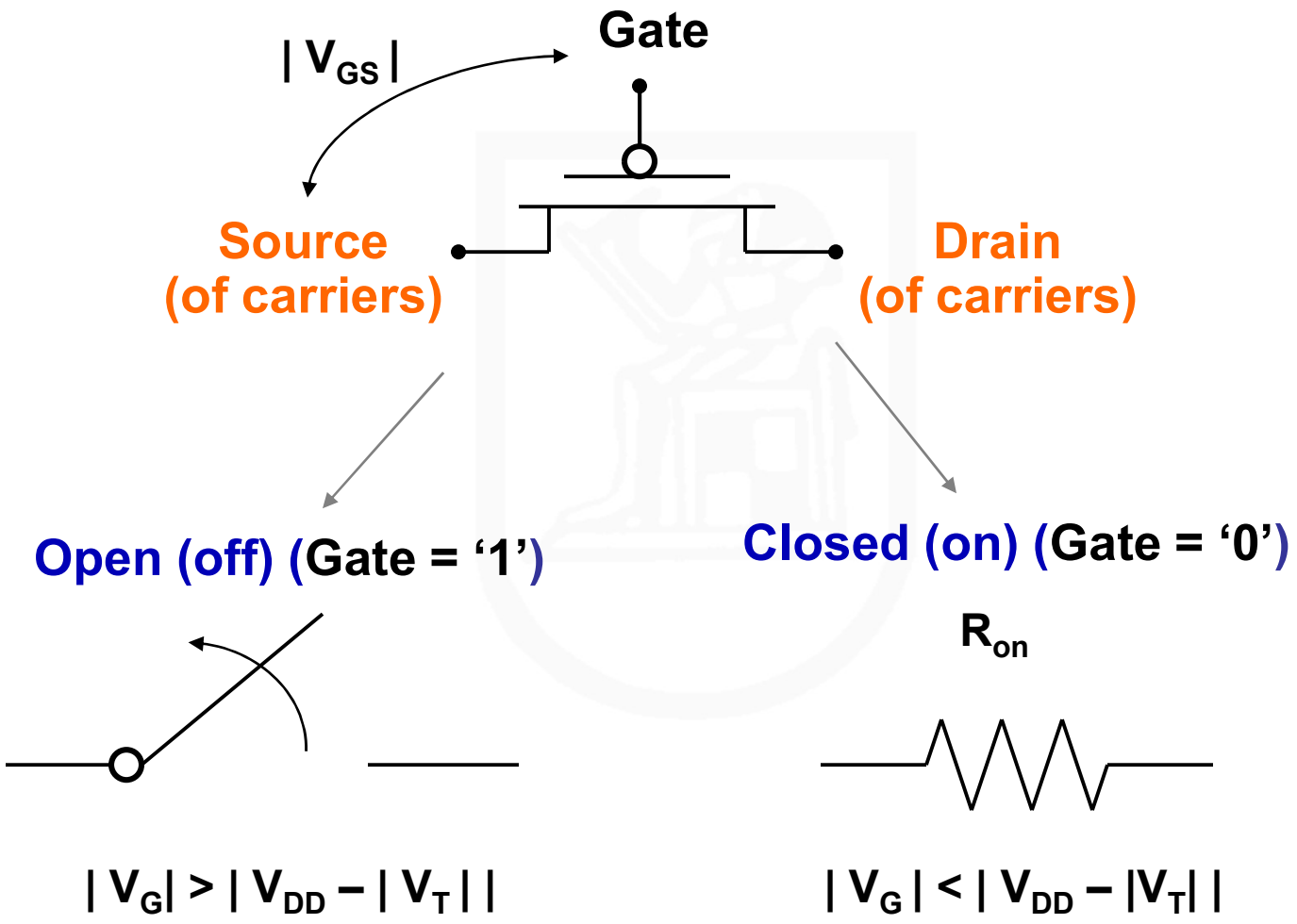


p areas have been doped with acceptor ions (boron) of concentration N_A - holes are the majority carriers

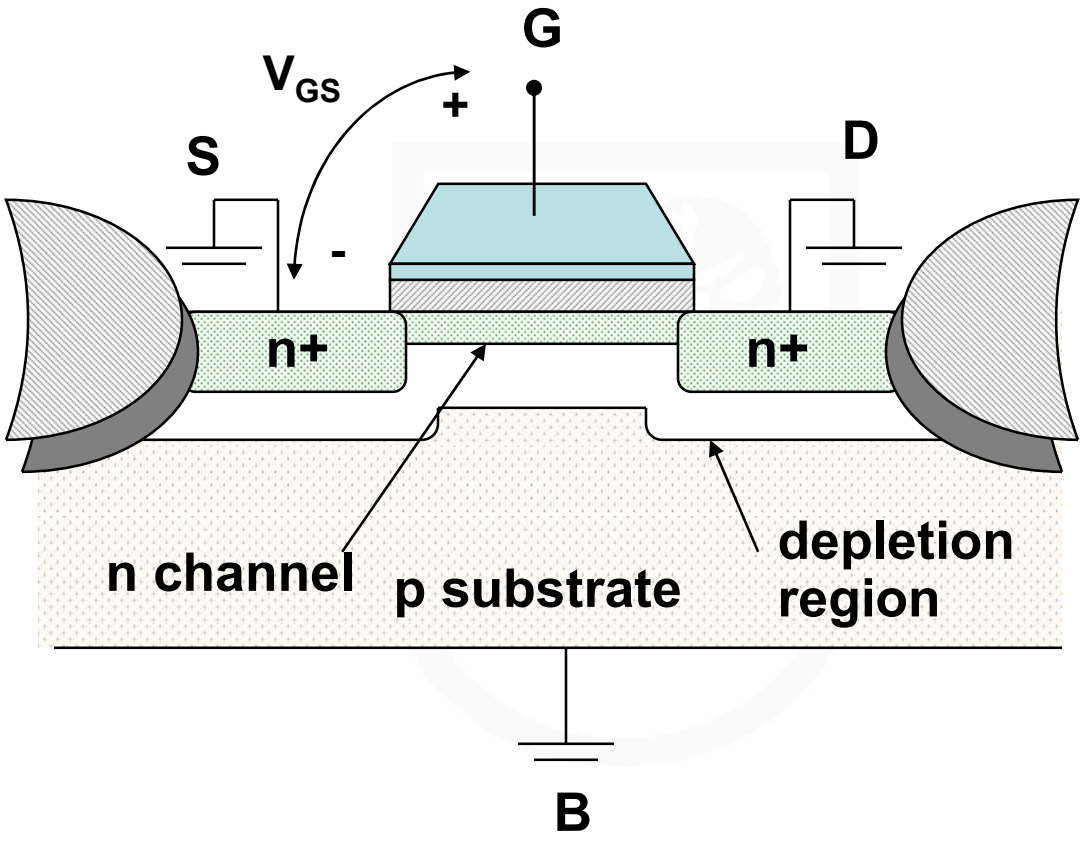
Switch Model of NMOS Transistor



Switch Model of PMOS Transistor



Threshold Voltage Concept



The value of V_{GS} where strong inversion occurs is called the threshold voltage, V_T

The Threshold Voltage

where $$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

V_{SB} is the source-bulk voltage

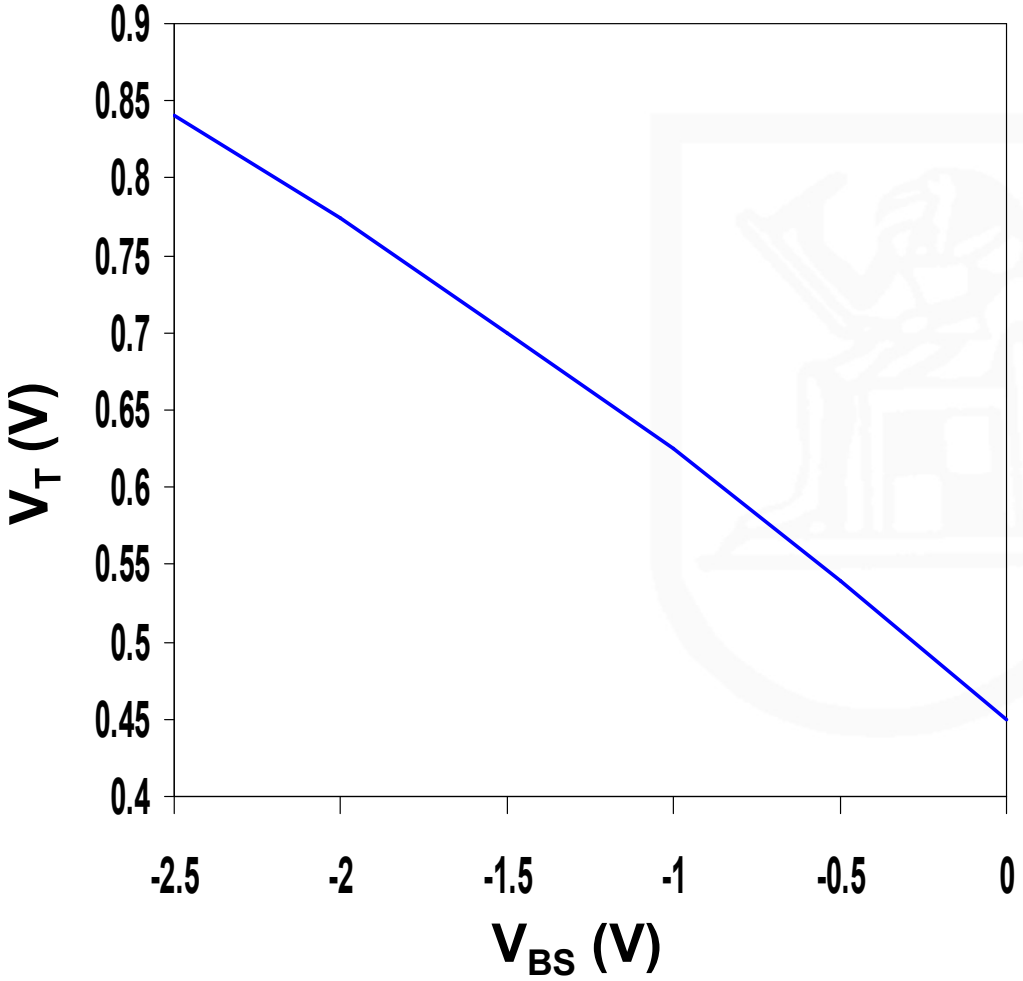
V_{T0} is the threshold voltage at $V_{SB} = 0$ and is mostly a function of the manufacturing process

Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.

$\phi_F = -\phi_T \ln(N_A/n_i)$ is the Fermi potential ($\phi_T = kT/q = 26mV$ at 300K is the thermal voltage; N_A is the acceptor ion concentration; $n_i \approx 1.5\times10^{10}\ cm^{-3}$ at 300K is the intrinsic carrier concentration in pure silicon)

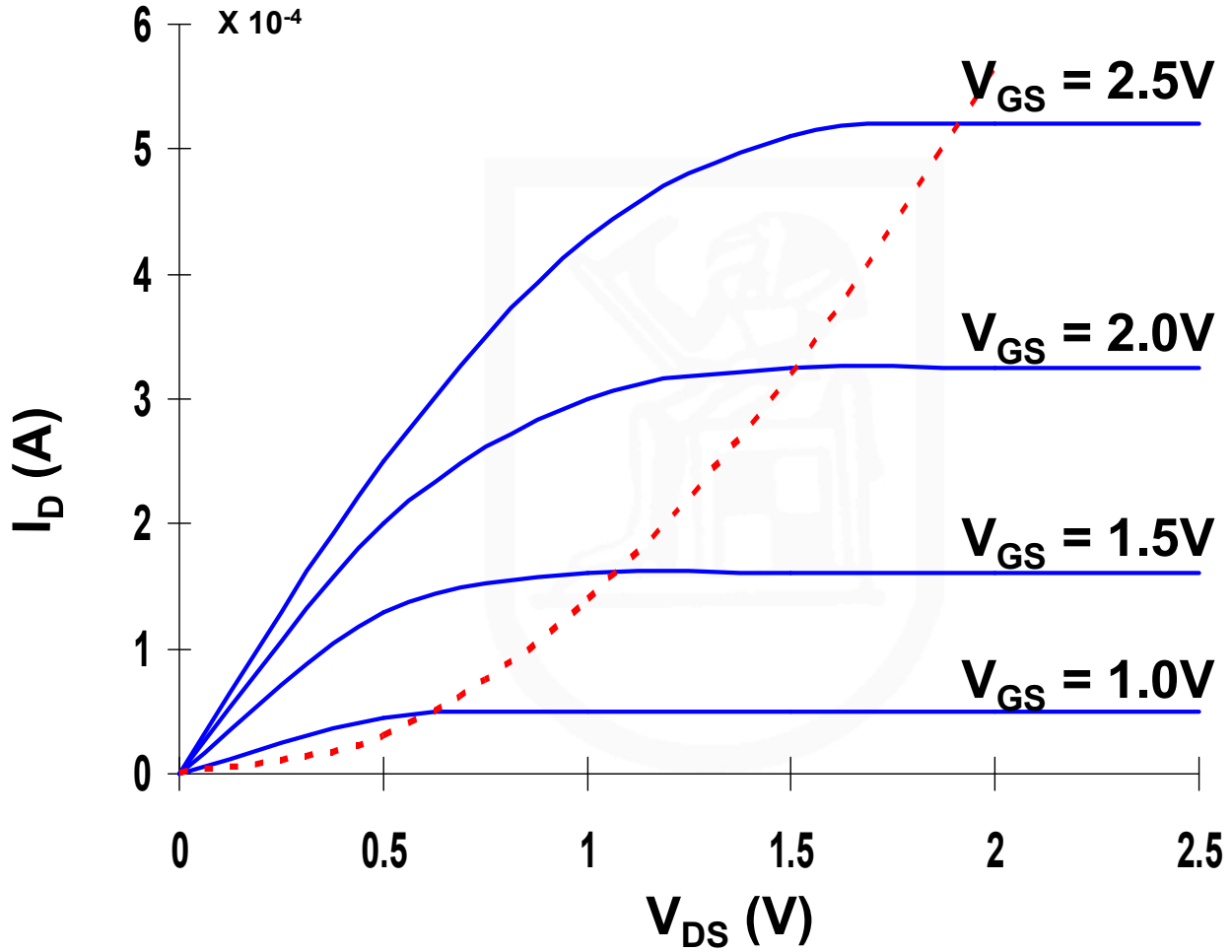
$\gamma = \sqrt{(2q\varepsilon_{si}N_A)}/C_{ox}$ is the body-effect coefficient (impact of changes in V_{SB}) ($\varepsilon_{si}=1.053\times10^{-10}F/m$ is the permittivity of silicon; $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance with $\varepsilon_{ox}=3.5\times10^{-11}F/m$)

The Body Effect



- V_{SB} is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)
- A negative bias causes V_T to increase from 0.45V to 0.85V

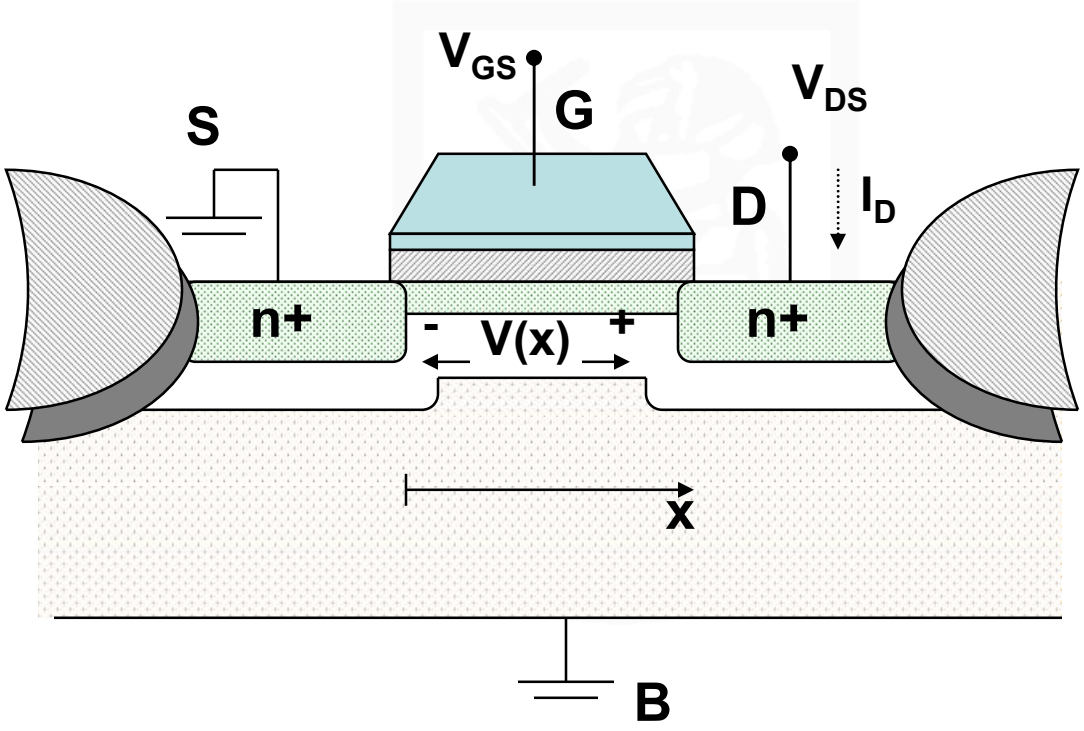
Long Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 10um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.43V

Transistor in Linear Mode

Assuming $V_{GS} > V_T$



The current is a linear function of both V_{GS} and V_{DS}

Voltage-Current Relation: Linear Mode

For long-channel devices (L > 0.25 micron)

- When $V_{DS} \leq V_{GS} - V_T$

$$\mathbf{I_D = k'_n\, W/L\, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]}$$

where

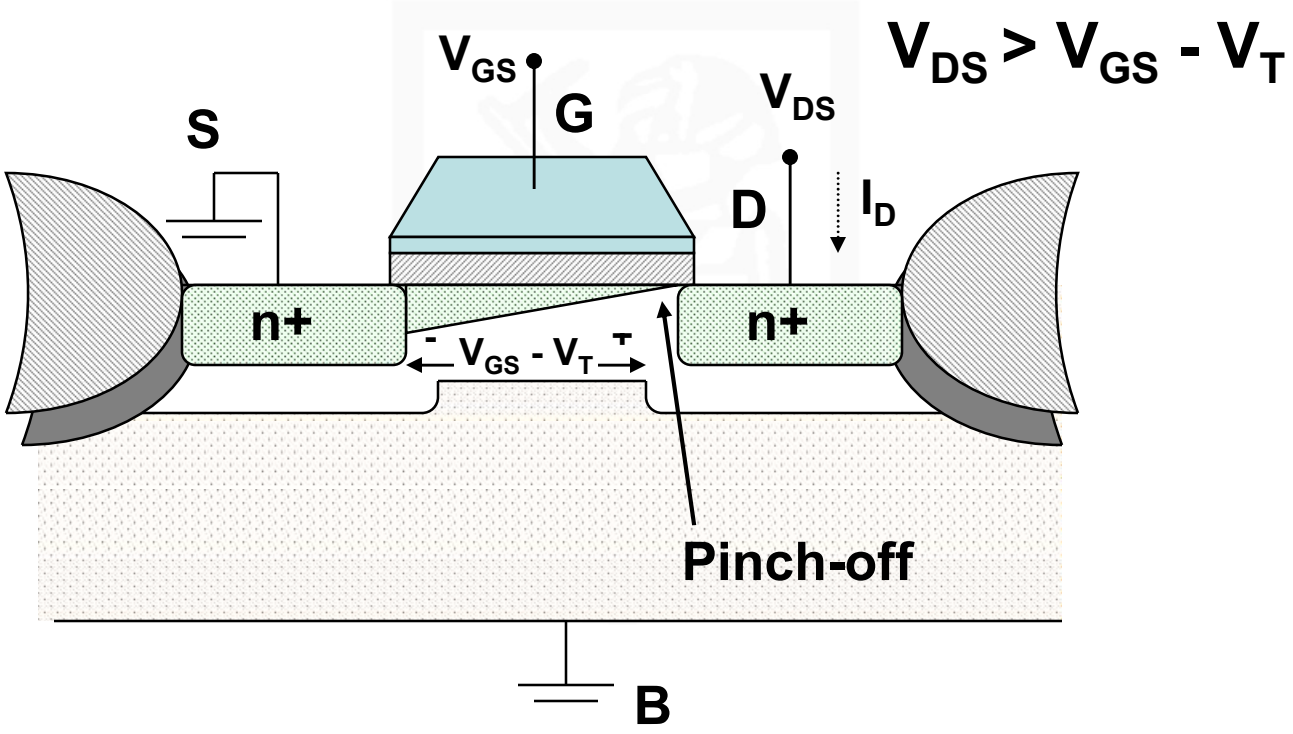
$k'_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox}/t_{ox}$ = is the process transconductance parameter (μ_n is the carrier mobility (m^2/Vsec))

$k_n = k'_n\, W/L$ is the gain factor of the device

For small V_{DS}, there is a linear dependence between V_{DS} and I_D, hence the name resistive or linear region

Transistor in Saturation Mode

Assuming $V_{GS} > V_T$



The current remains constant (transistor saturates)

Voltage-Current Relation: Saturation Mode

For long channel devices

- When $V_{DS} \geq V_{GS} - V_T$

$$\mathbf{I_D' = k'_n/2\ W/L\ [(V_{GS} - V_T)^2]}$$

since the voltage difference over the induced channel (from the pinch-off point to the source) remains fixed at $V_{GS} - V_T$

- However, the effective length of the conductive channel is modulated by the applied V_{DS}, so

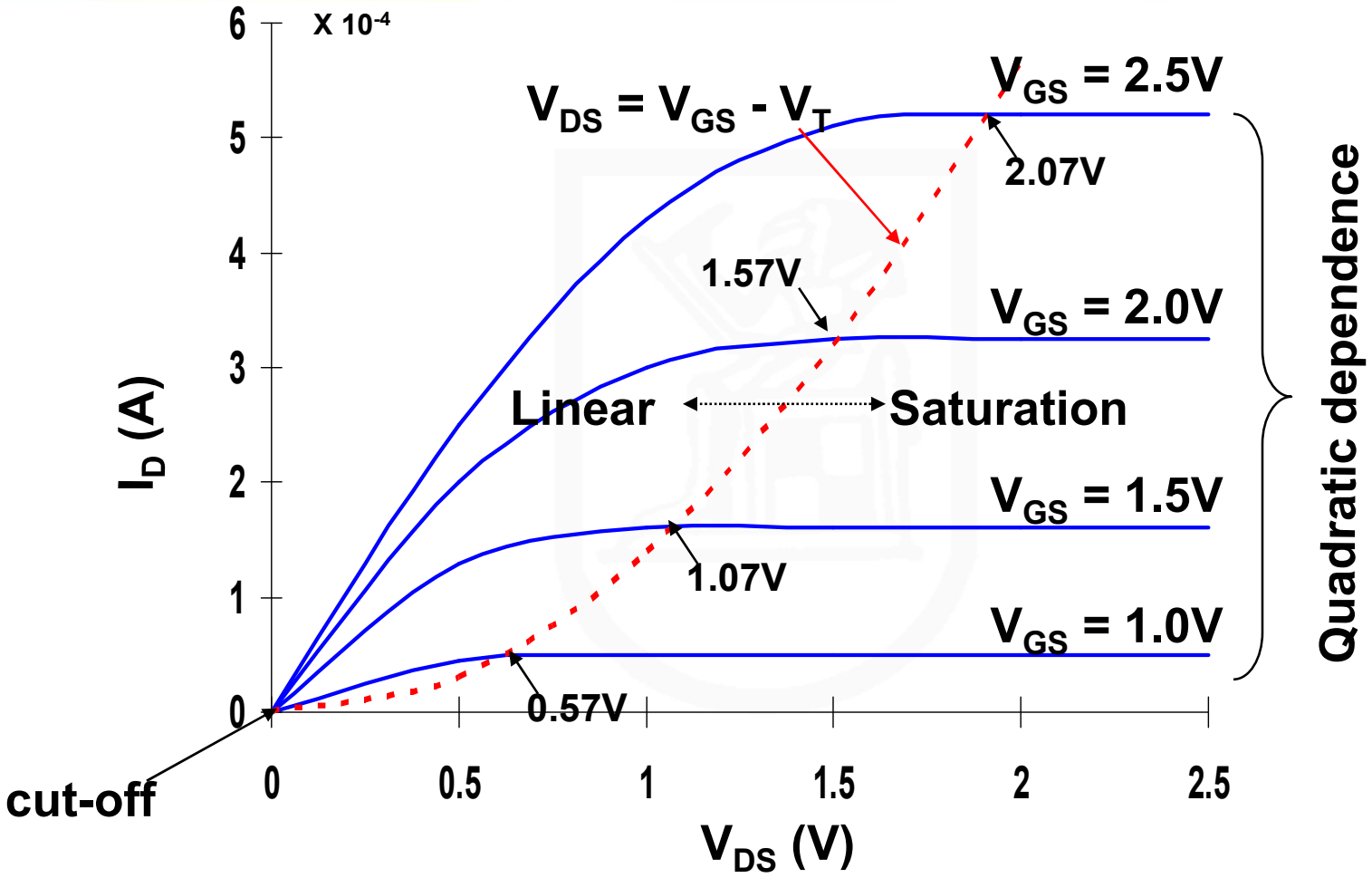
$$I_D = I_D' (1 + \lambda V_{DS})$$

where λ is the channel-length modulation (varies with the inverse of the channel length)

Current Determinates

- For a fixed V_{DS} and V_{GS} (> V_T), I_{DS} is a function of
  - the distance between the source and drain – L
  - the channel width – W
  - the threshold voltage – V_T
  - the thickness of the SiO_2 – t_{ox}
  - the dielectric of the gate insulator (e.g., SiO_2) – ε_{ox}
  - the carrier mobility
    - for n-fets: μ_n = 500 cm^2/V-sec
    - for p-fets: μ_p = 180 cm^2/V-sec

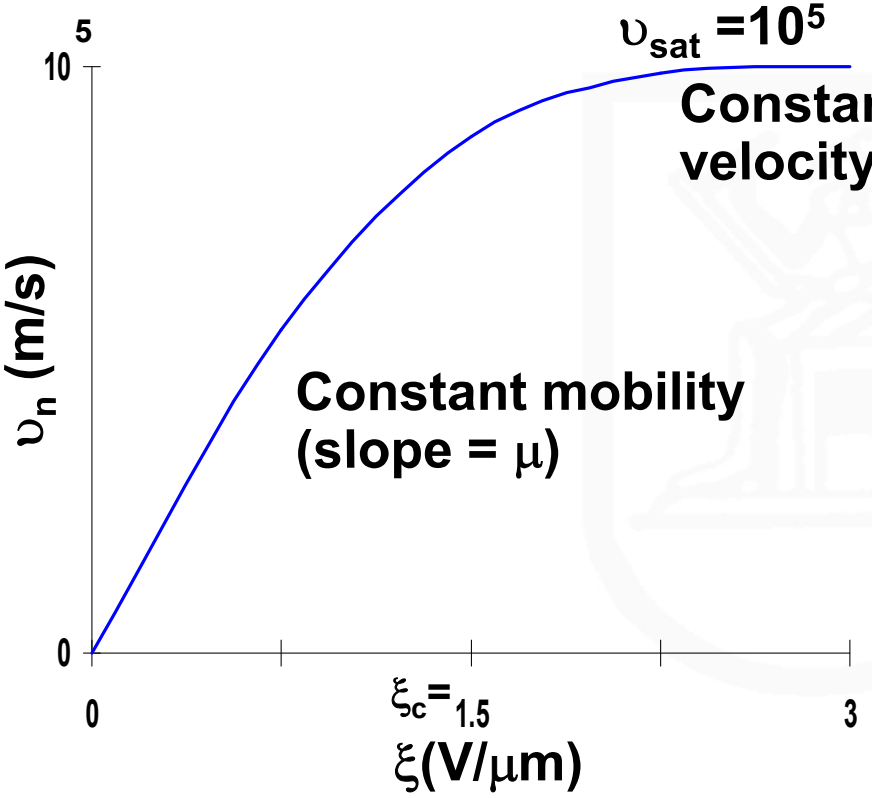
Long Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 10um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.43V

Short Channel Effects

Behavior of short channel device mainly due to



- Velocity saturation – the velocity of the carriers saturates due to scattering (collisions suffered by the carriers)

For an NMOS device with L of 0.25μm, only a couple of volts difference between D and S are needed to reach velocity saturation

Voltage-Current Relation: Velocity Saturation

For short channel devices

- Linear: When $V_{DS} \leq V_{GS} - V_T$

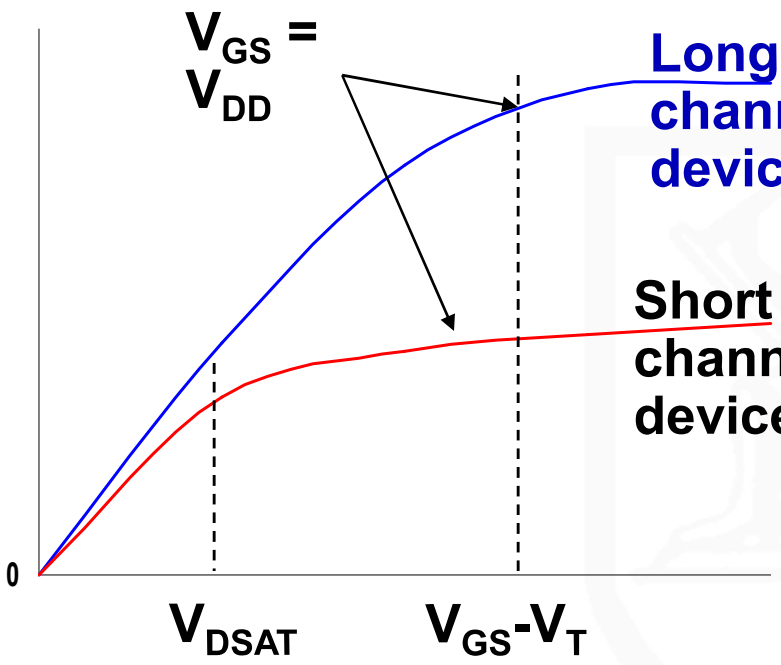
$$I_D = \kappa(V_{DS})\, k'_n\, W/L\, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

where $\kappa(V) = 1/(1 + (V/\xi_c L))$ is a measure of the degree of velocity saturation

- Saturation: When $V_{DS} = V_{DSAT} \geq V_{GS} - V_T$

$$I_{DSat} = \kappa(V_{DSAT})\, k'_n\, W/L\, [(V_{GS} - V_T)V_{DSAT} - V_{DSAT}^2/2]$$

Velocity Saturation Effects

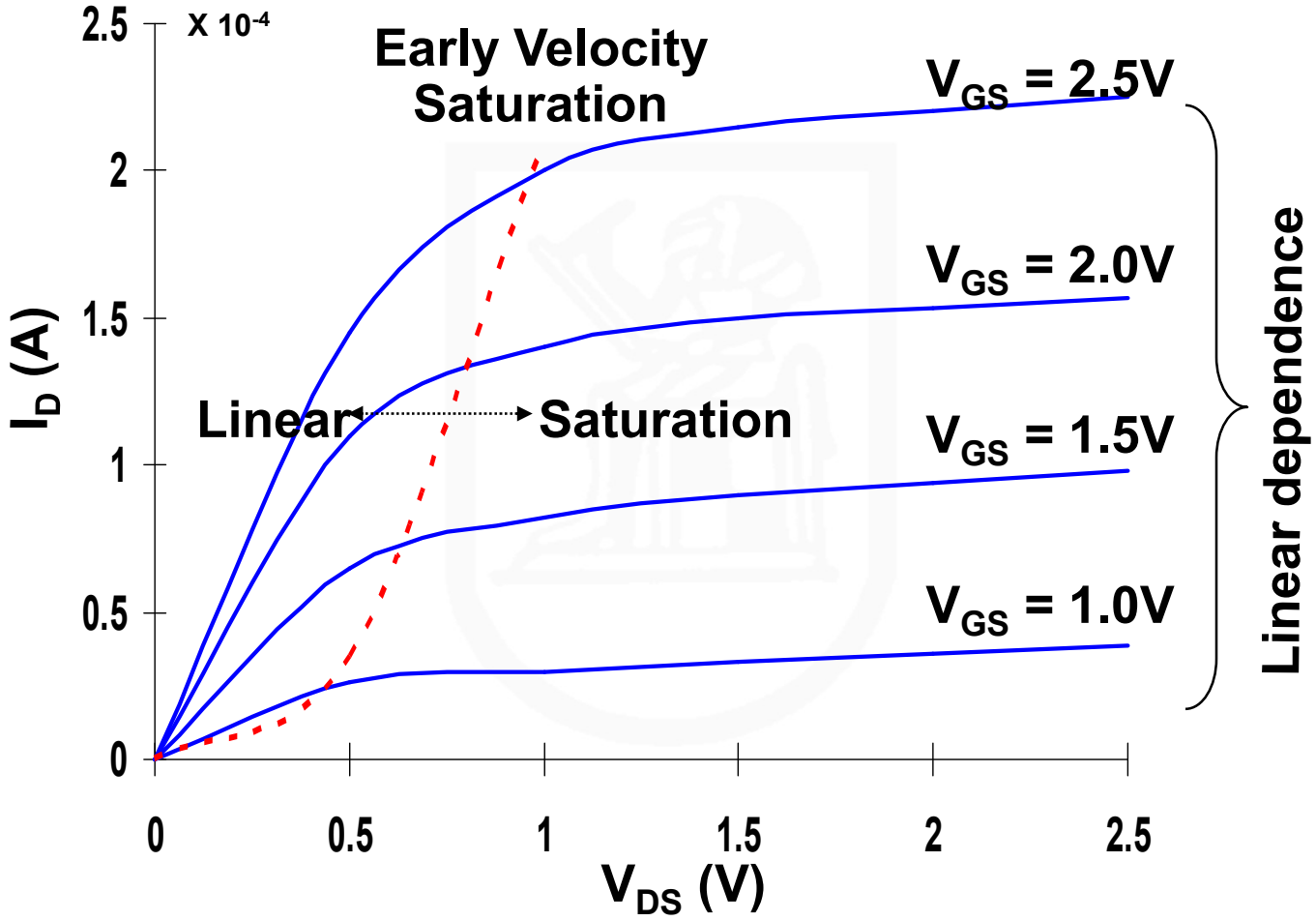


For short channel devices and large enough $V_{GS} - V_T$

$V_{DSAT} < V_{GS} - V_T$ so the device enters saturation before V_{DS} reaches $V_{GS} - V_T$ and operates more often in saturation

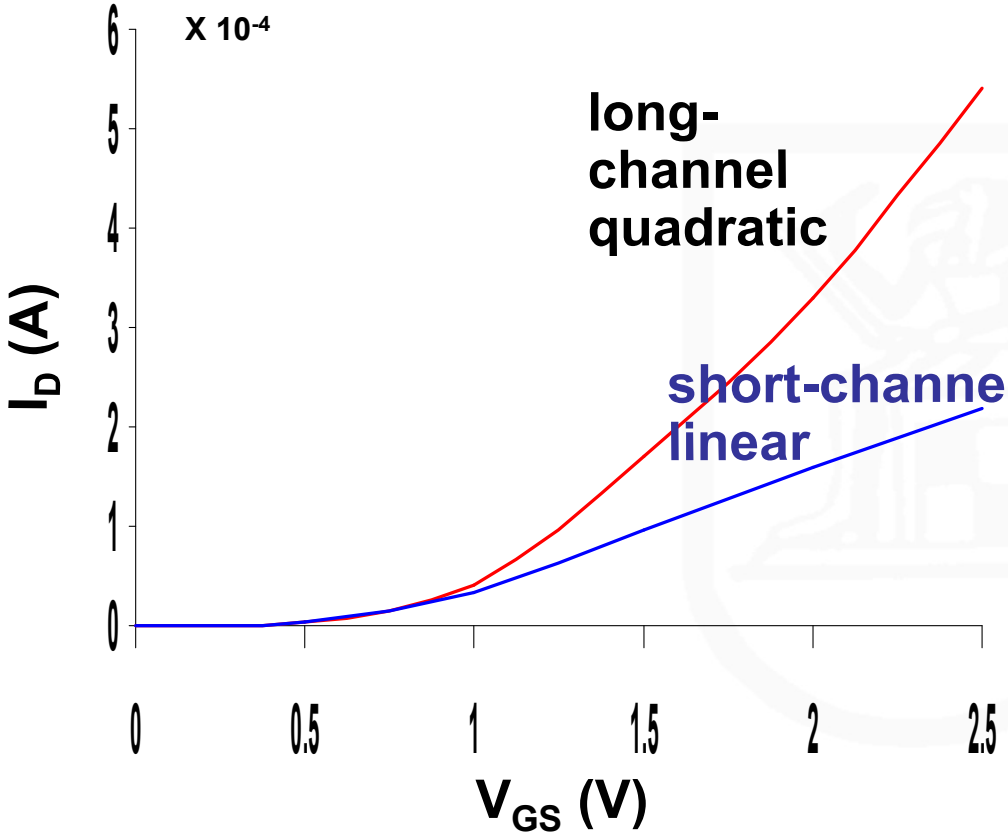
- I_{DSAT} has a linear dependence w.r.t. V_{GS} so a reduced amount of current is delivered for a given control voltage

Short Channel I-V Plot (NMOS)



NMOS transistor, 0.25um, L_d = 0.25um, W/L = 1.5, V_{DD} = 2.5V, V_T = 0.43V

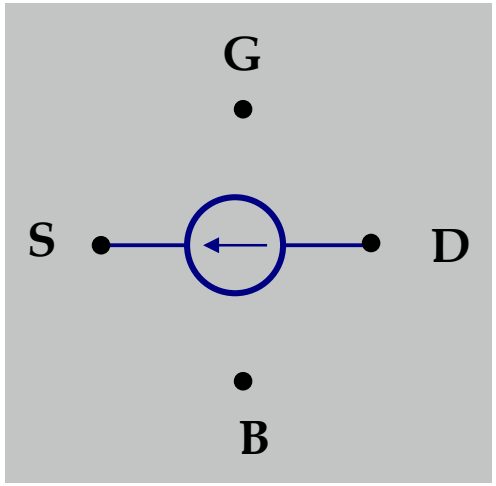
MOS I_D-V_{GS} Characteristics



(for V_{DS} = 2.5V, W/L = 1.5)

- Linear (short-channel) versus quadratic (long-channel) dependence of I_D on V_{GS} in saturation
- Velocity-saturation causes the short-channel device to saturate at substantially smaller values of V_{DS} resulting in a substantial drop in current drive

The MOS Current-Source Model



$I_D = 0$ for $V_{GS} - V_T < 0$

$I_D = k' W/L [(V_{GS} - V_T)V_{min} - V_{min}^2/2](1+\lambda V_{DS})$

for $V_{GS} - V_T \geq 0$

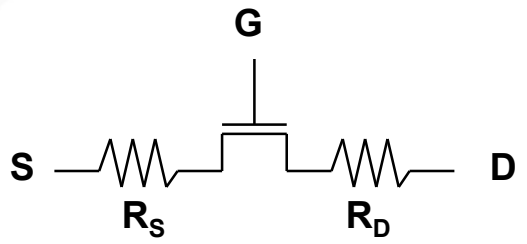
with $V_{min} = \min(V_{GS} - V_T, V_{DS}, V_{DSAT})$
and $V_{GT} = V_{GS} - V_T$

Determined by the voltages at the four terminals and a set of five device parameters

	$V_{T0}(V)$	$\gamma(V^{0.5})$	$V_{DSAT}(V)$	$k'(A/V^2)$	$\lambda(V^{-1})$
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

Other (Submicon) MOS Transistor Concerns

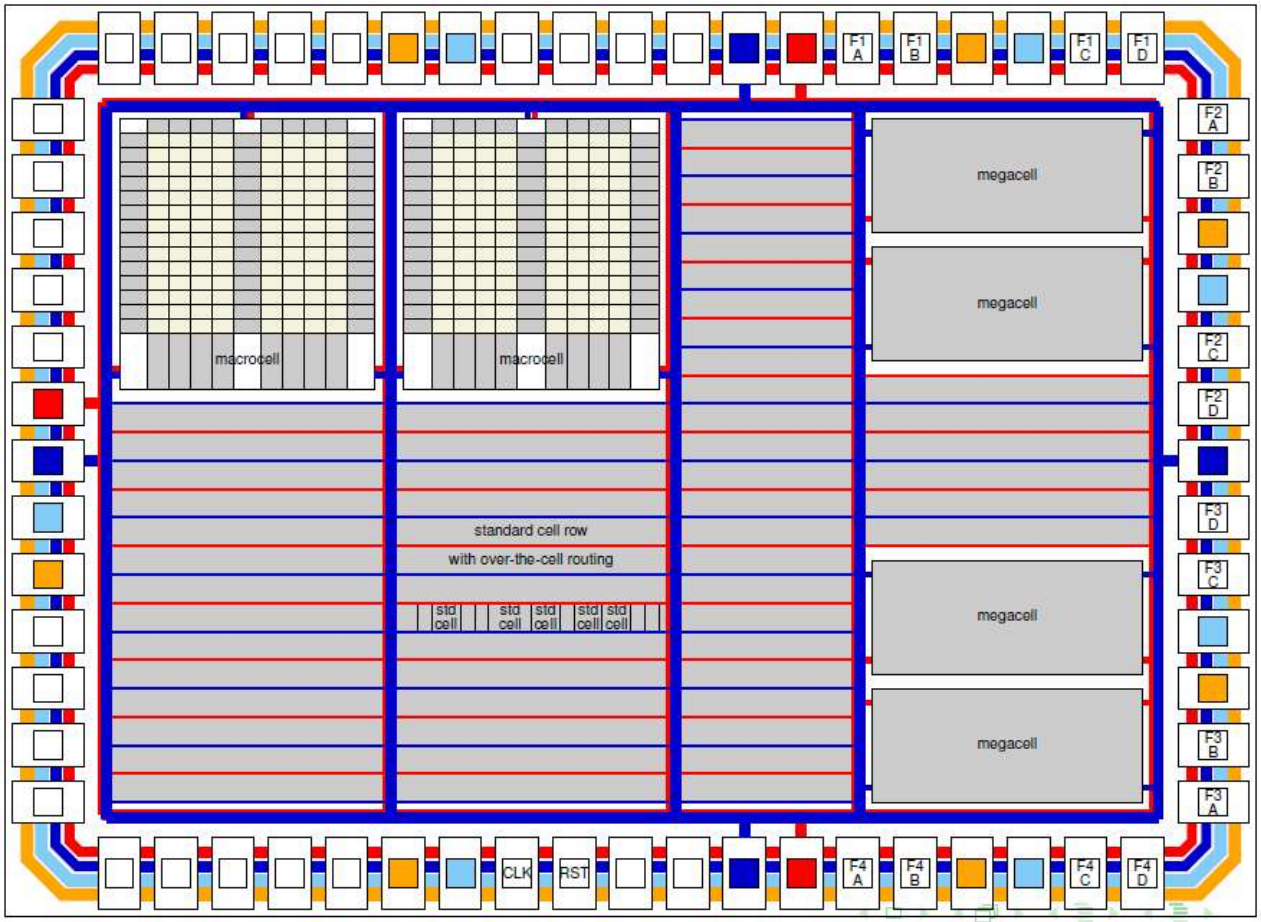
- **Velocity saturation**
- **Sub-threshold conduction (aka weak inversion)**
  - Transistor is already partially conducting for voltages below V_T
- **Threshold variations**
  - In long-channel devices, the threshold is a function of the length (for low V_{DS})
  - In short-channel devices, there is a drain-induced threshold barrier lowering (DIBL) at the upper end of the V_{DS} range (for small L)
- **Parasitic resistances**
  - resistances associated with the source and drain contacts
- **Latch-up**



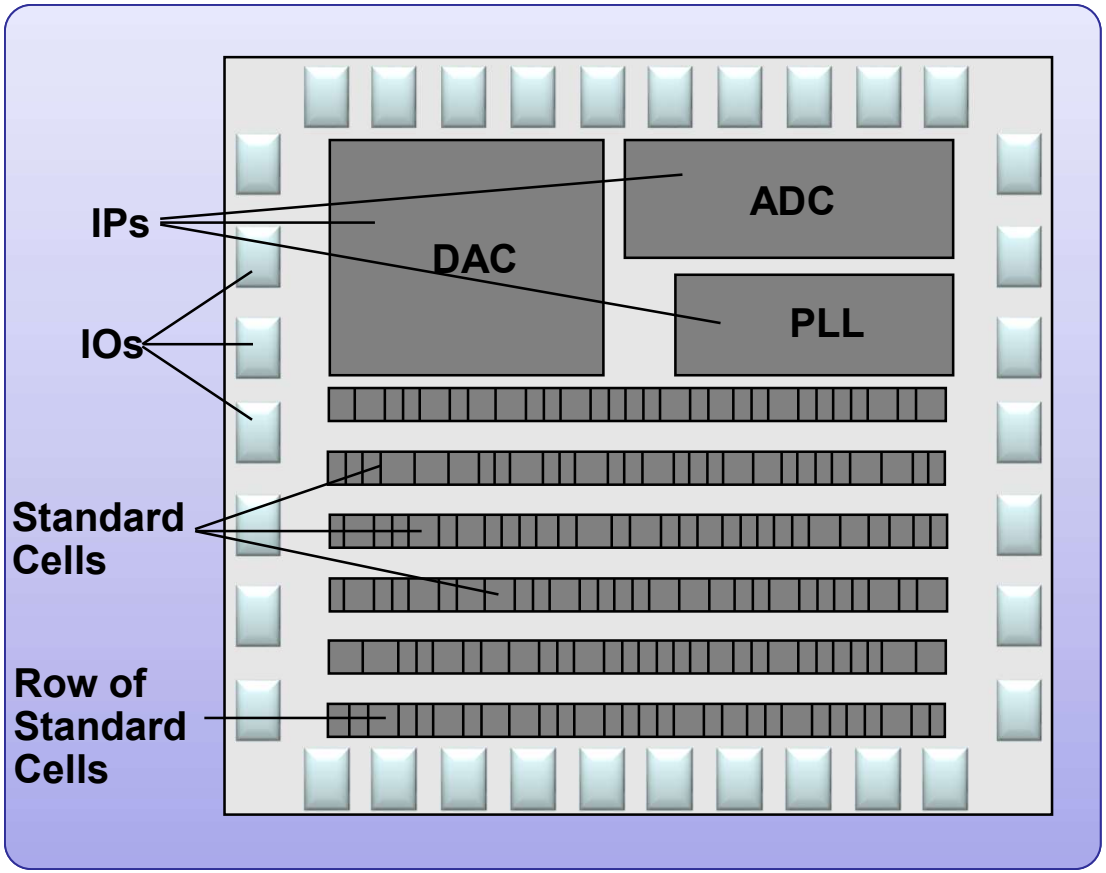
IC Design Flows

- The MOS Transistor
- **Analog and Circuit Design**
- Digital Logic Families
- Productivity Gap
- Digital Design Flows

Typical Chip Design

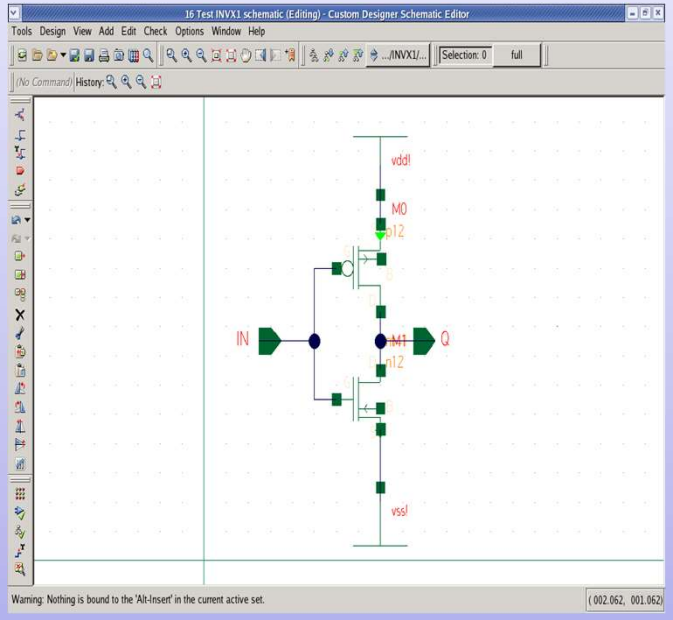


IC Component Types

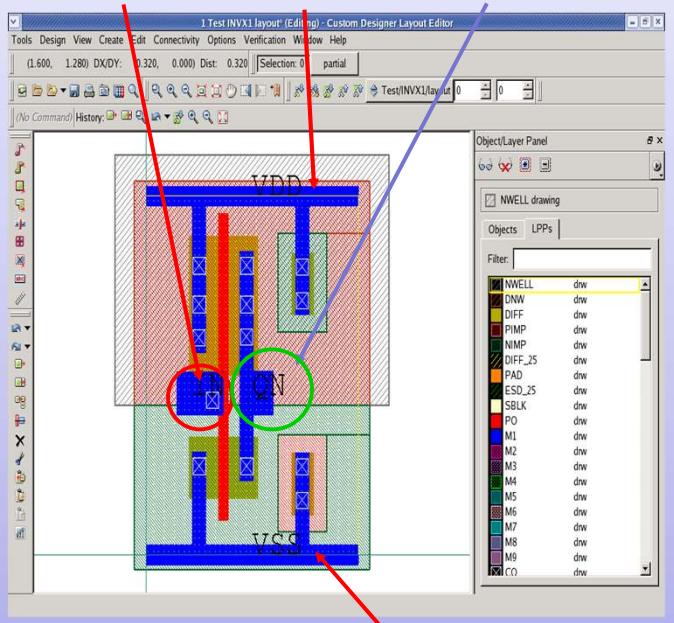


- Intellectual Property (IP) represents large blocks performing completed functions (DAC, ADC, PLL, etc)
- Standard Cells represent digital nodes performing simplest functions.

Circuit and Layout Editors



Circuit

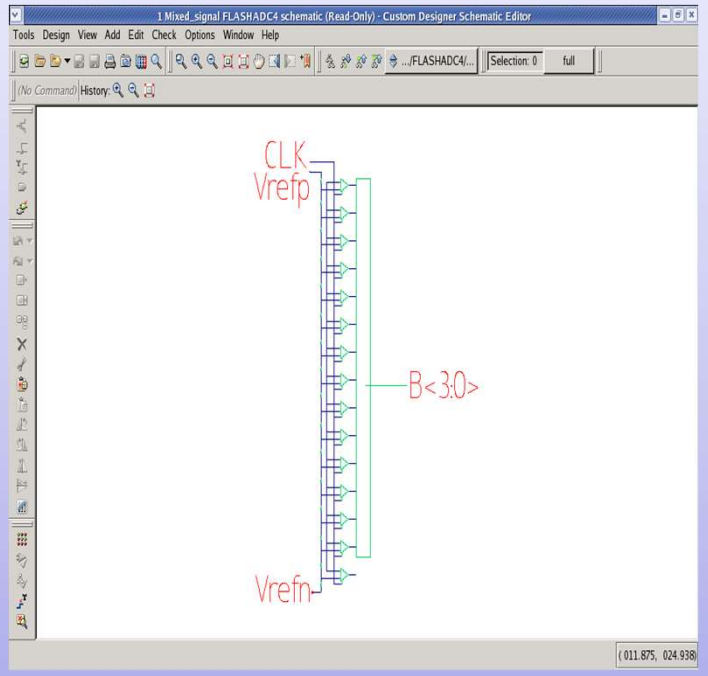


Layout

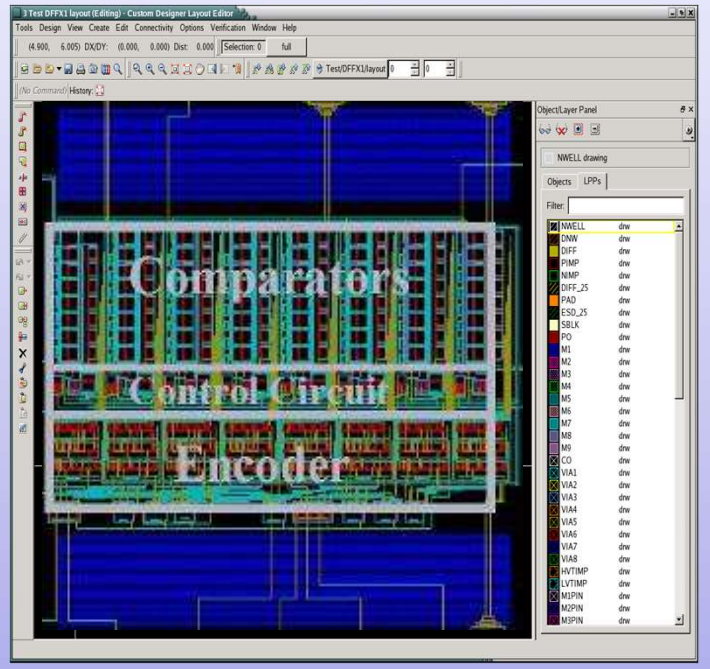
vss

Custom Design Example

FLASHADC4

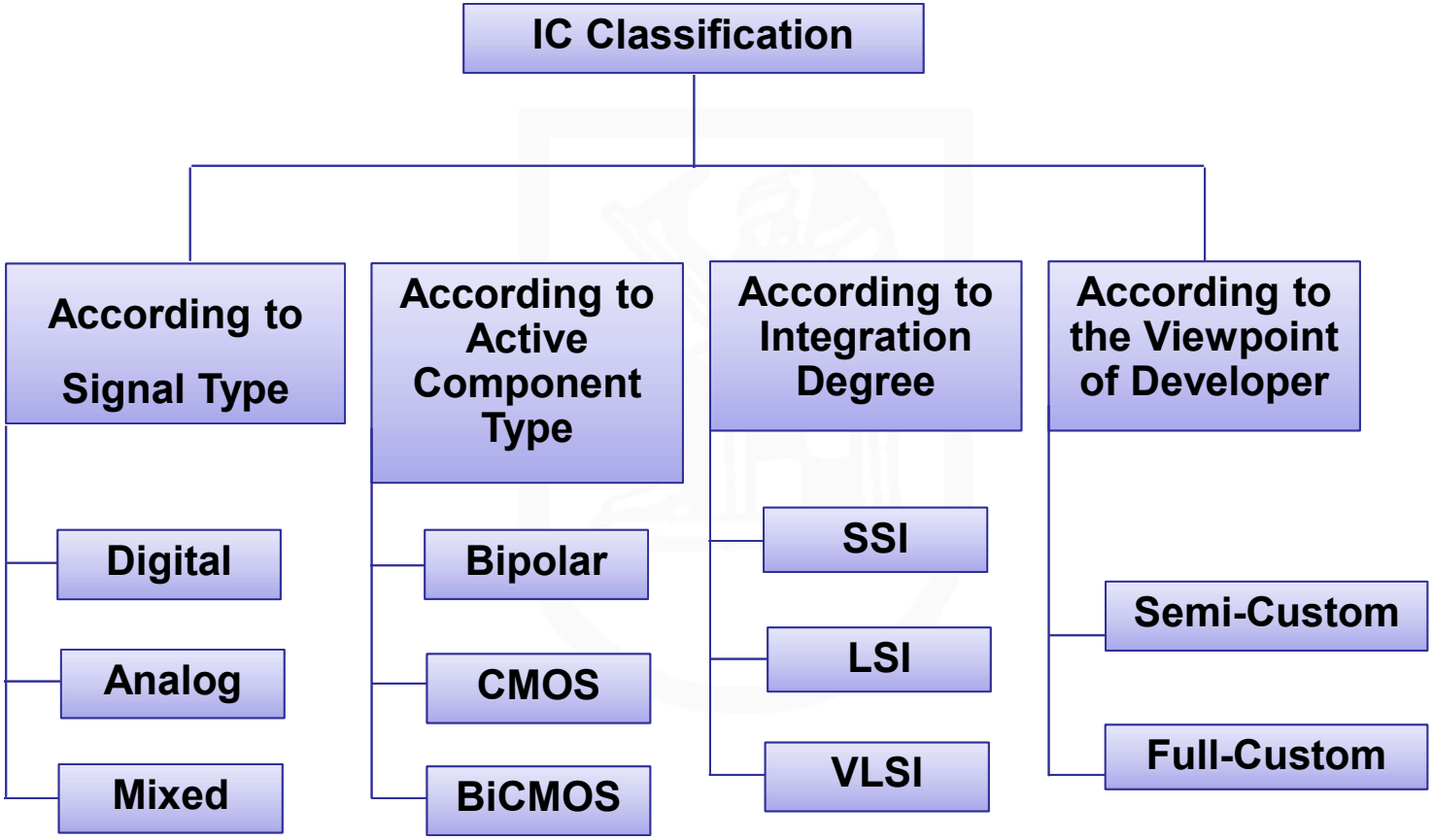


Circuit



Layout

IC Classification



IC Classification: Signal Type

Analog

Electrical levels move up and down continuously

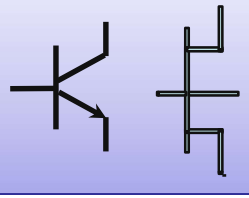
Digital

Electrical levels are either ON (“1) or OFF (“0”)

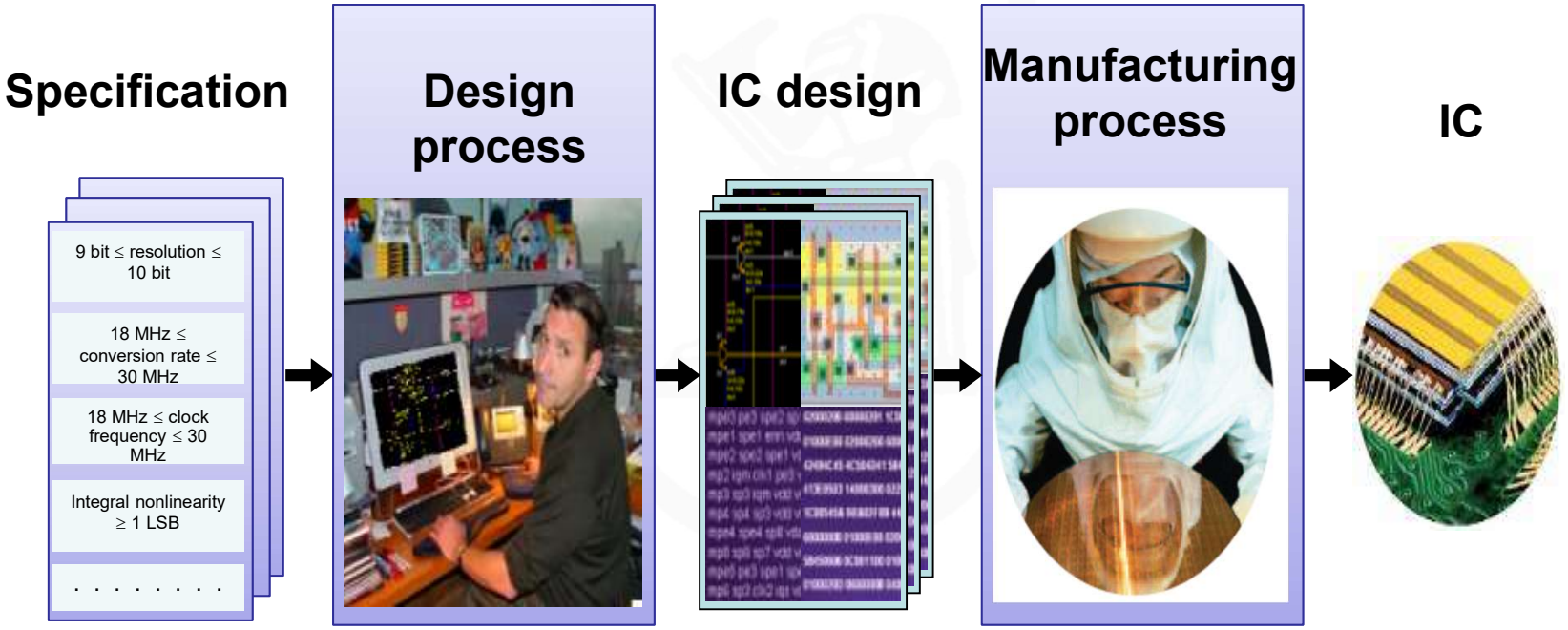
Mixed Signal

Combination of the first two

IC Classification:
Active Component Type

Bipolar		**High performance, large power consumption (..., TTL, ECL)**
CMOS		**Small performance, small power consumption**
BiCMOS		**Provision of compromise between performance and power**

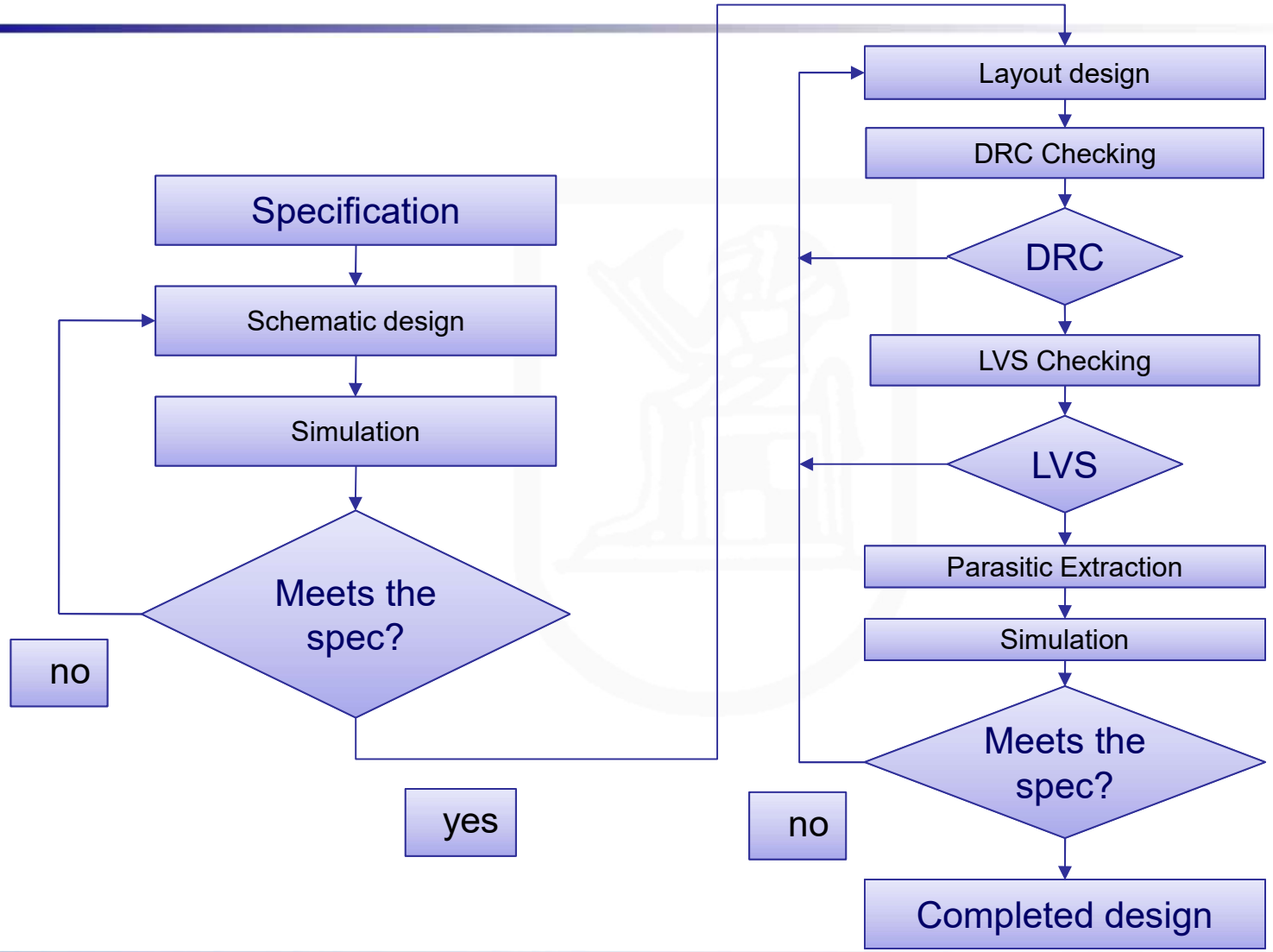
Phases of IC Design



Analog Specification Example

N0	Parameter description	Min	Typ	Max	Units
1.	Process	3.3V IO devices in TSMC 0.11			
2.	Resolution	9		10	Bits
3.	Conversion Rate	18		30	MHz
4.	Input Clock Frequency	18		30	MHz
5.	Integral Nonlinearity			1	LSB
6.	Differential Nonlinearity			0.5	LSB
7.	Gain Error		5		%FSR
8.	Offset error		5		%FSR
9.	Signal to Noise Ratio	56		62	DBc
10.	Harmonic Distortion		-60		DBc
11.	Temperature Drift			12	ppm/C
12.	Reference Voltage		1.25		V
13.	Analog Input Voltage		1.6		V
14.	Power Supply Voltage1	1.08	1.2	1.32	V
15.	Power Supply Voltage2	3	3.3	3.6	V
16.	Power Dissipation		125	180	mW
17.	Operating Temperature	0		125	°C
18.	Spurious Free Dynamic Range			-10	dB
19.	Effective Resolution Band Width		6		MHz
20.	Clock jitter			28	Ps

Analog/Circuit Design Flow



Circuit Selection

- Usually a known circuit structure is selected.
- Design can find a convenient structure which is known to be good for the problem being solved.

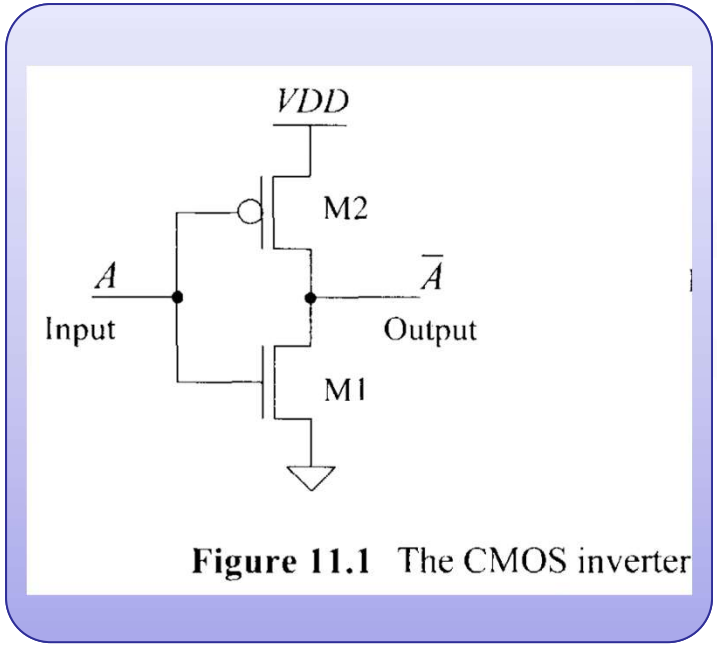
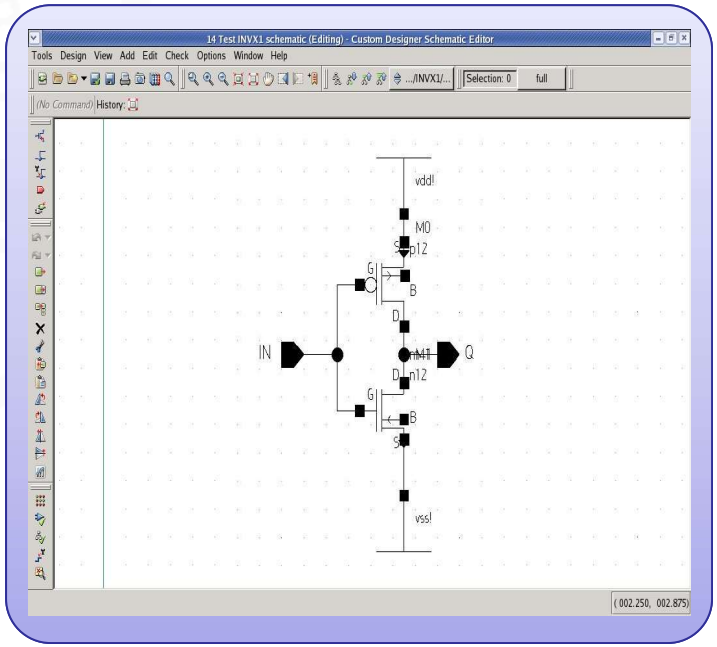
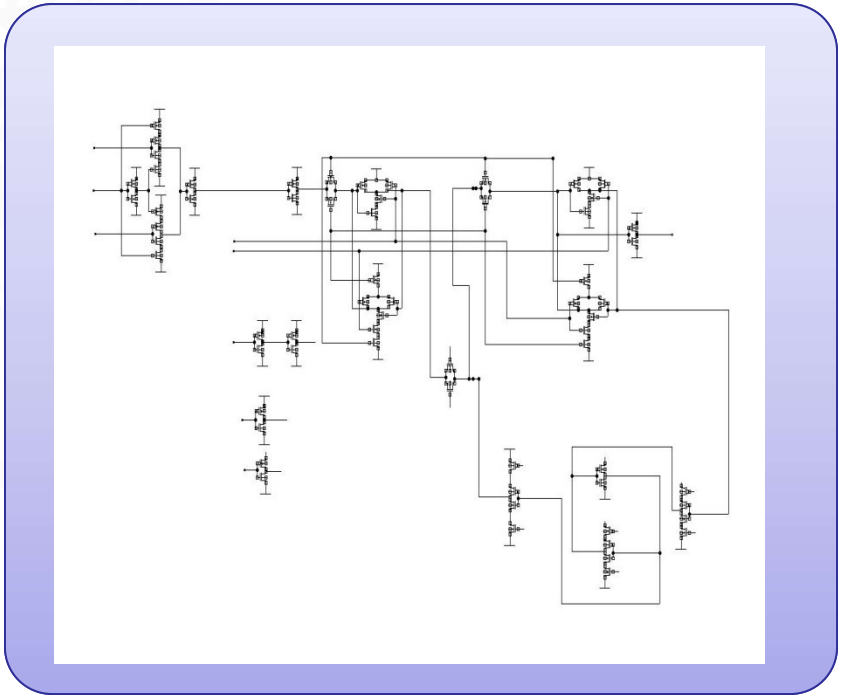


Figure 11.1 The CMOS inverter



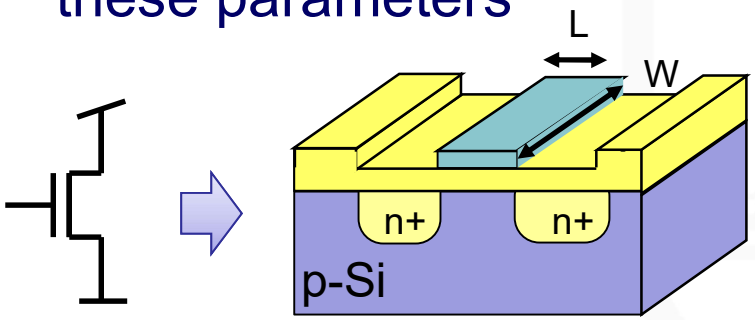
Circuit Design

- All detailed circuits of designed IC are being developed usually at the transistor level.
- The aim of schematic design is to create a circuit which works at operating conditions defined in specification and have the parameter values needed.
- Schematic design
  - Structural synthesis
  - Parametric synthesis
  - Parametric optimization

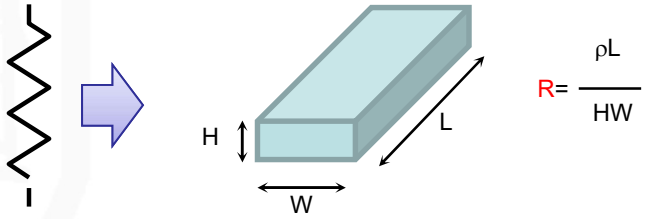


Parametric Optimization

- Each device has configurable parameters
- Schematic designer changes these parameters to get a circuit which meets the spec
- Iterations of changes and spice simulations are used to tune these parameters



W - gate width, L - gate length

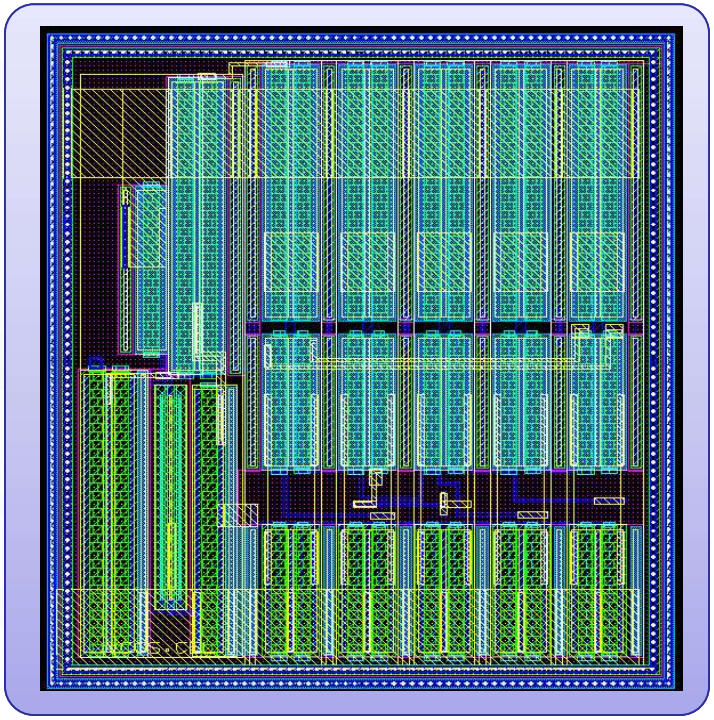


W - resistor width, L - resistor length

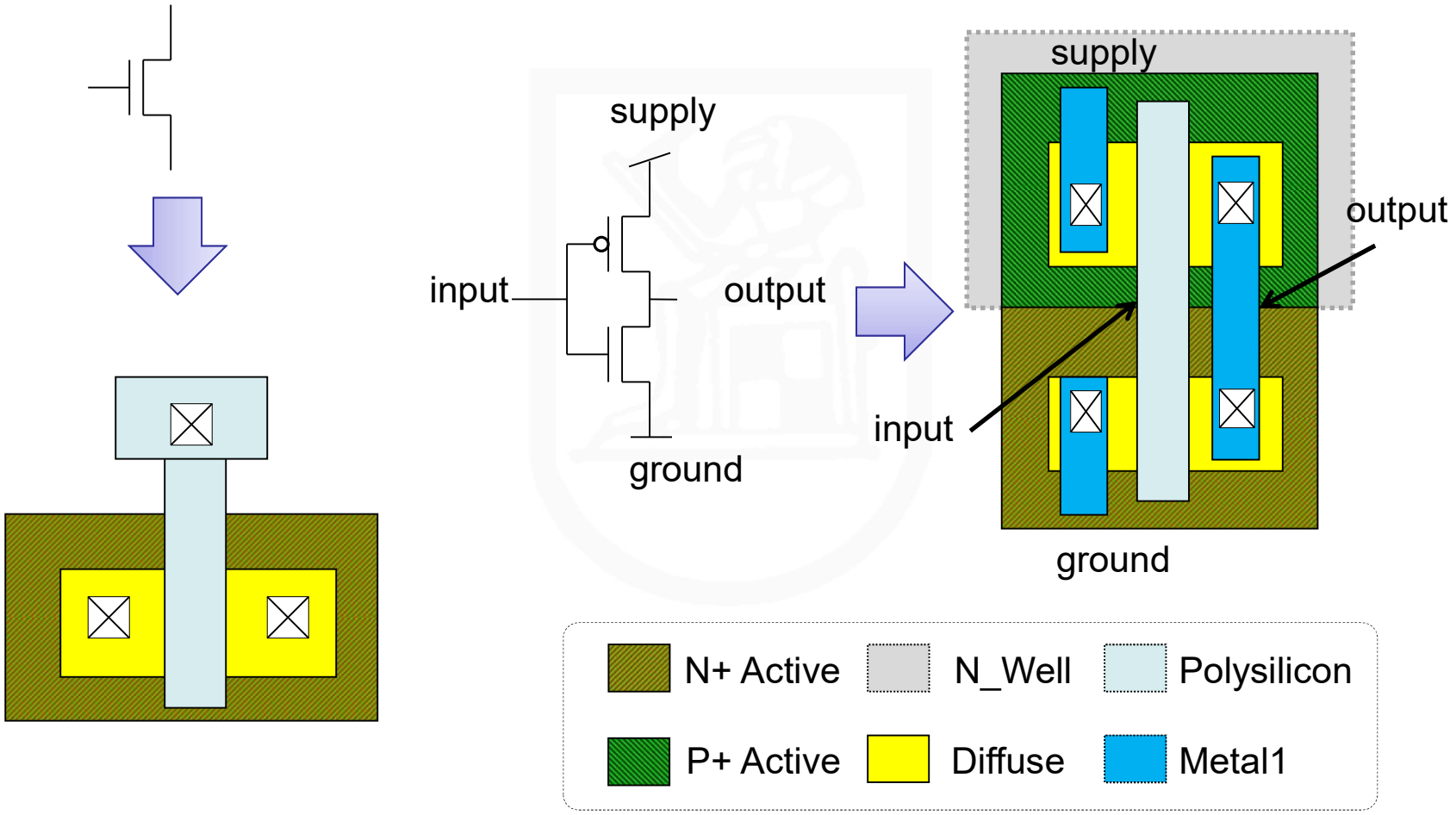
Transistor gate width and length, or resistor dimensions can be changed to change their electrical characteristics.

Physical Design (Layout)

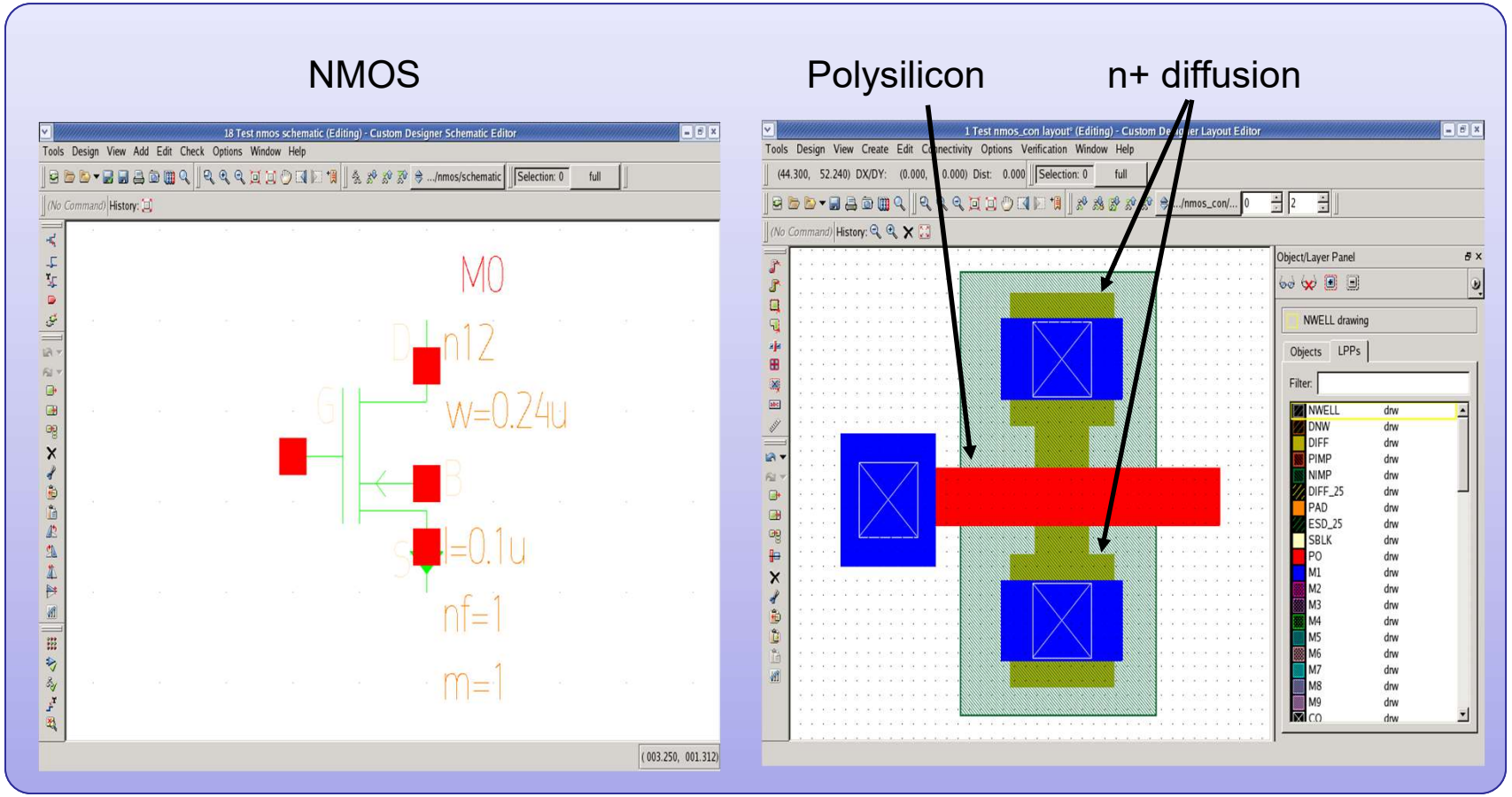
- The construction of the IC or its separate parts is being developed, i.e., geometrical sizes of separate elements, the material, etc.
- Place devices present in schematic and connect to each other according to schematic.
- Do necessary actions to ensure that Layout will not affect circuit operation and does not violate fabrication rules.



Physical Design (Layout)

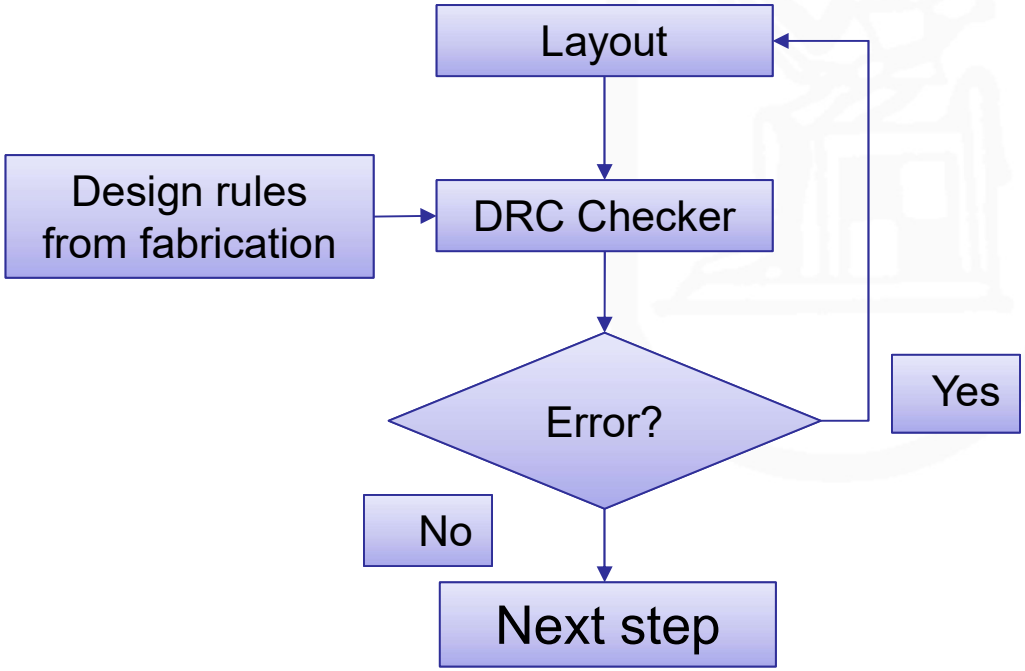


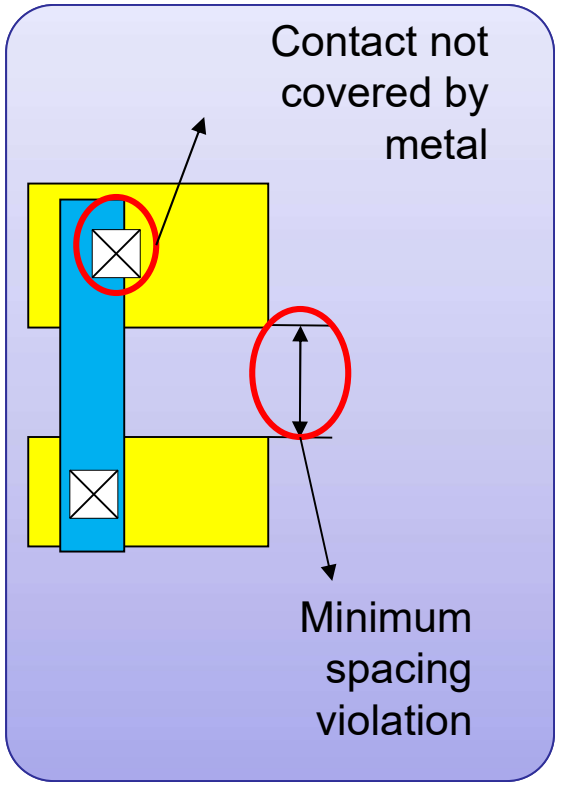
Physical Design (Layout)



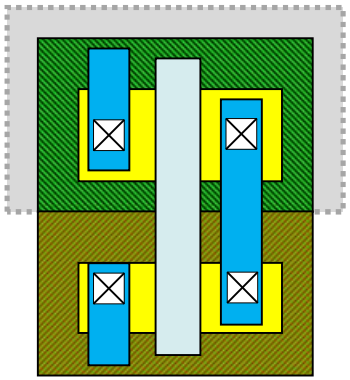
Design Rule Check (DRC)

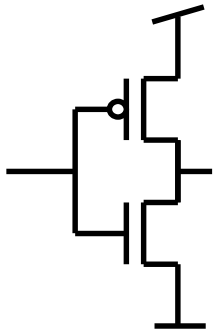
To ensure that Layout does not violate design rules there is a program that can check this

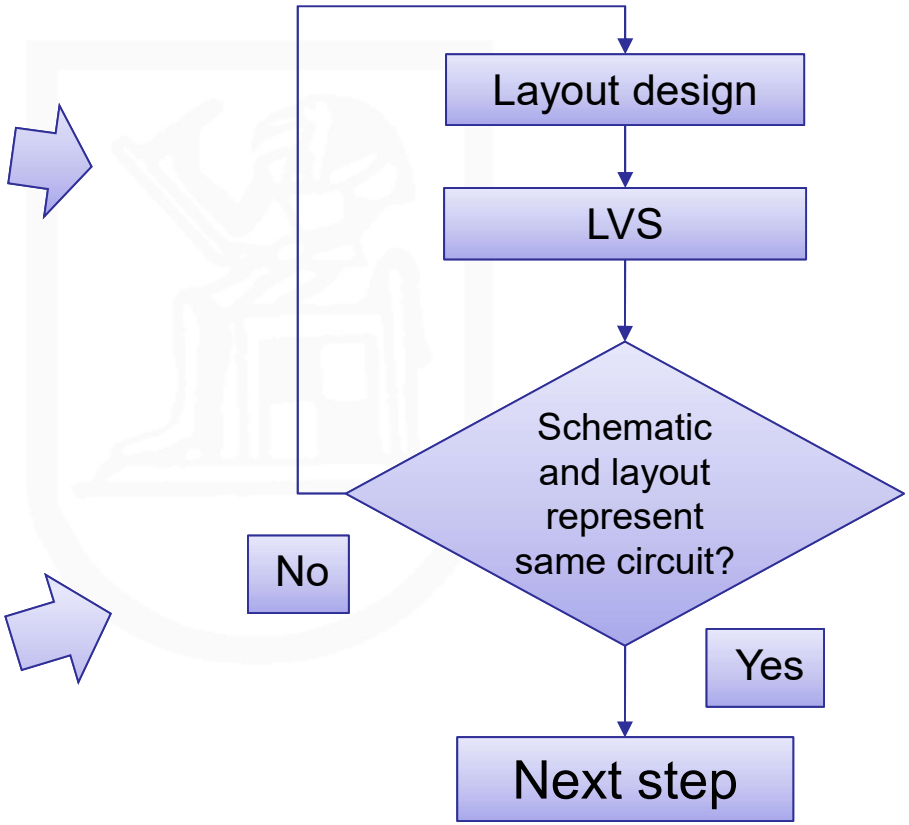




Layout Versus Schematic (LVS)

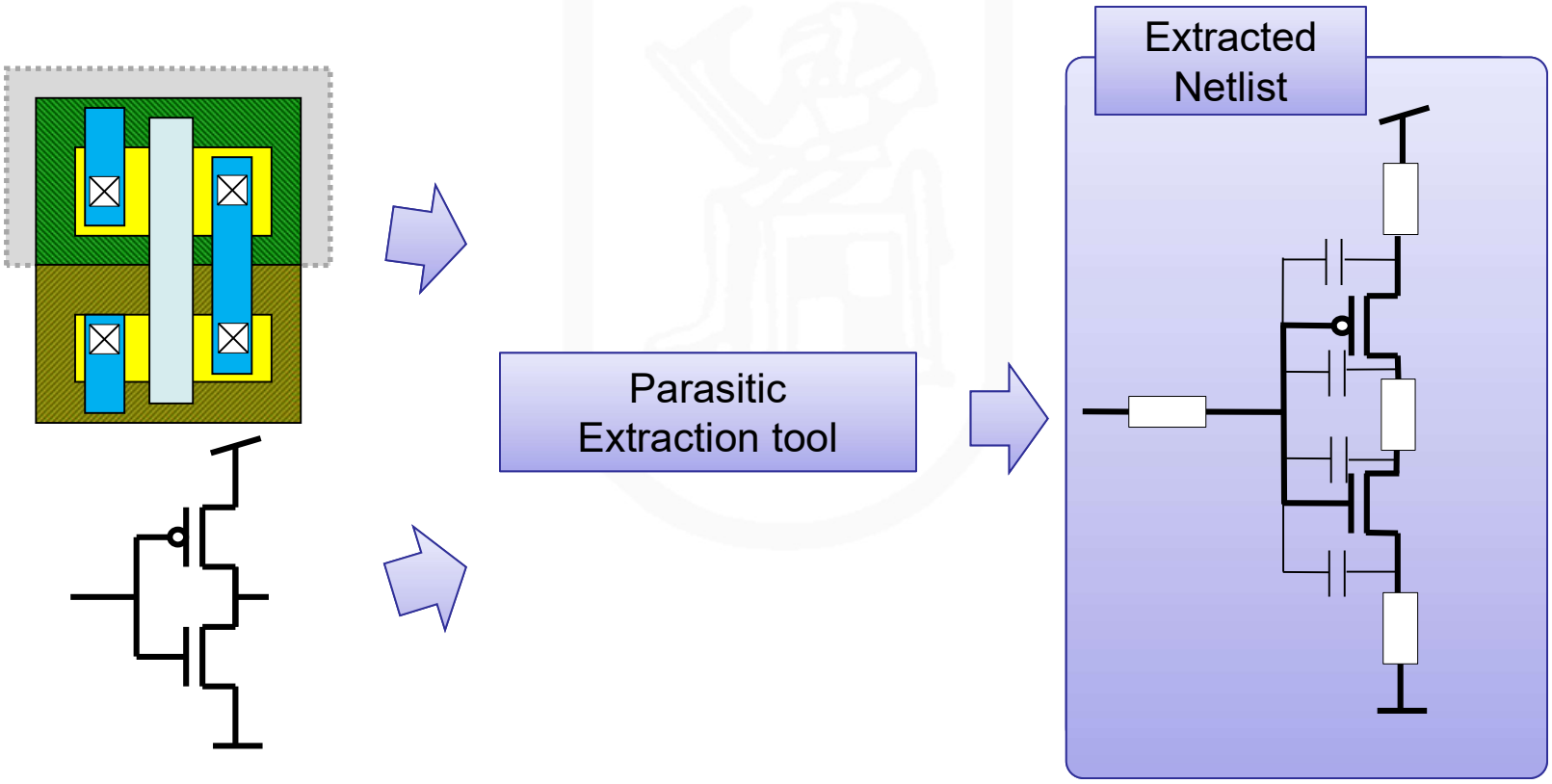






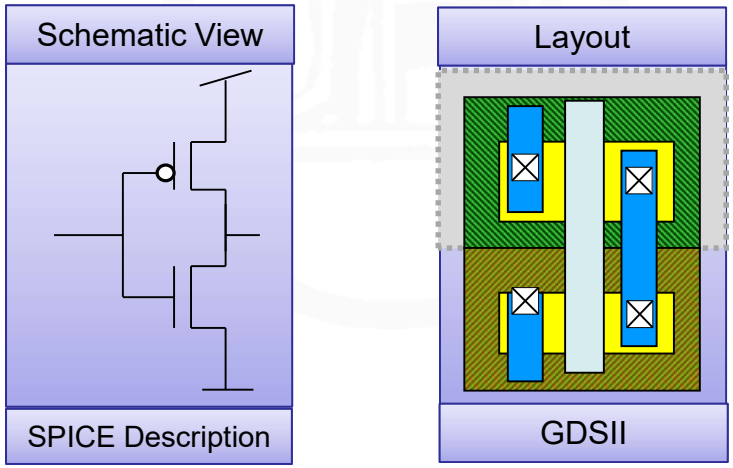
Layout Parasitic Extraction (LPE)

There is a parasitic extractor tool which calculates parasitic devices present in layout adds them back to circuit



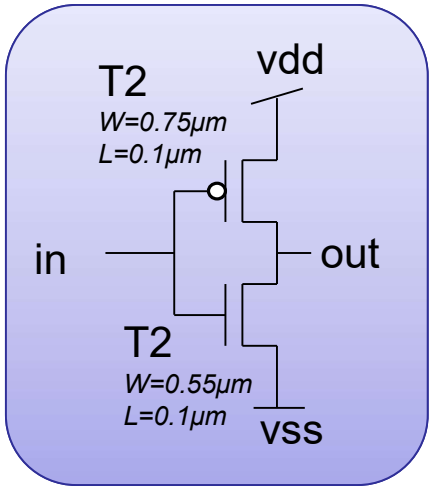
Deliverables

- **Completed design is a set of files which represent different design views:**
  - SPICE netlist format is used to deliver schematic view
  - GDSII binary format is used to deliver layout of the circuit



SPICE Description Example

- **SPICE is a hardware description language (HDL) which enables to describe circuit at device level**
- **It has text-based format that is readable and can be easily modified**

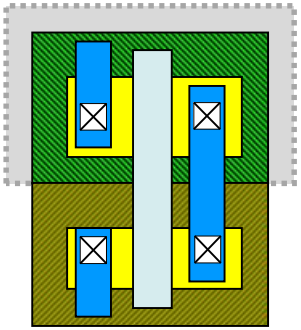


Inverter.sp

```
.subckt inverter
        mt1 out in vdd nmos l = 0.1u w = 0.75u
        mt2 out in vdd pmos l = 0.1u w = 0.55u
.ends
```

An Example of GDSII File

GDSII is binary format, therefore it is not readable



Inverter.gds

```
02000200 60000201 1C000300 02000600 .........`.... 000000
01000E00 02000200 60002500 01000E00 .....%.`..... 000010
42494C45 4C504D41 58450602 12002500 .%....EXAMPLELIB 000020
413E0503 14000300 02220600 59524152 RARY.."......>A 000030
1C00545A 9BA02FB8 4439EFA7 C64B3789 .7K...9D./..ZT.. 00004
60000000 01000E00 02000200 60000205 ...`.........` 000050
58450606 0C001100 01000E00 02000200 .............EX 000060
0100020D 06000008 04000045 4C504D41 AMPLE..... 000070
0000F0D8 FFFF0310 2C000000 020E0600 .....,..... 000080
FFFF204E 00001027 0000204E 00001027 '...N ..'...N .. 000090
0000F0D8 FFFFF0D8 FFFFF0D8 FFFFF0D8 ..... 0000A0
00000004 04000007 04000011 04001027 '..... 0000B0
00000000 00000000 00000000 00000000 ..... 0000C0
```

Test Chip and its Testing

- Samples of designed ICs in a small amount are being prepared.
- With the help of laboratory equipment different input signals are applied to manufactured ICs and the parameters relevant to the specifications are measured.
- In case of meeting all the requirements of the latter, IC large-scale fabrication starts.
- Otherwise, compared with the spec's requirements, the earlier phases of design are carried out to exclude the present incompatibility or problem.