



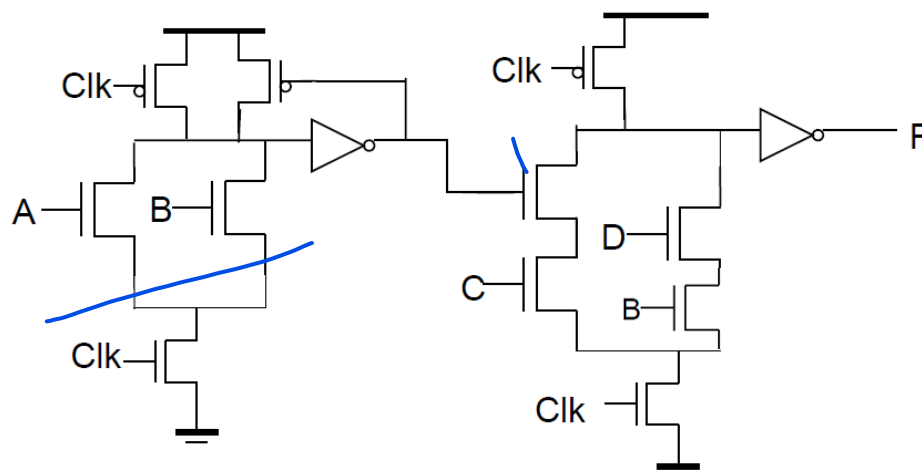
Name:

BN:

Question (1) True or False (wrong answers will be penalized):
(7 marks , min zero , it won't affect other questions)

1. Fabless Companies are limited by the available commercial technologies.
2. The critical dimension of the design is determined by the wavelength of the exposure light and the wafer used in fabrication
3. Self-Aligned gates are fabricated by implanting the wells then developing the gate
4. One disadvantage of the CMOS gates is the high noise margin
→ ✗ Active area defines the n+, p+ and gate regions.
6. Process engineers focus on <u>yield and reproducibility</u>
7. PMOS transistor passes weak zero and strong '1'
8. Scalable design rules are commonly used in industry than micron design rules
9. In NMOS, V_T decreases as the bias decreases (Substrate bias voltage) ✗
10. In Parasitic Extraction stage, it calculates the parasitic devices present in the layout and adds them back to the circuit
11. Dynamic CMOS are simpler, faster gates and have high noise margins.
12. Regenerative property ensures that an <u>attenuated signals returns back to nominal voltage level</u>
13. Domino Logic can implement inverting logic.
14. Footless Domino logic circuits are dynamic mos circuit with only pull up transistor and no pull down network

Question (2) (8 marks)



a) What is the function implemented in the above dynamic circuit?

$$F(A, B, C, D) = (A+B)C + DB$$

b) In the evaluation phase, find all input patterns (A, B, C, D) that will result in charge sharing on the second stage of the domino circuit.

Make sure you show the different capacitance affected on the diagram above.

c) Assuming a p-type substrate and using your color pencils, sketch the optimized Layout for the given function (Hint: use Euler path)

$$F = (A \text{ xor } B) \text{ and } C$$

Metal: Blue Polysilicon: Red n+: Green p+: orange or brown
Contacts and vias: Black Well (indicate whether p or n): Yellow

Take your time and draw something decent. Don't cross wires, Don't forget contacts