Sheet (6)_part1
Chapter 5 – Memory

1) [5.3] For Direct-Mapped Cache design with a 32-bit address, the following bits of the address are used to access the cache

Tag	Index	Offset
31–10	9–5	4–0

- What is the cache block size (in words)?
- How many entries does the cache have?
- What is the ratio between total bits required for such a cache implementation over the data storage bits?

2) Starting from power on, the following byte-addressed cache references are recorded.

Address											
0	4	16	132	232	160	1024	30	140	3100	180	2180

- How many blocks are replaced?
- What is the hit ratio?
- List the final state of the cache, with each valid entry represented as a record of <index, tag, data>

3) Consider the following program and cache behaviors.

Data Reads per 1000 Instructions	Data Writes per 1000 Instructions	Instruction Cache Miss Rate	Data Cache Miss Rate	Block Size (byte)
250	100	0.30%	2%	64

- For a write-through, write-allocate cache, what are the minimum read and write bandwidths (measured by byte per cycle) needed to achieve a CPI of 2?
- For a write-back, write-allocate cache, assuming 30% of replaced data cache blocks are dirty, what are the minimal read and write bandwidths needed for a CPI of 2?
- What are the minimal bandwidths needed to achieve the performance of CPI=1.5?