Cairo University
Faculty of Engineering
Computer Engineering Dept.

جامعة القاهرة

25.5

Computer Architecture
(CMPN3010)
Midterm Fall2021

Name: [redacted]

Answer ALL Questions (Full Mark 40 points) **Time Allowed: 75 mins**

Question 1: True/False, Correct the false statements (10 points): 8.5

1- There are 2 types of pipeline hazards only: data, and control hazards. (F)

There are 3 types of pipeline hazards : structural, data, and control hazards

2- The one-bit predictor is an example of a static branch predictor, while the two-bit predictor is an example of a dynamic branch predictor (F)

The one-bit ------ of a dynamic branch Predictor

3- Load-use hazards cannot benefit from forwarding at all. (F)

" " " can benefit from forwarding to reduce the stalling cycles. - here i only stall for one cycle

4- A forwarding unit is responsible for forwarding the appropriate operands when a data dependency that can be solved with forwarding is detected. (T)

5- We have two machines with different implementations of the same ISA. Machine A has a clock cycle time of 10 ns and a CPI of 2.0 for program P; machine B has a clock cycle time of 20 ns and a CPI of 1.2 for the same program. A is 50% faster than B. (F)

$\frac{E_{TB}}{E_{TA}} = \frac{I_C * CPI \times CT}{I_C * CPI * C.T} = \frac{1.2*20}{2*10} = 1.2$ Then A is 20% faster than B

6- When an exception arises in a pipelined processor, all the instructions within the pipeline are finished completely before switching to the exception handling routine. (F)

we switch imediatly to the exception handling routine

7- Program P runs on computer A in 10 seconds. Designer says clock rate can be increased significantly, but total cycle count will also increase by 20%. The clock rate that we need on computer B for P to run in 6 seconds is 200 x 10^9 Hz (Clock rate on A is 100 MHz). (T)

$E = \frac{\#C}{CR}$

$E_A = 10s \quad CR_A = 100MHz \quad \#C_A = E_A * CR_A = 10^{12}$

$E_B = 6 \quad CR_B = 200MHz \quad \#C_B = E_B * CR_B = 1.2 * 10^{12}$

$C_B = 1.2 C$

8- An instruction placed in the branch delay slot is only executed if the branch is not taken. (F)

is executed even if the branch is Taken

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9- Pipelining is used to improve the throughput of the entire workload by minimizing the single task latency. (F)

by minimizing the average CPI, - Pipelining doesn't help the Single Task Latency.

10- In the delayed branch technique, the compiler adds a branch prediction bit to the instruction to inform the processor whether to predict the branch as taken or untaken. (F)

-0.5

Question 2 (10 points):

1- Consider a program of 700 instructions categorized as in the following table. It is required to compare the execution of the program onto two different processors. The clock rates of the two processors are 1.5GHz and 2GHz, respectively. The CPI of different instruction categories on the two processors is also included in the table.

Instruction category	Number of instructions of different categories in the program	Processor 1: CPI of different categories	Processor 2: CPI of different categories
ALU	500	1	2
Load	100	2	2
Store	50	3	2
Branch	50	4	2

8

$CR_1 = 1.5\,GHz \qquad CR_2 = 2\,GHz$

a- [2 points] Which processor do you select for this program? both are the same

$$E_1 = \frac{\#cycles}{CR_1} = \frac{(500*1)+(100*2)+(50*3)+(50*4)}{1.5} = 700$$

$$E_2 = \frac{\#cycles}{CR_2} = \frac{(500*2)+(100*2)+(50*2)+(50*2)}{2} = 700$$

2

b- [2 points] If the number of load instructions is reduce by half, which processor do you select for the program?

load instructions = 50

$E_1 = 633.33$

$E_2 = 650$

2

→ The first processor is faster

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2- During the execution of a program, conditional branches have been executed 20 times.
The traces of taken (T) and Not-taken (NT) of each branch are listed below:
T- T- NT- T- T- T- NT- T- T- NT- NT- NT- T- T- T- NT- T- T- T- NT

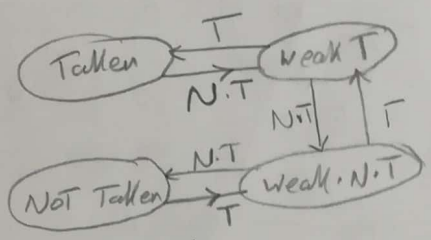
a. [2 points] What is the branch prediction accuracy of **Always Taken** predictor?

number of Taken branches = 13 , number of not Taken = 7 Total = 20
-assume always Taken
- accuracy = $\frac{\text{no of Taken}}{\text{Total}} \times 100 = 65\%$

b. [2 points] What is the branch prediction accuracy of **1-bit predictor** ?(the initial prediction of the 1-bit dynamic branch predictor is **Taken**):

number of right Predictions = 11
accuracy = $\frac{11}{20} \times 100 = 55\%$

c. [2 points] What is the branch prediction accuracy of **2-bit predictor**? (the initial prediction of the 2-bit dynamic branch predictor is **Weak Untaken**):



number of right predictions

Question 3 (10 points):

Consider the following MIPS assembly code:

```
LD R1, 45(R2)
ADD R7, R1, R5
SUB R8, R1, R6
OR R9, R5, R1
BNEZ R9, target    // NOT TAKEN
ADD R10, R8, R5
SW R10, 0(R9)
XOR R2, R10, R4
```

Read after write
Read after write
Use MIPS Six-stage pipeline (Fetch, Decode, EX1, EX2, Memory, Write-back). Assume the following:

- Register file writes in the first half of the clock cycle and reads in the second half cycle.

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- Branch is predicted perfectly (No Control Hazards).
- 1 Memory for instructions and data. → Structural Hazard
- **Both EX1 and Ex2 stages uses the ALU. Data will be ready after EX2**

9

FDE1E2MW

a. [2 points] Calculate how many clock cycles will take execution of this segment on the regular multi cycle (non-Pipelined) architecture (Assume Branch decision is known at EX2). Show calculations.

1- LD operation → Takes 6 stages, 2-Alu operations Takes 5 stages FDE1E2W
3- SW // Takes 5 stages, branch operation Takes 4 stages FDE1E2
FDE1E2M

2

Total number of cycles = (1*6) + (5*5) + (1*5) + (1*4) = 40 cycles

b. [4 points] Show how the above instructions will progress through this 6 stages pipe in case of **NO FORWARDING**. What is the number of cycles required to execute the above program? Calculate the Speedup of the pipelined processor compared to the non-pipelined processor (a).

3

- LD R1, 45(R2)
- ADD R7, R1, R6
- SUB R8, R1, R6
- OR R9, R5, R1
- BNEZ R9, Target
- ADD R10, R8, R5
- SW R10, 0(R9)
- XOR R11, R10, R4

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17

FDE1E2MW
FDDDE1E2MW
**FDE1E2MW
FDE1E2MW
FDDDDE1E2MW
PPPFDE1E2MW
PPPFDDDE1E2MW
PPPFDDDE1E2MW

* Circle refers to a bubble

n* cycles = 22

Speed up = 40/22 = 1.818

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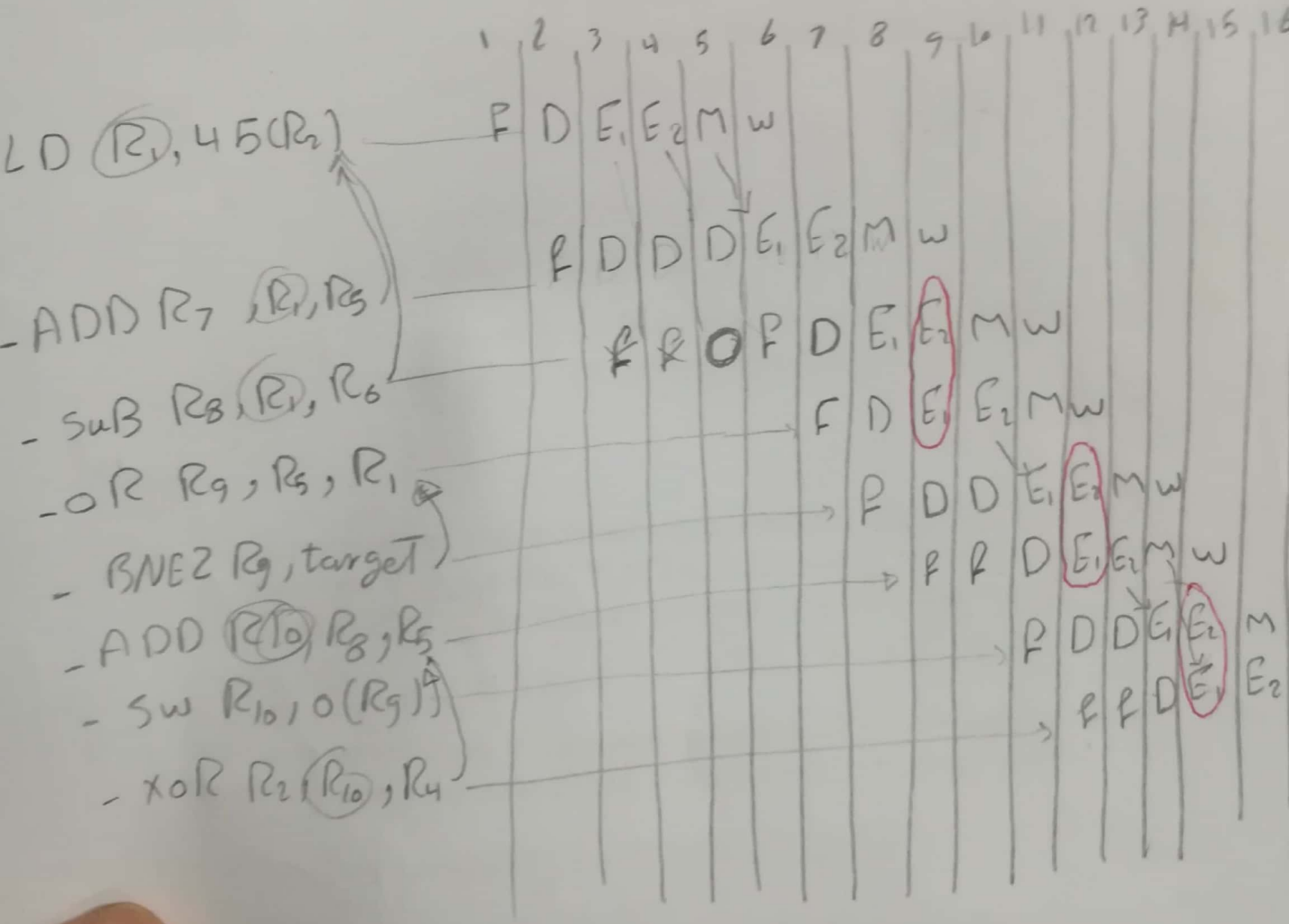
c. [4 points] Show how the above instructions will progress through this 6 stages pipe in case of **FULL FORWARDING**. What is the number of cycles required to execute the above program? Calculate the Speedup of the pipelined processor compared to the non pipelined processor (a).



n x = 18

Speedup = $\frac{40}{18}$

3

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