Sheet (5)
Chapter 4 – Superscalar Processor

1) If ADD/SUB take 1 cycle, LD/SW take 2 cycles (1 cycle for address calculation, 1 cycle for mem access), and MUL takes 7 cycles to execute, then:

a. What would be the first instruction to complete using Tomasulo's algorithm on the following program? Given infinite number of reservation station

```
MUL R6, R4, R8
ADD R2, R6, R7
SW R2, 8(R6)
ADD R2, R3, R4
SUB R4, R5, R2
LD R4, 16(R4)
ADD R1, R2, R3
```

b. How does register renaming help the "SW" instruction save the correct R2 value to the memory while still allowing later instructions to execute?

2) Assume that MUL takes 4 cycles, SUBI/BNEZ takes 1 cycle, SW take 3 cycles, and 1st LD takes 8 cycles while 2nd LD takes 1 cycle.
Show 2 iterations of the following program

```
Loop:  LD F0, 0(F1)
       MUL F4, F0, F2
       SW F4, 0(F1)
       SUBI F1, F1, 8
       BNEZ F1, Loop
```

Instruction status:

ITER	Instruction	*j*	*k*	*Issue*	*Comp*	*Result*

	Busy	*Addr*	*Fu*
Load1	No		
Load2	No		
Load3	No		
Store1	No		
Store2	No		
Store3	No		

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Reservation Stations:

Time	*Name*	*Busy*	*Op*	*Vj*	*Vk*	*Qj*	*Qk*	*S1*	*S2*	*RS*
	Add1	No								
	Add2	No								
	Add3	No								
	Mult1	No								
	Mult2	No								

Register result status

Clock	**R1**		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
0	**80**	*Fu*									

Load=8,1 Add=3 Mult=4 SUBI/BNEZ=1 Store=3

3) Assume that the superscalar processor has the following property:

a. 2 RESERVATION STATIONS (RS1, RS2) + **2 LOAD/STORE FU (LDU1, LDU2) (that means that you have 2 caches, not one memory) with latency 2 cycles.**

b. 2 RESERVATION STATIONS (RS3, RS4) + 2 ALU/BR FU (ALU1, ALU2) with latency 1 cycles

c. Static branch prediction for backward branches: "always taken"

Complete the following table using Tomasulo's algorithm

Instruction	Issue	Exe	WB	Hazard Type	FU	Src1	Src2	Dst
L1: LD R2, 0(R4)								
ADDI R2, R2, 1								
LD R3, 100(R4)								
ADDI R3, R3, 1								
ADD R5, R2, R3								
SW R5, 200(R4)								
ADDI R4, R4, 1								
BNE R4, R7, L1								

Calculate the speedup with respect to the simple 5-stage pipelined processor where, execution of LD/SW takes 2 * cycles time of the current processor, execution of ADD/SUB takes 1* cycles time of the current processor. (thus what is the pipleline cycle time ?)