Computer Engineering Department
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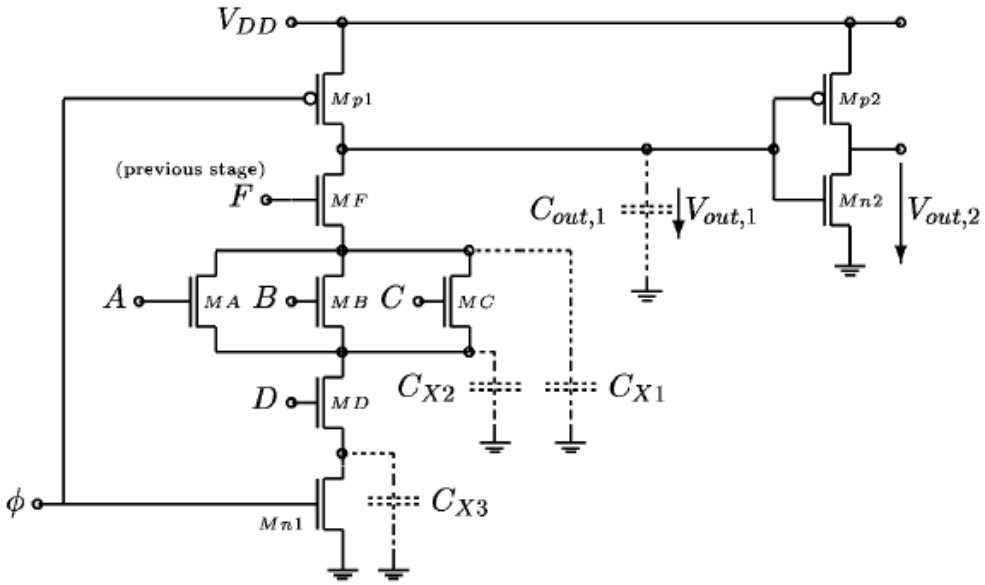
CMP3020 VLSI Design **Problem Set #2**

Problem #1:

The function: $Z = A\,(B + C + D + E + F)$

Must be implemented using domino logic. Could charge sharing effects occur? If yes, how can they be avoided?

Problem #2:



All input variables in the above circuit come from domino logic blocks, so that immediately after the precharge we have: $A = B = C = D = F = 0V$.

For which possible $0 \rightarrow 1$ transitions has the charge sharing effect the greatest influence?

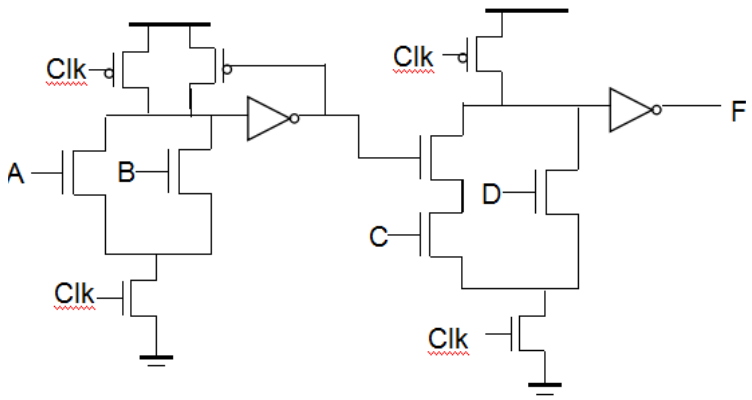
Problem#3

Suppose we wish to implement the two logic functions given by $F = A+B+C$ and $G=A+B+C+D$. Assume both true and complementary signals are available.

a) Implement these functions in dynamic CMOS as cascaded stages so as to minimize the total transistor count using dominos logic with pull-down only networks.

b) Implement these functions in dynamic CMOS as cascaded stages so as to minimize the total transistor count using dominos logic with alternating pull-down & pull-up networks.

Problem #4:



a) What is the function implemented in the above dynamic circuit?
F(A, B, C, D) =

b) In the evaluation phase, find all input patterns (A, B, C, D) that will result in charge sharing on the second stage of the domino circuit.
Make sure you show the different capacitance affected on the diagram above.