

Problem 1)

a) Roles in the Supply Chain of Semiconductor Industry

1. IC Design House

IDM	→ ^{No longer} IDM	Fabless (only design)
Intel, IBM, TI, Samsung, MagneChip	*	Qualcomm, AMD, Broadcom, Nvidia, MediaTek

2. IC Manufacturing

IDM	Pure Play (only manufacture)
Intel, IBM, TI	TSMC, UMC, SMIC,
Samsung, MagneChip	Global Foundries ↴ largest in China ↳ bought AMD's

3. EDA Vendors

Mentor Graphics, Cadence,
Synopsys, Magna (now Synopsys)

4. IC Design Service Companies

HCL Tech, Wipro, Tata Elxsi

5. IP Providers

ARM, MIPS

6. Packaging & Testing

ASE, Jittronware, Amkor

7. Wafer manufacturing

Siltronic, SUMCO

8. Equipment vendor*

Novellus, Hitachi

b) IC Design Services, because

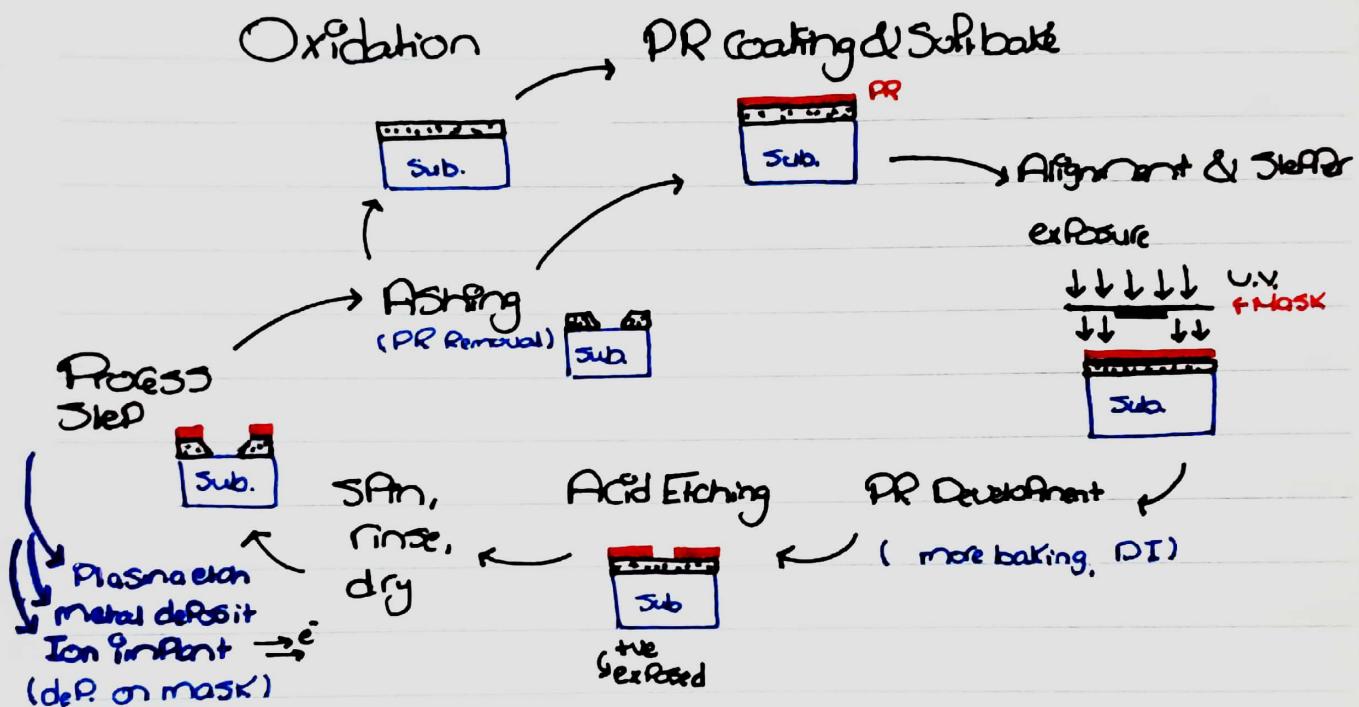
- It takes significant design experience + being well known and close to the market to compete as an IC Design Design House (Fabless Company)
- Other manufacturer-related roles require 365/24/7 operation and quick adaptations to technology (IC Manufacturing)
- The EDA vendors market is very well known and saturated
- Intellectual Property also requires being close to the market (along with innovation that gives an edge in price / features to compete)

c)

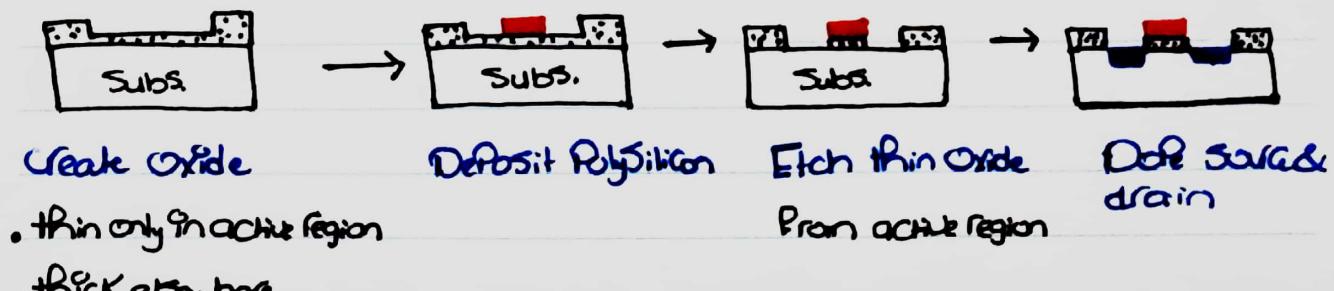
- Year One, the Company Starts as a design service. It can take its design skills while it gets closer to the market and gains more experience which will eventually pay the way for other roles such as IT providers or going public.

Overall, it can be a risky decision for a startup company unless the firm has a strategic objective

Photolithographic Process



SelP-Aligned Gates



→ Because the gate is considered as our mask the source and drain are self-aligned to the gate (it's self-aligned in that we didn't have to align a separate active mask to the gate to create the source and drain)

Design Rules

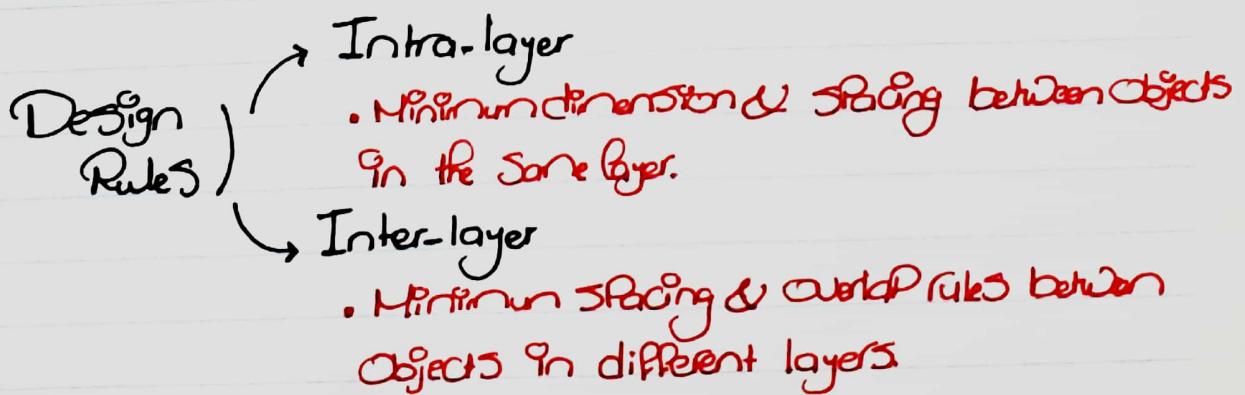
- Needed to tolerate fabrication errors such as mask misalignment, dust, rough surface, parametric defects.

Scalable Design Rules

- all rules are a function of one parameter λ
 - λ is specific to the process, typically critical dim. = 2λ
- Although scalable, it's only over a limited range (linearly)

Absolute Design Rules

- rules are expressed in absolute physical units (e.g. $CD = 7\text{nm}$)
- They are better because they help exploit the process features to the max.



Examples)

Intra-layer

- minimum spacing between two metals in the same layer
- minimum PolySilicon width

Inter-layer

- minimum spacing between PolySilicon & clear part of diffusion
- minimum spacing between metal and a PolySilicon line which is not electrically connected to.

2) iii)

Onha-layer

Onha-layer

- min enclosure of Contact = 0.3 x 0.3 = 0.09
- max overlap = 0.44 = 0.14
- min overlap of Contact = 0.14

$$3) t_{\text{su}} = 100 \text{ ps} \quad t_{\text{jitter}} = 25 \text{ ps}$$

$$t_{\substack{\text{cq} \\ \text{max}}} = 150 \text{ ps} \quad t_{\substack{\text{cq} \\ \text{min}}} = 100 \text{ ps}$$

a) Ignoring skew, we have

$$\overline{T}_{\text{ar}} = t_{\substack{\text{cq} \\ \text{max}}} + t_{\substack{l \\ \text{max}}} + 2t_{\text{jitter}} + t_{\text{su}}$$

$$= 150 + 0 + 2 \times 25 + 100 = 300 \text{ ps}$$

Hence, $P_{\text{avg}} = 3.3 \text{ GHz}$

b) At any frequeny (ignoring skew)

$$t_{\substack{\text{cq} \\ \text{min}}} + t_L > t_{\text{head}} + S$$

Hence, $t_{\text{head}} < 100 \text{ ps}$

100 + 300 + 100 051 + 003 + 051
150

100 + 000 + 100 75 + 300 + 100
250 + 300 + 150

BEEH

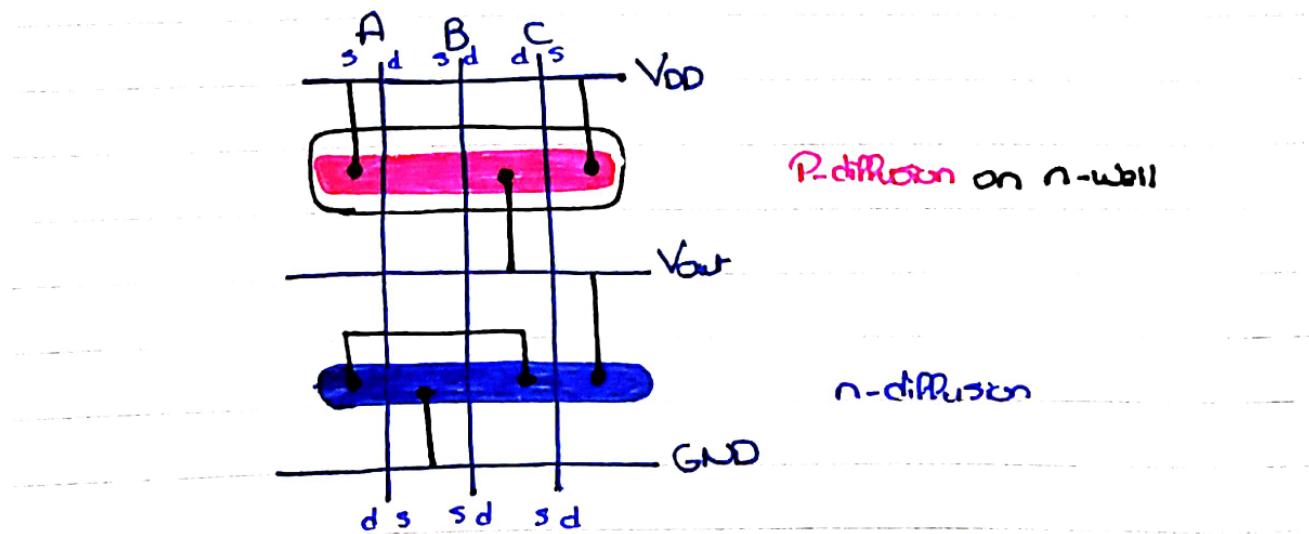
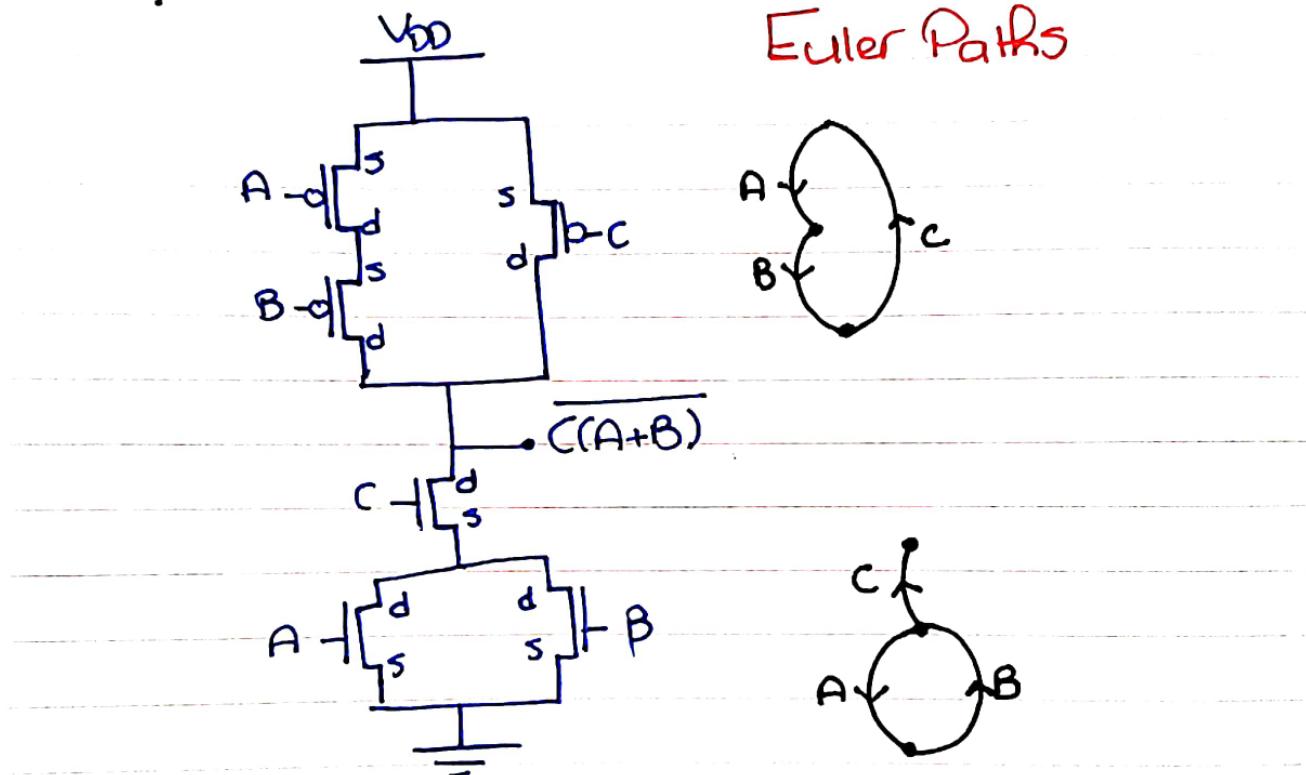
001 + 5t + 5t 051 + 5t + 150
250 + 50 + 150

Boat - Boat - Boat
Boat - Boat - Boat

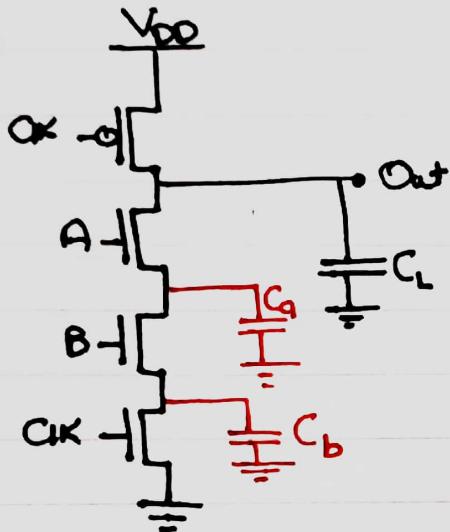
e)

Problem 4)

a)

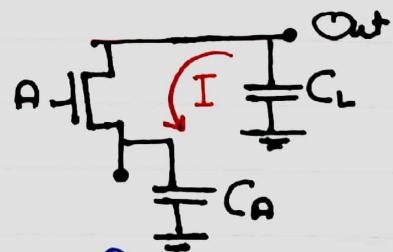


4) b)



• Let initially
 $A = B = 0, Q_A = 0$

then at evaluation if
 $A = 1$ and $B = 0$ the
 circuit becomes

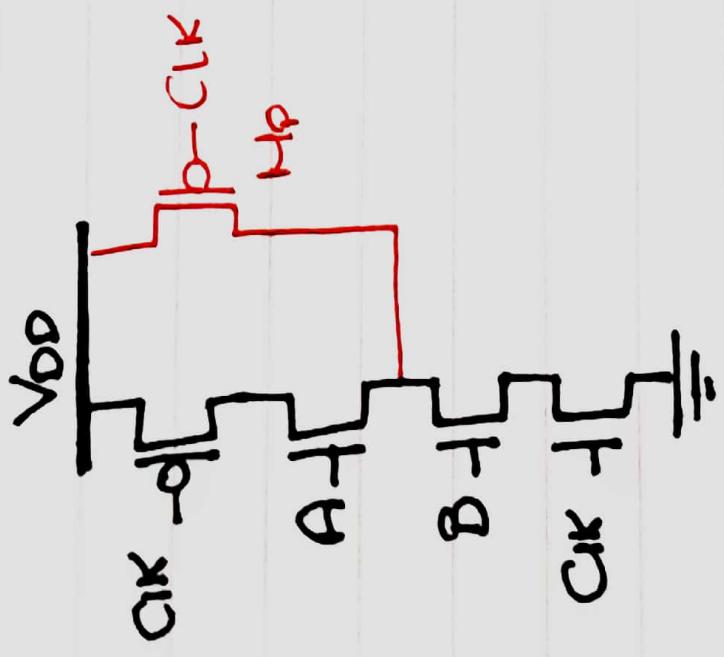


- Due to charge conservation, the output level will go below V_{DD} during evaluation as the charge on C_L gets shared with C_A.

$$\begin{aligned} Q_{\text{initial}} &= Q_{\text{evaluation}} \\ C_L V_{DD} &= C_L V_F + C_A V_F \end{aligned}$$

Hence, the final output level is $V_F = \frac{C_L}{C_L + C_A} V_{DD} < V_{DD}$

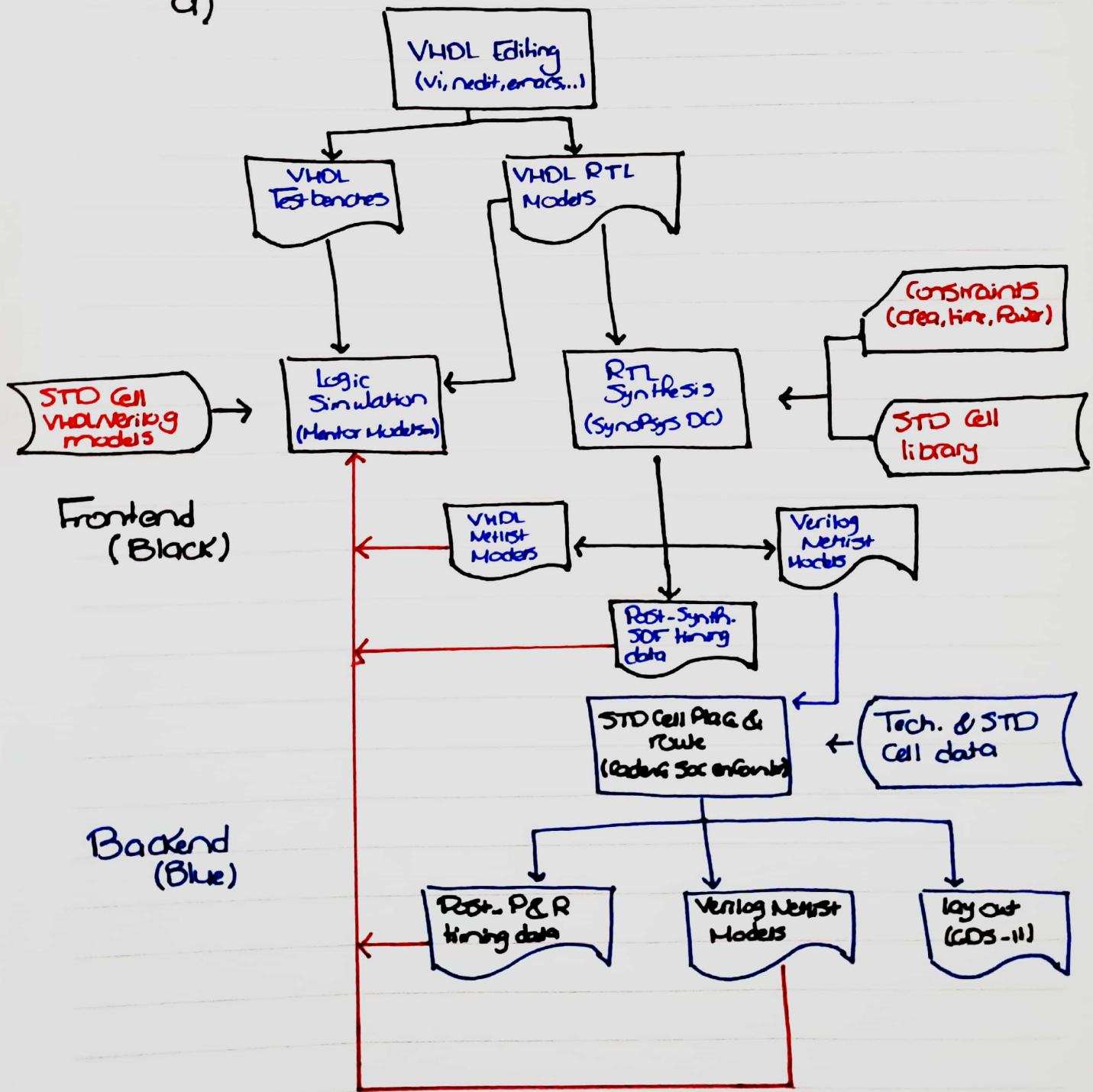
Circuit to solve Pre charge Sharing Problem



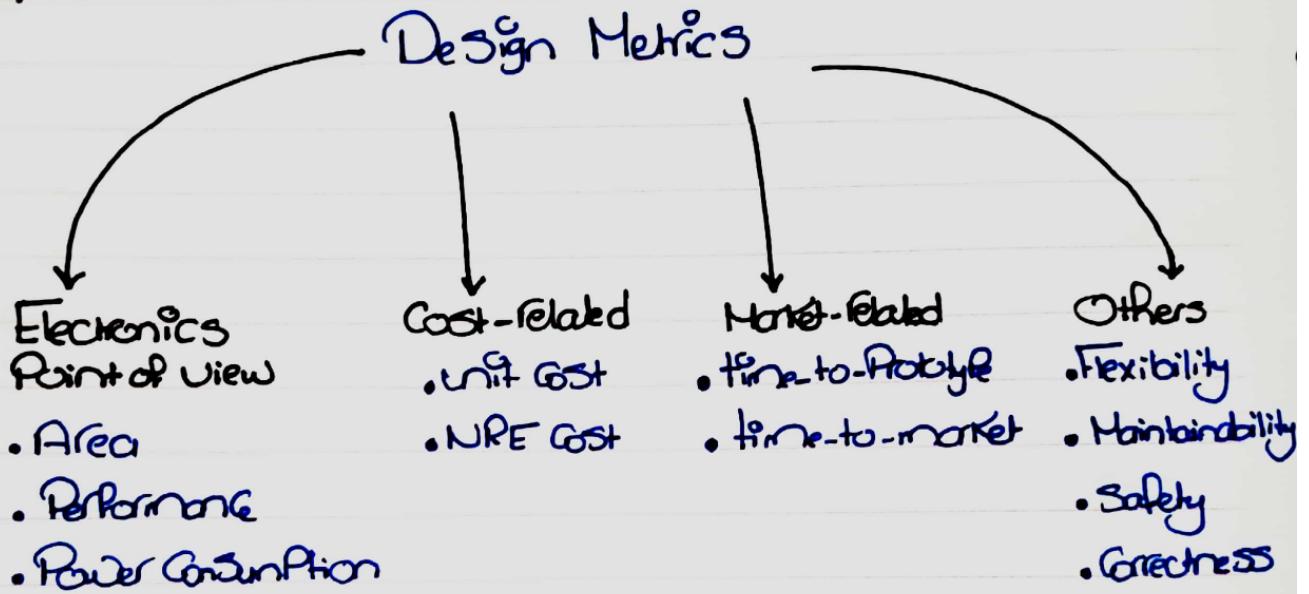
- H_p Charges C_L during Precharge
So that at evaluation both C_L and C_L are at V_{DD} and no charge redistribution occurs.

Problem 5)

a)



b)



- All of the metrics are important. Depending on the application/requirements the designer may choose to focus on specific metrics. (deem them as more important.)
- Taking into account other metrics, **Area**, **Performance** and **Power Consumption** are often considered the most important when it comes to making a leading-edge chip (Slimmer, Faster & long-lasting technology)

c)

analyze -format vhdl -lib -work topLevel.vhd

elaborate topLevel -arch detailed_RTL -lib WORK

Set_Operating_Conditions WCCOM

Create_clock CLK -Period 40 -Waveform {0 20}

Set_clock_latency 0.3 CLK

Set_input_delay 2.0 -clock CLK [all_inputs]

Set_output_delay 1.65 -clock CLK [all_outputs]

Set_load 0.1 [all_outputs]

Set_drive 0.3 [all_inputs]

Compile

report_timing