Cairo University   VLSI Design
Faculty of Engineering   Third Year
Computer Engineering Department   Midterm 2015-1 hour
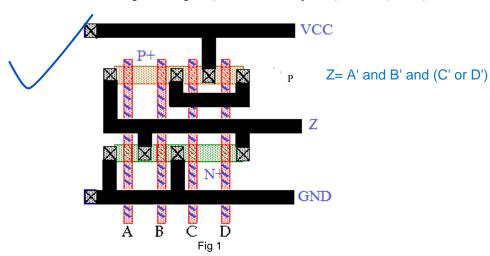
Name: BN:

Question (1) True or False (wrong answers will be penalized):
(7 marks , min zero , it won't affect other questions)

1.	Fabless Companies are companies that perform fabrication only
2.	The critical dimension of the design is determined by the wavelength of the exposure light only
3.	For a negative photo resist , the mask is opaque (dark) for the areas that needs to be processed
4.	One advantage of the CMOS gates are high output impedance
5.	The design rules act as the interface between the circuit designer and the process engineer
6.	The minimum space between the gate and the well boundary is an example of intra-layer design rule
7.	NMOs transistor passes weak zero and strong '1'
8.	Pass Transistor is considered a dynamic CMOS
9.	Pass transistor has generative properties
10.	One advantage of CMOS gates over CPL gates is its simple design
11.	Pass transistor Should never cascade in anyway
12.	In the traditional design flow , DRC checks are made before LVS
13.	LVS stage performs parasitic extraction
14.	Scalable design rules are usually used in industry

Question (2) (8 marks)

A) what is the function of the Stick diagram in Fig. 1 . (write down the equation)   (2 mark)

Z= A' and B' and (C' or D')

Fig 1

B) Assuming a p-type substrate and using your color pencils, sketch the Layout for **3-input** NOR CMOS **to scale**, with the following colors:

Metal: Blue   Polysilicon: Red   n+: Green   p+: orange or brown
Contacts and vias: Black   Well (indicate whether p or n): Yellow

Take care: you will be penalized if you broke a DRC rule (assume the measure, you don't need to remember it) take your time and draw something decent

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