It was a tough lab really !.

Lab 2 Requirements

1- Create 2 register files where each register file

- contains 8 registers
- each register is 16-bit width.
- One register file is created using for loop and the other is created using arrays (memory)
- Each register file has (read_enable,write_enable, read_data,write_data, clk,rst, read_addr,write_addr)
  - read_enable: enables reading from a certain registers
  - read_addr: determines which register to read from
  - read_data: is the data read from the chosen register
  - rst: reset all registers to 00s, it has a priority over any other signal.

2- Create a testbench to compare the 2 implementations of the register file, you need to cover at least different 8 cases

Hint: what will happen if you read and write to the register at the same time?

Bonus: use generics to create register of variable width & use monitor in testbench.

Make any necessary (logical) assumption.