Cairo University
Faculty of Engineering
Computer Engineering Department

VLSI Design
Third Year
Midterm 2017 - **1 hour**

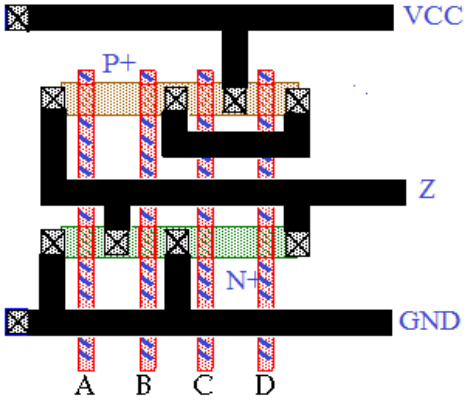
Name: Sec: BN:

Question (1) True or False & correct the false statements: (6 marks) red is how we can correct the answer

1.	IDM companies are NOT limited by available commercial technologies	False
2.	Critical Dimension of the design depends on the ~~wafer used in fabrication~~ lens & light wavelength	False
3.	Self-Aligned Gates are formed by implanting the Source & Drain ~~then~~ after developing the Gate	False
4.	Scalable design rules are NOT commonly used in industry than micron design rules	False
5.	Inter-Layer constraints are specified for ~~same~~ different layer wires	False
6.	Layouts violating DRC rules could or couldn't work properly, we can't guarantee	True
7.	Layout Verses Schematic stage checks for short/open circuits in the Layout should not be found	True
8.	Parasitic Extraction stage calculates the parasitic devices present in the layout and adds them back to the circuit	True
9.	~~High noise margin~~ Regenerative property is sufficient to guarantee that cascaded gates will reach nominal voltage	False
10.	CMOS gates have no static power consumption	True
11.	All CMOS gates have regenerative property	True
12.	CMOS gates have high input impedance and low output impedance	True

to guarantee you have to follow the DRC

Question (2) (9 marks)



a) What is the function implemented in the above Layout?
F(A, B, C, D) = (A + B + C.D)' = A'.B'.(C'+D')

b) Assuming a p-type substrate and using your color pencils, sketch the CMOS diagram & optimized stick diagram for **3-input XOR**
(Hint1: Use truth table or logic expressions to get the CMOS diagram)
(Hint2: Use Euler path for stick diagram optimization)

Metal: Blue Polysilicon: Red n+: Green p+: orange or brown
Contacts and vias: Black Well (indicate whether p or n): Yellow

Take your time and draw something decent. Don't cross wires, Don't forget contacts

3 input XOR has F = A.(B'.C' + B.C) + A'.(B'.C + B.C')
CMOS design & Stick diagram is a design problem