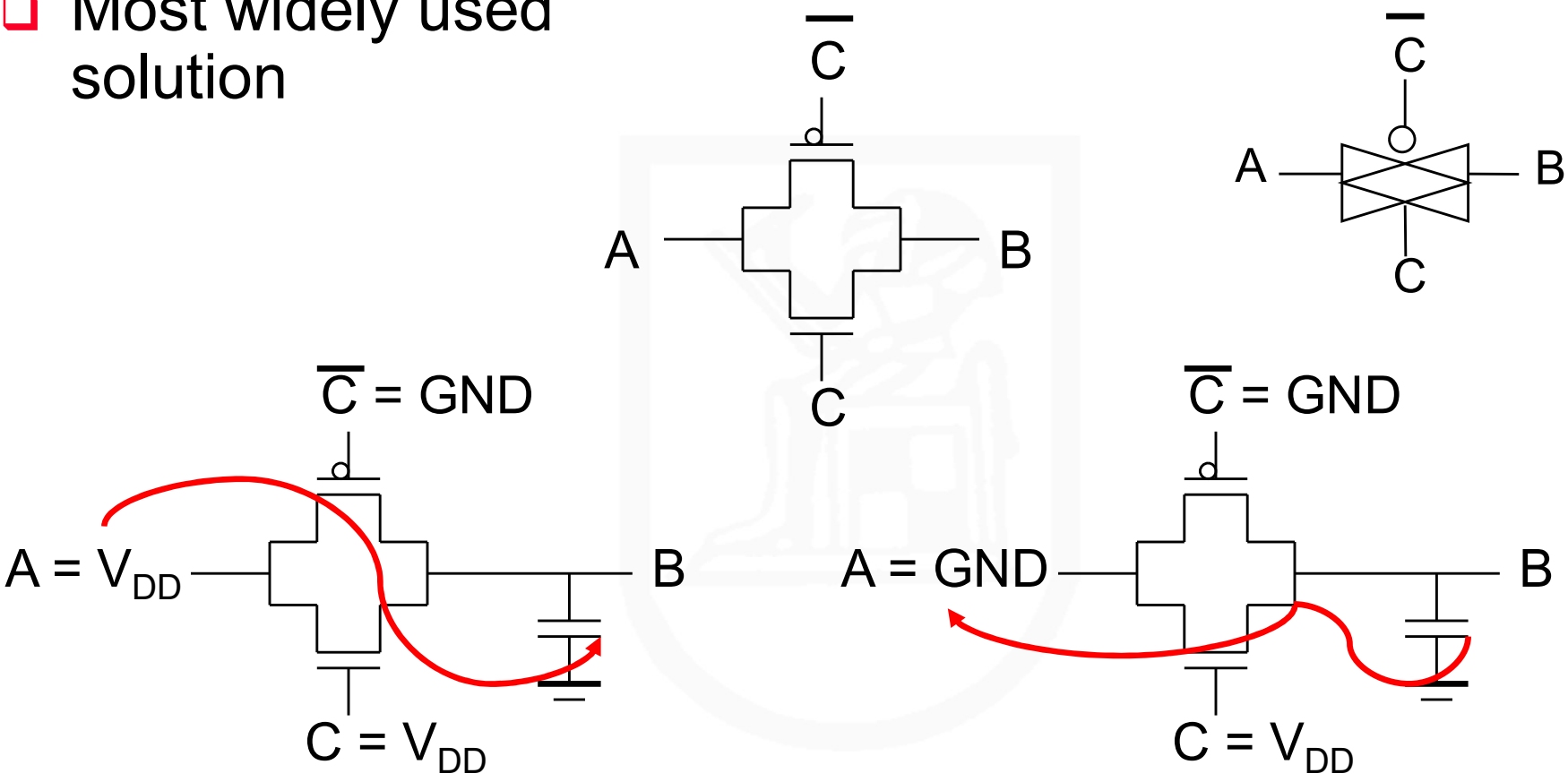
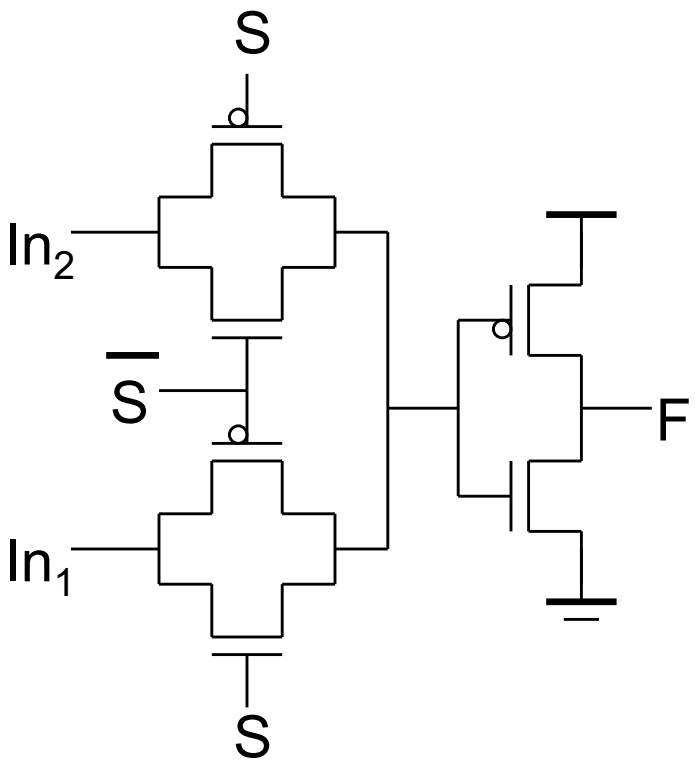
Solution 3: Transmission Gates (TGs)

- Most widely used solution

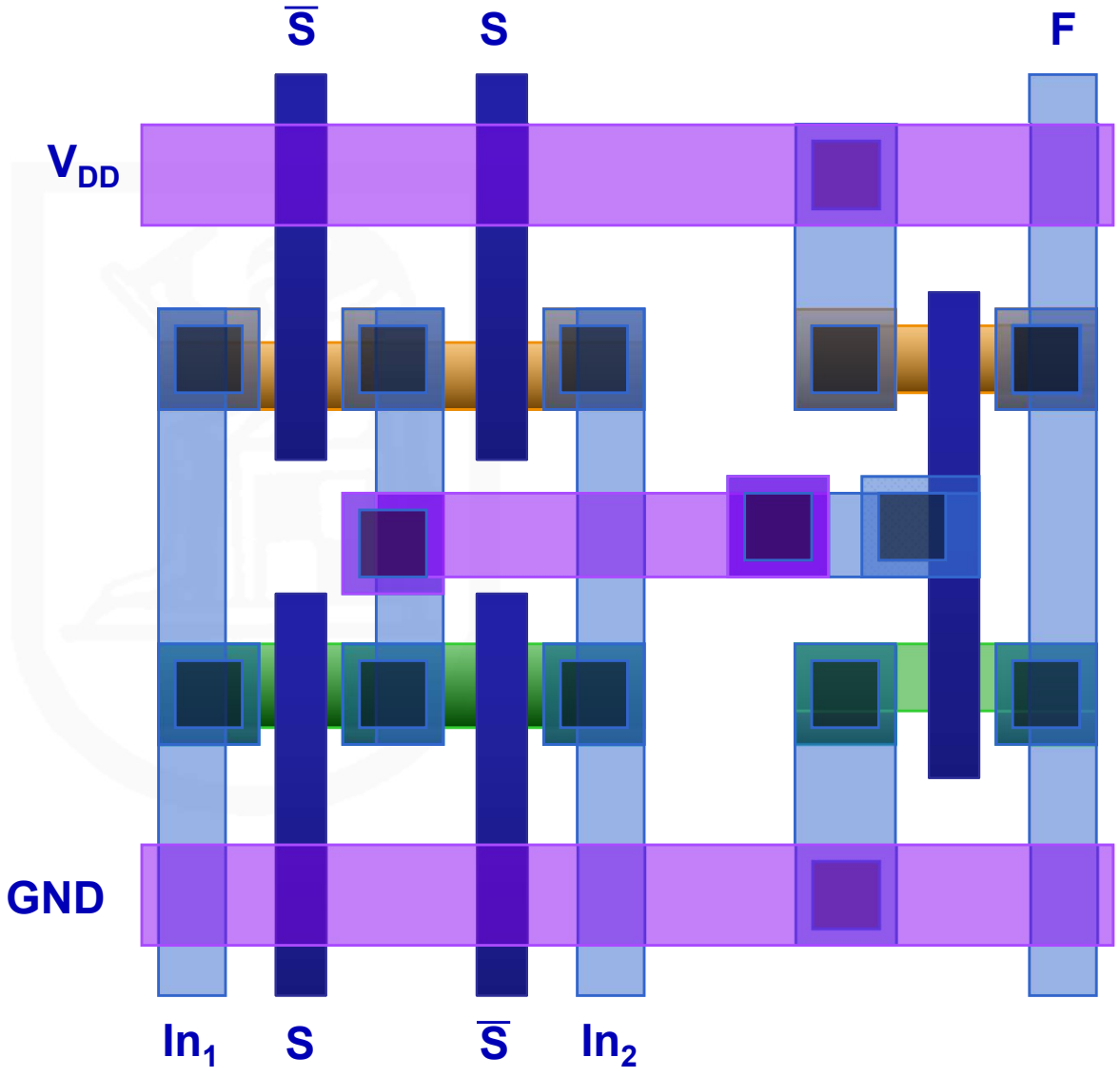


- **Full swing *bidirectional* switch controlled by the gate signal C, A = B if C = 1**

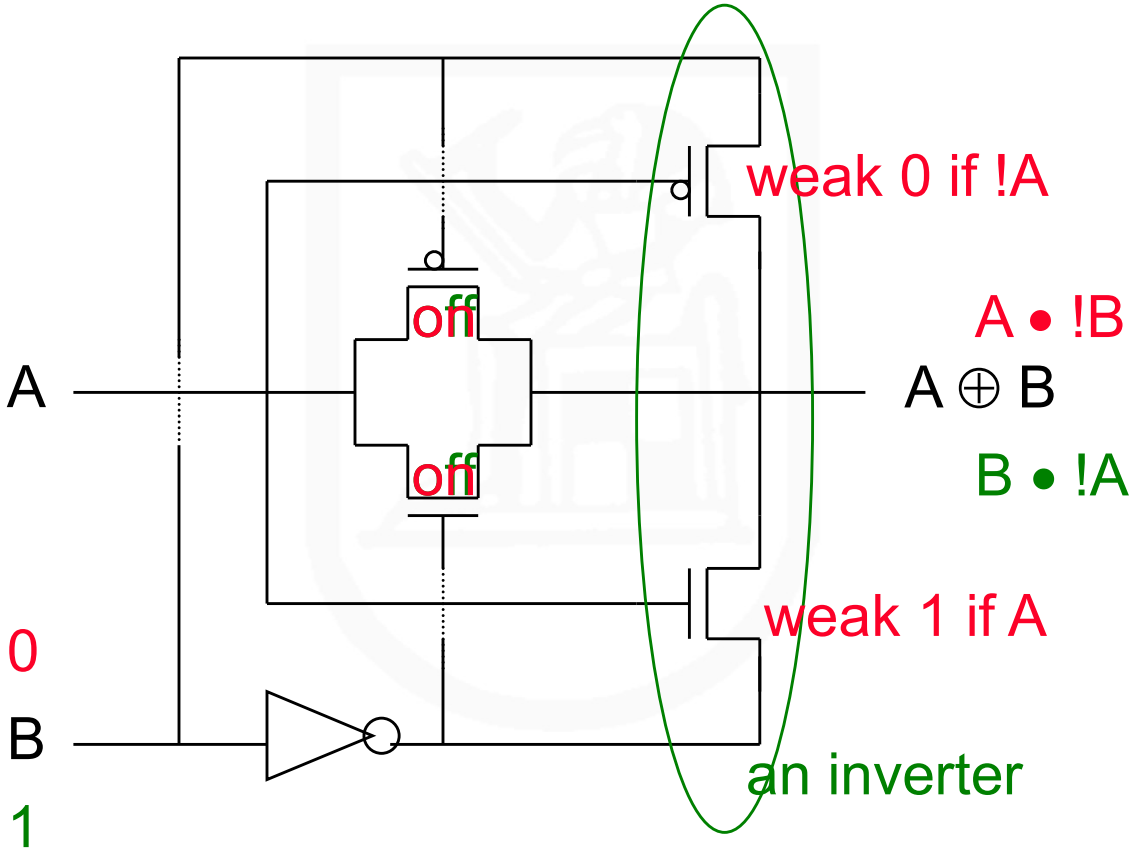
TG Multiplexer



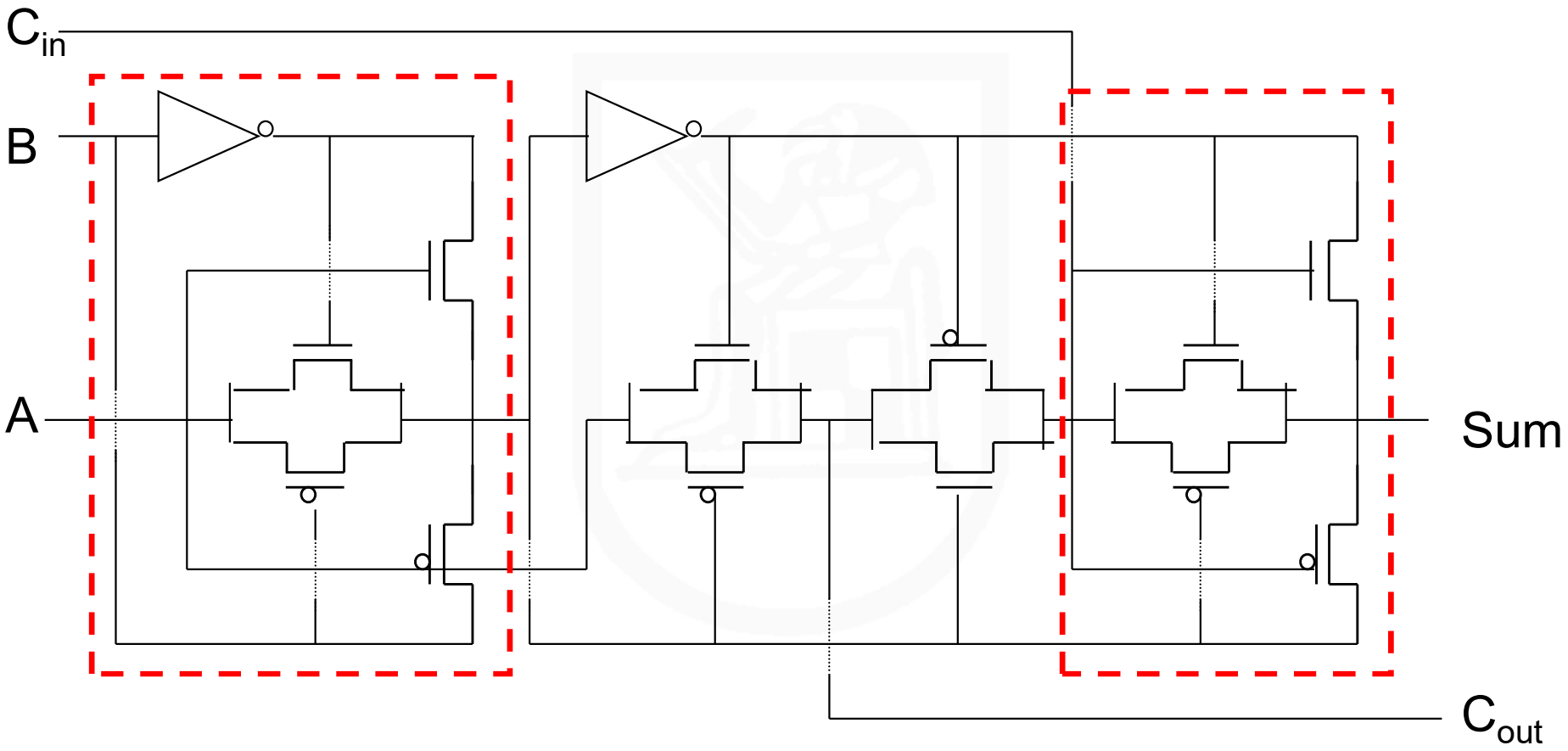
$$F = !(In_1 \bullet S + In_2 \bullet \overline{S})$$



Transmission Gate XOR



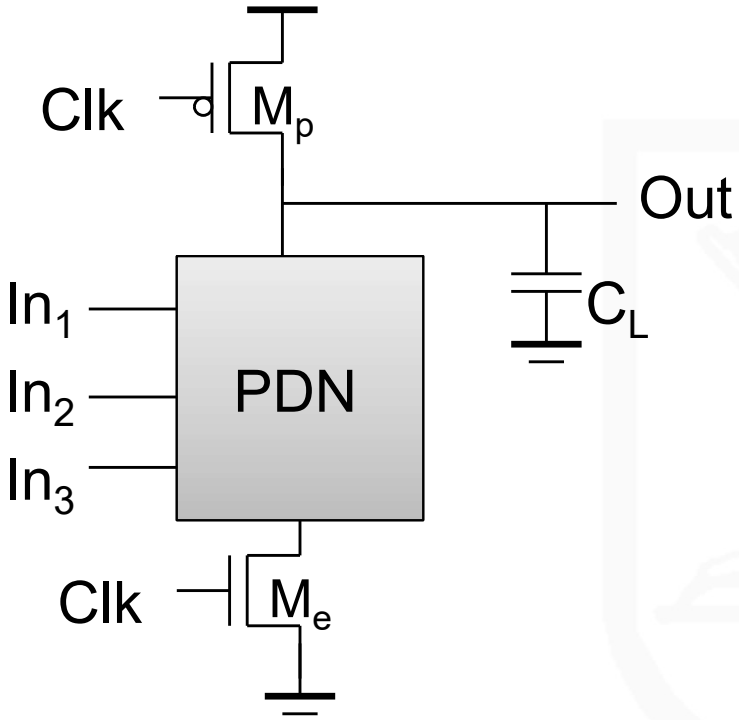
TG Full Adder

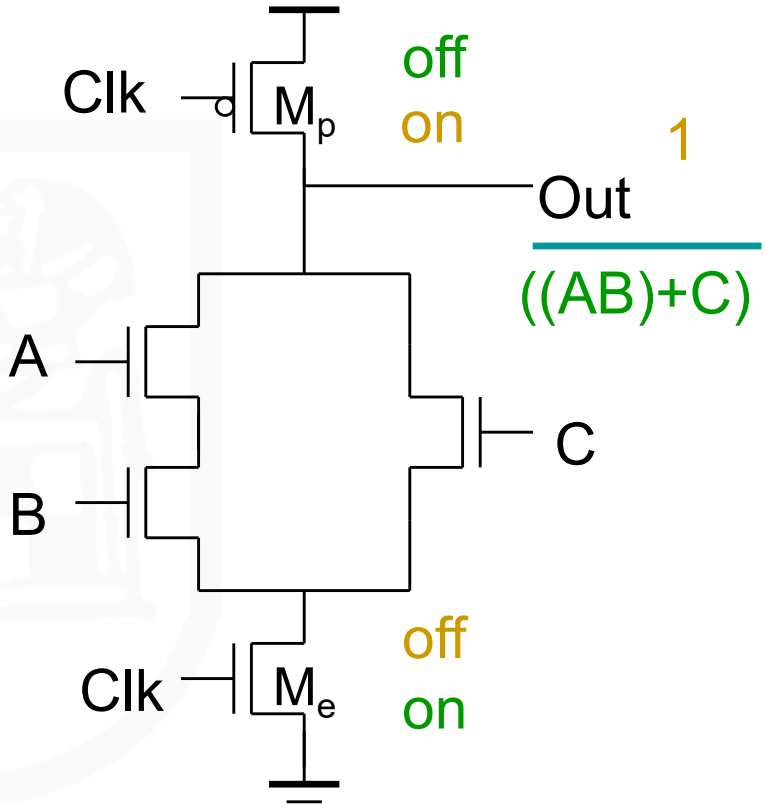


Dynamic CMOS

- **In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.**
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices
- **Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.**
  - requires on *n* + 2 (*n*+1 N-type + 1 P-type) transistors

Dynamic Gate





Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

Conditions on Output

- **Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.**
- **Inputs to the gate can make at most one transition during evaluation.**
- **Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L**

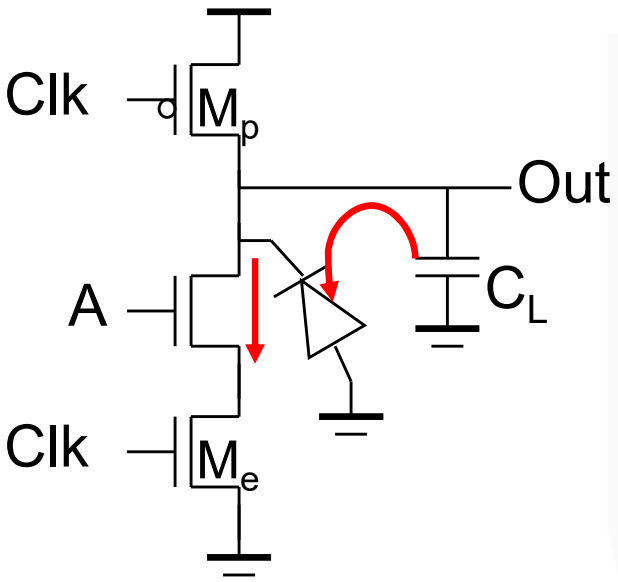
Properties of Dynamic Gates

- **Logic function is implemented by the PDN only**
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- **Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})**
- **Non-ratioed - sizing of the devices does not affect the logic levels**
- **Faster switching speeds**
  - reduced load capacitance due to lower input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (Cout)
  - no I_{sc}, so all the current provided by PDN goes into discharging C_L

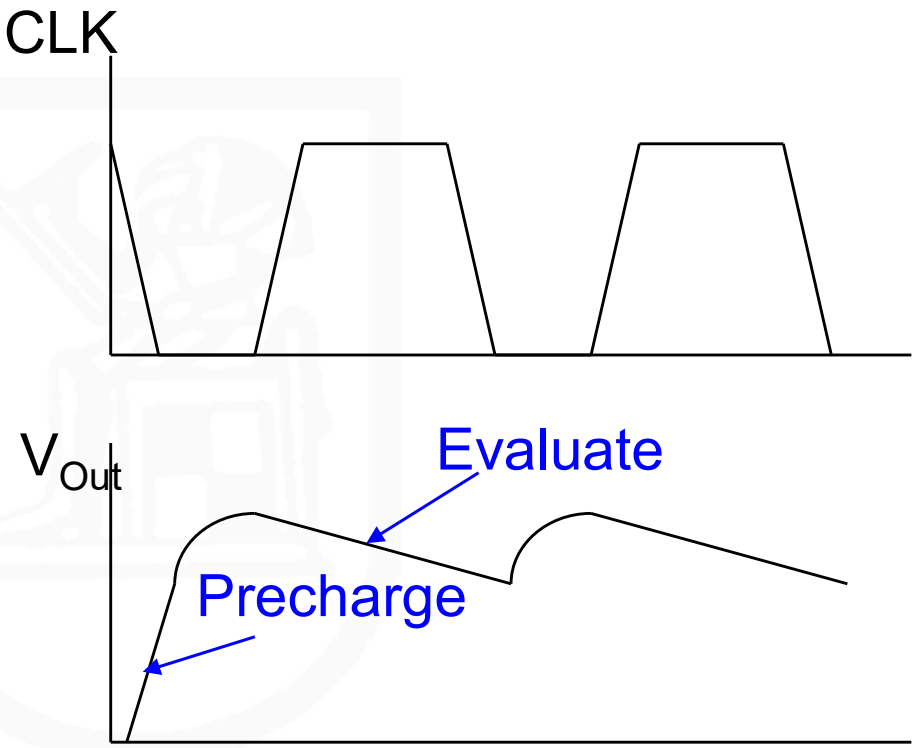
Properties of Dynamic Gates

- **Overall power dissipation usually higher than static CMOS**
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- **PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}**
  - low noise margin (NM_L)
- **Needs a precharge/evaluate clock**

Issues in Dynamic Design 1: Charge Leakage

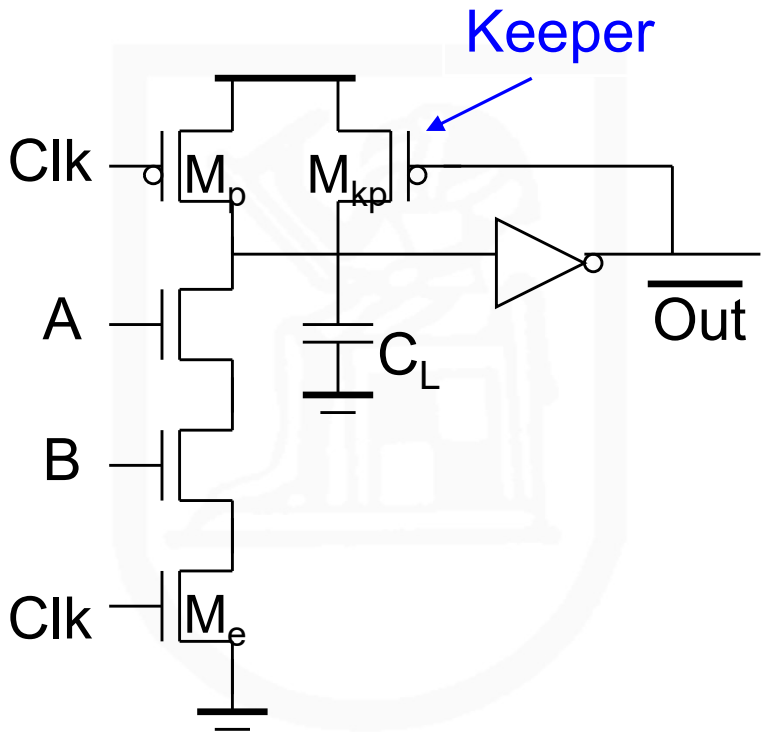


Leakage sources



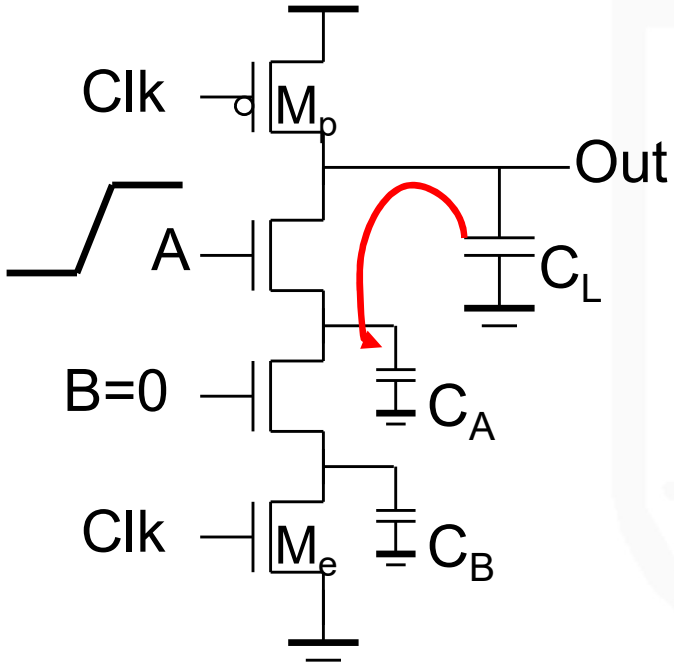
Dominant component is subthreshold current

Solution to Charge Leakage



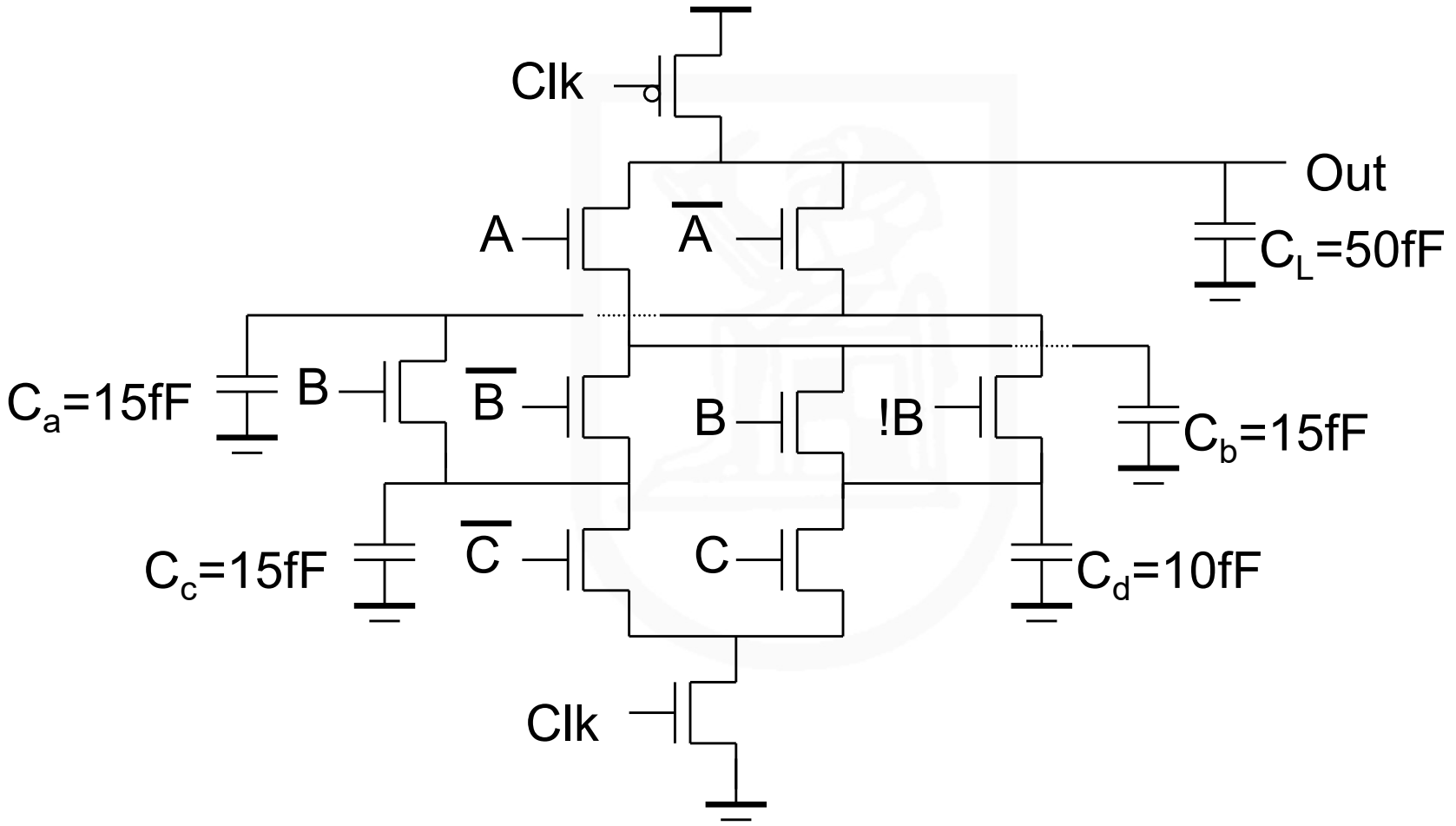
Same approach as level restorer for pass-transistor logic

Issues in Dynamic Design 2: Charge Sharing

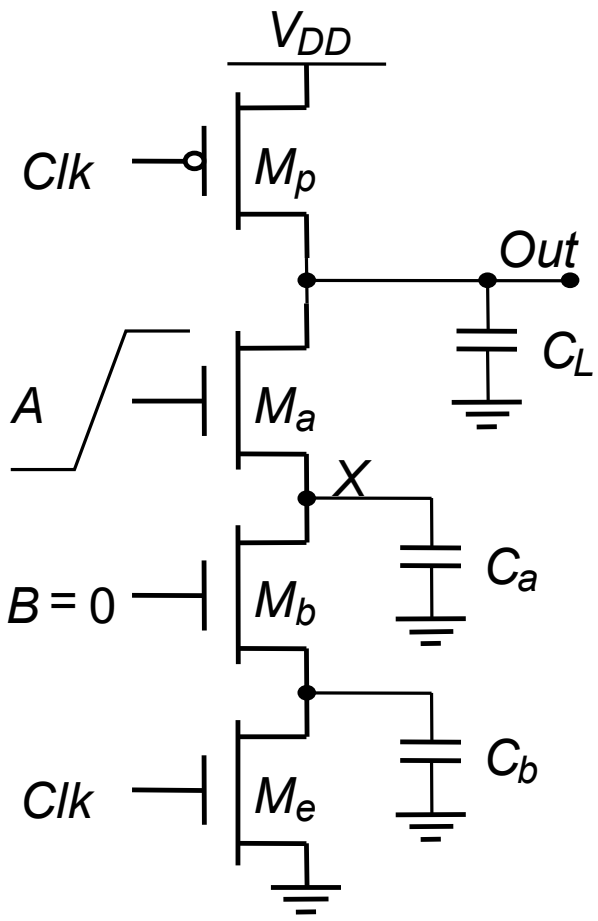


Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

Charge Sharing Example



Charge Sharing



case 1) if $\Delta V_{out} < V_{Tn}$

$$C_L V_{DD} = C_L V_{out}(t) + C_a(V_{DD} - V_{Tn}(V_X))$$

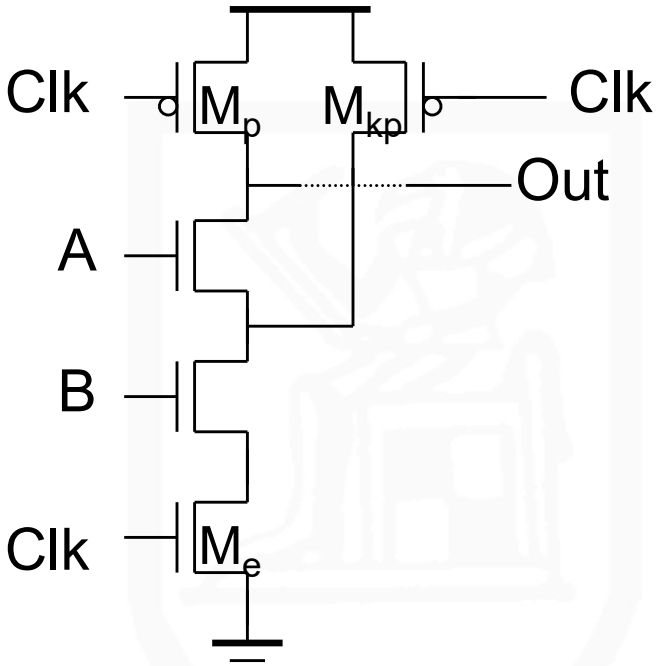
or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L}(V_{DD} - V_{Tn}(V_X))$$

case 2) if $\Delta V_{out} > V_{Tn}$

$$\Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right)$$

Solution to Charge Redistribution

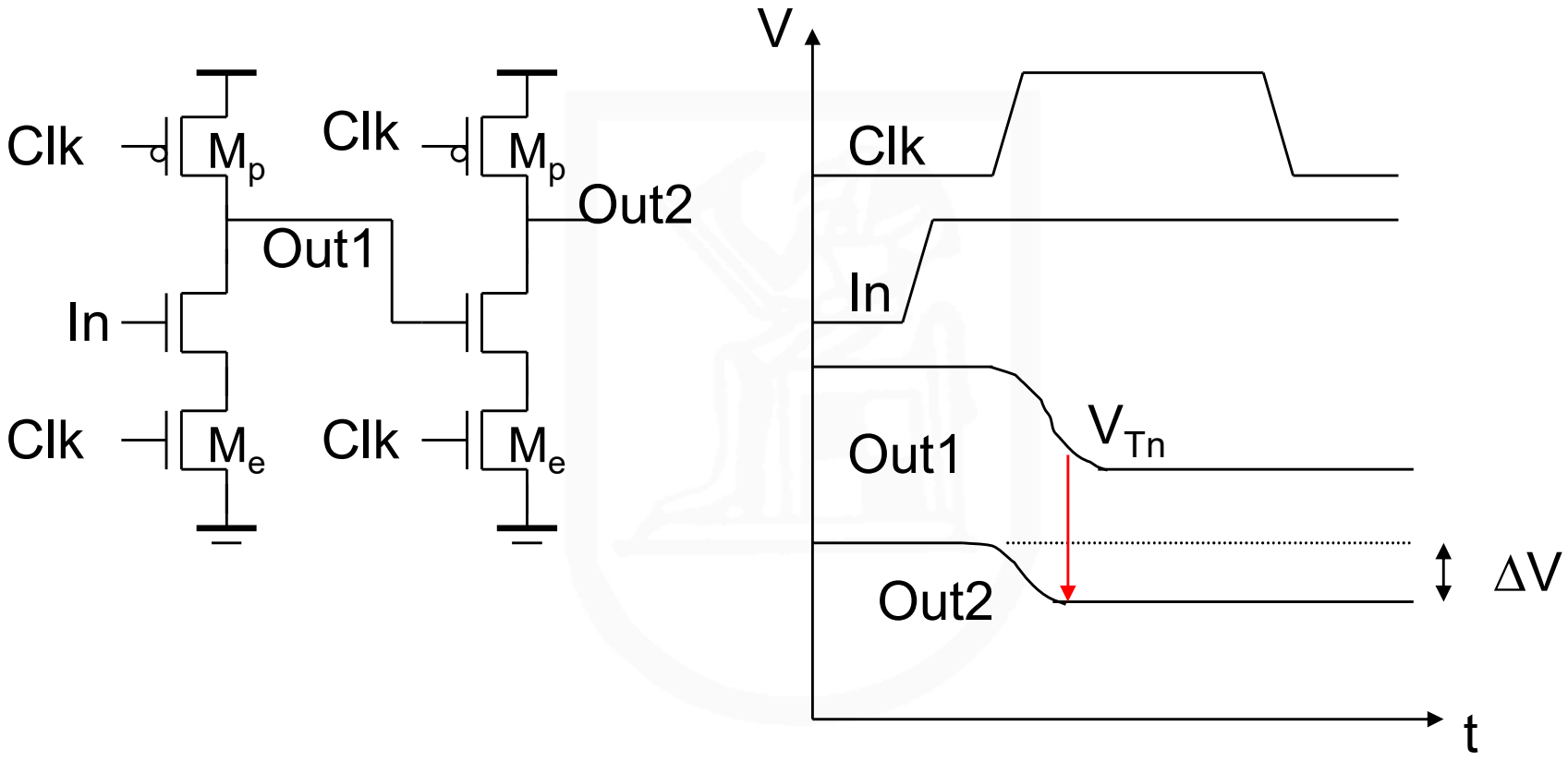


Precharge the internal nodes using a clock-driven transistor (at the cost of increased area and power)

Other Effects

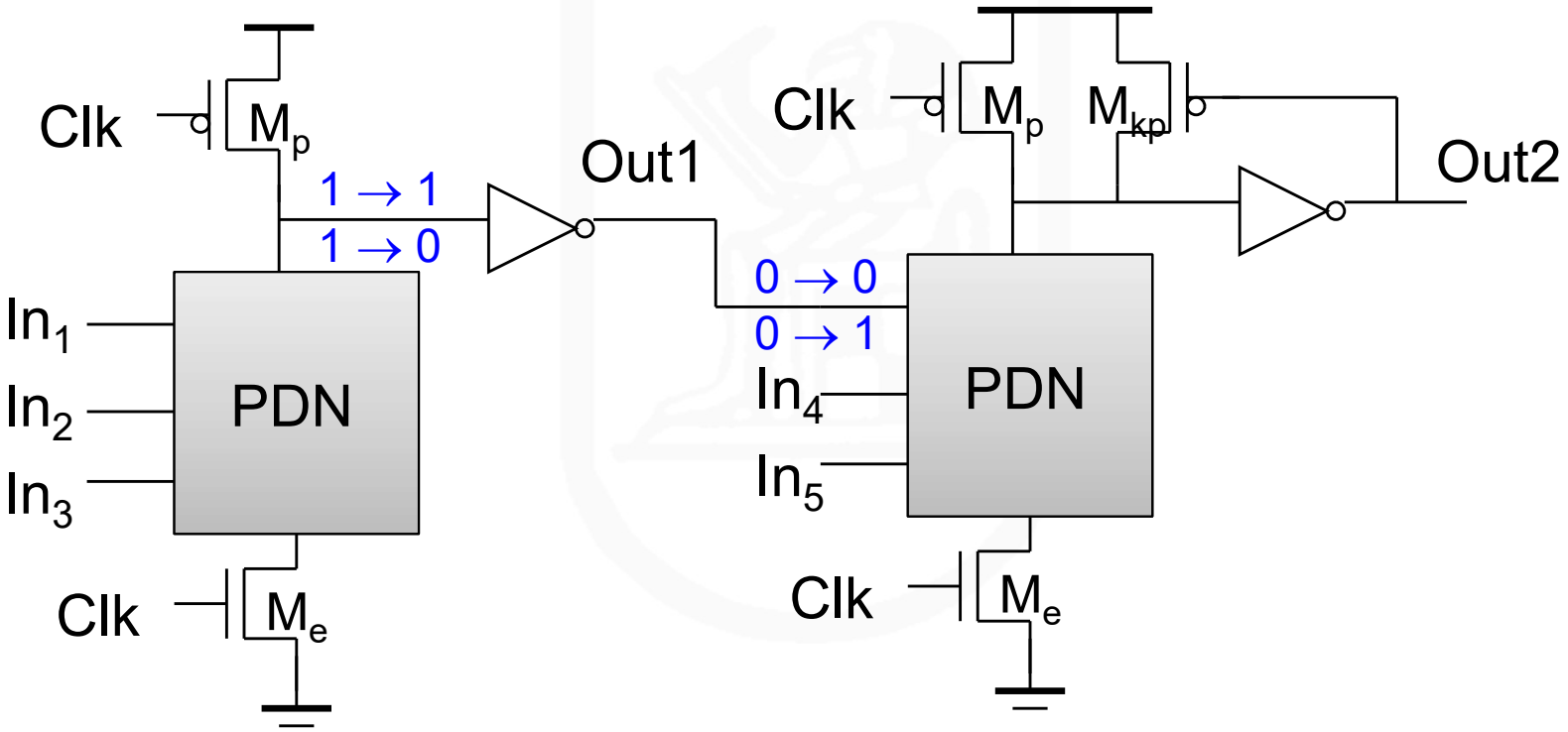
- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)

Cascading Dynamic Gates

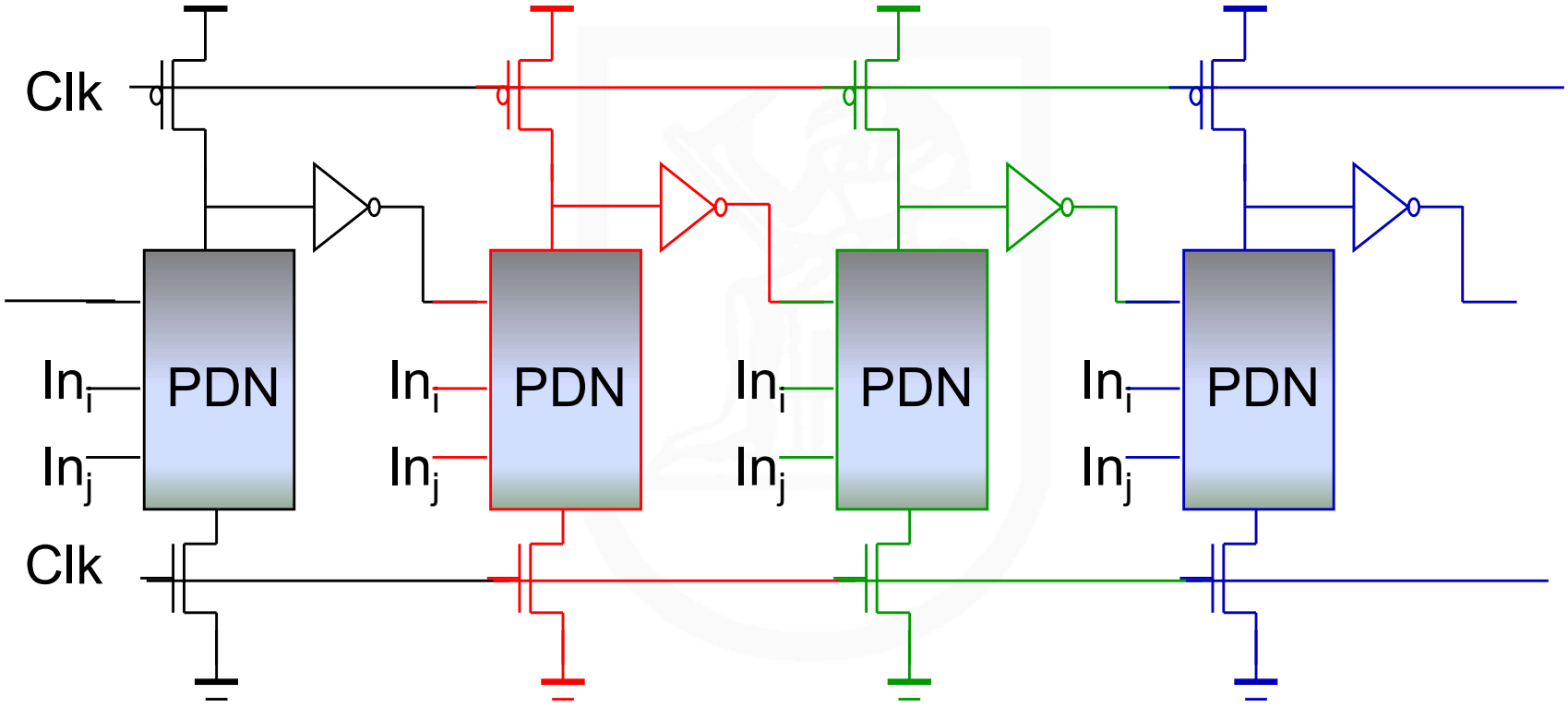


Only 0 → 1 transitions allowed at inputs

Domino Logic



Why Domino?

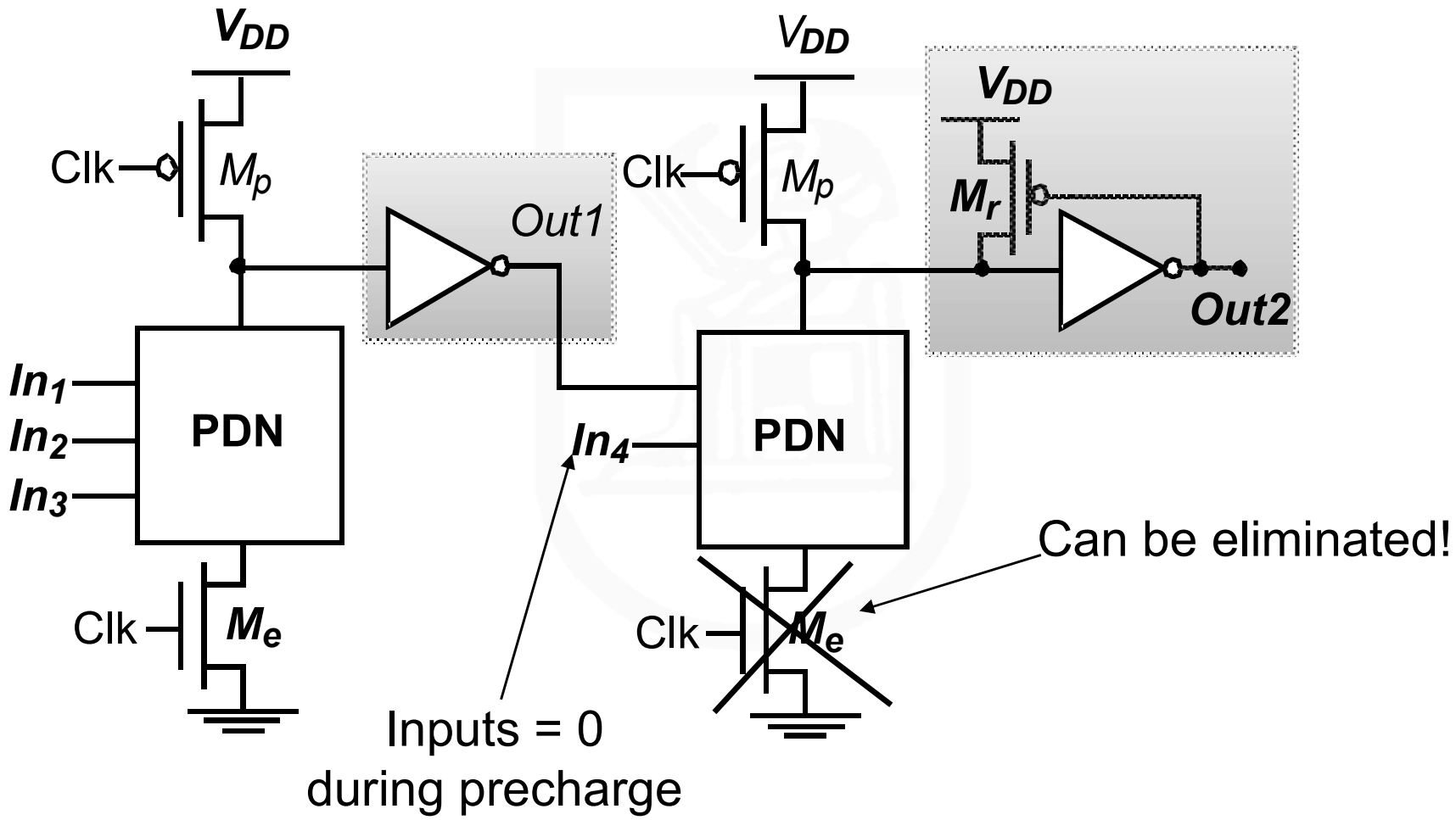


Like falling dominos!

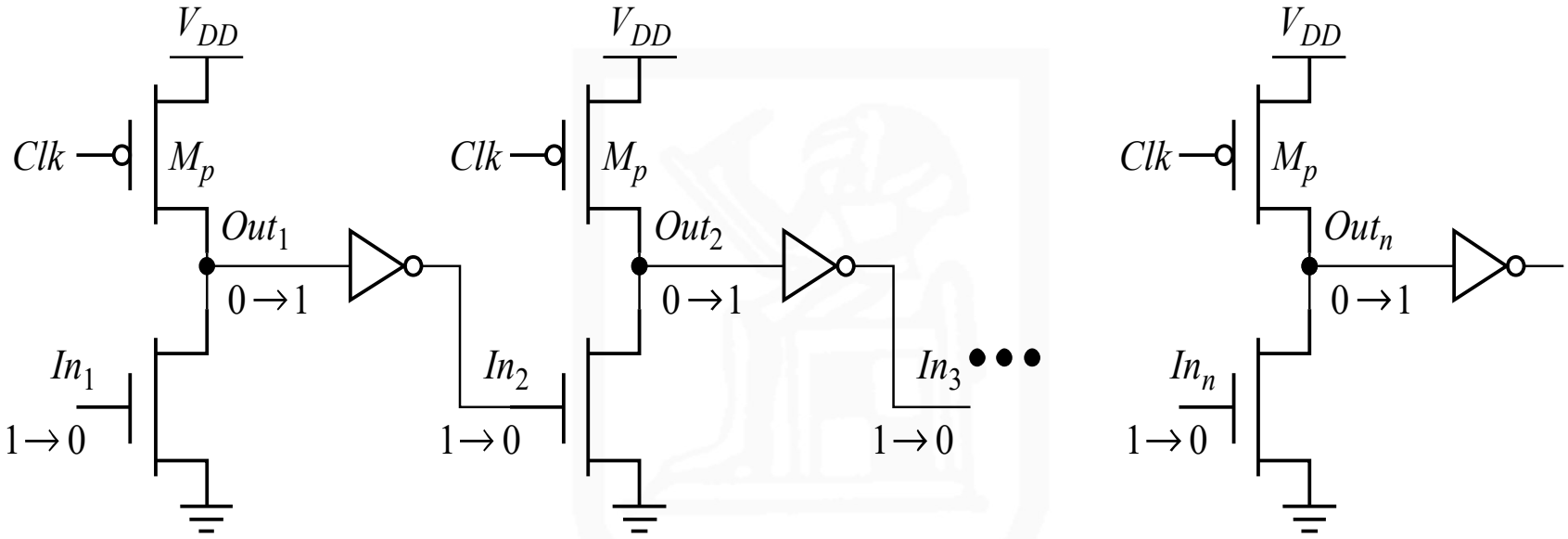
Properties of Domino Logic

- **Only non-inverting logic can be implemented**
- **Very high speed**
  - static inverter can be skewed, only L-H transition
  - Input capacitance reduced – smaller logical effort

Designing with Domino Logic



Footless Domino



The first gate in the chain needs a foot switch
Precharge is rippling – short-circuit current
A solution is to delay the clock for each stage