Industry & Technology Overview

- Introduction to the semiconductor industry
- Functional Structure of a Fabless Company
- Manufacturing Process
- **Design Rules**

Design Rules

- **VLSI designs and fab processes are very complex.**
- **Circuit designers want smaller designs**
  - leads to higher performance and higher circuit density.
- **Process engineers focus on reproducibility and yield.**
- **In this regard design rules are a compromise that attempts to satisfy both sides**
  - Specify the minimum dimensions and spacing allowed
  - Layouts violating DR may not get manufactured properly and reduce the yield.

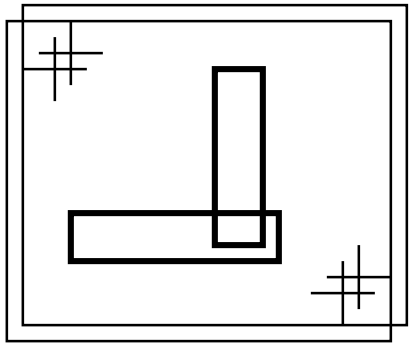
Design Rules

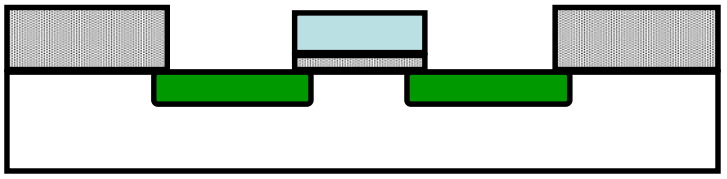
- **Interface between the circuit designer and process engineer**
- **Guidelines for constructing process masks**
- **Unit dimension: Minimum line width**
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)
- **Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur**
- **A complete set includes**
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

Why Have Design Rules?

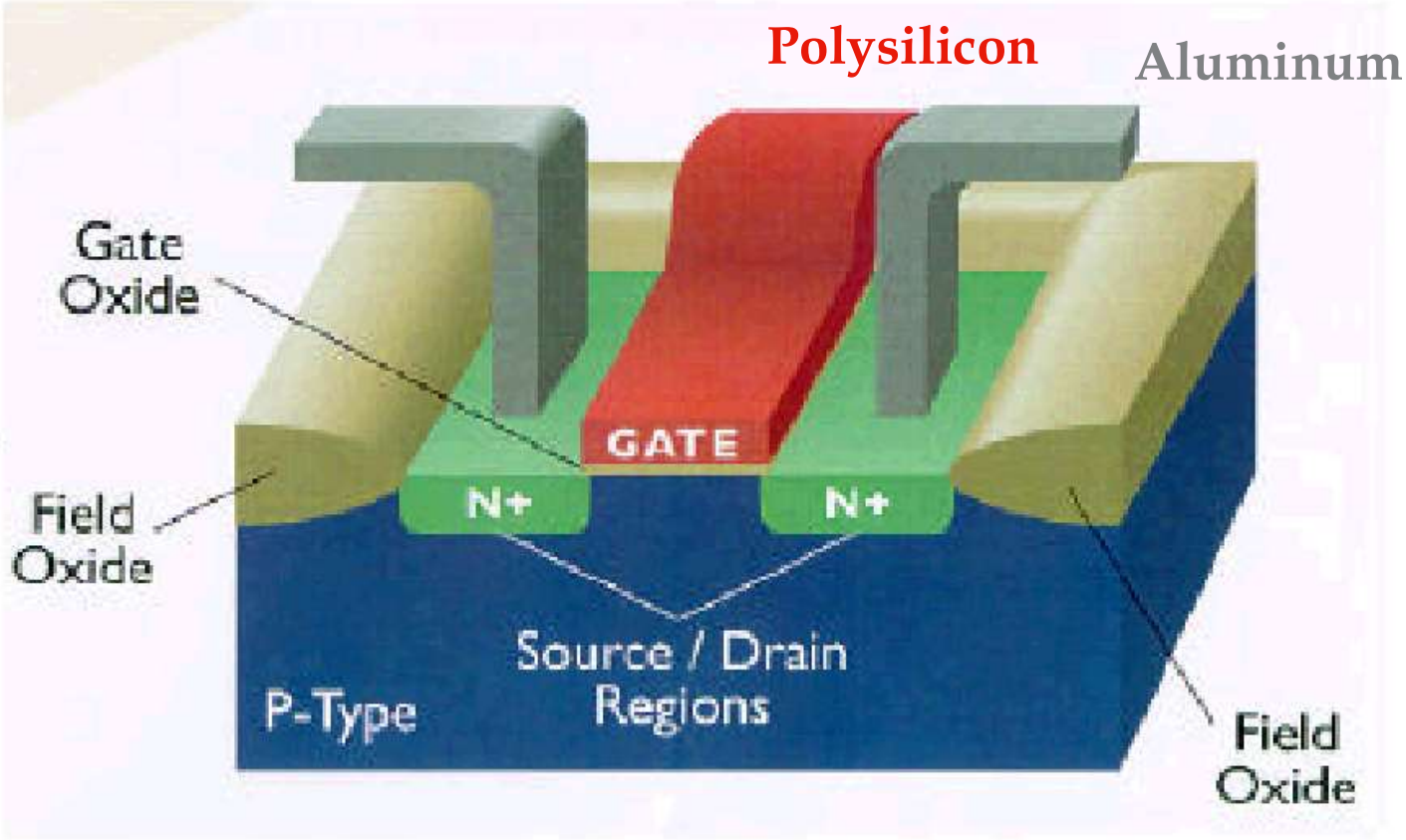
- **To be able to tolerate some level of fabrication errors such as**

1. Mask misalignment
2. Dust
3. Process parameters (e.g., lateral diffusion)
4. Rough surfaces



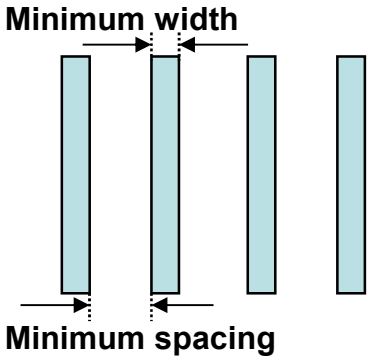


3D Perspective



Micron Design Rules

- **DRs consist of minimum width and minimum spacing constraints and requirements between objects on the same or on different layers.**
- **The fundamental unit in the definition of a set of DRs is the minimum line width – minimum mask dimension that can be safely transferred to the semiconductor material.**
- **DRs are expressed in absolute physical units, for example:**
  - poly width = 0,1 μm.
- **Minimum line-width:**
  - smallest dimension permitted in the layout drawing (minimum feature size)
- **Minimum spacing:**
  - smallest distance permitted between the edges of two layout lines



- **These rules originate from the resolution of the optical printing system, the etching process or the surface roughness.**

Scalable Design Rules

- **SDR define all rules as a function of a single parameter, most often called as λ (lambda).**
- **Scaling of the minimal dimension is accomplished by simply changing the value of λ.**
  - This results in a linear scaling of all dimensions.
- **For a given process, λ is set to a specific value and all other design rules (dimensions) are expressed in whole multiples of λ.**
- **Typically, the minimal line width of a process is set to 2 λ. For instance, for 0.25μm process (i.e. a process with a minimal line width of 0.25μm) λ equals 125nm.**
- **Feature size λ is equal to half the drawn gate length (poly width).**
- **The rules are chosen so that a design is easily scaled over a cross section of industrial processes.**

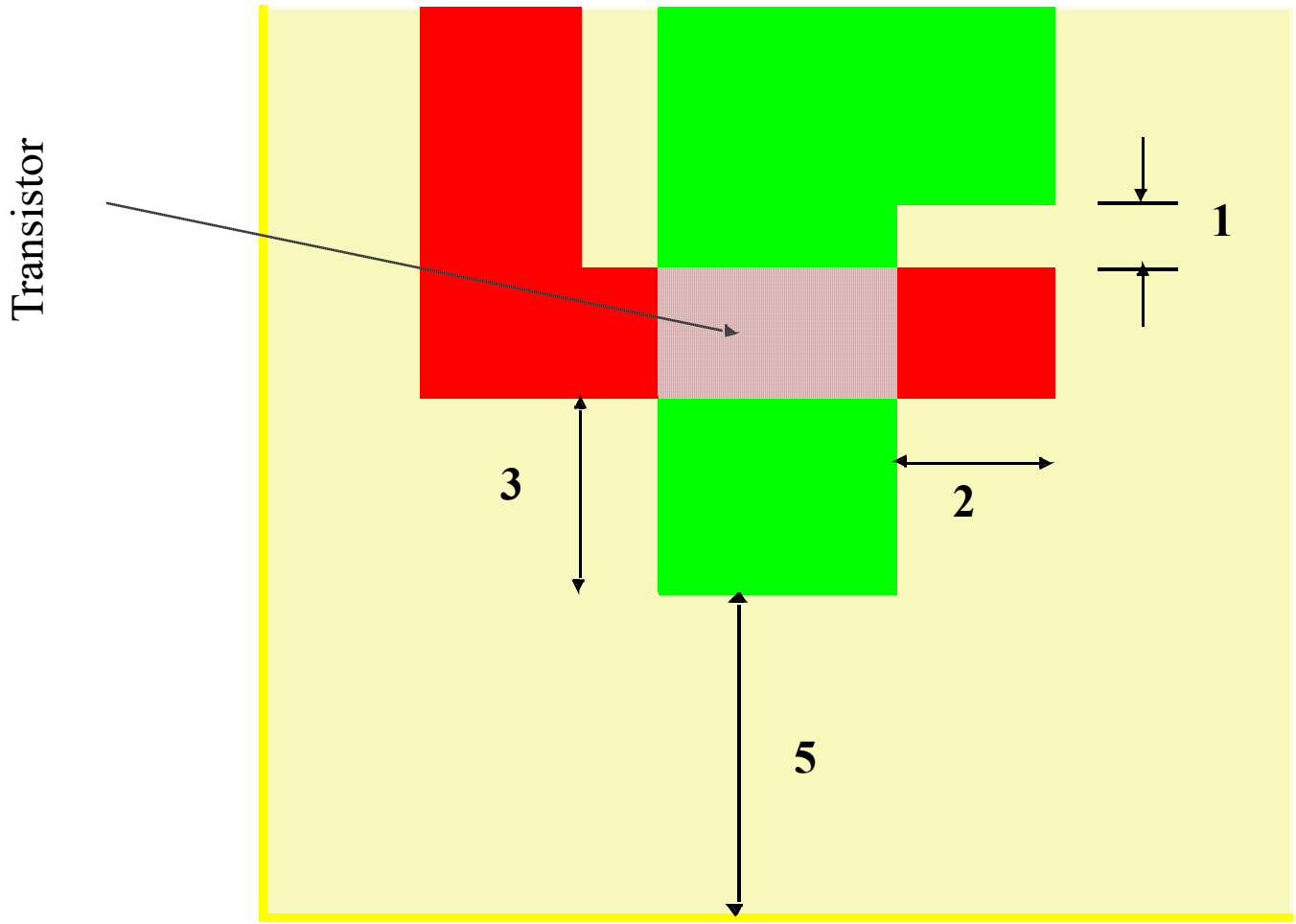
Scalable Design Rules

- **Disadvantages.**
  - Linear scaling is only possible over a limited range of dimensions (for instance, between 0.25μm and 0.15μm).
  - Scaling over large ranges cannot be adequately expressed by the linear scaling rules.
  - Scalable design rules are conservative.
- **The reason why scalable design rules are normally avoided in industry.**
  - Circuit density is a prime goal so designers tend to use micron rules where DRs are expressed in absolute dimensions to exploit the features of a given process to a maximum.

CMOS Process Layers

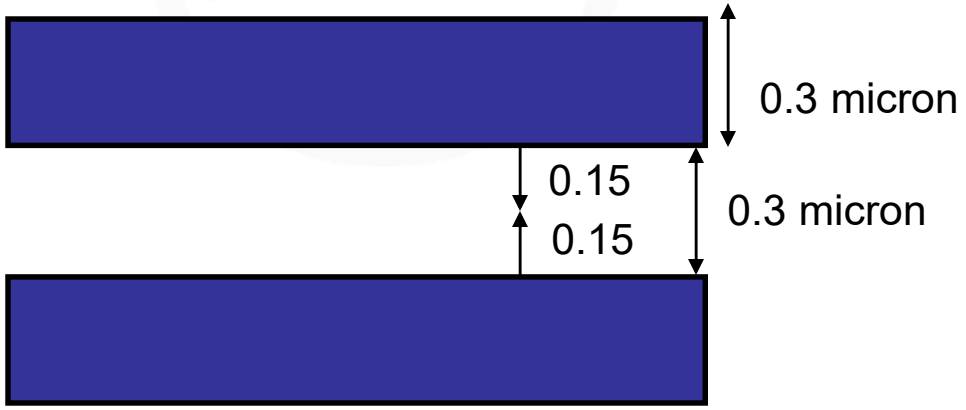
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Transistor Layout

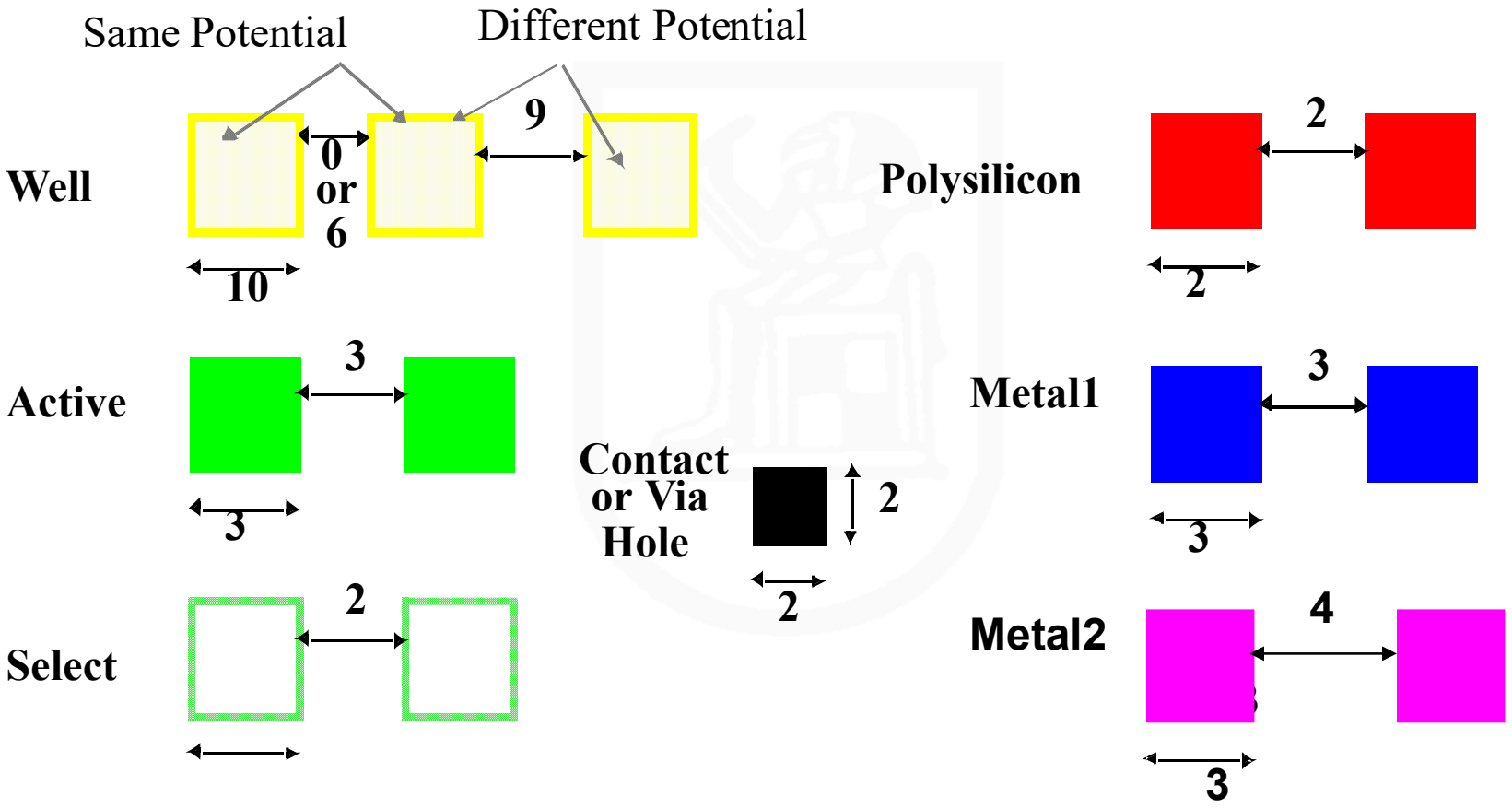


Intra-Layer Design Rules

- **Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab.**
  - minimum line width is set by the resolution of the patterning process (photolithography)
- **Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab.**



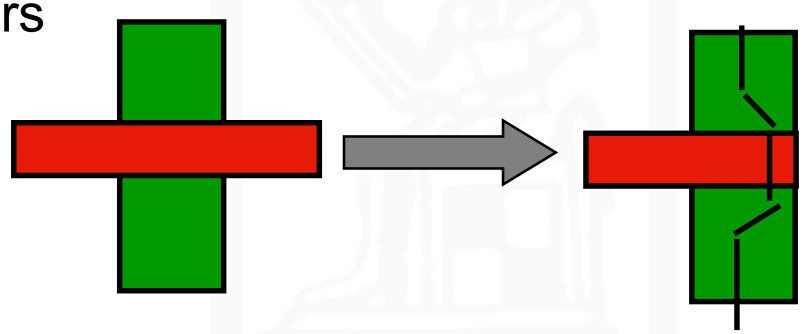
Intra-Layer Design Rules (cont.)



Inter-Layer Design Rules

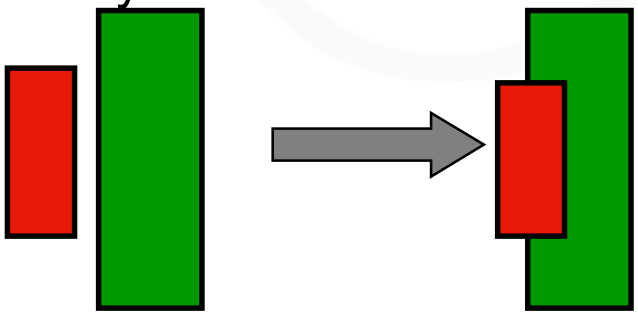
1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors



Catastrophic error

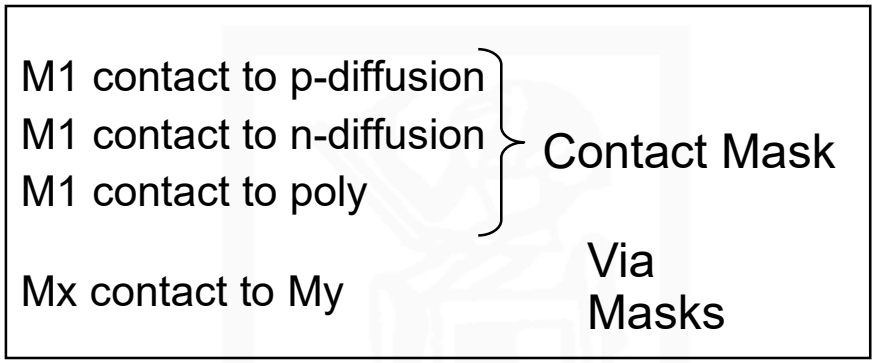
Unrelated Poly & Diffusion

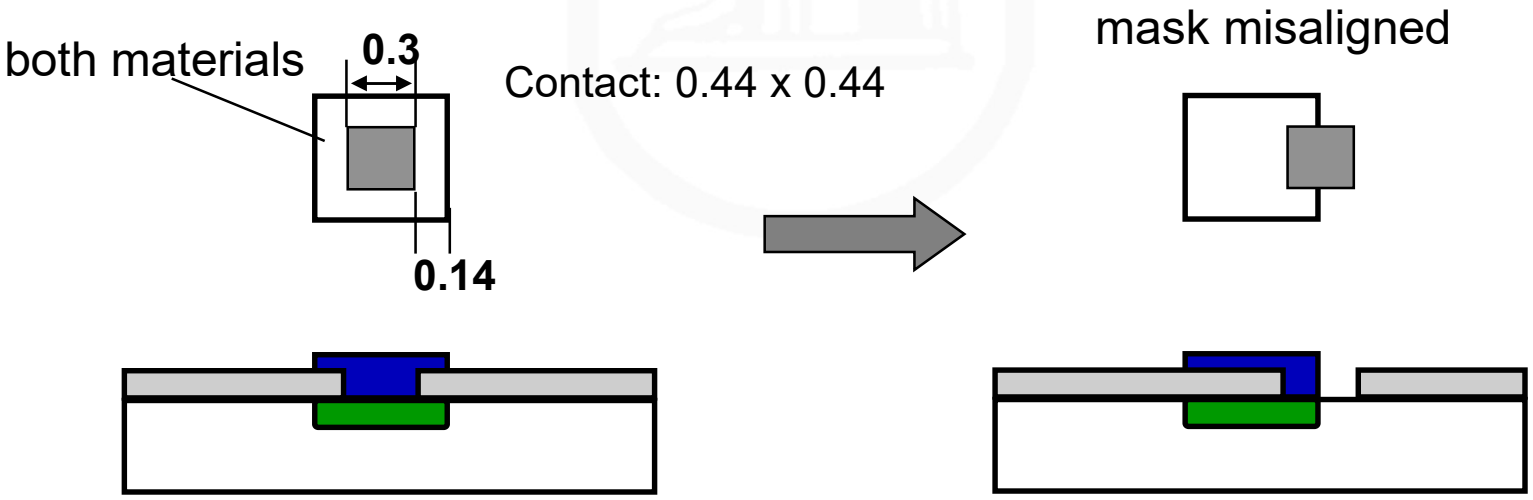


Thinner diffusion, but still working

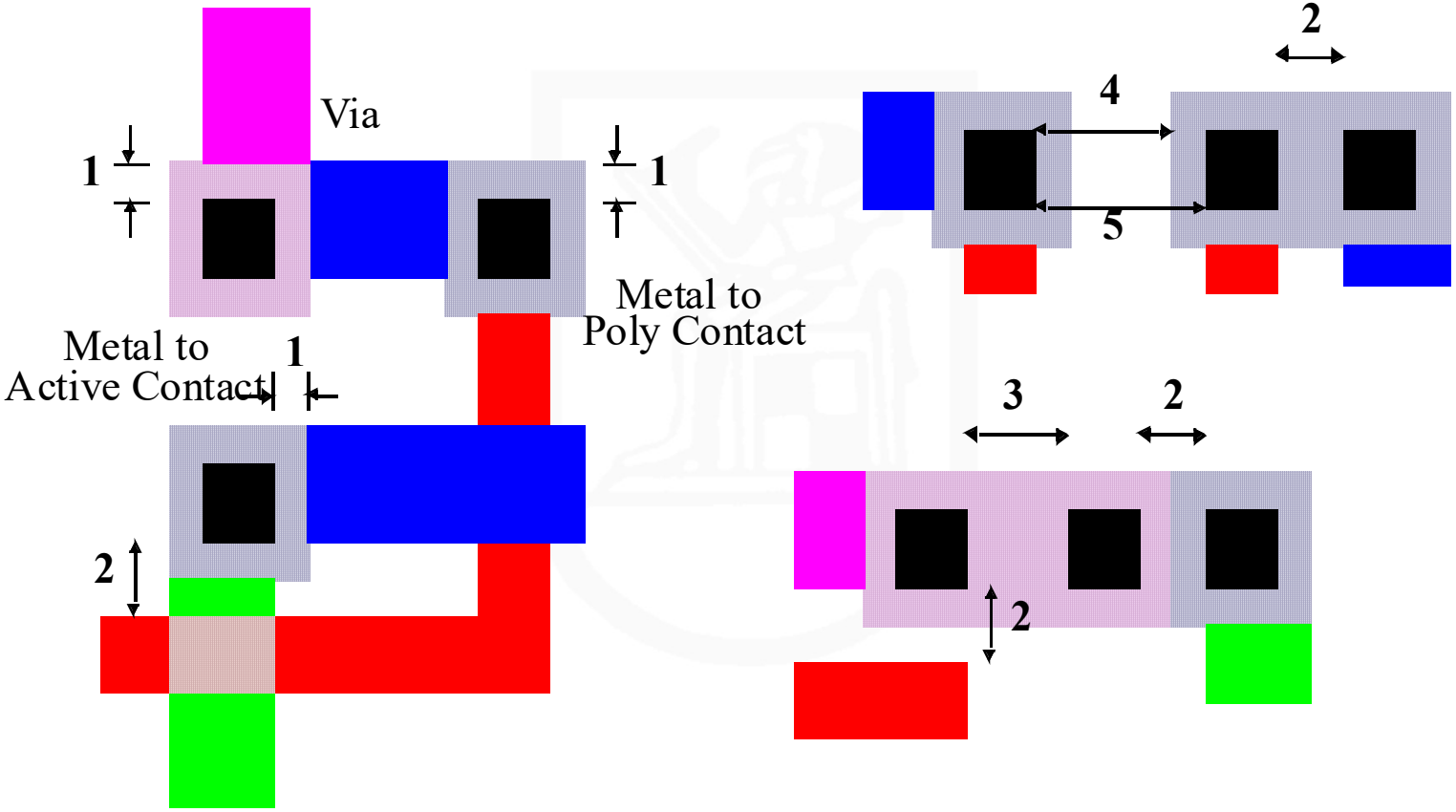
Inter-Layer Design Rule (cont.)

2. Contact and via rules

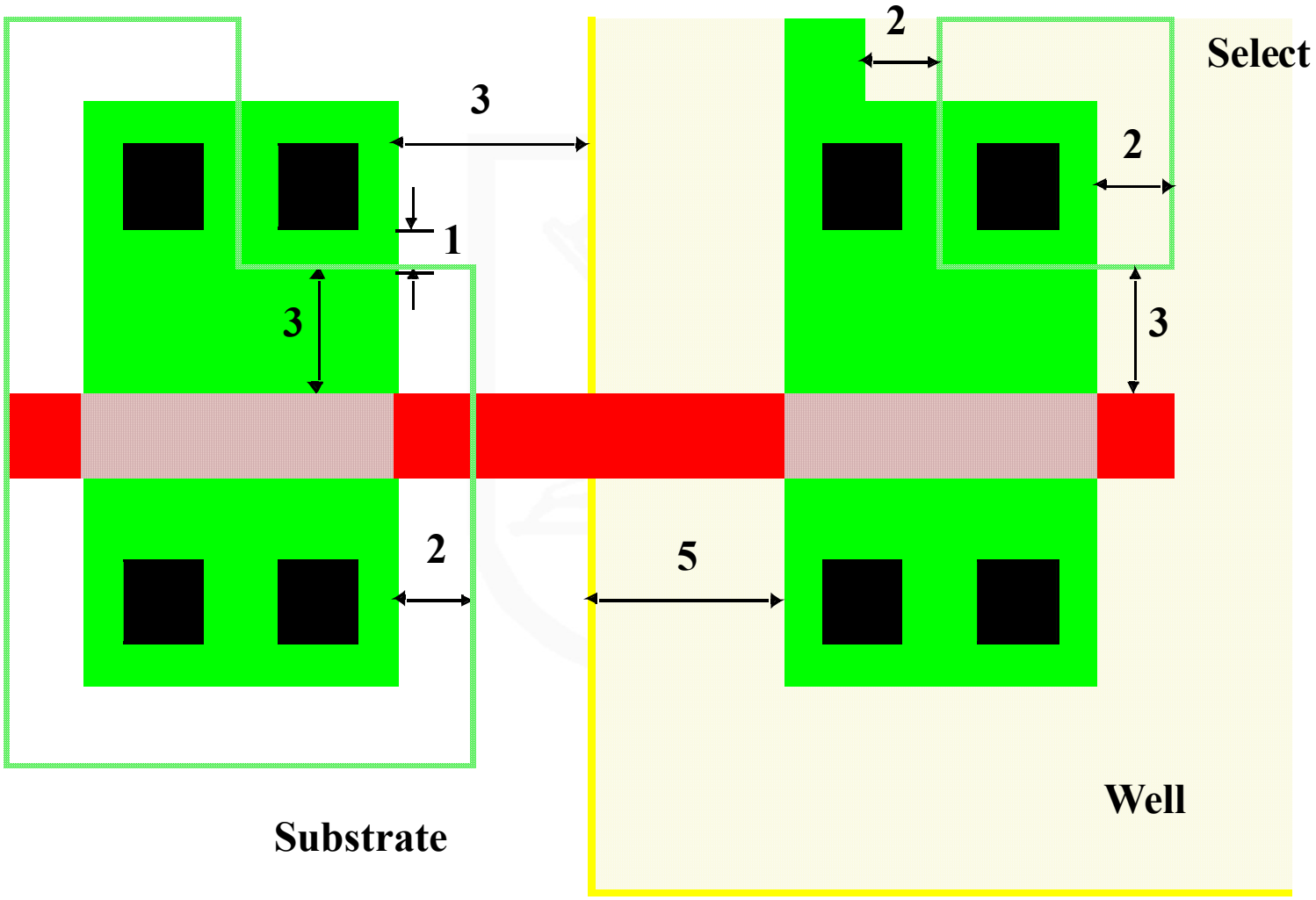




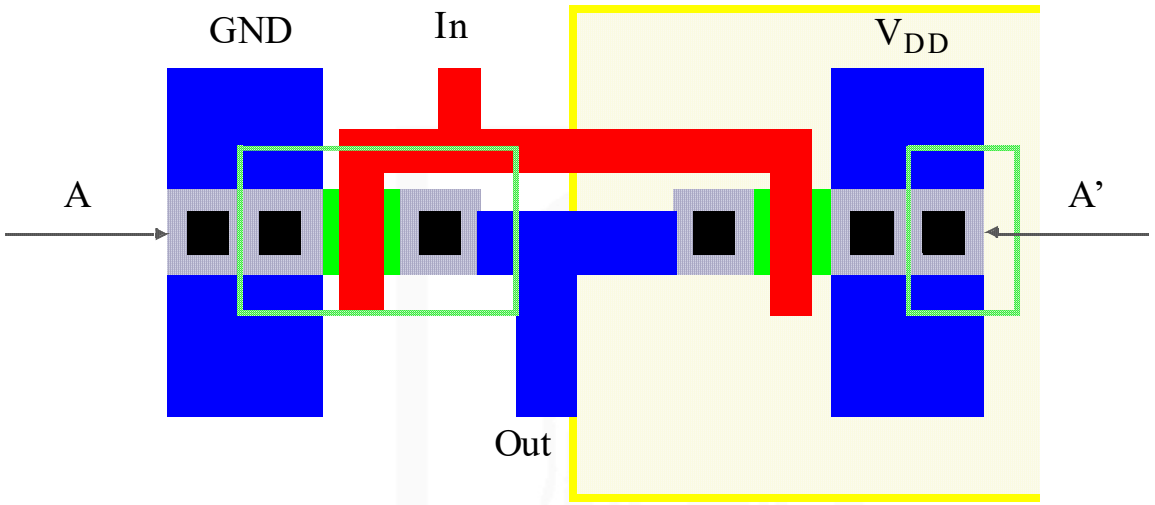
Vias and Contacts



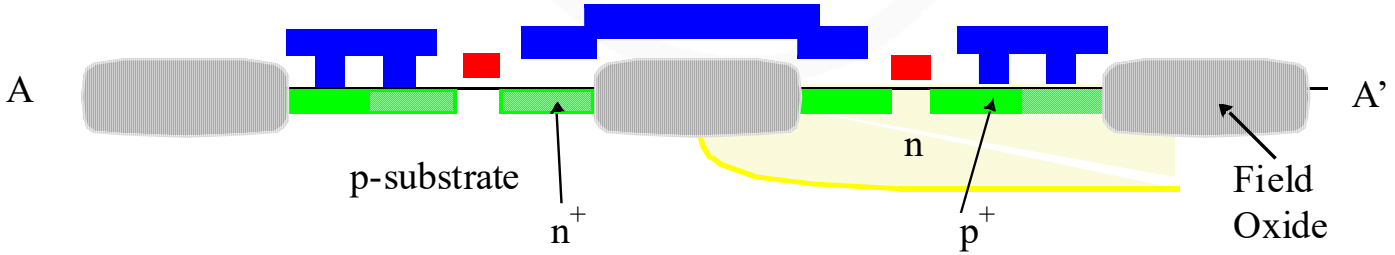
Select Layer



CMOS Inverter Layout

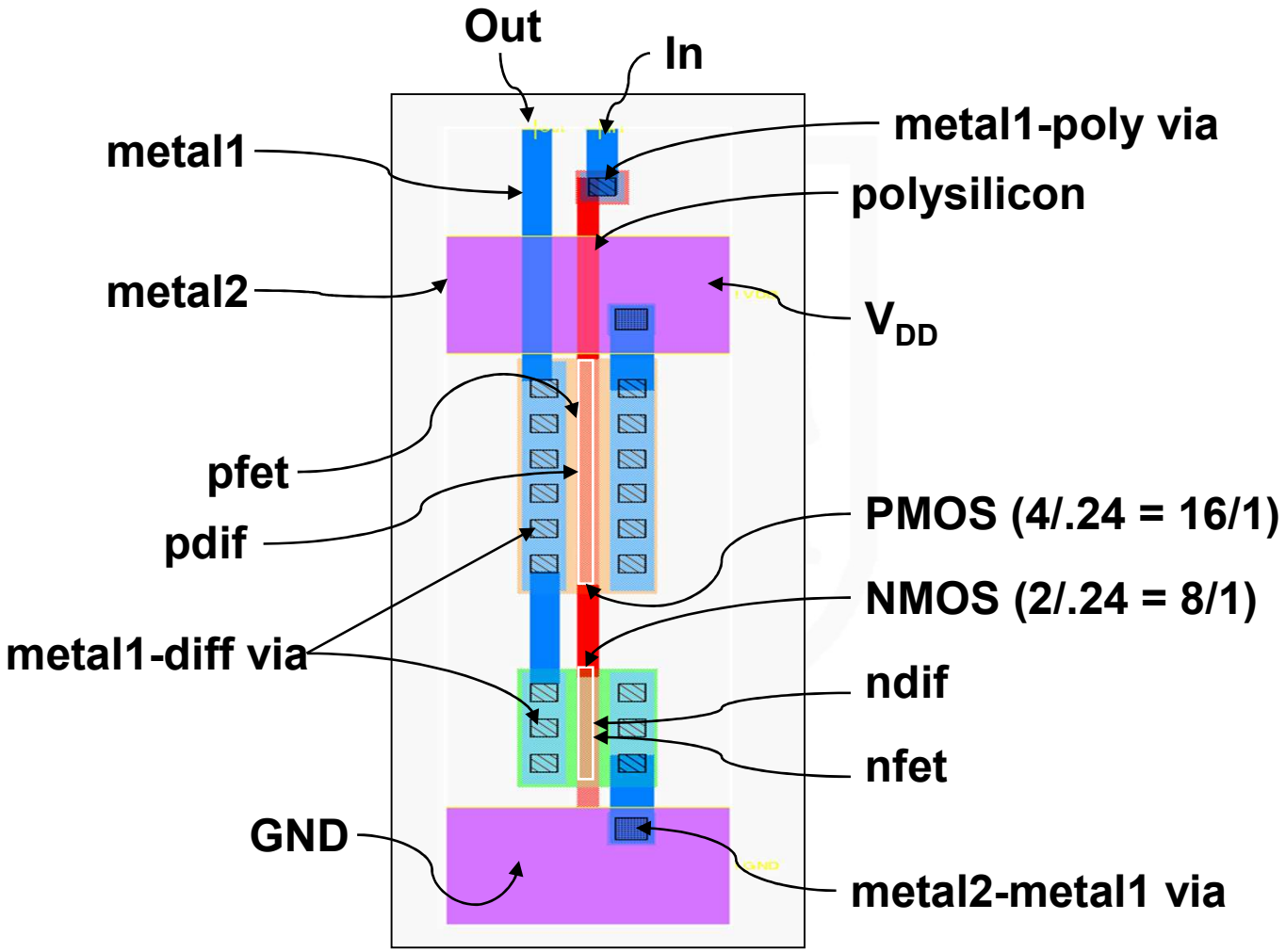


(a) Layout

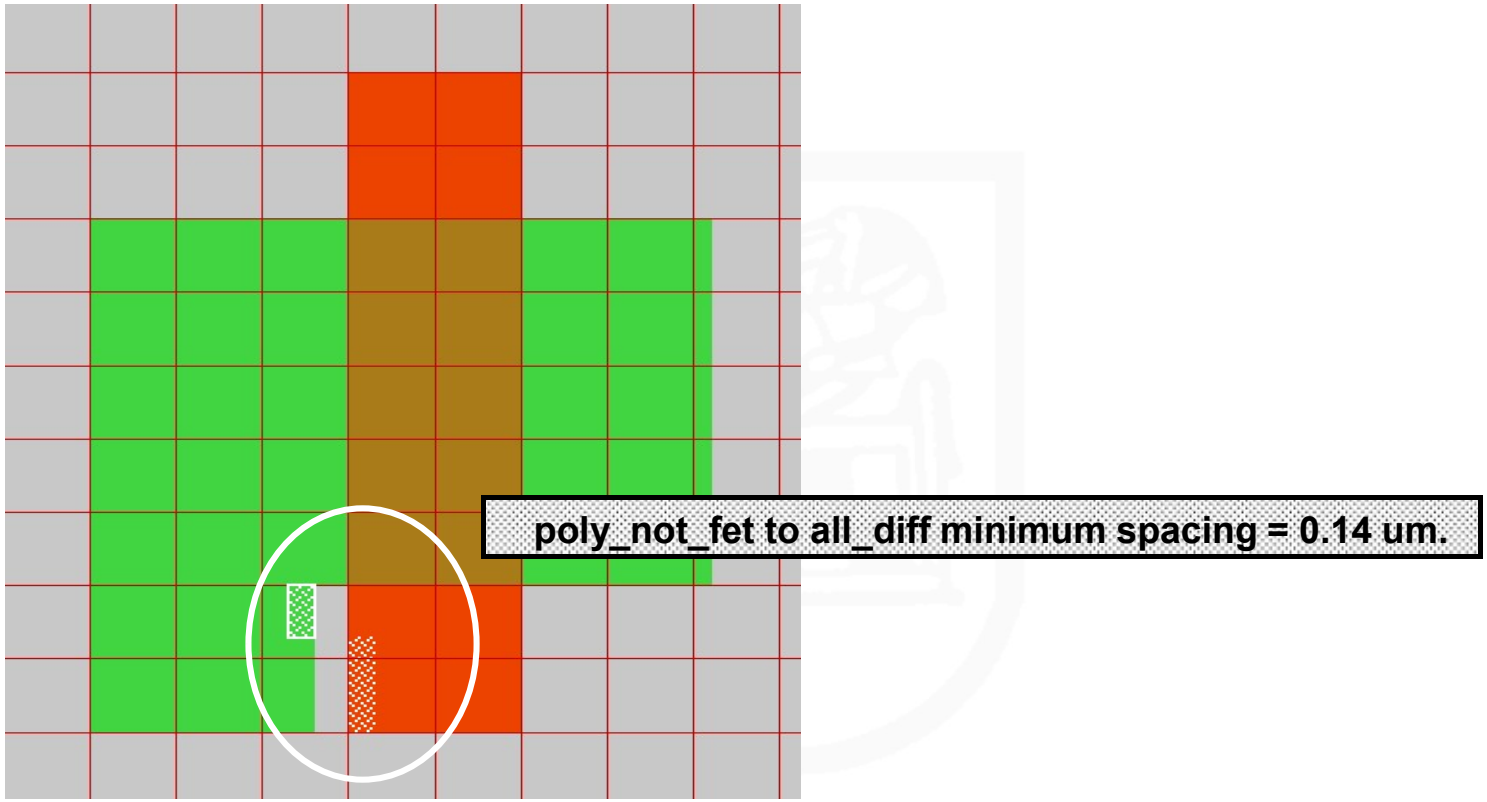


(b) Cross-Section along A-A'

CMOS Inverter *max* Layout

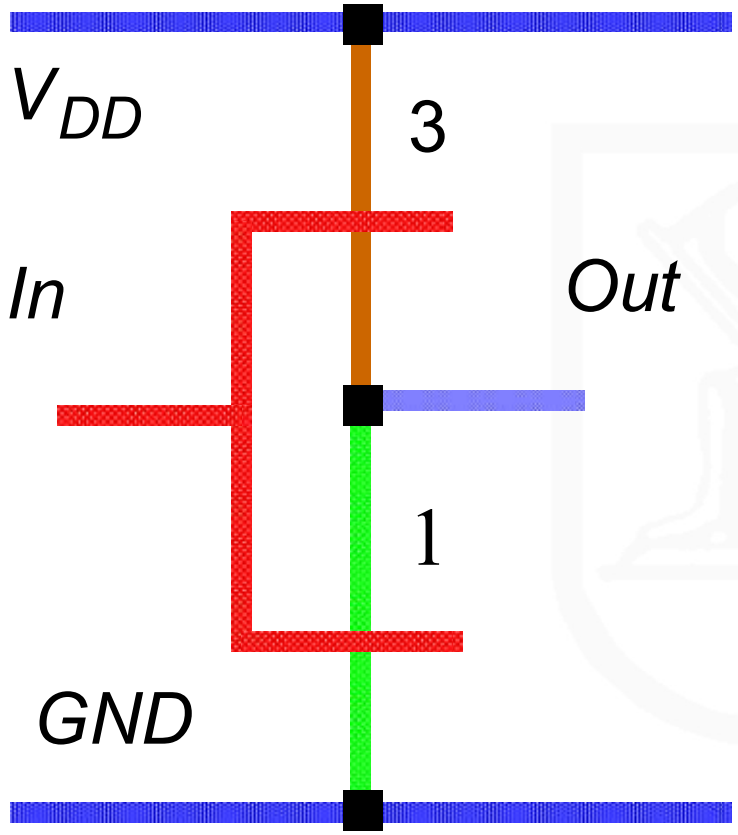


Design Rule Checker



- **The special programs Design Rule Checkers-DRC (e.g., Synopsys' Hercules or Mentor's Calibre) assist the layout designer to verify design rules.**

Sticks Diagram



Stick diagram of inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program

Design for Manufacture (DFM)

- In very deep submicron technologies, attaining large process windows and uniform manufacturing is difficult.
- With advanced processes of 90nm and below, designs with verified DRC check can still result in poorly yielding or even non-functioning silicon.
- Design rules have become more complex with the introduction of conditional rules and recommended rules which makes the design and verification tasks harder.
- With advanced technologies the number of design rules has increased by 300% over previous (130nm, etc.) technologies and absolute design rules are no longer sufficient.

Design For Manufacture (DFM)

- A new adaptive/evolving method is needed between a designer and manufacturer for communicating yield issues.
- This new communication loop is an important step in adopting and implementing a design for manufacture (DFM) flow.
- DFM is a joint work of fabrication, design and mask manufacturers based on a thorough knowledge of process-to-design and design-to-process interactions.

Design For Manufacture (DFM)

- Designers need immediate access from the process engineer to show how various layout characteristics impact chip yield.
- Production-enhancing DFM rules improve information flow between design and manufacturing.
- They are easy-to-implement and proven steps, developed in collaboration with the EDA partners.
- DFM Goal – Increase Yield and Accelerate Time To Entitled Yield

Design For Manufacture (DFM)

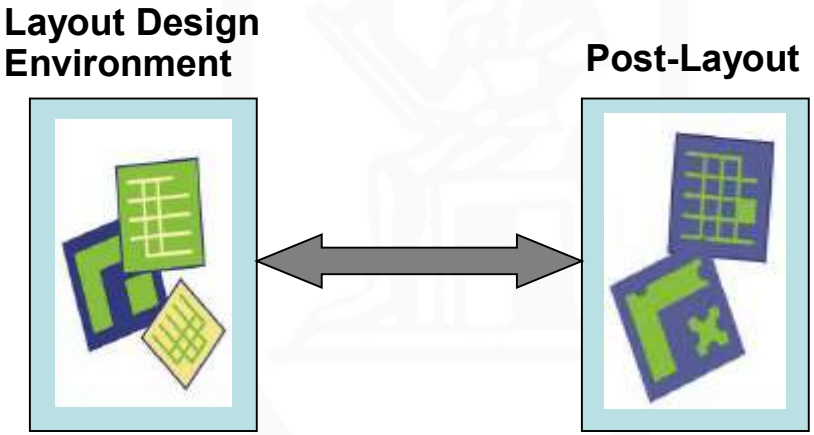
- **Some of these design rules are related to complex lithography effects.**
  - For instance, corners cannot be exactly manufactured as corners and always results in a curvature.
  - This could be a problem if the curvature happens in a sensitive design feature such as a transistor gate.

- **Two options are then available:**
  - Use conservative design rules to avoid corners close to transistor gate
  - Take into account the performance impact in the extraction flow of the transistor characteristics.

- **DFM trades-off competing area, performance, flow complexity and manufacturability.**

Communication Loop Between Process Engineer and Designer

- DFM requires a new level of communication, education and partnership between design companies and foundries.



- The design environment must be implemented for successful DFM methodology.
- Manufacturability starts at the chip design level.

Simulation Based Checks Required

- **With advanced processes of 90nm and below, designs that are verified DRC clean still result in poor yielding or even non-functioning silicon.**