المقدمة

العنصر	الوصف
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عنوان البحث / اللغة الانجليزية	An open source tool for synthesizing and functional verification of asynchronous circuits
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التخصص العام	INFORMATION SYSTEMS
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INTRODUCTION:

1. Background to the research proposal:

Design, testing, and implementing of electronic circuits and systems require the existing of reliable Electronic Design Automation (EDA) and Computer Aided Design (CAD) tools. Since the introduction of EDA/CAD tools, the area of synchronous EDA/CAD tools has witnessed extensive research and software produced by leading universities and companies around the world. On the other hand, the field of asynchronous EDA/CAD tools receives little attention from academic and industrial sectors. At the same time, asynchronous design is essential in many academic programs and industrial applications.

The main aim of this project is to develop an open source tool for synthesizing and functional verification of microelectronic asynchronous circuits. This tool is provided for two groups of users. The first group is undergraduate and postgraduate students who are studying asynchronous circuit design in their programs and the second group is the circuit designers who are working in small-size industrial companies. The said tool is supposed to mainly help the users in:

1. Automating the process of synthesizing asynchronous circuits.
2. Detecting important types of faults and safety violation conditions (e.g. race, deadlocks).
3. Verifying the delay model of timed-circuits (e.g. Speed-Independent).
4. Verifying the functionality of asynchronous circuits.

2. Importance of the proposed research:

Following the sequence of the following points will demonstrate the importance of this research project:

1. EDA/CAD tools are crucial for synthesizing and verifying the functionality of circuits and systems.

2. Asynchronous circuits and systems are essential for many industrial applications (e.g. micro-pipelines and GALS systems) and academic programs.
3. In Saudi Arabia, a survey covers 25 public universities shows that "asynchronous design" is an essential part of the curriculum of 20 universities. Importantly, a number of national industrial companies require designing small-size asynchronous circuits and systems as a part of their regular work.
4. Enterprises-scale EDA/CAD tool companies (e.g. Cadence Design Systems Inc., Synopsys Inc., and Mentor Graphics Inc.) have given little attention to asynchronous design. Leading companies in the area of asynchronous design like ARM and Fulcrum Microsystems Inc. (has been acquire by Intel Corporation) do not license their tools.
5. International academic institutions have noticed this gap and tried hard to fulfilled this need (this is demonstrated in section number 4 in the literature review part) by developing a number of asynchronous EDA/CAD tools and techniques.
6. Despite the efforts put by leading universities into developing EDA techniques and CAD tools, most of the existing attempts does not fulfill the current national and international needs (this is demonstrated in section number 4&5 in the literature review part). Importantly, a reflection upon the large number of attempts that were made by international universities also highlights the importance of this topic of research.

3. Scope of work:

The scope of this project covers EDA techniques and CAD tools for synthesizing and functional verification of asynchronous circuits. Specifically, the research will involve proposing a novel technique for synthesizing and functional verification of asynchronous data-path and timing control circuits. The proposed EDA technique is expected to generate a gate level netlist. The research project will critically study the input formats for different existing asynchronous EDA techniques (e.g. burst-mode, STG, Petri-net) to propose a suitable one for students and beginner designers. The functional verification will cover detecting safety issues (e.g. race, deadlock) as well as checking the correct functionality of

the circuit. Following that, the project will target developing a technology-independent open-source desktop-based CAD tool for the proposed technique. A website that allows downloading the tool along with its user manual is within the scope of this project.

4. Relationship to the priority areas of the Strategic Technologies:

This research project perfectly fits the aims of the National Science, Technology and Innovation Plan (NSTIP) of Saudi Arabia in more than one track under the Information Technology Strategic Priorities:

1. The project aims to develop an open source tool, accordingly, it serves the "Open Source Software (OSS) Engineering" sub-track under the "Software Engineering and Innovated Systems" track.
2. The work will involve analysis and design of a CAD tool, hence, it benefits the "System Analysis and Design" sub-track under the "Software Engineering and Innovated Systems" track.
3. The research will involve computer modelling and simulation of electronic circuit components. Therefore, it fits in the "Computer Modelling" & "Computer Simulation" sub-tracks under the "Scientific Computing" track.

Moreover, the research project will propose a technique and tool for electronic circuits, therefore it fits the "Electronics, Communication & Photonics" Strategic Priorities.

Importantly, the main outcome of this project will save the budget of local universities that are teaching circuit design, by providing them an open-source tool.

SUMMARY ARABIC:

إن تصميم الدوائر والنظم الالكترونية الدقيقة يعتمد بقوة على وجود برامج ممكن الاعتماد عليها لميكنة التصاميم الإلكترونية والتصميم بمساعدة الكمبيوتر. تقوم هذه البرامج بنمذجة السلوك الحقيقي للمكونات الإلكترونية داخل شرائح السيليكون بالإضافة إلى إعطاء تقادير للمعايير الأساسية للدوائر الإلكترونية ضمن نطاق مقبول من الخطأ. وعلاوة على ذلك، فأن هذه البرامج تمكن الكثير من الأنشطة والمهام الشاقة والمعقدة التي من المفترض أن يقوم بها المصممين.

بناءاً على المسح الادبي، فإن الدوائر الالكترونية الدقيقة يمكن تقسيمها إلى دوائر متزامنة ودوائر غير متزامنة. الدوائر المتزامنة تعتمد في عملها على وجود ساعة واحدة تقوم بمزامنة أنشطة الأجزاء المختلفة، في حين أن الدوائر غير المتزامنة تعتمد في عملها على أكثر من ساعة أو قد لاتعتمد على إي ساعة.

منذ استحداث برامج ميكنة التصاميم الإلكترونية والتصميم بمساعدة الكمبيوتر، شهد مجال تطوير تلك البرامج للدوائر المتزامنة بحث واسع و برمجيات انتجتها كبريات الجامعات والشركات في جميع أنحاء العالم. من ناحية أخرى، فإن مجال تطوير تلك البرامج للدوائر غير المتزامنة لقي القليل من الاهتمام من القطاعات الأكاديمية والصناعية. في الوقت نفسه, فإن تصميم الدوائر الالكترونية غير المتزامنة أساسي في كثير من البرامج الاكاديمية والتطبيقات الصناعية.

يقترح هذا المشروع البحثي تطوير أداة مفتوحة المصدر لتجميع والتحقق من وظيفية الدوائر الالكترونية الدقيقة غير متزامنة. وهذه الأداة سيستفيد منها الطلاب الذين يدرسون تصميم الدوائر في التخصصات الاكاديمية وكذلك أساتذة الجامعات الذين يدرسون أو يبحثون في هذا المجال. وستستهدف هذه الأداة أيضا مساعدة مصممي الدوائر غير المتزامنة في الشركات الصناعية. بناءاً على ذلك، فإن هذا المشروع سيعزز إلى حد كبير تطوير البحث والتعليم والتكنولوجيا والصناعة في المملكة العربية السعودية وكذلك في جميع أنحاء العالم.

سيبدأ هذا المشروع بالمسح الأدبي الشامل للدوائر غير المتزامنة وبرامج ميكنة التصاميم الإلكترونية والتصميم بمساعدة الكمبيوتر. بعد ذلك سيقوم المشروع بإقترح إطاراً وأجراءاً متكاملاً لتجميع والتحقق من وظيفية الدوائر غير المتزامنة. بعد ذلك، سيتم تطوير أداة مفتوحة المصدر لإنجاز هذه الإجراءات. وأخيرا، سيتم اختبار الأداة ونشرها.

SUMMARY ENGLISH:

Design of microelectronic circuits and systems strongly replies upon the existence of mature Electronic Design Automation (EDA) and Computer Aided Design (CAD) tools. The purpose of these tools is to model the real behavior of electronic components inside silicon pieces as well as provide an estimation of key parameters of the circuit with an acceptable range of error. Moreover, these tools automate various tedious and complex activities that the designers are supposed to perform.

According to literature, microelectronic circuits can be divided into synchronous and asynchronous circuits. The operation of the former depends upon the existence of one clock that synchronize the activities of various parts, while the later has no clock or more than one clock.

Since the introduction of EDA/CAD tools, the area of synchronous EDA/CAD tools has witnessed extensive research and software produced by leading universities and companies around the world. On the other hand, the field of asynchronous EDA/CAD tools receives little attention from academic and industrial sectors. At the same time, asynchronous design is essential in many academic programs and industrial applications.

This research project proposes to develop an open source tool for synthesizing and functional verification of microelectronic asynchronous circuits. Such tool will benefit students who are studying circuit design in their programs as well as academic professors who are teaching or researching such an area. The tool also targets helping asynchronous circuit designers in industrial companies. Accordingly, this project will significantly enhance the development of research, education, technology, and industry in Saudi Arabia as well as worldwide.

The project will start by covering the literature of asynchronous circuits and exiting EDA/CAD tools. Based upon the results obtained from the literature, the project will propose a complete framework & procedure for synthesizing & functional verification of asynchronous circuits. Following that, the proposed procedure will be implemented in an open source tool. Finally, the tool will be tested and published.

LITERATURE REVIEW :

Microelectronic systems are manufactured in silicon chips to carry out computation and data processing, where these activities are represented in silicon layers by movement of signals [1]. These signals are actually flow of electrons inside system components. In order for the whole system to achieve its function correctly and reliably, every signal has to arrive and leave its relevant hardware component in the right time. Otherwise, if the signal arrives early than its right time, it will deliver wrong data to the component and if the signal leaves the hardware component later than its right time, it will collect wrong data [2]. Both cases result in a functional failure of the electronic system, which will appear as wrong computation and/or processing.

In order for the microelectronic system to regulate its internal signals, so that each signal arrives its corresponding hardware component in the right time and leaves it in the right time, it requires a timing controller [3]. Based upon this timing controller, the system can be categorized into two main categories, synchronous and asynchronous system [1].

1. Synchronous systems:

In synchronous system, all hardware components that are required to exchange data with their neighbors are connected to a single unit called clock generator as shown in Figure 1. This generator produces a square wave signal called clock. Clock generator has to satisfy the fan-in/out conditions of the system [2]. Therefore, additional circuitry called clock buffer circuits are usually added to the system to buffer the clock signal. Circuit components that contains clock buffers and its connected gates are called clock distribution networks or clock tree [3].

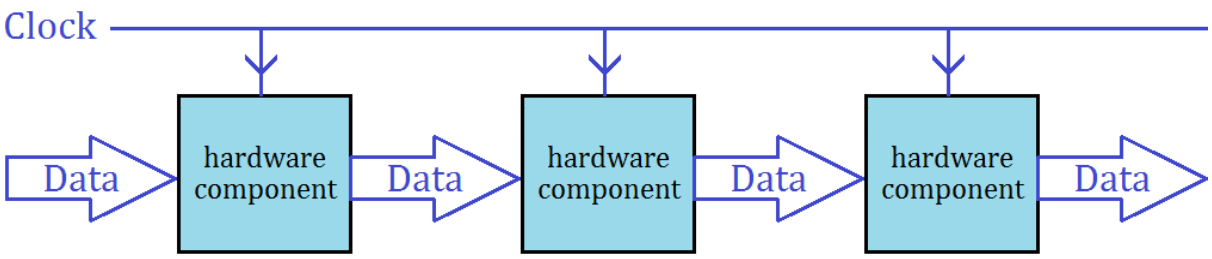

Figure 1. Block diagram of a synchronous system that works based on a global clock.

Clock regulates the data flow between different components according to a utilized global protocol. An example of this protocol could be as follows [3]:

1. Falling edge of the clock means that the input data are stable and ready for collection. Hence every hardware component starts collecting its input data after the falling edge.
2. Rising edge of the clock means that the input data are not stable anymore and could be changed anytime. Therefore, before the rising edge, every hardware component should have already latched its input data.
3. After rising edge, every hardware component starts processing its input data in order to make it ready and stable before the next falling edge.

Initially, the specifications of the clock (e.g. frequency and duty cycle) is determined by the time required by the slowest hardware component in the system to complete its relevant tasks. Then, safe margin is added to the specifications in order to accommodate expected reliability concerns that might appear after fabrication. Reliability issues include Process, Voltage, Temperature, and Ageing (PVTA) variations [1-3].

The reliance of synchronous systems on clock puts several limitations on them. As the system increases in complexity and size, the scale of these limitations increases as well. The main of these limitations are skew of clock signal, power consumption of clock, operating the system based on worst case performance, and the need of synchronizing external inputs [3-4].

2. Asynchronous systems:

In asynchronous systems, there is no global clock. Instead, every two or more components, that are supposed to exchange data, communicate via a local predefined protocol. According to literature, there are two main types of protocols [4]:

1. Bundled data: In this protocol, each set of data is bundled with a request and acknowledgment signals, hence the name of the protocol. Figure 2 shows a block diagram of an asynchronous system that utilizes a bundled data protocol. Exchanging data starts by issuing the data and then sending a request signal to the successor component to inform it that the data is stable and ready for collection. After the receiver latches the data, it sends an acknowledge signal to the predecessor component to inform it that the data was successfully collected. After sending the acknowledgement signal, the receiver starts processing the data, then issues the output and sends request signal to its successor and so on.

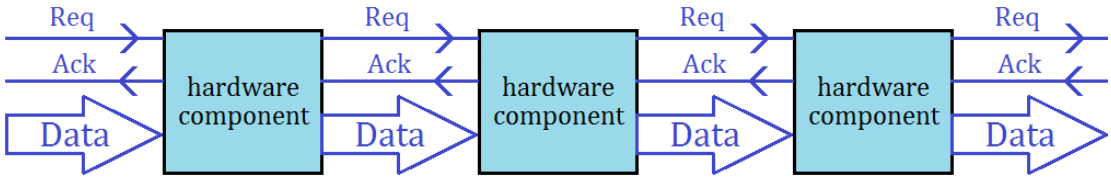

Figure 2. Block diagram of an asynchronous system that utilizes a bundled data protocol.

2. Dual rail: Dual rail protocol combines the request signal with every bit of the data, which results in doubling the number of data bits. Combing request with data is called dual rail encoding, where the interpretation of a two bit encoded data is described in the Table 1. The first bit is called the true bit of data, which is abbreviated to (d.t), while the second bit is called the false bit of data and is abbreviated to (d.f). Figure 3 shows a block diagram of as asynchronous system that utilizes a dual rail protocol. Similar to bundled data, the sender issues the encoded data, which contains the request signal as well. Then receiver latches the data and return with the acknowledgement signal and so on [4].

Table 1. The interpretation of two-bit encoded dual rail data.

Data	First bit (d.t)	Second bit (d.f)	Interpretation
00	0	0	Empty (E)
01	0	1	Valid data (0)
10	1	0	Valid data (1)
11	1	1	Not used

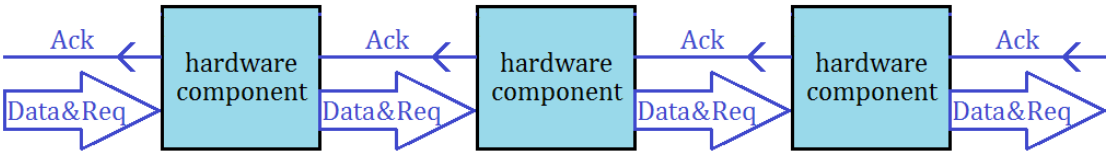

Figure 3. Block diagram of an asynchronous system that utilizes a dual rail protocol.

Based on the number of actions per communication process, the protocol described above can be implemented either in 2-phase signaling or 4-phase signaling [4]:

1. Four-phase signaling scheme: as the name suggests, this protocol contains 4 actions for each communication process between two or more hardware components. An example of 4-phase dual rail protocol would be as follows: 1) the sender issues a valid encoded data (01 or 10), 2) the receiver collects the data and then sets the acknowledgement signal high, 3) the sender issue an empty data (00), and 4) the receiver sets the acknowledgment signal low. This scheme is also called return-to-zero because the acknowledgement signal (in dual rail) and request & acknowledgement signals (in bundled data) returns to zero at the end of each communication process.
2. Two-phase signaling scheme: as the name suggests, this protocol contains 2 actions for each communication process between two or more hardware components. An example of 2-phase bundled data protocol would be as follow: 1) the sender issues a valid data and then flips the request signal (if it is 0, changes it to 1 and if it is 1, changes it to 0). 2) the receivers collects the data and then flips the acknowledgement signal (if it is 0, changes it to 1 and if it is 1, changes it to 0). This scheme is also called non-return-to-zero because the acknowledgement signal (in dual rail) and request & acknowledgement signals (in bundled data) does not return to zero at the end of each communication process.

According to the literature, two-phase systems are faster and consumes less energy than four-phase systems. However, four-phase systems is easier to implement and test than two-phase systems [1,4].

Moving one level downward from the system level to circuit level requires specifying how the handshaking signals are generated and how the temporal configurations of the circuit components are defined. This is generally called delay model of asynchronous circuits and it can be defined as the maximum delay the circuit component can tolerate before it malfunctions. Accordingly, asynchronous circuits can be classified based upon its delay model to [4,5]:

1. Speed Independent (SI): speed independent asynchronous circuit is an asynchronous circuit that works correctly regardless of the delay of its gates as long as its wire delay is zero or negligible.
2. Delay insensitive (DI): delay insensitive asynchronous circuit is an asynchronous circuit that works correctly regardless of the delay of its gates and wires.

Based upon that, delay insensitive circuits are more robust, in terms of delay tolerance, than speed independent circuits. Unfortunately, delay insensitive circuit is more difficult to design, implement, and test than speed independent circuit. Generally, only inverters and C-elements can be used to construct delay insensitive circuits [4].

The absence of clock in asynchronous systems puts several limitations on them. As the system increases in complexity and size, the scale of these limitations increases as well. The main of these limitations are the latency of handshaking, the failure due to hazards and race conditions, and most importantly the lack of mature and available asynchronous EDA/CAD tools [1,3,4,6,7].

3. Importance of Asynchronous Design:

As mentioned earlier, many EDA/CAD tools support synchronous design. Therefore, designing, synthesizing, and testing of synchronous circuits and systems are easier than asynchronous ones. However, asynchronous design is attractive for some applications and mandatory for others. It is attractive whenever the designer would like to avoid the overhead associated with the clock, or operate the system based on average-case performance instead of worst-case one. Importantly, asynchronous design is mandatory for

some applications such as Globally Asynchronous Locally Synchronous (GALS) and multiple clock systems. Furthermore, asynchronous design is an essential part of circuit design module in most academic programs [1-4].

4. Asynchronous EDA/CAD tools:

Design of microelectronic circuits and systems strongly replies upon the existence of mature EDA/CAD tools. Since the introduction of EDA/CAD tools, the area of synchronous EDA/CAD tools has witnessed extensive research and software produced by leading universities and companies around the world [1,8]. On the other hand, the field of asynchronous EDA/CAD tools receives little attention from academic and industrial sectors. The text below covers asynchronous EDA/CAD tools that have been mentioned in the literature in a comprehensive manner. For each tool, the text mentions the maintainer of the tool, its availability, and its features [9-11]:

1. 3D by University of California: The tool is not available anymore. It is claimed that the tool is capable of synthesizing sequential and delay-insensitive circuits after reading the specifications in extended burst-mode (XBM).
2. ACK by University of Utah: The tool is not available anymore. It is claimed that ACK is a synthesize tool that automate the design from high-level specifications all the way down to layout.
3. Balsa by University of Manchester: The tool is available for download but it is still under development & testing. The purpose of the tool is synthesizing asynchronous handshaking circuits from high-level specifications. One of the limitations of Balsa is that it requires prior knowledge to a number of uncommon languages including Balsa and Breeze, which are relatively easy for an experienced user. Importantly, Balsa cannot verify the functionality of the circuits.
4. CADP by INRIA Rhone-Alpes: The tool is available for free for academic institutions only. CADP is dedicated to simulate protocols & concurrent models written in special language called LOTOS.
5. CASCADE by Kaiserslautern University of Technology: The tool is still under development. Developers wish to enable users to generate Verilog netlists of asynchronous sequential circuits from specifications written in a format known as generalized STG (gSTG).

6. CAST by California Institute of Technology: The tool is only available internally at Caltech and Situs Logic. CAST is a powerful tool that covers high-level synthesize, logic synthesize, and physical design as well. The tool reads user inputs in a special language called CHP.
7. CCS-based specification by The University of Edinburgh: The tool is available for educational and research purpose only. The tool is dedicated for modelling and property checking of asynchronous pipelines. CSS language is required to use this tool.
8. Clp by Newcastle University: The tool can be downloaded and used for academic and research purpose only. It is proposed to check some safety features (e.g. deadlock freeness) of Petri-Net.
9. ConfRes by Newcastle University: The tool can be downloaded and used for non-commercial purpose. ConfRes is provided to resolve coding conflicts in STG specifications.
10. DESI by Kaiserslautern University of Technology: The tool is not available anymore. It was provided mainly to decompose STG specifications into components.
11. di2pn, syndi, and diana by London South Bank University: The tools are available for download for educational and research purpose only. The tools are dedicated to generate Petri-Nets from the specifications that is supplied as inputs to the tools.
12. DGC by University of Erlangen-Nuremberg: The tool is available for download but it is still under development and bug fixing stage. It is claimed that DGC can read user inputs in the form of bust-mode description and then generate gate-level netlist as well as physical layout of any asynchronous state machine.
13. FIREMAPS/Process Spaces by McGill University and Canada & University of Auckland: The tool is not available anyone. It is claimed that the tool is capable of designing, testing, and verifying asynchronous circuits.
14. Handshake Technology Design Flow by Handshake Solutions, Philips Technology Incubator, and Eindhoven: This tool is not free. The purpose of this tool is generating gate-level netlists of handshaking circuits from user inputs written in special language called Haste.
15. LARD by University of Manchester: This tool is not available anymore. It just provides an asynchronous system hardware-description-language.

16. MINIMALIST by Columbia University: This tool is available for non-commercial use only. MINIMALIST is dedicated to generate hazard-free gate-level netlists of asynchronous circuits from specifications written in burst-mode. One of the important limitations of this tool is producing the output in two forms only either two-level circuit or generalized C-elements.
17. OptiMist by Newcastle University: This tool is available for download. It accepts STG specification of asynchronous circuit in text format. Then, it processes the specification and maps it into an asynchronous circuit. The main drawback of this tool is that it only maps STGs into David-Cells (DCs) realizations. OptiMist does not verify the functionality of asynchronous circuits.
18. Petrify by Universitat Politenica de Catalunya: This tool is available for download. It is a text-based tool that requires user to enter STG specification of the asynchronous circuit in special format. Then Petrify processes the STG, encodes the states and generates the equations of the gate-level netlist. Unfortunately, Petrify does not verify the functionality or safety properties of the synthesized circuits, Moreover, for some types of STGs, Petrify fails to find a solution, even if it exists.
19. Punf by Newcastle University: The tool is available for download. It is dedicated to take Petri-net as inputs and generate a finite complete prefix of its unfolding.
20. SIS by University of California at Berkeley: The work on this tool has stopped since 1994. According to the tool developers: “SIS is currently not maintained and may be hard to use, not only compile”. The purpose of SIS is generating a gate-level net-list from STG specifications.
21. TAST by TIMA Laboratory: This tool is not available anymore. TAST is dedicated to produce Petri-nets from high-level specification of the asynchronous circuit in form of CHP (Communicating Hardware Processes) language.
22. Theseus NCL Synthesis Flow by Theseus Logic, Inc.: This tool is not free for any purpose. The purpose of the tool is producing DI circuits by utilizing NULL Convention Logic (NCL) technique.
23. Transyt by Universitat Politenica de Catalunya: This tool is still under development. Its main purpose is verifying a number of safety properties of timed systems.
24. Veraci by University of Cambridge: This tool is still under development. Veraci is provided to conduct formal verification of asynchronous circuits.

25. VeriMap by Newcastle University: This tool is still in testing stage and it is available for download. The purpose of the tool is converting single-rail RTL Verilog netlists to dual-rail ones.
26. VerySAT by Newcastle University: The tool is claimed to be available for download but it is not. This tool is supposed to process STG specifications to detect any safety issues in them and then derive gate implementation of the circuit.
27. VSTGL by Technical University of Denmark: The tool is available for download. This tool allows the user to graphically create an STG specification, simulate it, and generate a text file that describes it.
28. ATACS by University of Utah: This tool is not available for public anymore. It accepts inputs in different formats including VHDL, Petri-nets, and burst-mode. It is claimed that the tool is capable of synthesizing and analysing timed circuits.
29. Butler by MBDA: This tool is not available anymore.
30. Oolong by University of Manchester: This tool is not available anymore.
31. PipeFitter by Politecnico di Torino: This tool is claimed to be available but it is not.
32. Weaver/Gate Transfer Level (GTL) synthesis by Boston University: This tool is not available anymore.
33. XDI by Eindhoven University of Technology: This tool is not available anymore.

In conclusion, some of the previously developed tools perfectly fit the research gap, however, the institution that owns the tool does not licence it for any purpose. Some other tools partially fit the research gap, but they are either still under development or very restricted in terms of the inputs and outputs format.

5. Research Gap and Problem Statement:

This research project proposes to develop an open source tool for synthesizing and functional verification of microelectronic asynchronous circuits. Such tool will benefit students who are studying circuit design in their programs as well as academic professors who are teaching or researching such an area. The tool also targets helping asynchronous circuit designers in industrial companies. Accordingly, this project will significantly enhance research, educational, technological and industrial development in Saudi Arabia as well as worldwide.

RESEARCH METHODOLOGY :

This project contains six coherent phases, which are:

1. **Study and reviewing phase:** the main tasks in this phase are reviewing and performing critical study of asynchronous synthesizing and functional verification techniques. The reviewing will cover highly cited publications including journals, conferences, and books. Importantly, the study will cover all parts of the asynchronous system including data-path and timing controller. Moreover, for each part the study will investigate the existing design techniques (e.g. completion detection, delay elements, delay models, handshaking, etc.).
2. **Assessment phase:** the main task in this phase is assessing the available Electronic Design Automation (EDA)/Computer Aided Design (CAD) tools in their ability to synthesize and verify the functionality of asynchronous circuits including both the data-path and the timing controller. The output of the assessment phase will show for each tool if that tool meets all/some/none of the requirements of synthesizing and functional verification. The assessment will be based upon a complete framework, which will be develop in this phase as well.
3. **System analysis, design, and development phase:** The first task in this phase is proposing a complete procedure that allows synthesizing and functional verification of asynchronous circuits including both data-paths and control circuits. The second task is analyzing the requirements and completing the use-case of the system. The third and fourth tasks in this phase are designing the data structure and software structure of the tool, respectively. The designing of data structure is of crucial importance because the right data structure will help in describing the circuit elements and their models in the right way. Following that, this phase will contain a task to review the available open source environments and programming languages in order to select the one that fits the data designed structure and the requirements of the tool. The final tasks in this phase are coding the individual modules and integrating all modules under one menu.

4. **Tool testing and error correction phase:** The first task in this phase are testing the tool to check the validation of the data in the back end of the tool. If the data validation test is successful, the following tasks are performing exception and functional test.
5. **Producing tool documentations and manuals phase:** the first task in this phase is compiling and producing the system documentation that allows future development and bug fixing. The second task is producing the user manuals, which will help new users in mastering the tool. The third and last task of this phase is producing the project final report.

VALUE TO THE KINGDOM:

As demonstrated earlier, circuit design whether it is synchronous or asynchronous strongly replies upon the existence of mature EDA/CAD tools. While the field of synchronous EDA/CAD tool has witnessed extensive research and software produced by leading universities and companies around the world, asynchronous tools have received little comparable attention. Existing tools are either mature but cannot be licensed for any purpose or immature and are free for limited usage.

This research project proposes to develop an open-source tool for synthesizing and functional verifications of asynchronous circuits. Such a tool will benefit students who are studying circuit design in their academic programs as well as academic professors who are teaching or researching such an area. Circuit designers who are working in small-size industrial companies will be able to use this tool as well. The said tool is supposed to mainly help the users in automating the synthesizing of asynchronous circuits, detecting faults, verifying the delay model of the timed-circuit, and verifying the functionality of asynchronous circuits.

The introduction and literature review sections have demonstrated that asynchronous design is an essential part of the curriculums at academic institutions that teach circuit design, digital design, IC design, or similar modules. In Saudi Arabia, a survey covers 25 public universities shows that 20 of them teach asynchronous design in one or more modules per year. Unlike other EDA/CAD tools, the provided tool is free and open-source. Therefore, it will be easy for students to download and utilize this tool in their

personal computers without working on campus or connecting to laboratory servers. Accordingly, the tool produced by this research project will directly enhance the national academic education and teaching. At the same time, it will indirectly enhance the national training and career development through providing such a tool to improve the understanding of asynchronous circuit design. In the field of academic research, asynchronous design is a vital research area as well. Since 1994, IEEE has been sponsoring the International Symposium on Asynchronous Circuits and Systems (ASYNC) in a yearly basis. Also, it has been demonstrated that asynchronous design is crucial to industrial and commercial sectors that are specialized in electronic circuits and systems. Importantly, processors in smart phones and tablets that are supplied by Apple Inc. and Samsung are all ARM technologies, which are all based on asynchronous design techniques. In Saudi Arabia, a number of industrial companies utilize asynchronous circuits to synchronize data and control machines. So, asynchronous design is important for educational, research, and industrial sectors both nationally and internationally. Therefore, this research project will enhance the development of the mentioned sectors in Saudi Arabia and worldwide. This project will involve theoretical research in the field of circuit design and real implementation in the field of software engineering. On one hand, the project will advance the industrial capabilities in the field of circuit design to meet the critical needs in the Kingdom. On the other hand, the project will support the expanding and innovative IT industry in the Kingdom. Importantly, the project will enhance the quality of research and education in the Saudi universities though publishing a number of manuscripts in international highly cited journals and conferences.

This research project perfectly fits the aims of the National Science, Technology and Innovation Plan (NSTIP) of Saudi Arabia in more than one priorities, tracks, and sub-tracks. In priorities, it serves the “Information Technology” and “Electronics, Communication &

Photonics" Strategic Priorities. In terms of tracks, it benefits the "Software Engineering and Innovated Systems" and "Scientific Computing" tracks. It terms of sub-tracks, it fits the "Open Source Software (OSS) Engineering", "System Analysis and Design", "Computer Modelling", and "Computer Simulation" sub-tracks. Finally and importantly, educational institutions can license this tool for free. Therefore, it will save the budget of local universities. Research institutions that will utilize this tool will have to acknowledge MOHE, KACST, NSTIP, and UQU. This will increase the appearance of these institutions names in publications. Despite that industrial companies can license this tool for free, companies that require special support or customization for utilizing this tools, will have to pay for this service. This will create an opportunity for potential market for this tool and will make this research project a strong basis to support the Saudi knowledge-based economy.

مراحل المشروع

مسلسل	المرحلة	وصف المرحلة
1	Phase 1	phase 1

أهداف المشروع

مسلسل	الهدف
1	Objective 1

طريقة تحقيق أهداف المشروع

مسلسل	الهدف	طريقة تحقيق الهدف
1	Objective 1	Objective 1 Objective 1 Objective 1 Objective 1

خريطة أهداف - مراحل- مهام المشروع

الهدف	المرحلة	المهمة
Objective 1	Phase 1	task1

أدوار الفريق البحثي ومدة التنفيذ لكل عضو

أعضاء الفريق - الدور	مدة التنفيذ
عبدالله عمر محمد باز --- باحث رئيسي	12 شهر
فيصل احمد خليل علاف --- باحث مشارك	5 شهر
اداري-1	4 شهر
فني-1	2 شهر

خطة العمل - الجدول الزمني

المراحل والمهام	الفريق البحثى	مدة المشروع											
		1	2	3	4	5	6	7	8	9	10	11	12
Phase 1	عضو الفريق / الدور												
task1	عبدالله عمر محمد باز --- باحث رئيسي												
task1	فيصل احمد خليل علاف --- باحث مشارك												
task1	اداري-1												
task1	فني-1												

خريطة مخرجات وأهداف المشروع البحثى والأهداف الاستراتيجية للبرنامج

مخرجات المشروع المتوقعة	أهداف المشروع المطلوب تحقيقها	الأهداف الإستراتيجية للبرنامج					
		1	2	3	4	5	6
outcome 1	Objective 1		Y		Y		

الأهداف الإستراتيجية للبرنامج

مسلسل	الهدف الإستراتيجي
1	إدماج أعضاء هيئة التدريس الجدد في العملية البحثية، وتوفير احتياجاتهم البحثية
2	إتاحة الفرصة للباحثين الجدد للتعرف على أوعية البحث العلمي المتاحة، وتشجيع ثقافة المبادرة
3	تحقيق الاستدامة العلمية، والبحثية، وكسر الفجوة بين الأجيال، ونقل الخبرات بين أعضاء هيئة التدريس القدامى، والجدد
4	تشجيع أعضاء هيئة التدريس الجدد على الوصول إلى مبدأ الريادة
5	تدريب أعضاء هيئة التدريس الجدد على إدارة المشروعات البحثية، وكتابة، ونشر البحوث، والتقارير العلمية
6	إيجاد الآليات، والحوافز اللازمة لاستقطاب المبدعين، والمبتكرين المتميزين من الوطنيين للعمل في المراكز البحثية

البند	القيمة بالريال السعودي
الموارد البشرية	
الموارد البشرية	48,000.00
الاجمالي	57,380.00
المواد	
الأدوات	200.00
التجهيزات الأساسية	600.00
الأعمال المهنية	200.00
المواد	0.00
الاجمالي	1,000.00
السفريات	
المؤتمرات	500.00
التدريب	0.00
الزيارات الميدانية	600.00
الاجمالي	1,100.00
مصروفات أخري	
تكاليف النشر	400.00
مساعدات الكتابة	0.00
الكتابة العلمية	0.00
الاجمالي	400.00
الاجمالي	59,880.00

Manpower Justifications:

All tasks in this research project will be conducted by two investigators, two research assistants, and a consultant. The text below shows the track record of the researchers that are relevant to the area of this project along with the tasks assigned to each one.

Principle Investigator (PI): Dr. Abdullah Baz is an active researcher and the Vice Dean of Deanship of Scientific Research (DSR) in Umm Al-Qura University (UQU). He has good experience in asynchronous circuit design since he was with the "Next Generation Energy-Harvesting Electronics: A Holistic Approach". This project was funded by **£1.6M** from the UK Engineering and Physical Sciences Research Council (EPSRC). During this project Dr.Baz has successfully designed, implemented, and fabricated two functional ICs. The first one is a self-timed SRAM that works based on completion detection, for which he has designed an SI timing circuit. The second IC is an asynchronous voltage sensor. More details: about the project can be found in: http://www.holistic.ecs.soton.ac.uk/. Dr.Baz has good experience in software development. After completing of his BSc degree, he joined the Deanship of Information Technology (DIT) in UQU. He worked in DIT as a software developer for five years. Dr.Baz master thesis was about developing a software package for solving engineering dilemmas. He also has another master degree, where his thesis was about developing a software that simulate the error performance of communication channels. Dr.Baz has been awarded the best paper award in the 20th international workshops on Power & Timing Modelling, Optimization and Simulation (PATMOS-2010). He has been invited to submit a journal paper to the Journal of Low Power Electronics (JoLPE), the submitted paper has been published in Volume 7, Number 2 (April 2011) pp.123-301. Dr.Baz has completed a number of training courses that give him the capability to master the enterprise-scale EDA/CAD tools provided by Cadence, Synopsys, and Mentor-Graphics. The training courses cover digital, analogue, and mixed-signal IC design and also cover the whole flow starting from schematic down to the layout. The certificates of the courses are attached below, where all courses are provided by Europractice, which is the multi-project-wafer-service for the UK and European countries.

Science & Technology Facilities Council
Rutherford Appleton Laboratory

Microelectronics Support Centre

This is to certify that

Mr Abdullah Baz

attended the following training course

Introduction to Digital IC Implementation (extended 4 day course)

10 - 13 May 2011

Presented by

The Microelectronics Support Centre
Science and Technology Facilities Council
Rutherford Appleton Laboratory

This course introduced the basic implementation steps and tools required to produce a digital Integrated Circuit. The course focused on taking an RTL description of a design through to layout ready for manufacture. Hands-on practical exercises used design tools from Synopsys and Cadence to implement a realistic design in a modern 90nm CMOS process.

Course Administration

Microelectronics Support Centre TRAINING

Microelectronics Support Centre
www.msc.stfc.ac.uk

Science and Technology Facilities Council,
Rutherford Appleton Laboratory, Didcot, Oxfordshire, OX11 0QX, United Kingdom

Science & Technology Facilities Council
Rutherford Appleton Laboratory

Microelectronics Support Centre

This is to certify that

Mr Abdullah Baz

attended the following training course

Introduction to Analogue IC Design: Layout and Post Layout Verification

14 - 16 December 2010

Presented by

The Microelectronics Support Centre
Science and Technology Facilities Council
Rutherford Appleton Laboratory

This course introduced the Cadence IC 6.1 back-end design flow for analogue IC implementation. Practical sessions illustrated layout and physical verification of a variety of custom circuits. The course covered polygon-level layout, schematic-guided layout, layout verification, parasitic extraction and export of GDSII.

Course Administration

Microelectronics Support Centre TRAINING

Microelectronics Support Centre
www.msc.stfc.ac.uk

Science and Technology Facilities Council
Rutherford Appleton Laboratory, Didcot, Oxfordshire, OX11 0QX, United Kingdom

Science & Technology Facilities Council
Rutherford Appleton Laboratory

Microelectronics Support Centre

This is to certify that

Mr Abdullah Baz

attended the following training course

Mixed Signal IC Design and Implementation

7 - 9 December 2010

Presented by

The Microelectronics Support Centre
Science and Technology Facilities Council
Rutherford Appleton Laboratory

This course explored the design methodology and design tool flow required to design and implements a mixed-signal IC. The course focused on enabling attendees to take designs from behavioural block simulations, through circuit design considerations at the D-A and A-D interface and physical implementation, to full chip extraction and simulation. Hands-on practical exercises used tools from Synopsys and Cadence to implement design examples in a modern 150nm CMOS process.

Course Administration

Microelectronics Support Centre TRAINING

Microelectronics Support Centre
www.msc.stfc.ac.uk

Science and Technology Facilities Council,
Rutherford Appleton Laboratory, Didcot, Oxfordshire, OX11 0QX, United Kingdom

Science & Technology Facilities Council
Rutherford Appleton Laboratory

Microelectronics Support Centre

This is to certify that

Mr Abdullah Baz

attended the following training course

Introduction to Analogue IC Design: Schematic Entry and Simulation

26 - 28 January 2010

Presented by

The Microelectronics Support Centre
Science and Technology Facilities Council
Rutherford Appleton Laboratory

This course introduced the Cadence IC 6.1 front-end design flow for analogue IC design. Practical sessions illustrated the design flow for a typical circuit. Topics covered included schematic entry, simulation, corner analysis, optimisation, Monte Carlo and hierarchal design.

Course Administration

Microelectronics Support Centre TRAINING

Microelectronics Support Centre
www.msc.stfc.ac.uk

Science and Technology Facilities Council,
Rutherford Appleton Laboratory, Didcot, Oxfordshire, OX11 0QX, United Kingdom

The tasks assigned to Dr.Baz are:

1. Reviewing and performing critical study of asynchronous synthesizing and functional verification techniques.
2. Assessing the available Electronic Design Automation (EDA)/Computer Aided Design (CAD) tools in their ability to synthesize and verify the functionality of asynchronous circuits including both the data-path and the controller.
3. Proposing a complete procedure that allows synthesizing and functional verification of asynchronous circuits including both datapaths and control circuits.
4. Analysing the requirements and completing the usecase of the system.
5. Design and development of the tool components.
6. Reviewing the available open source environments and programming languages in order to select one of them that fit the requirements of the designed data structure.
7. Testing the tool to check the validation of the data in the back end of the tool.
8. Performing exception and functional test.
9. Compiling and producing the system documentation.
10. Producing the project final report.

Co-Investigator-1: Dr.Ahmed Alahmadi is an active researcher and the Head of the Electrical & Electronic Engineering Department in UQU. He has very good experience in circuit design and on-chip testing. Dr. Alahmadi is a recipient of the best paper award in the 15th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems for his paper entitled "Reconfigurable time interval measurement circuit incorporating a programmable gain time difference amplifier". The design and testing techniques presented in this paper are asynchronous. The tasks assigned to Dr.Alahmadi are:

1. Investigating the existing asynchronous design techniques (e.g. completion detection, delay elements, delay models, handshaking, etc.).
2. Proposing a complete framework to help electronic circuit designer in assessing the available EDA/CAD tools in the context of asynchronous system design and choosing the right tool for his/her design task.
3. Analysing the requirements and completing the usecase of the system.
4. Design and development of the tool components.

5. Reviewing the available open source environments and programming languages in order to select one of them that fit the requirements of the designed data structure.
6. Testing the tool to check the validation of the data in the back end of the tool.
7. Performing exception and functional test.
8. Producing the user manuals.
9. Producing the project final report.

Consultant: Prof. Yehia Massoud is the Head of the Electrical and Computer Engineering (ECE) department at Worcester Polytechnic Institute (WPI). He is also the Director of the WPI Center for Integrated Systems. He received his PhD degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1999. He was a member of the Technical Staff at the Advanced Technology Group at Synopsys Inc., Mountain View, CA from 1999 to 2003. He joined Rice University in July 2003, where he was the founding director of the Nanoelectronic Systems Laboratory (NSL), and a tenured associate professor from 2007 to 2010 and an assistant professor from 2003 to 2007 in the Electrical and Computer Engineering at Rice University. Before joining WPI in September 2012, he was the W.R. Bunn Head of the Electrical and Computer Engineering Department at the University of Alabama at Birmingham.

Yehia Massoud **is Fellow of the IEEE**. He was named distinguished lecturer by the IEEE Circuits and Systems Society for 2014-2015. He is the editor of mixed-signal letters-The Americas. He is also an Associate Editor of the IEEE Transactions on Very Large Scale Integration Systems (TVLSI), the IEEE Transactions on Circuits and Systems I (TCAS-I) and the Journal of Circuits, Systems, and Computers. He also served as a guest Co-Editor of the May 2010 special issue of the IEEE Transactions on Circuits and Systems I. He also serves on the founding editorial board of the NanoCom Journal. He has served as the 2009 General Program co-Chair and the 2007 Technical Program Co-Chair of the IEEE/ACM Great Lakes Symposium on VLSI. He has chaired or co-chaired more than conference tracks in many IEEE/ACM international conferences.

Dr. Massoud leads research efforts in various areas of Electrical and Computer Engineering and their application to Biotechnology and Nanotechnology. He has published more than 200 papers in peer reviewed journals and conferences. He served as the theme leader for Novel Interconnects and Architectures in the SRC Southwest Academy of Nanoelectronics (SWAN) from 2006-2011. He is an elected member of the

IEEE Nanotechnology Council from 2009 to 2011. He was awarded the Rising Star of Texas Medal in the 2007 Nanosummit and was selected as one of ten MIT Alumni featured in the 2012 MIT EECS newsletter. He is a recipient of the National Science Foundation CAREER Award in 2005, the DAC fellowship in 2005, the Synopsys Special Recognition Engineering Award in 2000, several Best Paper Award Nominations, and two Best Paper Awards at the 2007 IEEE International Symposium on Quality Electronic Design and the 2011 IEEE International Conference on Nanotechnology. Prof.Massoud will advise the research team during the whole project and will be on-campus with them during the important tasks of the project, which are:

1. Proposing a complete procedure that allows synthesizing and functional verification of asynchronous circuits including both datapaths and control circuits.
2. Performing exception and functional test.