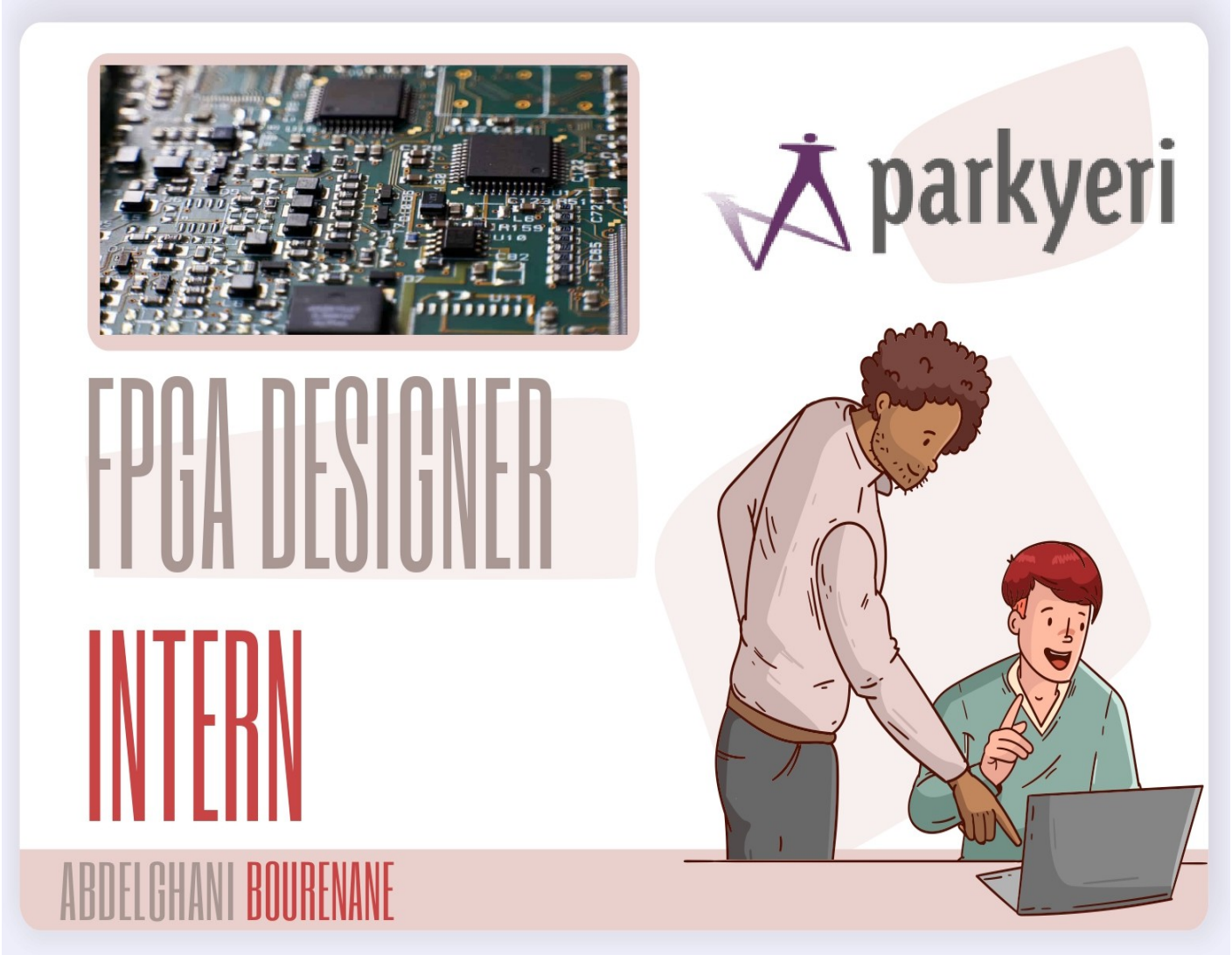
Internship Report



Intern: Abdelghani Bourenane
Position: FPGA Designer
Company: Parkyeri
Mentor: Giray Pultar

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General Information:

Full Name: Abdelghani Bourenane
Intern position title: FPGA Designer
Host Company: Parkyeri
Internship starting Date: 01/04/2021
Internship Ending Date: 30/09/2021
Place of work: Virtual Internship
Position Description:
Work as a digital electronics circuit designer as well as an FPGA designer whose tasks include working on existing and designing new digital electronics circuits for IoT applications as well as generating designs for Altera and/or Xilinx field programmable gate arrays.
Work will be tailored according to the capabilities and career growth potential of the candidate as well as company requirements.

Chapter 01: Internship project description, company vision and goals, working methodology and mechanisms

Company :

Parkyeri is an Istanbul-based company that has been founded in 2001 and since then has scored for itself a renowned position between the Turkish companies. Its fields of business include consultancy, operations, and software development. The scopes of projects and solutions that it covers include task management, research and development, custom-software solutions, industry-specific solutions, and IT system for small and medium enterprises. Consulting wise, the company offers system and project management, scaling, software development methods and database set up and management. The company's internship project is culturally inclusive as it is offered for students from different countries.

Project Description and Working methodology:

The internship program constitutes of different teams including the "FPGA team", "Application team" and the "Electronics team". The internship relies on the Agile software development methodology for managing the project; it is a process by which the solutions of the faced problems are processed through the collaboration and organization between the different teams involved.

The different teams work on the project that is creating a learning management platform for a school where the student can track his/her grades, courses, and assignments.

A sprint meeting is held at the beginning of each week where the tasks that were assigned for each member are reviewed and commented on. In addition to that, daily meetings are held throughout the week for reporting the work that has been done in regard to the project and the work that is planned to be done as well as reviewing any tasks that are in the review section Gitlab, in addition to raising attention to any issues faced by anyone during his work, so others could offer their help and guidance. All this is monitored by the scrum master who is assigned every two weeks. The meetings are held via Discord and with elaboration through gitlab.

Team Collaboration through Pair programming:

Collaboration between the interns is one of the methods that contributed to accelerating the achievement rate as well as strengthening the relationship between teammates, collaboration was present through the pair programming sessions, where one of the interns sit for one to two hours sharing his code with an other intern, through this sort of meetings, we seek for insights and directions about the issues and errors that our code

includes, this sessions have immensely increased the productivity of each one as well as gave each intern the opportunity to discover what others are working on so he could get introduced to various topics and tips in other fields.

Chapter 2: The FPGA group role in the project, objectives and assignments

The project is different from other typical applications in that the computation is going to be done on an FPGA rather than a CPU for better performance and higher speed, computing the average of a student's grade would take less time if it were done on an FPGA .
For me I have applied for an FPGA designer position so I take a part of "FPGA team" where I, along with my teammates, are responsible for building FPGA based modules to be implemented in the overall project requirements. So the goal of the FPGAteam is to perform real time calculation needed by the application through hardware based designs.

Chapter 3: The FPGA team tools

For all the hardware designs that we generate during this internship a python based tool is used, this tool is Migen which is a python toolbox that is used rather than VHDL or Verilog in building “complex digital hardware” as it is more efficient than the latter.
Migen Fragmented Hardware Description Language (FHDL) library uses ideas of combinatorial and synchronous statements, has arithmetic rules that make integers continuously behave like mathematical integers, and the most important part is that it allows the design's logic to be built by a Python program. This final point empowers hardware designers to take advantage of the richness of Python – object oriented programming, work parameters, generators, libraries, operator overloading etc. – to construct well organized, reusable and rich designs.

LiteX IP is used in addition to the Migen toolbox, LiteX is responsible for generating Verilog netlists on the front-end as well as driving “proprietary build back-ends” like Vivado for creating bitstreams for the FPGAs .
LiteX is created and used by Enjoy-Digital since 2012 to develop full-systems with some partners and provide convenient and efficient designs to create SoCs on FPGA. The LiteX framework provides a helpful and effective foundation to make FPGA Cores/SoCs, to explore different design architectures and make full FPGA based systems.

Seeing as the internship program is virtual, the project is created on Gitlab where the different tasks to be assigned and reviewed are there, Gitalb also allows for massive and ease collaboration between all the team.
The place where the team works and do daily and weekly meetings is Discord which is a communication software that offers text and voice channels to easily collaborate.

Chapter 4: project challenges, working flow

Work progress during the first days:

early starting days of the internship were a time to install all the working tools, first we installed linux based OS on our machines since most of the tasks needs a linux based software, after that we installed Vivado as it is the official Xilinx Software that supports the Xilinx FPGAs which are the boars that we use in our project, finally installing Litex which is the digital design tool that we use to generate our designs, as well as programming and communicating to our boards.

Later on, we have started familiarizing our selves with migen based syntax, rewriting codes and following tutorials provided by our mentors. Simultaneously, we have worked on discovering how Litex works and what are its features and applications, as well as reading about this new development tool what are the goals behind creating it, and how could we get out the best of it

Work progress after a good period:

after being familiarized with the working tools including migen and Litex, we have started to develop some meaningful designs, starting from creating a blinking led example to working on average calculation modules, meanwhile we have worked on understanding and creating communication protocols to establish connection with our boards, and we ended by choosing wishbone as our targeted protocol to be used in all of our designs, this after creating some wishbone related designs using migen.

One of the main tasks that we have worked on is looking for a proper way to store data on the FPGA, so we were able to create storage memory that could handle hundreds of addresses and words, but also with the ability to communicate to this memory through a wishbone interface, hence having the capability to write to the memory and read from it according to the communication protocol rules.

To make the data management operation highly appropriate and flexible for the user, we decided to adopt a new data representation methodology which is the key-value pair that consists of two related data elements, key which mainly refers to an address memory or a location that hold a piece of data referred to as value, the main goal of this application is to make the communication between the user and the storage module easier, this is

established with the help of the wishbone interface and communication protocol

Chapter 5: Overall results, achievements and learning outcomes

The tasks provided as well as the mentoring offered by my supervisor Giray has given me the chance to develop the skills of problems solving and specially debugging and solving coding problems to build meaningful digital designs for the sake of creating new optimized computing modules appropriate for our applications, the internship experience has given me various insights about the open hardware tools as well as the use of programming languages including python and C++ to describe digital circuits and embedded hardware.

I had the chance to collaborate and work on implementing different designs from computational to communication modules aimed at generating optimized outputs, I am aiming to carry on this journey by experiencing creating my own customized SoC but also contributing to the spread of this new technology represented in Litex and Migen through creating content explaining this tools for beginners who would explore it.