Lab 4
COMPENG 3DQ5

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In our implementation, firstly starting with Y[k], since we are dealing with signed numbers, the MSB of each number (from read_data) is checked to see if they are either both 1 (both negative) or both 0 (both positive). If this is the case, the result is just the subtraction of W and X. If the two numbers have different signs, a check is done to determine which number is the negative number. If X is negative (MSB of read_data_a[1] is 1), the result is then W minus the absolute value of X (for example, 1+(-1) is the same as 1-1). If W is negative (MSB of read_data_a[0] is 1) the result is then computed by doing the absolute value of X minus the absolute value of W (this is the same as W+X in this case). The method for computing the absolute value of W and X is described in the next section below

For Z[k], the MSB of W and X is checked and if either of them is a 1 (indicating the number is negative), the absolute value is taken by flipping all the bits and adding 1'b1 (two's complement). Finally, a check is continually done to see which address is currently being read from and if this value is less than 256, the result of Z is the absolute value of W minus the absolute value of X. Once the read address goes over 256, the result of Z is now the addition of the absolute value of W and the absolute value of X all divided by 2. Dividing by two is done by dropping the LSB of the addition result in this case. Note that before the addition occurs, an extra bit is concatenated to avoid an arithmetic overflow.

After reviewing the compilation report, it was noted that a total of 23 logic registers were used in the design from the report all of which came directly from the experiment file. Only registers that are used with non blocking assignment are counted in the register count within quartus. After manually counting all the registers used in the design (FSM and the combinational logic block we implemented) that were used with non blocking assignment within the code, the number of registers counted was a total of 23, exactly the same as the value from the compilation report.

After viewing the timing analyzer in quartus, it was noted that the critical path was about 9 ns. Based on our design structure, the longest path for an input to reach the output is for computing Y[k] when W is negative and X is positive. The critical path time value likely stems from this path.