

Sheet 5

Q1

a) Starting address = $30_{16} \times 4_{16} = C0_{16}$

b) i) $21_{16} = 100\ 001_2$

∴ interrupt mask = 001

ii) Level of Interrupt = 1 (IRQ 1)

Q2

a) Memory-mapped I/O → single address space

∴ range from 0 to 127 distributed between memory and I/O

b) Isolated I/O → Two separate address spaces

∴ range from 0 to 127 for memory and another range from 0 to 127 for I/O

Q3 ① interrupt executing ISR 3

② execute ISR 5 completely

③ Return to finish ISR 3

④ Start executing ISR 2 then interrupt when ISR 6 is activated

⑤ execute ISR 6 completely

⑥ execute ISR 4 completely

⑦ return to finish ISR 2

⑧ execute ISR 1 completely

b)

ISR 3 \rightarrow 011ISR 5 \rightarrow 101ISR 3 \rightarrow 011ISR 2 \rightarrow 010ISR 6 \rightarrow 110ISR 4 \rightarrow 100ISR 2 \rightarrow 010ISR 1 \rightarrow 001